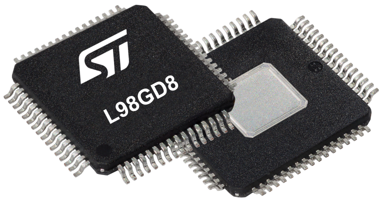
L98GD8

Datasheet

Automotive fully configurable 8-channel High/Low side MOSFET pre-driver suitable for systems at 48 V



Product status link
L98GD8

Product summary		
Order code	**Package**	**Packing**
L98GD8TR	TQFP64 (exposed pad down)	Tape and reel

Features

- AEC-Q100 qualified
- 12 V, 24 V and 48 V battery systems compliance
- 3.3 V and 5 V logic compatible I/O
- 8-channel configurable MOSFET pre-driver
  - High-side (N-channel and P-channel MOS)
  - Low-side (N-channel MOS)
  - H-bridge (up to 2 H-bridge)
  - Peak & Hold (2 loads)
- Operating battery supply voltage 3.8 V to 58 V
- Operating VDD supply voltage 4.5 V to 5.5 V
- Programmable gate charge/discharge currents for improving EMI behavior
- Individual diagnosis for:
  - Short circuit to battery
  - Open load
  - Short circuit to ground
- Highly flexible overcurrent sensing implementation
  - Possibility of monitoring external MOS drain to source voltage
  - Possibility of monitoring voltage on external shunt resistor
  - 64 programmable overcurrent thresholds independent for each channel
  - Ultra-fast output shutdown in case of overcurrent
- Current limitation for H-Bridge configuration
- 32-bit SPI protocol available for configuration and diagnostics
  - Failures latched even if they occur during diagnostics reading
  - Daisy chain operation
  - SDO protected against overvoltage
- Safety features
  - Fast switch off redundant output disable by two external pins
  - Built In Self Test (BIST) for logic operation
  - Hardware Self Check (HWSC) for VDD5 overvoltage comparator
  - Configurable Communication Check (CC) watchdog timer available
  - Disable feedback by bi-directional pin
  - Highly redundant output monitoring by dedicated SPI registers
- 10-bit ADC for battery and die temperature measurements available by SPI
- VDD5 monitoring for over/under voltage
- VPS (battery) monitoring for under voltage

Applications

- Automotive 12 V, 24 V and 48 V applications
- Low-side, high-side, Peak and hold and H-Bridge load control
- Designed for driving relays, motors, and all the resistive and inductive loads

Description

The L98GD8 is an 8-channel MOSFET pre-driver configurable for low-side, high-side, peak and hold and H-Bridge load control. It is designed to comply with the requirements of automotive passenger vehicles with 12 V and 48 V battery systems, as well as automotive commercial vehicles with 24 V battery systems.

All outputs can be PWM controlled. Six outputs are capable of driving safety relevant loads. One output can be dedicated to the actuation of safety relevant loads requiring a dedicated enable pin (EN6).

The device offers the possibility of controlling two independent H-Bridges.

The device can also drive up to two loads requiring "peak & hold" control strategy.

The driver outputs are protected against short circuit condition.

The device protects the external MOS in case of an overcurrent event.

Each output provides full diagnostic information such as short to battery, short to ground and open-load. Each output status can be constantly monitored through dedicated SPI registers.

The voltage slew rate of the external transistors 1-8 is controlled during turn ON and turn OFF in order to improve EMI behavior.

A double, redundant, external disable source is available through DIS and NDIS pins in order to improve safety.

The device is configurable via SPI through a 32-bit protocol.

1 Block diagram

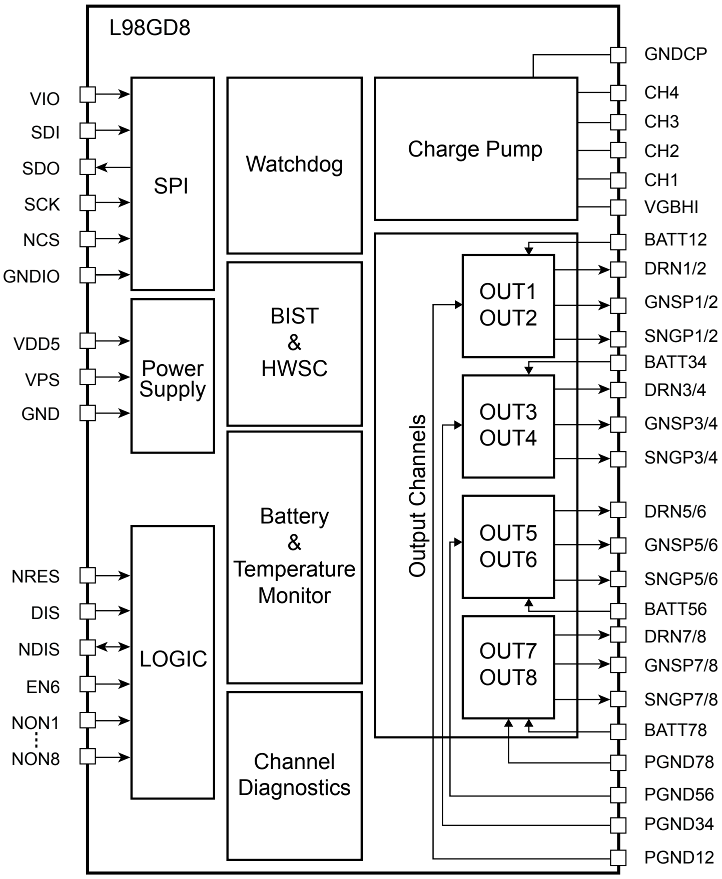


Figure 1. Block diagram

2 Output configurations

The device offers three different configuration options for the output channels: High-Side/Low-Side, Peak & Hold and H-Bridge. P&H configuration requires 2 or 4 channels, while H-Bridge requires 4 or 8 channels. Channels not used in P&H or H-Bridge are available for HS/LS usage. All the configurations involving channel 6 require the output driver 6 to be enabled through the EN6 input.

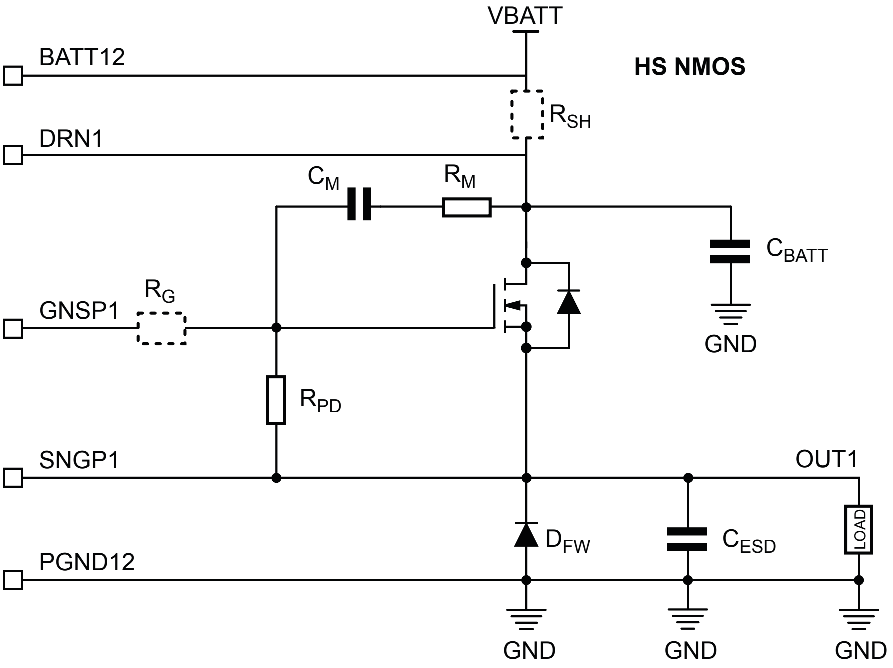
2.1 High-Side / Low-Side, with configurable FET type (N channel or P channel)

Each channel features a dedicated SPI register where the user can specify:

- MOS side: High-Side or Low-Side, through the LS_HS_config_xx bit;
- MOS type: NMOS or PMOS, through the N_P_config_xx bit;
  - PMOS type is available only for High-Side.

The picture below shows an example of High-Side configuration with NMOS transistor on channel 1. Refer to this schematic in order to understand how the external FET must be mounted with respect to the DRNx/GNSPx/SNGPx/BATTx pins.

Figure 2. **Example of High-Side configuration with NMOS on channel 1**



Note: the freewheeling diode is needed only in case of inductive load.

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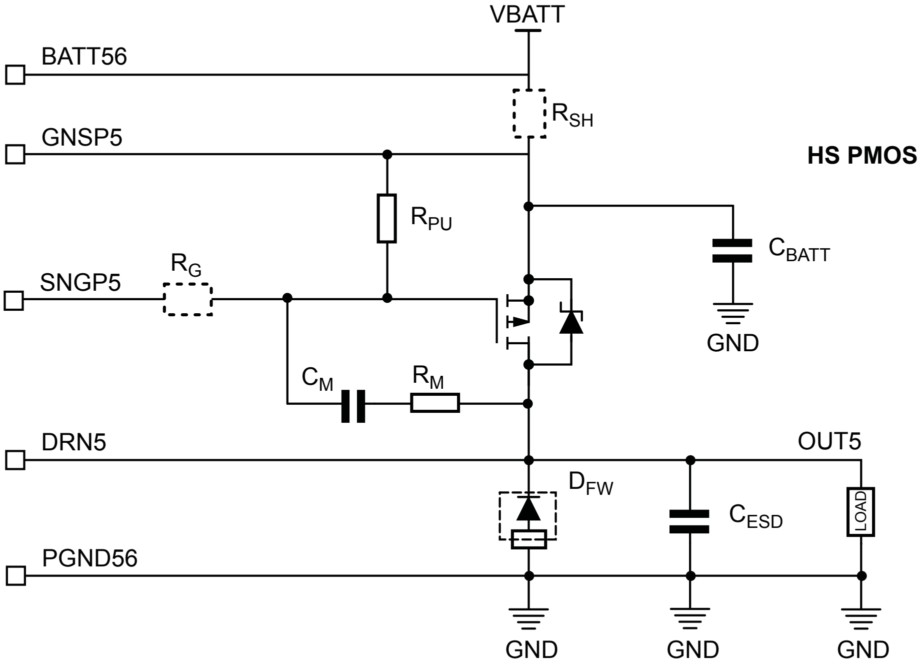
The following picture shows an example of High-Side configuration with PMOS transistor on channel 5. Refer to this schematic in order to understand how the external FET must be mounted with respect to the DRNx/GNSPx/SNGPx/BATTx pins.

Figure 3. **Example of High-Side configuration with PMOS on channel 5**



Note: the freewheeling diode is needed only in case of inductive load.

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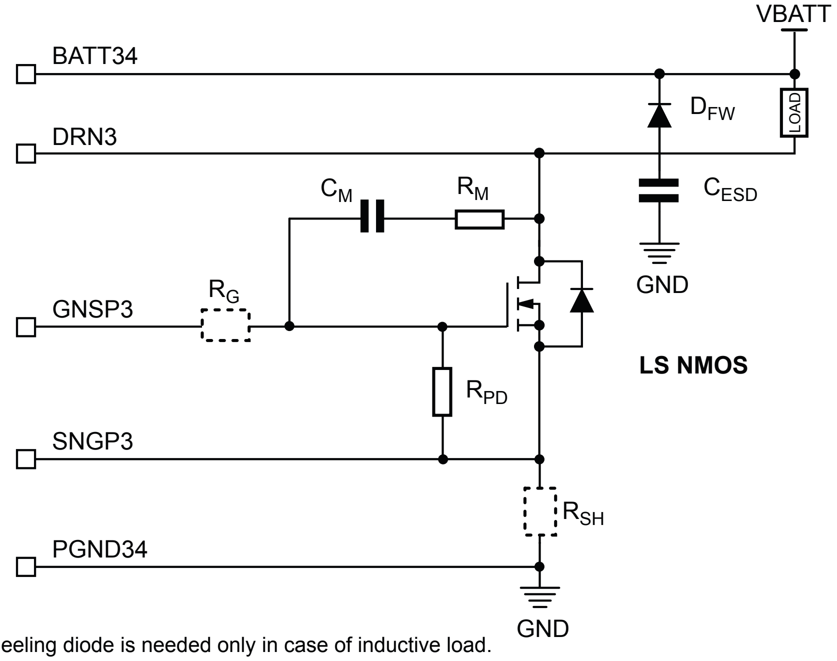
The picture below shows an example of Low-Side configuration with NMOS transistor on channel 3. Refer to this schematic in order to understand how the external FET must be mounted with respect to the DRNx/GNSPx/SNGPx/PGNDx pins.

Figure 4. **Example of Low-Side configuration with NMOS on channel 3**



Note: the freewheeling diode is needed only in case of inductive load.

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Note: When using channel 6, the EN6 input must be set high to enable the output driver.

The LS/HS configuration is suitable for driving whatever high-side/low-side loads as:

- Lamps (any channel);
- ON/OFF electrovalves (any channel);
- Any safety relevant load (channel 6 has dedicated EN6 enable input);
- Lambda probe heater (any channel);
- Limp home functionalities or not safety related loads (channels 7 and 8 not affected by external disable input).

2.2 Peak & Hold

The device can handle up to two peak & hold loads. There are two possible configurations which can co-exist:

- P&H1: it involves channels 1 (HS) and 4 (LS) and can be selected through the **PH1_config** bit
- P&H2: it involves channels 2 (HS) and 3 (LS) and can be selected through the **PH2_config** bit

Once a peak & hold configuration is selected through its config bit, the corresponding output channels are automatically configured according to the pre-determined transistor side. The FET type for the High-Side can be selected through its **N_P_config_xx** bit.

Figure 5. **Example of peak & hold configuration with NMOS (HS) on channel 1 and NMOS (LS) on channel 4**

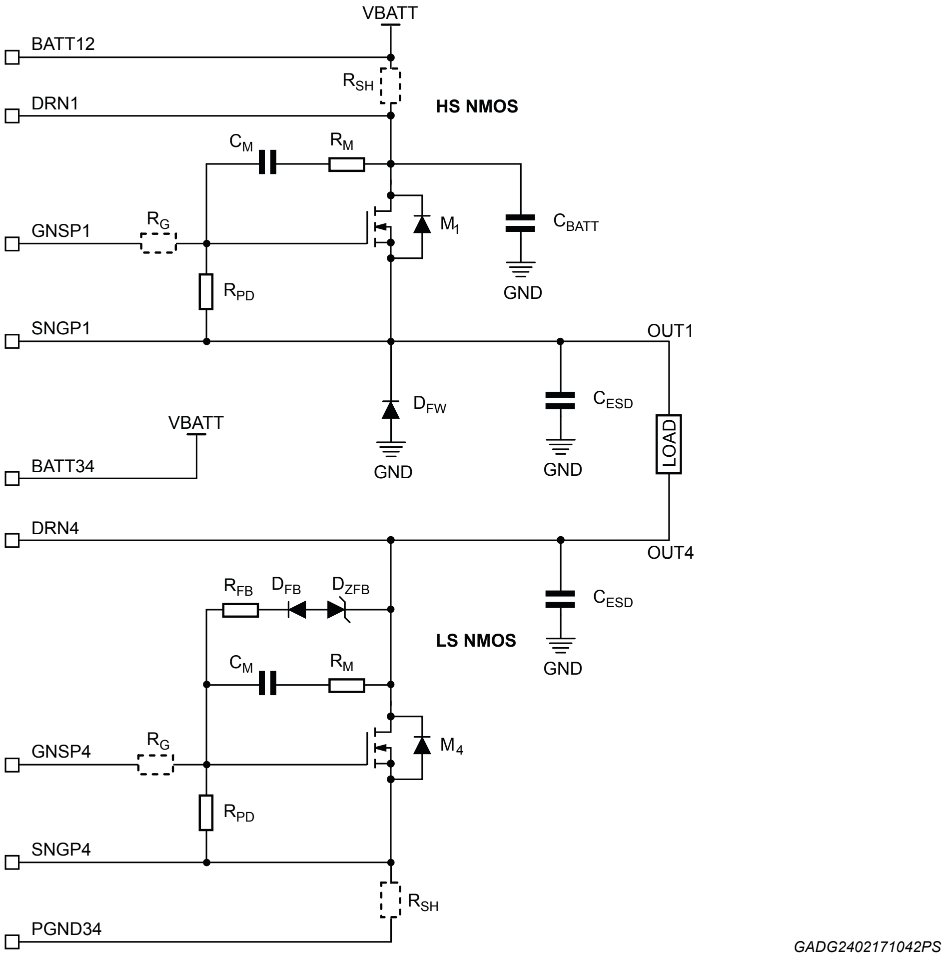


Figure 5. Example of peak & hold configuration with NMOS (HS) on channel 1 and NMOS (LS) on channel 4 shows an example of P&H1 configuration with NMOS transistor on the High-Side. Refer to this schematic in order to understand how the external FETs must be mounted with respect to the DRNx/GNSPx/SNGPx/PGNDx/BATTx pins.

In case of PMOS on the High-Side, refer to Figure 3. Example of High-Side configuration with PMOS on channel 5 in order to understand the DRNx/GNSPx/SNGPx/BATTx pin connection.

The peak and hold configuration is suitable for driving several types of loads as:

- Injectors;
- Fuel pump;
- Other type of electrovalves and coils that may benefit from peak and hold control.

2.3 H-Bridge

The device can handle up to two H-Bridges. There are two possible configurations which can co-exist:

- H-Bridge 1: it involves channels 1 (HS), 2 (HS), 3 (LS) and 4 (LS) and can be selected through the **HB1_config** bit
- H-Bridge 2: it involves channels 5 (HS), 6 (HS), 7 (LS) and 8 (LS) and can be selected through the **HB2_config** bit

Once an H-Bridge configuration is selected through its config bit, the corresponding output channels are automatically configured as reported above. The FET type for the High-Side transistors can be selected through their **N_P_config_xx** bit.

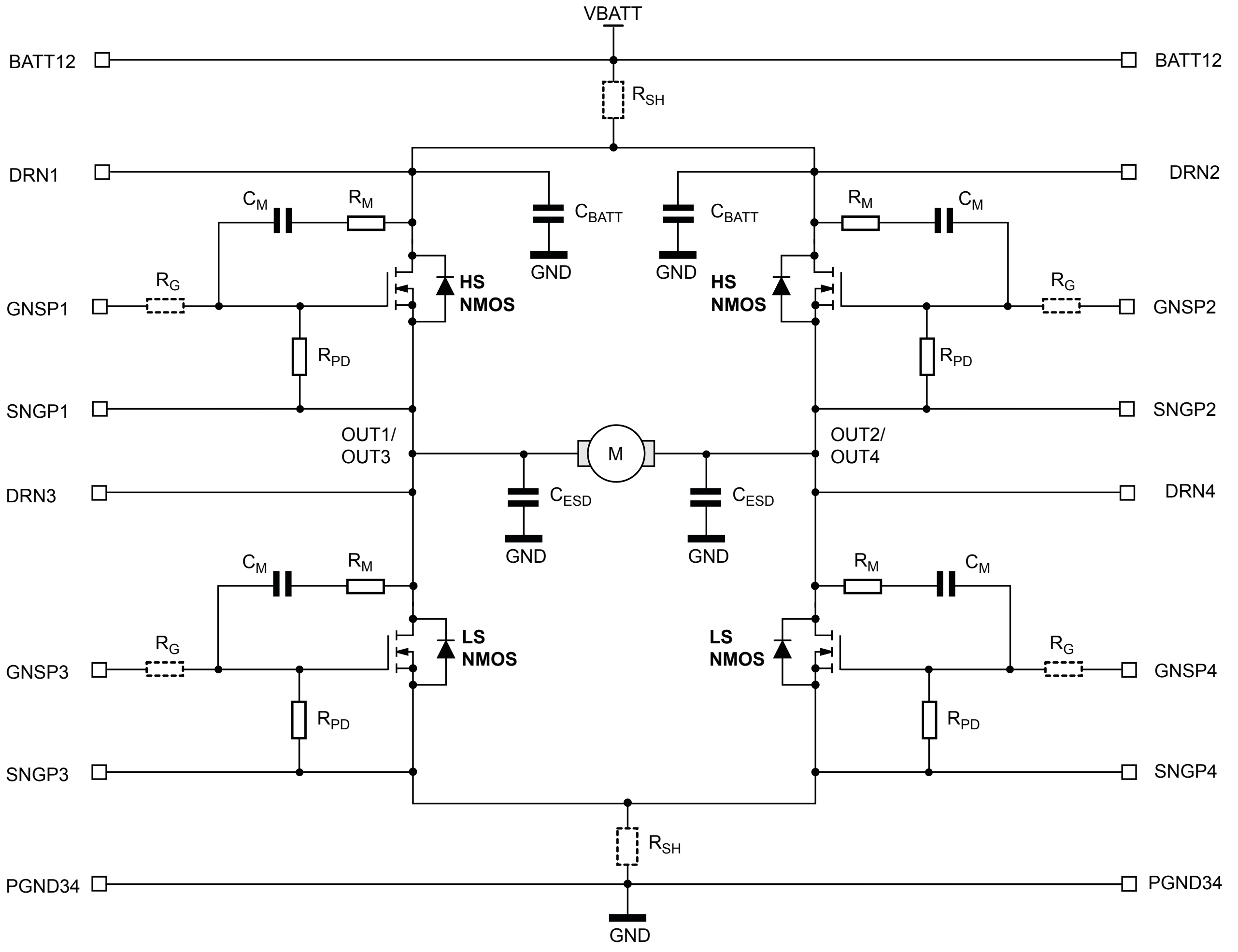
In case of H-bridge with PMOS on the High-Side, refer to Figure 3. Example of High-Side configuration with PMOS on channel 5 in order to understand how DRNx/GNSPx/SNGPx/BATTx are mounted with respect to NMOS pin connection.

The H-Bridge configuration is suitable for driving the following types of loads:

- Brushed DC motors

Note: When configuring H-Bridge 2, the EN6 input must be set high to enable the output driver.

Figure 6. Example of H-Bridge configuration with NMOS as HS and LS transistors (channels 1-4 used)



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3 Device pins

This section contains the device pinout, the pin description and configuration and the electrical characteristics.

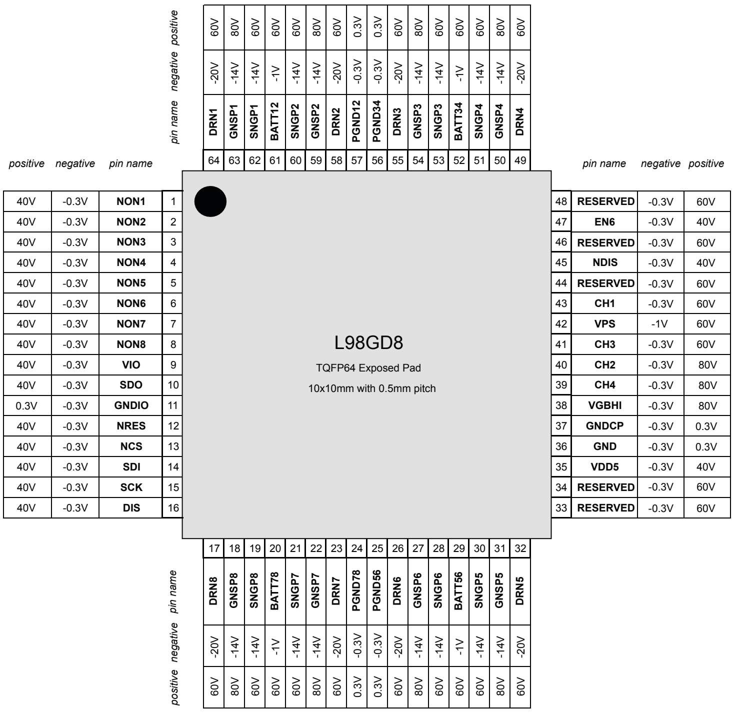
3.1 Pinout

The picture below shows the device pinout. Each pin also features the absolute maximum ratings.

The maximum differential voltage allowed across the following pins is 20 V:

- GNSPx and SNGPx;
- CH2 and VPS;
- CH4 and CH2;
- VGBHI and VPS;
- VGBHI and CH4.

Figure 7. **L98GD8 pinout**



3.2 Pin names and functions

The table below lists all the information about device pins.

Note: *The package exposed pad must be soldered on the PCB and connected to ground. Pins GNDIO and GNDCP must be shorted and ground connected.*

Syntax: P = Power, G = Ground, D = Digital, A = Analog, I = Input, O = Output, NA = Not Available, L = Low, H = High, PU = Pull Up, PD = Pull Down.

Table 1. **Pin list**

Pin #	Pin Name	Pin type		PU/PD	Active State	HBM ESD [(1)]	Description
Power Supply And Ground							
42	VPS	P	NA	NA	NA	4 kV	Battery Input, used to supply charge pump

Pin #	Pin Name	Pin type		PU/PD	Active State	HBM ESD (1)	Description
36	GND	G	NA	NA	NA	2 kV	Ground
35	VDD5	P	NA	NA	NA	2 kV	5 V Input (usually output of external regulator)
Digital inputs (connected to external microcontroller)							
1	NON1	D	I	PU	L	2 kV	Output 1 ON-OFF signal NPWM signal for H-Bridge 1
2	NON2	D	I	PU	L	2 kV	Output 2 ON-OFF signal DIR signal for H-Bridge 1
3	NON3	D	I	PU	L	2 kV	Output 3 ON-OFF signal HIZ signal for H-Bridge 1
4	NON4	D	I	PU	L	2 kV	Output 4 ON-OFF signal
5	NON5	D	I	PU	L	2 kV	Output 5 ON-OFF signal NPWM signal for H-Bridge 2
6	NON6	D	I	PU	L	2 kV	Output 6 ON-OFF signal DIR signal for H-Bridge 2
7	NON7	D	I	PU	L	2 kV	Output 7 ON-OFF signal HIZ signal for H-Bridge 2
8	NON8	D	I	PU	L	2 kV	Output 8 ON-OFF signal
Output pre-driver							
64	DRN1	A	I	NA	NA	4 kV	FET drain on channel 1
63	GNSP1	A	O	NA	NA	4 kV	NFET gate / PFET source on channel 1
62	SNGP1	A	O	NA	NA	4 kV	NFET source / PFET gate on channel 1
61	BATT12	P	I	NA	NA	4 kV	Battery for channels 1 and 2
57	PGND12	G	I	NA	NA	4 kV	Power ground for channels 1 and 2
58	DRN2	A	I	NA	NA	4 kV	FET drain on channel 2
59	GNSP2	A	O	NA	NA	4 kV	NFET gate / PFET source on channel 2
60	SNGP2	A	O	NA	NA	4 kV	NFET source / PFET gate on channel 2
55	DRN3	A	I	NA	NA	4 kV	FET drain on channel 3
54	GNSP3	A	O	NA	NA	4 kV	NFET gate / PFET source on channel 3
53	SNGP3	A	O	NA	NA	4 kV	NFET source / PFET gate on channel 3
52	BATT34	P	I	NA	NA	4 kV	Battery for channels 3 and 4
56	PGND34	G	I	NA	NA	4 kV	Power ground for channels 3 and 4
49	DRN4	A	I	NA	NA	4 kV	FET drain on channel 4
50	GNSP4	A	O	NA	NA	4 kV	NFET gate / PFET source on channel 4
51	SNGP4	A	O	NA	NA	4 kV	NFET source / PFET gate on channel 4
32	DRN5	A	I	NA	NA	4 kV	FET drain on channel 5
31	GNSP5	A	O	NA	NA	4 kV	NFET gate / PFET source on channel 5
30	SNGP5	A	O	NA	NA	4 kV	NFET source / PFET gate on channel 5
29	BATT56	P	I	NA	NA	4 kV	Battery for channels 5 and 6
25	PGND56	G	I	NA	NA	4 kV	Power ground for channels 5 and 6
26	DRN6	A	I	NA	NA	4 kV	FET drain on channel 6
27	GNSP6	A	O	NA	NA	4 kV	NFET gate / PFET source on channel 6
28	SNGP6	A	O	NA	NA	4 kV	NFET source / PFET gate on channel 6

Pin #	Pin Name	Pin type		PU/PD	Active State	HBM ESD [1]	Description
23	DRN7	A	I	NA	NA	4 kV	FET drain on channel 7
22	GNSP7	A	O	NA	NA	4 kV	NFET gate / PFET source on channel 7
21	SNGP7	A	O	NA	NA	4 kV	NFET source / PFET gate on channel 7
20	BATT78	P	I	NA	NA	4 kV	Battery for channels 7 and 8
24	PGND78	G	I	NA	NA	4 kV	Power ground for channels 7 and 8
17	DRN8	A	I	NA	NA	4 kV	FET drain on channel 8
18	GNSP8	A	O	NA	NA	4 kV	NFET gate / PFET source on channel 8
19	SNGP8	A	O	NA	NA	4 kV	NFET source / PFET gate on channel 8
SPI block (used for communication with external microcontroller)							
15	SCK	D	I	PU	NA	2 kV	SPI clock
14	SDI	D	I	PU	NA	2 kV	SPI data in
10	SDO	D	O	NA	NA	2 kV	SPI data out. An external pull-down resistor in the [10k - 47k] range must be mounted vs GNDIO.
13	NCS	D	I	PU	L	2 kV	SPI chip select
9	VIO	P	NA	NA	NA	2 kV	Supply voltage for SDO. Must be connected to the same power supply as the SPI of the master device (usually the external microcontroller)
11	GNDIO	G	NA	NA	NA	2 kV	Ground for SPI. Must be shorted to GNDCP
Reset / Disable							
12	NRES	D	I	PU	L	2 kV	Reset input. Must be connected to ECU reset
16	DIS	D	I	PU	H	2 kV	Disable input. Must be connected to the external microcontroller to allow the disabling of the outputs 1-6.
45	NDIS	D	I/O	PD	L	2 kV	Negated disable input/output. Can be used as a negated disable input. Can also be used as output to generate an interrupt in the external microcontroller whenever the NDIS node is pulled down (internal disable event)
47	EN6	D	I	PD	H	2 kV	Output 6 Enable. Can be used to enable output driver for safety relevant load control.
Charge Pump							
38	VGBHI	P	NA	NA	NA	2 kV	Charge pump output (battery + 12 V). Connected to VPS pin through a “tank” capacitor
43	CH1	A	I/O	NA	NA	2 kV	1st node for flying capacitor 1
40	CH2	A	I/O	NA	NA	2 kV	2nd node for flying capacitor 1
41	CH3	A	I/O	NA	NA	2 kV	1st node for flying capacitor 2
39	CH4	A	I/O	NA	NA	2 kV	2nd node for flying capacitor 2
37	GNDCP	G	NA	NA	NA	2 kV	Ground for charge pump. Must be shorted to GNDIO
Other pins							
44	RESERVED	D	I	NA	NA	2 kV	Tie low
48	RESERVED	NA	NA	NA	NA	2 kV	Leave floating
34	RESERVED	NA	NA	NA	NA	2 kV	Leave floating
46	RESERVED	NA	NA	NA	NA	2 kV	Leave floating
33	RESERVED	NA	NA	NA	NA	2 kV	Leave floating

1. *See Table 4. ESD performanceand Figure 8. ESD ratings on pinout.*

4 Product electrical and thermal characteristics

This section contains the Absolute Maximum Ratings (AMR), the latch-up trials, the ESD classification and the range of functionality of the device. The information provided here refers to the global behavior of the device. For specific information about the electrical characteristics of each interface/component, refer to the related section of the datasheet.

4.1 Absolute maximum ratings

Within the maximum ratings, no damage to the component or latch-up occurs and the defined leakage currents won't be exceeded. However, the full functionality of the device is guaranteed only in the functional range.

This part may be irreparably damaged if taken outside the specified absolute maximum ratings. Operation above the absolute maximum ratings may also cause a decrease in reliability.

Note: A negative current is flowing out of the L98GD8, a positive current into the L98GD8.

Table 2. Absolute maximum ratings capability

Symbol	Parameter description	Comment	Min.	Max.	Unit
Supply Pins					
VDD5	VDD5 voltage range		-0.3	40	V
V_{VPS_sta}	Static VPS voltage range	Ext. HS, Static Max voltage: VGBHI – VPS = 20 V	-1	60	V
V_{VPS_dyn}	Dynamic VPS voltage range	Dynamic; 2 ms test pulse 1	-2	60	V
VGBHI	VGBHI voltage range (Ch. Pump)	Max voltage: VGBHI – VPS = 20 V	-0.3	80	V
V_{VIO}	VIO voltage range	Supply for SDO	-0.3	40	V
Output Pre-Driver					
V_{SNGPx}	SNGPx voltage range	Max voltage: GNSPx - SNGPx = 20 V (in all conditions) BATTxx – SNGPx ≥ 0 V (When DSM is used for OC detection)	-14	60	V
V_{GNSPx}	GNSPx voltage range	Max voltage: GNSPx - SNGPx = 20 V	-14	80	V
V_{DRNx}	DRNx voltage range	-	-20	60	V
V_{BATTxx}	BATTxx voltage range	Max voltage: BATTxx – SNGPx ≥ 0 V When DSM is used for OC detection	-1	60	V
Ground pins: GND, GNDIO, GNDCP, PGNDxx					
V_{GND_PINS}	Ground voltage range	-	-0.3	0.3	V
Charge Pump					
$V_{CH1\&3}$	CH1 & CH3	-	-0.3	60	V
$V_{CH2\&4}$	CH2 & CH4	Max voltage: CH2 - VPS = 20 V CH4 - CH2 = 20 V VGBHI - CH4 = 20 V	-0.3	80	V
Digital HV pins: NONx, NRES, NDIS, DIS, EN6, NCS, SCK, SDI, SDO					
V_{DIG_IO}	Input voltage range	SDO and NDIS have to withstand this voltage also in ON-condition	-0.3	40	V

Refer to Figure 7. L98GD8 pinout for the device pinout with AMR indicated for each pin.

4.2 Latch-up trials

The table below lists the information about the Latch-up trials.

Note: *A negative current is flowing out of the L98GD8, a positive current into the L98GD8.*

Table 3. **Latch-up trials**

Symbol	Parameter description	Comment	Min.	Max.	Unit
LU	Latch-up Test	For all pins according to JEDEC78 class II level A	100	-	mA

4.3 ESD performance

The table below contains all the information about the ESD characterization of the device.

Note: *A negative current is flowing out of the L98GD8, a positive current into the L98GD8.*

Table 4. **ESD performance**

Symbol	Parameter description	Comment	Min.	Max.	Unit
ESD Classification, refer to Figure 8					
V_{ESD}	Human Body Model (HBM) (100 pF/ 1.5 kΩ)	For pins: DRNx, SNGPx, GNSPx, BATTxx, PGNDxx, VPS According to Q100-002	-4	4	kV
		For all other pins according to Q100-002	-2	2	kV
	Charged Device Model (CDM)	For corner pins DRN1, DRN4, DRN5 according to Q100-011	-600	750	V
		For corner pin T1 according to Q100-011	-750	600	V
		For corner pin NON1 according to Q100-011	-600	600	V
		For corner pin DIS according to Q100-011	-600	500	V
		For corner pins T4, T8 according to Q100-011	-750	750	V
		For all other pins	-500	500	V
Protection diodes current					
I_{ESD_SUP}	ESD protection diode current	For pins VPS, VDD5, VGBHI, VIO	-1	1	mA
I_{ESD_DRNx}	ESD protection diode current	For DRNx pins	-1	1	mA
I_{ESD_DIG}	ESD protection diode current	For pins NONx, NRES, NDIS, DIS, SDI, SCK, EN6, NCS, SDO	-1	1	mA

Figure 8. **ESD ratings on pinout**

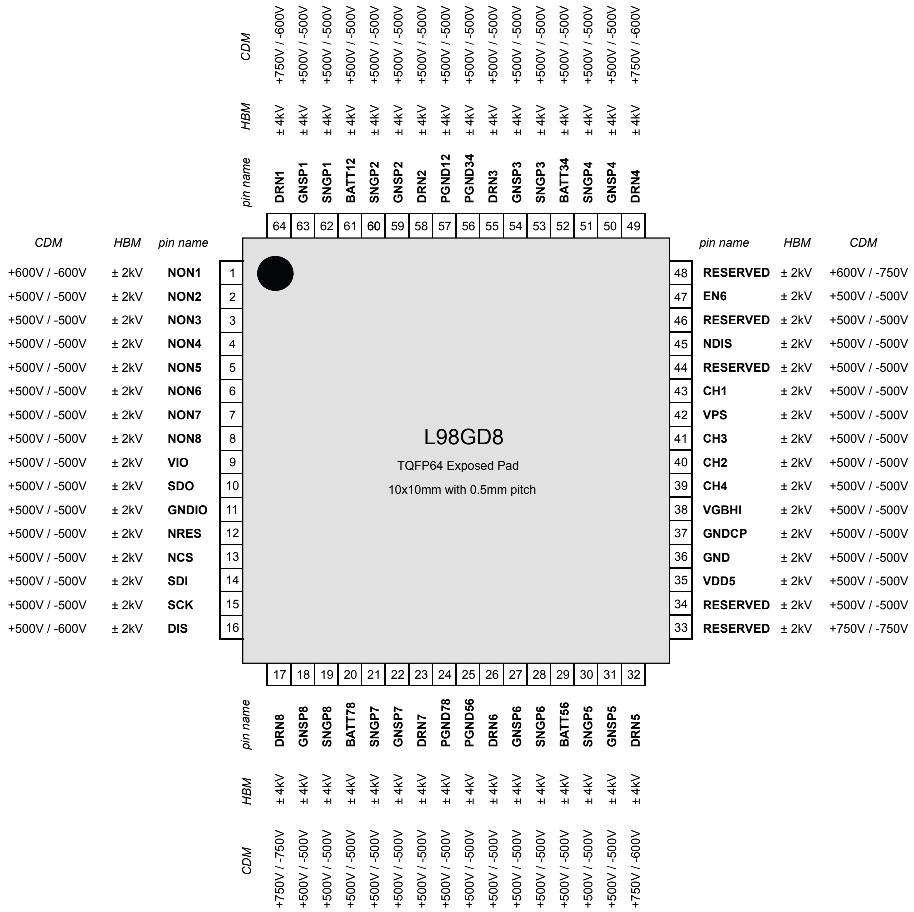


Figure 8. ESD ratings on pinout summarizes the ESD ratings for each pin according to both CDM and HBM models.

4.4 Thermal behavior

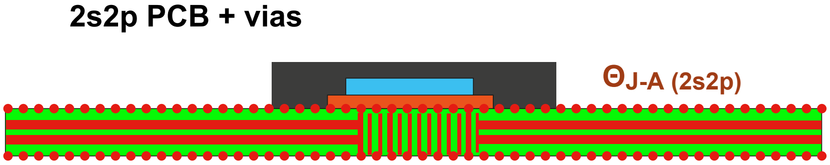
The table below contains the temperature ranges and the thermal resistance information. The device functionality is lifetime guaranteed up to 150 °C (junction temperature). If the junction temperature crosses TOT_OFF, overtemperature is detected. Status of the overtemperature comparator can be monitored reading **OT_STATE** bit via SPI. The external microcontroller can either read the temperature measured by the Temperature ADC or monitor OT_STATE bit: in case of overtemperature, the device must be disabled via external input.

Note: *$V_{VPS\_UV} < V_{VPS} < 60$ V, all supplies are independent; 4.5 V < VDD5 < 5.5 V; 3.0 V < VIO < 5.5 V, unless otherwise noted.*

Table 5. Thermal behavior

Symbol	Parameter description	Comment	Min.	Max.	Unit
Temperature ranges					
T_{j_op}	Operating / Lifetime (junction)	Lifetime guaranteed	-40	150	°C
T_{stg}	Storage temperature	-55 °C is allowed for a maximum of 15h	-40	+150	°C
T_{j_fct}	Functional (junction)	Transient condition	150	T_{OT_OFF}	
T_{OT_OFF}	Over temperature comparator threshold	-	165	190	°C
t_{Off_prot}	Comparator reaction time including analogue deglitching filter	-	100	900	ns
Thermal resistance					
$R_{th\_j\_c}$	Thermal resistance (junction to case)	Values are according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board (see Figure 9. Sketch of a 2s2p PCB with thermal vias)	-	2.4	°C/W
$R_{th\_j\_a}$	Thermal resistance (junction to ambient)		-	30	°C/W

Figure 9. Sketch of a 2s2p PCB with thermal vias



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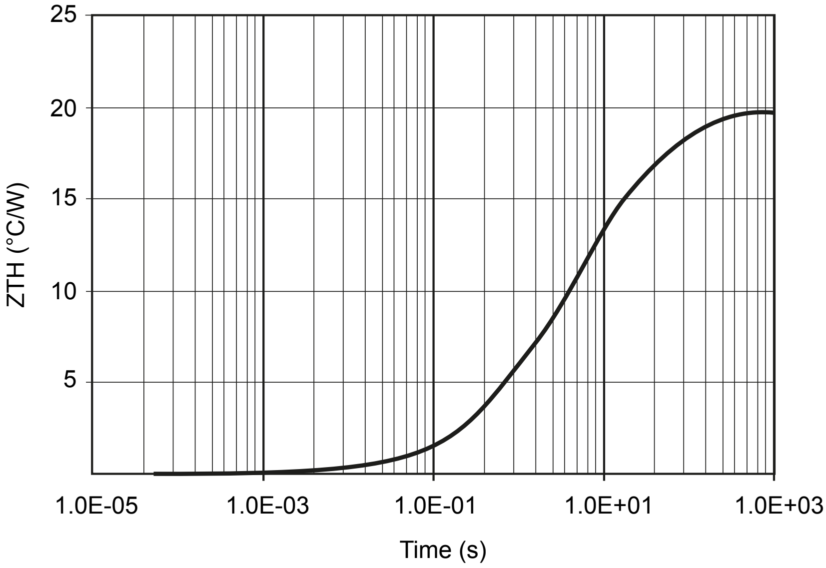
Note: *In "2s2p", the "s" suffix stands for "Signal" and the number before indicates how many PCB layers are dedicated to signal wires. The "p" suffix stands for "Power" and the number before indicates how many PCB layers are dedicated to power planes.*

The graph below shows the thermal impedance of the package.

Figure 10. Thermal impedance diagram



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4.4.1 Temperature ADC

An internal ADC monitors the junction temperature. Measure is available reading Temp_ADC[x] bit and applying the following conversion law:

Eq. (1): Junction temperature conversion law

$$T_j = \left(0.28 \times CODE\right) - 65 \quad (1)$$

The table below reports the electrical characteristics for the temperature ADC.

Note: *$V_{VPS\_UV} < V_{VPS} < 60$ V, all supplies are independent; 4.5 V < VDD5 < 5.5 V; 3.0 V < VIO < 5.5 V, unless otherwise noted.*

Table 6. Temperature ADC electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
ADC_res	Resolution	-	-	10	-	bit
f_{ADC}	Conversion rate	-	-	62.5	-	kHz
T_j_ADC_in	Temperature range	-	-40	-	190	°C
T_ACC	Temp accuracy	From -40 °C to 190 °C	-10	-	10	°C

4.5 Range of functionality

The table below lists the range of functionality for the electrical parameters.

Note: *Junction temperature is assumed $T_j = T_{j\_fct}$ unless otherwise noted.*

Table 7. Range of functionality

Symbol	Parameter description	Comment	Min.	Max.	Unit
Supply pins					
V_{VPS}	External load and charge pump supply	Extended Operational	3.8	58	V
		Operational[1]	3.8	48	V
V_{VDD5}	Supply for internal digital, analog and SPI (except SDO)	$T_j = T_{j\_op}$	4.5	5.5	V
V_{VIO}	Supply for SPI pin SDO	$T_j = T_{j\_op}$	3.0	5.5	V

1. voltage range fitting with VPS ADC range

5 Functional description

This section contains the functional description of this device. A general description of the device functionality is provided along with the detailed operation of each sub-block. Relations and interconnections between various sub-blocks are explained. For a detailed diagnostic analysis, refer to Section 6.2: Diagnostics overview.

5.1 General description

The device contains eight pre-drivers for external FETs. Each pre-driver can be configured to drive a high-side or low-side external driver (**LS_HS_config_xx** bit). The external FET can be either N-channel (low-side and high-side) or P-channel (high-side). FET type is selectable through **N_P_config_xx** bit. Complex configurations for P&H and H-Bridge are automatically applied programming the corresponding bit via SPI (**HBx_config** or **PHx_config**).

The outputs are controlled either directly by pins **NONx** or via SPI commands (programming **SPI_ON_OUTxx** bit). For each channel, control strategy is selected by programming the **SPI_input_sel_xx** bit.

Output channels must be enabled prior to use by programming the **en_OUT_xx** bit in the corresponding output register. Channel 6 requires also the EN6 input to be set high in order to be enabled (suitable for safety relevant load control).

IC provides charge pump for driving external low-side and high-side NMOS. Gate charge/discharge currents can be either constant, with value selectable via SPI, or limited by external resistor. **GCC_config_xx** bit defines the charge/discharge strategy. An external capacitor connected between transistor gate and drain is recommended to improve EMI performances.

External FET is protected against overcurrent (OC) during the ON phase by rapidly switching OFF the transistor with a high gate current in case of OC detection. The value of such shutdown current can be programmed via the **GCC_OVERRIDE_CONFIG** bit. Two detection strategies are available: either monitoring the voltage between transistor drain and source (DSM) or monitoring the drop on an external shunt resistor. Detection strategy is selectable via **OC_DS_Shunt_xx** bit. OC threshold is programmable via SPI (**OC_config_xx** bit). The device offers the possibility of compensating the OC threshold with respect to temperature (**OC_Temp_comp_xx** bit) and battery variations (**OC_Batt_comp_xx** bit). In case of an OC event, output re-engagement strategy is selectable through **prot_config_xx** bit.

Detection of Open Load (OL) and STB/STG failures is performed during the OFF phase. The diagnostic phase durations and currents can be selected through **tdiag_config_xx** and **diag_i_config_xx** bit.

In peak and hold configuration, the OFF diagnostic strategy can be programmed through **PHx_diag_strategy** bit.

In H-Bridge mode, the dead time to avoid cross conduction on the same branch of the bridge can be programmed through the **HBx_dead_time** bit. An extended set of OFF diagnostic times is available for the H-Bridge mode by programming the **HBx_tdiag_ext_config** bit.

A current limitation feature is available for H-Bridge configuration.

The diagnostic status of each channel is reported in the next received frame after having sent the following SPI command: **0x9AAA0001**.

Note: The "x" in the bit names symbolize the generic channel number or the configuration index (e.g. NONx refers to NON1, NON2, … , NON8. PHx_diag_strategy refers to PH1_diag_strategy and PH2_diag_strategy).

5.2 Supply concept

The device has 4 supply pins: **VDD5**, **VPS**, **VGBHI**, and **VIO**.

- VDD5 has to be provided by the ECU power supply and feeds most of the internal sub-blocks. Two internal regulators are used to generate separate 3.3 V supplies for analog and digital domains.
- VPS has to be provided by the battery and is used to feed the internal charge pump.
- VGBHI is the output voltage of the charge pump and it is used for driving the gate of the external FETs.
- VIO is a separate power supply dedicated for the SDO pin of the Serial Peripheral Interface. It must be connected to the same voltage level of the SPI master. The VIO pin is implemented in order to be compliant with both 3.3 V and 5 V systems.

5.2.1 VDD5 supply block

The VDD5 pin is internally split between analog and digital domain to reduce interference between the different parts of the component. Two regulators are implemented in order to provide separate 3.3 V domains:

- **VDD_int_a** is generated out of VDD5. It is the overvoltage protected internal supply of the low voltage analog part, such as diagnostic comparators, gate drives for integrated low-side, bias currents, bandgap etc.;
- **VDD_int_d** is generated out of VDD5. It is the overvoltage protected internal supply for the digital part.

The component starts operation when VDD5 is higher than the power-on reset threshold (VPOR). Details about the reset block are given in the Section 5.3: Reset.

The VDD5 is monitored to generate over (OV) and under voltage (UV) disable in case of fault. The disable signal acts both internally and externally: in case of output disable due to failure on VDD5, the NDIS bidirectional pin is internally pulled down. The purpose is providing a feedback to the external microcontroller monitoring the device status. Detailed information about disable sources is given in the Section 6.1: Disable sources paragraph.

Range of characteristic is defined for VDD5 from **4.5 V** to **5.5 V**. In this range, the component works according to the specification without any restrictions and all parameters are in the specified range.

The table below lists the electrical characteristics of the VDD5 supply block.

Note: *$T_j = T_{j\_op}$; $V_{VPS\_UV} < V_{VPS} < 60$ V, all supplies are independent; 4.5 V < VDD5 < 5.5 V; 3.0 V < VIO < 5.5 V, unless otherwise noted.*

Table 8. **VDD5 supply block electrical characteristics**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{VDD5_opm}	VDD5 operating mode current	All outputs controlled ON	7	-	35	mA
I_{VDD5OV}	VDD5 current in case of overvoltage	5.5 V < VDD5 ≤ 36 V	8	-	40	mA
V_{VDD5_UV}	VDD5 UV threshold	Undervoltage	4.5	-	4.7	V
$V_{VDD5\_UV\_HYS}$	VDD5 UV hysteresis	VVDD5_UV	10	-	50	mV
t_{VDD5_UV1}	VDD5 undervoltage filter time	-	2	2.6	3.25	ms
$t_{VDD5\_UV\_react}$	VDD5_UV Comparator output reaction time	-	100	-	700	ns
t_{VDD5_UV2}	VDD5 under voltage filter time for NDIS activation	-	415	500	625	ms
V_{VDD5_OV}	VDD5 overvoltage disable threshold	Self-checked by HWSC	5.3	-	5.5	V
$V_{VDD5\_OV\_HYS}$	VDD5 OV disable hysteresis	-	10	-	50	mV
t_{VDD5_OV}	VDD5 overvoltage filter time	-	2.0	2.6	3.25	ms
$t_{VDD5\_OV\_react}$	VDD5_OV Comparator output reaction time	-	100	-	700	ns
V_{POR}	POR release threshold	Related to VDD5	4.15	-	4.45	V
V_{POR_HYS}	POR hysteresis	-	0.15	-	0.25	V
t_{POR_D}	POR RESET delay time	POR delay at startup of VDD5	10	-	50	μs

5.2.2 VPS supply block

The VPS pin is a battery supply. It is used for the internal charge pump to drive the N-channel external MOSFETs. The VPS line is monitored to detect low voltage on VPS. In case the voltage on VPS is lower than V_{VPS_UV} the pre-drivers are actively turned off. Such event is latched in **VPS_LATCH**, cleared on SPI readout. The undervoltage comparator output can be monitored reading **VPS_STATE** bit via SPI.

The table below lists the electrical characteristics for the VPS supply block:

Note: *$T_j = T_{j\_op}$; $V_{VPS\_UV} < V_{VPS} < 60$ V, all supplies are independent; 4.5 V < VDD5 < 5.5 V; 3.0 V < VIO < 5.5 V, unless otherwise noted.*

Table 9. **VPS supply block electrical characteristics**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{PS_leak}	Leakage on pin VPS	POR or NRES active; VPS ≤ 36V	-	-	20	μA
I_{VPS_OPM}	VPS operating mode current	-	3	-	50	mA

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{VPS_UV}	VPS low battery detection threshold	-	3.5	-	3.8	V
t_{VPS_react}	VPS Comparator output reaction time	-	100	-	700	ns
t_{LBD_FIL}	Filter time for VPS low battery detection	-	0.5	-	5	µs

5.2.3 VPS ADC

The device has an internal ADC monitoring VPS. Measure is obtained reading VPS_ADC[x] bit and applying the following conversion law:

Eq. (2): Battery monitor conversion law

$$V_{PS} = 0.048 \times CODE \tag{2}$$

The table below reports the electrical characteristics of the VPS ADC.

Note: *$T_j = T_{j\_op}$; all supplies are independent; 4.5 V < VDD5 < 5.5 V; 3.0 V < VIO < 5.5 V, unless otherwise noted.*

Table 10. **VPS ADC electrical characteristics**

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
ADC_res	Resolution	-	-	10	-	bit
f_{ADC}	Conversion rate	-	-	62.5	-	kHz
VPS_ADC_in	Input range VVPS	-	0	-	48	V
VPS_ACC	V_{VPS} accuracy	3.5 V < V_{VPS} < 12 V	-400	-	400	mV
		12 V < V_{VPS} < 48 V	-3.3	-	3.3	%

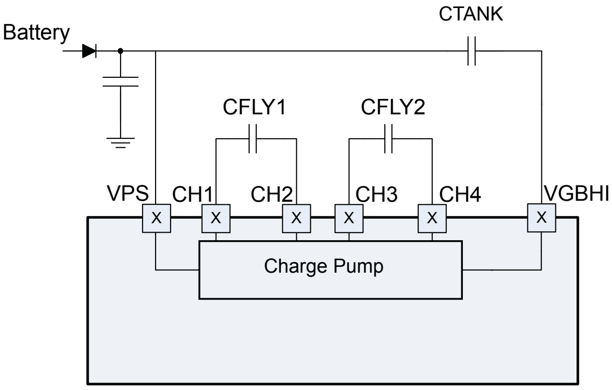
5.2.4 Charge pump (VGBHI)

To effectively bias the high side drivers and fail safe switch, a charge pump is used to drive the gate voltage above VPS. The charge pump switching frequency is nominally 200 KHz.

A built-in monitoring circuit checks if the charge pump output voltage is sufficient to control the high side valve driver. In case of undervoltage (VGBHI < VCP_UV), the outputs are actively turned off and **VCP_UV_LATCH** is set (readable via SPI, cleared on readout). The output of the undervoltage comparator can be monitored reading **VCP_UV_STATE** via SPI.

At power ON, the charge pump is enabled when VDD5 is above VPOR and NRES is not asserted.

Figure 11. **Charge pump connections**



Ratings:
CTANK: 16 V
CFLY1, CFLY2: 50 V for 12 V systems, 100 V for 48 V and 24 V systems.

The table below lists the electrical characteristics of the charge pump:

Note: *$T_j = T_{j\_op}$; $V_{VPS\_UV} < V_{VPS} < 60$ V, all supplies are independent; 4.5 V < VDD5 < 5.5 V; 3.0 V < VIO < 5.5 V, unless otherwise noted.*

Table 11. Charge pump electrical characteristics

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{VGBHI}	Charge pump voltage versus charge pump load current	VVPS ≥ 8 V; IVGBHI = 15 mA (DC)	VVPS+9	VVPS+12	VVPS+16	V
		VVPS_UV ≤ VVPS < 8 V; IVGBHI = 6 mA (DC)	VVPS+5	-	VVPS+16	V
f_{CP}	Charge pump frequency	Dependent on t_{SYS}	184	200	216	kHz
C_{TANK}	Charge pump tank capacitor	Connected to VPS IVGBHI = 15 mA	420	470	520	nF
C_{FLY}	Charge pump flying capacitors	Connected between CH1-CH2, CH3-CH4; IVGBHI = 15 mA	198	220	242	nF
V_{CP_UV}	Under voltage threshold	Referenced to VVPS	VVPS+3.9	-	VVPS+5.1	V
Vh_{CP_UV}	Under voltage hysteresis	Referenced to VVPS	250	-		mV
t_{CP_UV}	Under voltage filter time	-	10	-	30	µs
V_{VGBHI_MAX}	Charge pump max voltage	Referenced to GND	-	-	80	V
$t_{CPstartup}$	Startup time	-	-	-	2	ms
I_{BIAS_ON}	Internal absorption in when V_{GNSPx} = ON	Design info. Not tested in ATE	-	-	530	µA
I_{BIAS_OFF}	Internal absorption in when V_{GNSPx} = OFF	Design info. Not tested in ATE	-	-	480	µA

5.2.5 VIO supply pin & SDO pin characteristics

The VIO supply pin is used to feed SDO output driver. It can be connected either to 5 V or 3.3 V supply, in order to be compatible with different external I/O logic.

In case of an overvoltage condition at the SDO output, the SDO driver is switched off and eventual back feeding current towards VIO is blocked. Once the over-voltage is removed from SDO-pin, the output is re-activated at NCS low-to-high transition. SDO overvoltage event is latched in **SDO_OV_LATCH**, cleared via SPI readout.

Table below lists the electrical characteristics for the SDO output pin.

Note: *$T_j = T_{j\_op}$; $V_{VPS\_UV} < V_{VPS} < 60$ V, all supplies are independent; 4.5 V < VDD5 < 5.5 V; 3.0 V < VIO < 5.5 V, unless otherwise noted.*

Table 12. SDO pin electrical characteristics

Symbol	Parameter	Test condition	Min.	Max.	Unit
t_{sdo_trans}	SDO Rise and Fall time	C_{LOAD} = 20 to 150 pF	5	35	ns
t_{pcld}	Propagation delay – incl. Rise/Fall time (SCLK to data at SDO active)	C_{LOAD} = 150 pF	-	50	ns
t_{csdv}	NCS = LOW to output SDO active	C_{LOAD} = 150 pF	-	90	ns
t_{pchdz}	NCS L/H to SDO @ high impedance	-	-	75	ns
C_{IN_SPI}	Input capacitance at SDI; SDO; SCLK; NCS	-	-	10	pF
V_{SDOH}	High output level	ISDO = -2 mA	V_{IO} - 0.4 V	-	V
V_{SDOL}	Low output level	ISDO = 3.2 mA		0.4	V
I_{SDO_Leak}	Tri state leakage current	NCS = HIGH; $0 < V_{SDO} < V_{IO} – 0.3$ V	-5	5	µA

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{SDO_Leak}	Tri state leakage current	NCS = HIGH; $V_{SDO} = V_{IO} – 0.3$ V	-5	15	µA
		NCS = HIGH; $V_{SDO} = V_{IO}$	2	30	µA
V_{OV_SDO}	Over voltage detection threshold at SDO output (for reverse supply protection)	Prevent output from damage; avoid back supply to VIO; no hysteresis required	VIO + 0.05	VIO + 0.2	V
$t_{OV\_SDO\_fil}$	Overvoltage detection analog filter time	-	100	700	ns
$t_{OFF\_PROT\_OV}$	Overvoltage detection HS turn OFF/ON time at SDO.	Includes analog filter time and comparator reaction time until 50% IOVpeak_SDO_HS	0.5	5	µs
$I_{OVpeak\_SDO\_HS}$	Maximum possible peak reverse current at SDO HS before protection Turn Off	VSDO = 36 V; VIO = 3 V; limited by R_{DSON} only; HS channel On	90	250	mA

Note: The SDO pin electrical characteristics are also reported in the SPI table. SDO PCB trace must be routed carefully in order avoid spikes on SDO pin, which may generate an overvoltage failure. A pull-down resistor in the [10 - 47] kΩ range on SDO pin is also recommended.

5.3 Reset

The device is reset by the following two events:

Power On Reset (POR)

- 0 ≤ VDD5 ≤ VPOR:
  - Logic is reset;
  - Outputs are in three-state, diagnostics regulators for open load detection are OFF;
  - No violation of leakage current requirements;
  - Charge pump is disabled.
- VPOR ≤ VDD5 ≤ 4.5 V:
  - SPI functional (if VIO is stable);
  - Internal oscillator is functional and the logic is working correctly;
  - The outputs can switch according to the control;
  - Regulators for open load detection may provide wrong diagnostic;
  - Overcurrent shutdown is active but thresholds may be inaccurate.

NRES assertion:

- NRES input is active low;
- It is typically connected to the VDD5 reset of the ECU power supply;
- NRES is internally pulled up: in case of NRES pin left unconnected, NRES is inactive;
- Open load failure detection is inactive during NRES assertion;
- Charge pump is disabled while NRES is asserted.

Both POR and NRES events are latched and readable via SPI:

- After POR, the **n_POR_LATCH** is set and can be cleared via SPI readout;
- When NRES is active, **NRES_LATCH** is set and can be cleared via SPI readout.

The two reset events are ORed, so that full functionality is achieved only when both POR and NRES are released.

The default configuration for the outputs after reset is Low-Side with NFET. Channels are three-stated until the output is enabled through the **en_OUT_xx** bit.

After configuration and enable, all outputs follow the control signal as long as reset (NRES, POR) is not active. In case of a reset all outputs will be immediately disabled and all diagnostic and protection information will be lost.

5.4 Output pre-drivers

This paragraph contains the available configurations for the output pre-drivers. Enable and control strategies are explained. Output diagnostic is also explained, along with other useful application information.

5.4.1 Available configurations

There are eight pre-driver channels. Each channel can be independently configured in three different ways, via SPI configuration commands:

- Low-Side with NFET;
- High-Side with NFET;
- High-Side with PFET.

Channel side is programmed through **LS_HS_config_xx** bit, while FET type is selected through **N_P_config_xx** bit. Refer to Section 2: Output configurations in order to understand how the external FET must be mounted with respect to device pins. Complex configurations for Section 5.5: H-Bridge and Section 5.6: Peak & Hold are presented in their respective section.

5.4.2 Default configuration and output enable

After reset channels are configured as Low-Side with NFET by default. Outputs are in three-state until they are configured and enabled through the **en_OUT_xx** bit.

Channel 6 has an additional enable control via the EN6 input: **EN6** is in logical AND with en_OUT_06 bit, meaning that both signals have to be set high in order to enable the output driver. This feature makes it suitable for safety relevant load control. EN6 status can be monitored reading **EN6_STATE** bit via SPI. If channel 6 has been disabled setting EN6 low, the event is latched in **EN6_LATCH**, cleared on SPI readout.

5.4.3 Output control

The outputs can be controlled ON and OFF via SPI bit SPI_ON_OUTxx or input pins NONx. The selection of the control signal is independent for each channel and is programmed via the SPI_input_sel_xx bit:

- **SPI_input_sel_xx** = 0: control via NONx input
  - The NONx inputs are active low, meaning that the output is ON when the input is low and vice-versa
- **SPI_input_sel_xx** = 1: control via SPI_ON_OUTxx bit
  - The SPI_ON_OUTxx bit are positive asserted, meaning that the output is ON when the input is high and vice-versa

The table below summarizes output behavior depending on control strategy and control input.

Table 13. **Output status depending on control strategy and control input**

SPI_input_sel_xx	NONx	SPI_ON_OUTxx	External FET status
0	0	X(1)	ON
0	1	X	OFF
1	X	0	OFF
1	X	1	ON

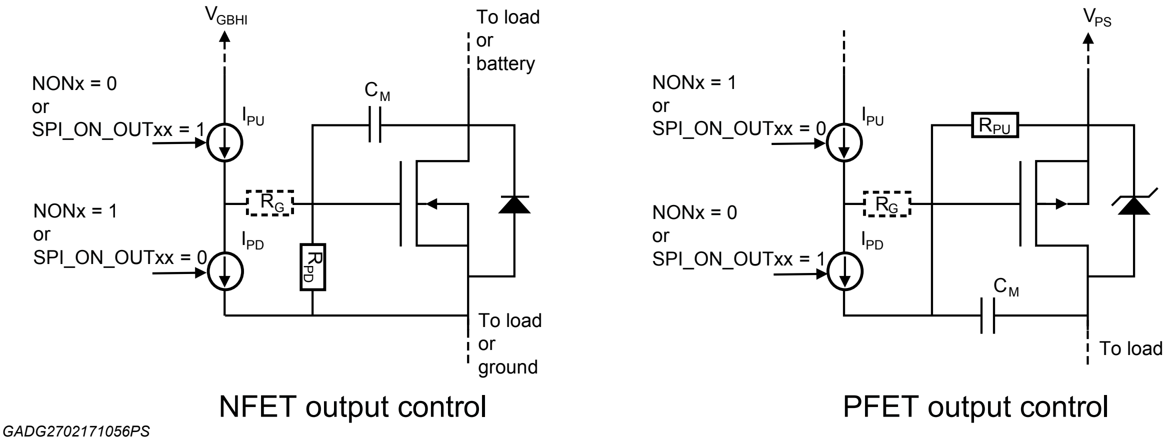
1. *All “X” = don't care.*

5.4.4 Gate charge/discharge currents

During normal operation external FET is actively switched ON/OFF by means of a pull up/pull down current source, as shown in Figure 12. Output pre-driver control.

Figure 12. **Output pre-driver control**

Ratings: C_M = 50 V for 12 V systems, 100 V for 24 V and 48 V systems.



NFET output control

PFET output control

The pull up/pull down currents can be programmed via SPI through the GCC_config_xx bit, as shown in the table below:

Table 14. **Selection of gate charge/discharge currents**

GCC_config_xx	I_{PU} / I_{PD} [mA]
00	Limited by external resistor (R_G) Internally clamped to I_{Ch0Gx}/I_{DCh0Gx}
01	20
10	5
11	1

In case GCC_config_xx is programmed "0b00", an external resistor RG is required for protecting the transistor gate against excessive current: the resistor must be mounted in series on the IPU / IPD path, as shown in Figure 12. Output pre-driver control. However, to prevent charge pump stress, the device internally limits the maximum charge/discharge current to ICh0Gx/IDCh0Gx (refer to Table 15. Output pre-driver stages electrical characteristics).

External measures have to be taken to keep the external MOS reliably OFF in case of output three-state. For external NMOS a gate pull down resistor RPD is needed and for external PMOS a gate pull up resistor RPU is necessary (refer to Figure 12. Output pre-driver control).

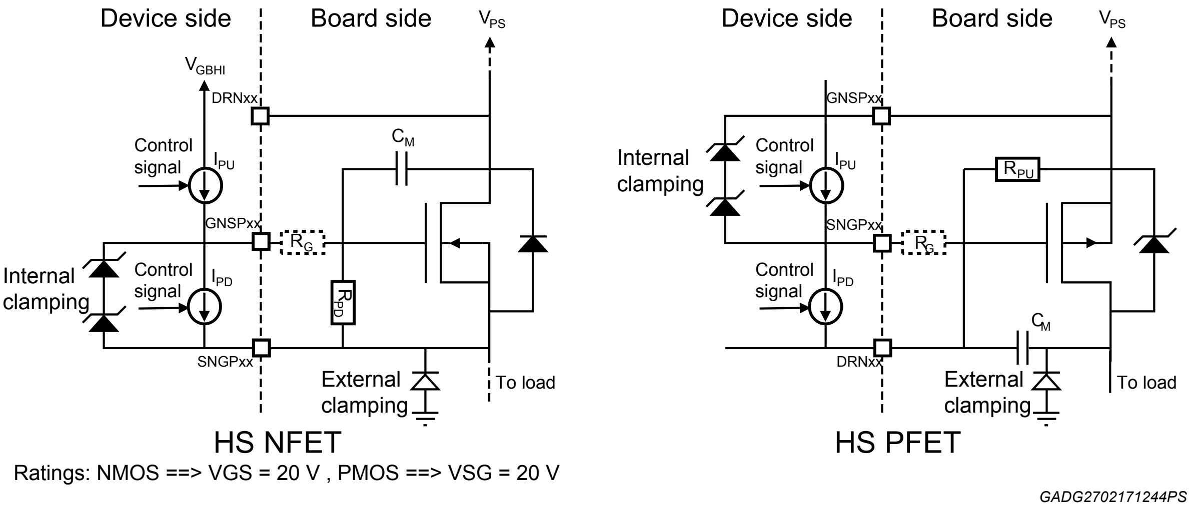
In order to improve EMI behavior, an external Miller capacitor CM can be mounted between transistor gate and drain. Value of this capacitor depends on:

- The switching frequency required by the application;
- The programmed charge/discharge current.

5.4.5 Internal and external clamping

The device guarantees a maximum gate to source voltage of 20 V by means of an internal clamping circuitry which limits the overdrive. However, such a clamp is not intended as a protection against external spikes or failures (STB/STG).

Figure 13. **Clamping for HS configuration**



Above figure shows the recommended clamping for the external FETs used in HS configuration. The internal clamping is meant to protect against overdrive but is not intended to be a recirculation path for the current. An external freewheeling diode is needed for inductive switching loads.

Figure 14. **Clamping for LS configuration**

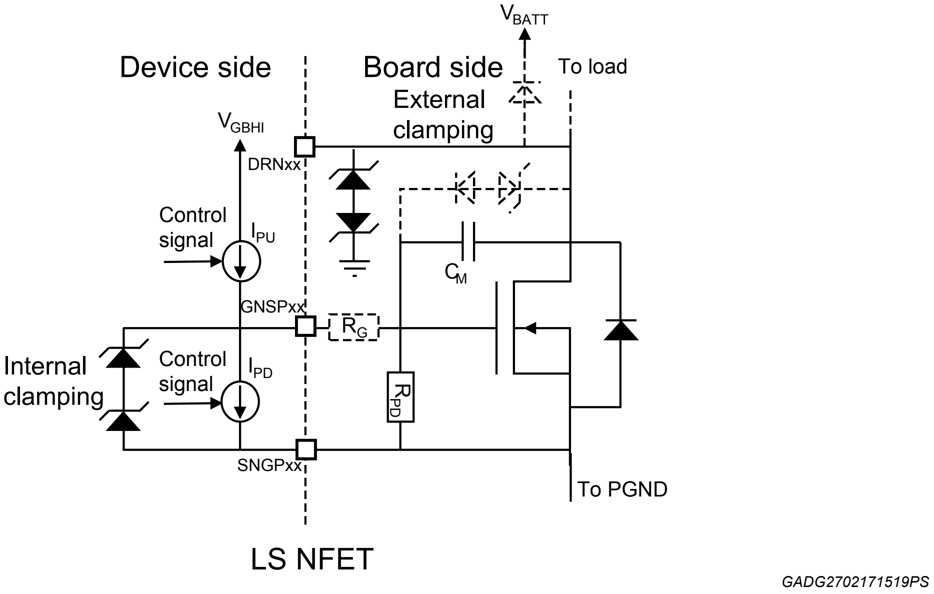


Figure 14. Clamping for LS configuration shows the recommended clamping solutions for the LS configuration. Voltage on the DRNx pin has to be limited to prevent component damage. A suppressor circuit can be used to clamp the voltage on DRNx pin (AMR is 60 V). For the freewheeling of inductive loads:

- A Zener feedback to the gate can be a solution to allow active freewheeling;
- A diode on DRNx pin can be used to allow passive freewheeling towards battery.

5.4.6 Electrical characteristics

The table below lists the electrical characteristics for the output pre-drivers.

Note: *$T_j = T_{j\_op}$; $V_{VPS\_UV} < V_{VPS} < 60$ V, all supplies are independent; 4.5 V < VDD5 < 5.5 V; 3.0 V < VIO < 5.5 V, unless otherwise noted. A current flowing out of the device has minus (-) sign; a current flowing into the device has plus (+) sign. Charge currents turn ON the NMOS and OFF the PMOS. Discharge currents turn OFF the NMOS and ON the PMOS.*

Table 15. **Output pre-driver stages electrical characteristics**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{GNSP} -V_{SNGP}	Gate Output voltage (Reversed for PMOS)	-	10	-	14	V
I_{Ch3Gx}	Gate charge current NMOS	GCC[1:0] = [1, 1]	-1.88	-	-1.1	mA
	Gate charge current PMOS		-1.85	-	-0.55	mA
I_{Ch2Gx}	Gate charge current NMOS and PMOS	GCC[1:0] = [1, 0]	-8.6	-	-4	mA
I_{Ch1Gx}	Gate charge current NMOS and PMOS	GCC[1:0] = [0, 1]	-32.4	-	-19.6	mA
I_{Ch0Gx}	Gate charge current NMOS	GCC[1:0] = [0, 0]	-100	-	-40	mA
	Gate charge current PMOS		-77	-	-43.5	mA
I_{DCh3Gx}	Gate discharge current NMOS and PMOS	GCC[1:0] = [1, 1]	0.75	-	1.9	mA
I_{DCh2Gx}	Gate discharge current NMOS and PMOS	GCC[1:0] = [1, 0]	3.8	-	7.4	mA
I_{DCh1Gx}	Gate discharge current NMOS and PMOS	GCC[1:0] = [0, 1]	16.8	-	27.4	mA
I_{DCh0Gx}	Gate discharge current NMOS and PMOS	GCC[1:0] = [0, 0]	55	-	101	mA
T_{sw_GC}	Delay to switch from GCC[a,b] to GCC[c,d]	-	-	-	0.1	µs
I_{peak}	Minimum peak current capability VPS > 7.5V	Tested at VPS > 7.5 V and output shorted to GND	40	-	-	mA
C_{LOAD}	Equivalent capacitive load to be driven	-	0.1	-	-	nF
t_{d_OFF}	Turn ON/OFF delay 50% NONx to 50% OFF gate current	test condition: 0.1 nF checked for LS/HS config (switch)	-	-	1.5	µs
t_{d_ON}	Turn OFF/ON delay 50% NONx to 50% ON gate current	test condition: 0.1 nF checked for LS/HS config (switch)	-	-	1.5	µs
I_{CR_CON}	Pre-driver Cross conduction current	guaranteed by design	-	-	2	mA
I_{LEAK_Gx}	GNSPx leakage current in tristate	GNSP-SNGP voltage requirements < 20 V in case of external P-channel (Gate to SNGPx)	-10	-	10	µA
I_{DRNx}	DRNx input leakage current	POR or NRES active; V_DRNx = 0 V to 28 V	-10	-	10	µA
I_{LEAK_S}	SNGPx input leakage current	POR or NRES active or Normal mode; V_SNGPx = 0 V to 52 V	-10	-	10	µA
$V_{\mathbf{GNSP}}$-$V_{\mathbf{SNGP}}$	GNSP to SNGP voltage when OFF gate current is on	-	-	-	100	mV

5.5 H-Bridge

The pre-drivers can be configured into two independent H-Bridges. In this configuration Channels 1-4 are used for H-Bridge 1, while Channels 5-8 are used for H-bridge 2.

The device can handle up to two H-bridge. There are two possible configurations which can co-exist:

- **H-Bridge 1**: it involves channels 1 (HS), 2 (HS), 3 (LS) and 4 (LS) and can be activated by setting **HB1_config = 1**
- **H-Bridge 2:** it involves channels 5 (HS), 6 (HS), 7 (LS) and 8 (LS) and can be activated by setting **HB2_config = 1**

Configurations above are automatically applied once the HBx_config bit is set.

The **N_P_config_xx** bit set the MOSFET type (NMOS, PMOS) used in the H-bridge high-side. For H-bridge 2, **EN6** must be set high to enable channel 6.

5.5.1 H-Bridge driving modes

The H-Bridge must be controlled via the external NONx pins. Such inputs have different meanings while in H-Bridge mode:

Table 16. **NONx signals in H-bridge configuration**

HB1	HB2	Signal description
NON1	NON5	NPWM – Negative asserted Pulse Width Modulation signal
NON2	NON6	DIR – Direction signal
NON3	NON7	HiZ – High Impedance (all FETs actively switched off, load floating)
NON4	NON8	Not used

Any attempt to control channels via SPI is ignored while H-Bridge mode is active.

In driving mode the H-bridge work according to the following table:

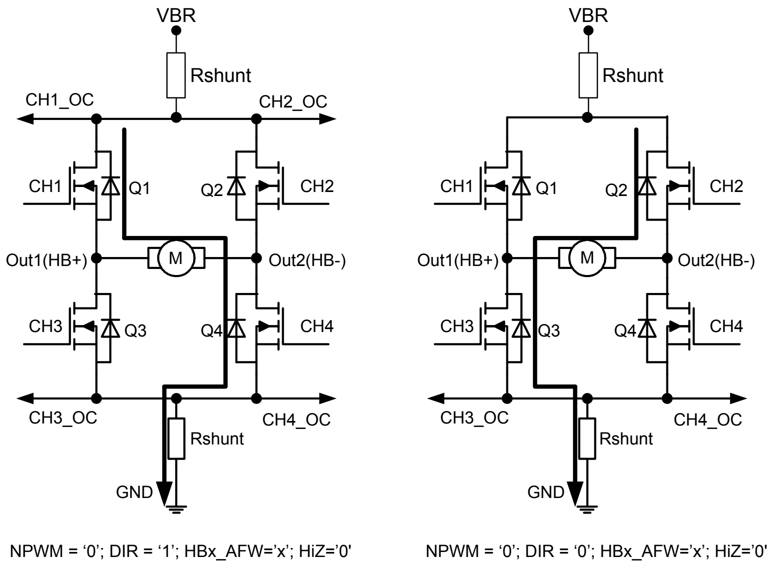
Table 17. **Truth table**

HiZ	DIR	NPWM	HBx_AFW	Q1	Q2	Q3	Q4	Load’s driving direction
0	0	0	X [1]	OFF	ON	ON	OFF	Reverse
0	0	1	0	OFF	OFF	ON	OFF	Freewheeling (reverse)
0	0	1	1	OFF	OFF	ON	ON	Active freewheeling (reverse)
0	1	0	X	ON	OFF	OFF	ON	Forward
0	1	1	0	OFF	OFF	OFF	ON	Freewheeling (forward)
0	1	1	1	OFF	OFF	ON	ON	Active freewheeling (forward)
1	X	X	X	OFF	OFF	OFF	OFF	High Impedance

1. *X = don't care.*

The freewheeling is performed on low side, as shown in Figure 15. H-bridge driving configurations. Software brake mode can be performed by setting the active freewheeling bit (**HBx_AFW**).

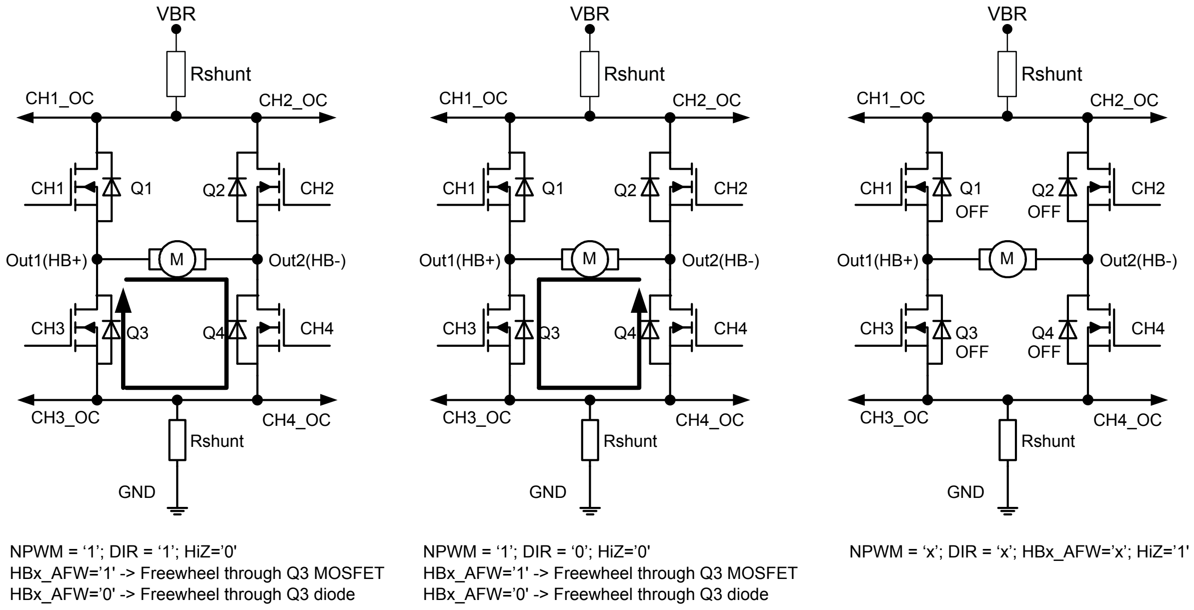
Figure 15. **H-bridge driving configurations**



(Active) Freewheeling
low-side (forward)

(Active) Freewheeling
low-side (reverse)

High impedance



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5.5.2 H-Bridge diagnostics

H-bridge status can be monitored by reading each channel diagnostic as if they operated independently (refer to Section 6.2: Diagnostics overview). However, different OC sensing strategies can be implemented, as discussed in Overcurrent detection. While in H-Bridge configuration, an extended set of values is available for OFF state diagnostic timer (t_{DIAG}), as shown in H-Bridge OFF state diagnostic timings.

5.5.3 H-bridge dead time

To prevent shoot-through (e.g. Q1 and Q3 ON) it's possible to choose different dead time values for both H-bridges independently. Such parameters are selectable via SPI through the **HBx_dead_time** bit according to the following table.

Table 18. **Dead time values**

HBx_dead_time [1]	HBx_dead_time [0]	Dead time (min)	Dead time (typ)	Dead time (max)	Unit
0	0	0.5	1	1.5	µs
0	1	1	2	3	µs
1	0	3	4	5	µs
1	1	7	8 (default)	9	µs

Note: *x = H-bridge number*

The dead time intervenes in case of H-Bridge direction change, that is upon DIR transitions. The following table describes the output behavior in case of DIR transition.

Table 19. **Output response in case of DIR transition**

DIR Transition	Q1/Q5	Q2/Q6	Q3/Q7	Q4/Q8
0 → 1	Turns ON after **HBx_dead_time**, if **NPWM** was **‘0’** before DIR switch and did not toggle during dead time	Turns OFF immediately	Turns OFF immediately	Turns ON after **HBx_dead_time**
1 → 0	Turns OFF immediately	Turns ON after **HBx_dead_time**, if **NPWM** was **‘0’** before DIR switch and did not toggle during dead time	Turns ON after **HBx_dead_time**	Turns OFF immediately

Note: *NPWM should be stable before applying the DIR transition, and it should not be switched during the dead-time due to DIR switch. Otherwise, once dead-time for DIR switch event has expired, the dead-time for NPWM transition will start, resulting in twice the dead-time applied.*

Once NPWM has been toggled at t_{NPWM_SWITCH} time instant, DIR input shall not be switched within a defined grey-zone in respect to t_{NPWM_SWITCH} . Grey zone is defined by:

$$t_{GREY} = t_{\mathrm{NPWM\_SWITCH}} + HBx\_dead\_time \pm \frac{5}{f_{MAIN\_CLK1}}$$

The dead timers also operate during NPWM switching activity. Transitions are described in the following table.

Table 20. **Output response in case of NPWM transition**

	DIR = 1	DIR = 0	DIR = 1		DIR = 0	
NPWM Transition	**Q1/Q5**	**Q2/Q6**	**Q3/Q7**		**Q4/Q8**	
			HBx_AFW = 0	HBx_AFW = 1	HBx_AFW = 0	HBx_AFW = 1
0 → 1	Turns OFF after **HBx_dead_time** if **NPWM** is still ‘1’	Turns OFF immediately	Kept OFF	Turns ON after **2*HBx_dead_**time if **NPWM** is still **‘1’**	Kept OFF	Turns ON after **2*HBx_dead_**time if **NPWM** is still **‘1’**
1 → 0	Turned OFF immediately. Then, it turns ON after **HBx_dead_time** if **NPWM** is still ‘0’	Turns ON after **HBx_dead_**time if **NPWM** is still **‘0’**	Kept OFF	Turned OFF immediately	Kept OFF	Turned OFF immediately

Note: *in case NPWM is switched with a very high frequency, which is incompatible with **HBx_dead_time**, the HS will be kept OFF. This happens because every time NPWM toggles 1 → 0, the HS output is reset to its default value of ‘0’. However, this condition should be avoided by choosing switching frequency and duty-cycle in order to allow dead-timer to expire after both transitions.*

5.5.4 H-bridge disabling

When DIS/NDIS is asserted the H-bridge is disabled and all the pre-drivers are actively turned off. The same behavior is observed when HiZ or NRES is asserted.

Table 21. **H-bridge state for different DIS/NDIS and NRES**

NRES	HiZ	HBx_config	DIS	NDIS	H-bridge state
0	0	1	0	1	All 4 MOSFET actively OFF
1	1	1	0	1	All 4 MOSFET actively OFF
1	0	1	0	0	All 4 MOSFET actively OFF
1	0	1	0	1	Normal operation
1	0	1	1	0	All 4 MOSFET actively OFF
1	0	1	1	1	All 4 MOSFET actively OFF

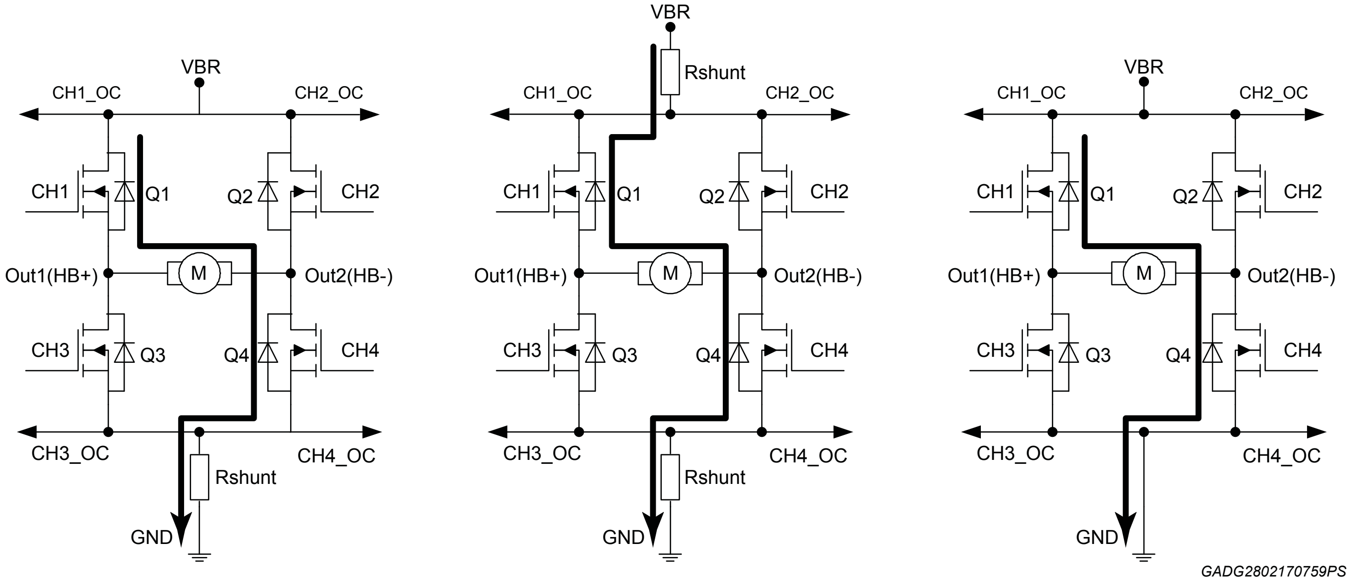
HBx_config must not be changed while H-Bridge is operating.

5.5.5 Overcurrent detection strategies for H-Bridge

The over current detection can be performed either by measuring the voltage drop on external shunt resistors or through the Drain to Source Measurement of each transistor (DSM). Each transistor of the H-Bridge can detect overcurrent independently. If an OC event occurs on a channel, the four devices will be actively shut-off and H-Bridge outputs will be three-stated. Diagnostic latches have always to be cleared before re-engaging the H-Bridge after an overcurrent detection. Different scenarios for OC detection are possible:

- OC detection through one shunt resistor mounted on the low-side between SNGPx and PGNDxx pins, as shown in Figure 16. OC detection strategies for H-Bridge: (left) one shunt resistor for LS, DSM for HS; (center) two shunt resistors; (right) DSM. DSM used for OC detection on the HS transistors.
  - To avoid inhomogeneous OC protection over the H-Bridge, OC threshold programmed for HS via DSM must be adapted to the ones programmed on the LS via shunt sensing. OC threshold adaption must account for the RDSon of the HS devices.
- OC detection through two shunt resistors. The first mounted on the low-side between SNGPx and PGNDxx pins, the second mounted on the high-side between GNSPx (PMOS)/DRNx (NMOS) and BATTxx pins (see Figure 16. OC detection strategies for H-Bridge: (left) one shunt resistor for LS, DSM for HS; (center) two shunt resistors; (right) DSM).
  - To avoid inhomogeneous OC threshold for the H-Bridge, the two shunt resistors must be equal and the four OC thresholds must hold the same value.
- OC detection through DSM (see Figure 16. OC detection strategies for H-Bridge: (left) one shunt resistor for LS, DSM for HS; (center) two shunt resistors; (right) DSM)
  - In case the 4 MOSFETs are equal, the 4 OC thresholds must be equal;
  - In case the 2 FETs used on high-side are different from the ones on low-side, a different value for OC threshold must be specified for the HS pair. OC threshold adaption must account for the RDSon of the HS devices.

Figure 16. **OC detection strategies for H-Bridge: (left) one shunt resistor for LS, DSM for HS; (center) two shunt resistors; (right) DSM**



When shunt measurement is selected, current limitation feature is available.

- In case current limitation feature is enabled (**HBx_ILIM_en** = 1), the comparator on CH3/CH7 is used for current limitation while the one on CH4/CH8 detects OC. In order to guarantee full protection of the load and the FETs, CH4/CH8 overcurrent comparator is enabled even if transistor is OFF phase. Therefore, in case Rshunt is shorted to battery, the OC event will be immediately detected;
- In case current limitation feature is disabled (**HBx_ILIM_en** = 0), both LS channels are used for OC detection. OC comparators are active only in the ON phase of the transistors.

OC detection timings depend on the selected sensing strategy, as explained in Section 6.3.3: OC sensing strategy. Once an actual OC event has been recognized, behavior depends on the current limitation feature:

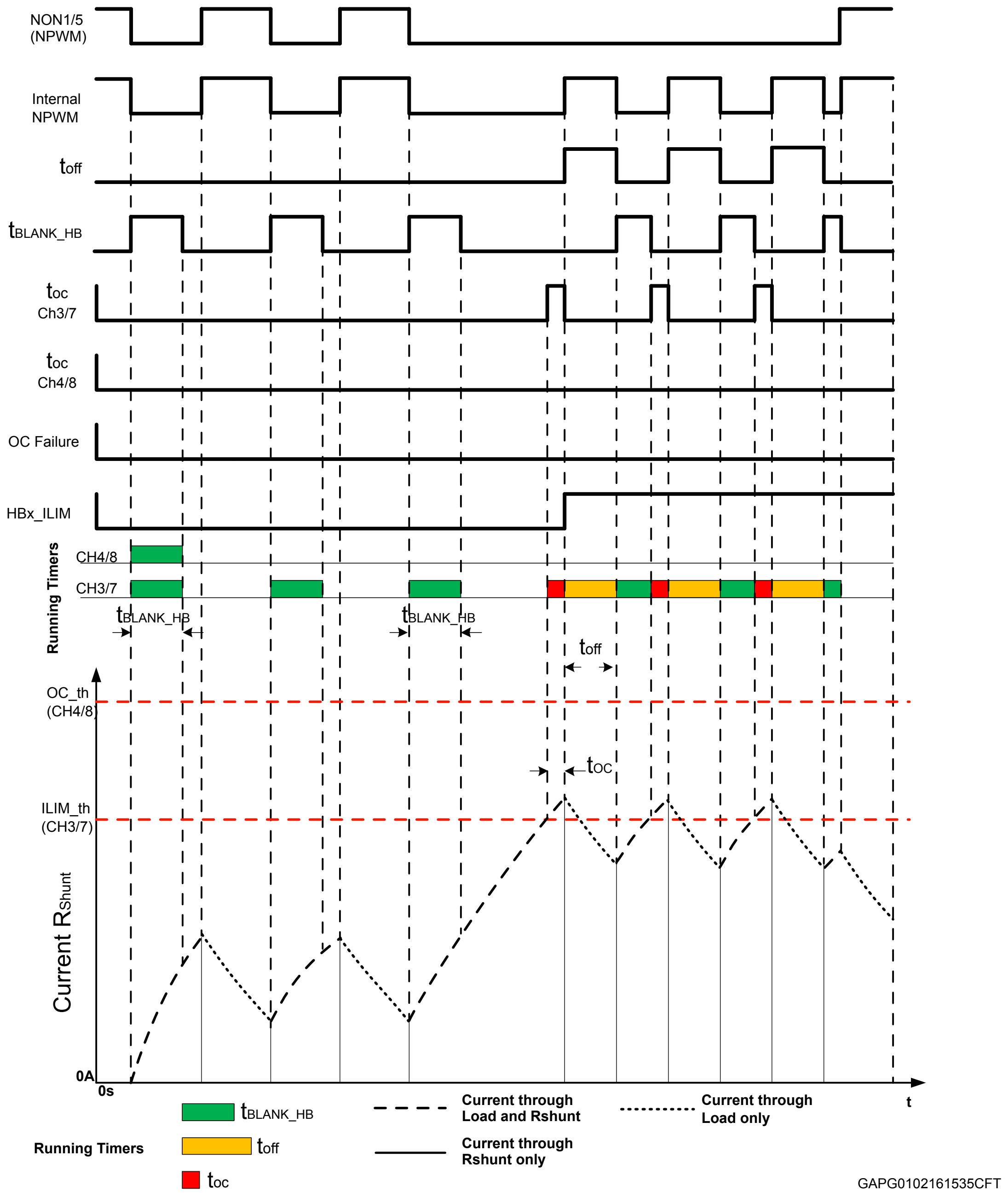
- If **HBx_ILIM_en** = 0, the current limitation feature is disabled and the H-Bridge is three-stated (all FETs actively OFF, load floating);
- If **HBx_ILIM_en** = 1, the current limitation feature is enabled. The device will limit the current one more time after OC threshold crossing and, in case of failure still persisting, the H-Bridge is three-stated (all FETs actively OFF, load floating) after t_{OC} + t_{OFF} (refer to Figure 18. Current limitation iterations (until OC failure)).

5.5.6 Current limitation for H-Bridge

Current limitation feature is able to limit the maximum current in the load modulating the NPWM signal, as shown in Figure 17. Current limitation timing diagram. This allows keeping the current of the load below the current limitation threshold (ILIM_th). Current limitation function is available only when shunt measurement is selected and can be activated setting **HBx_ILIM_en** = 1.

Current limitation threshold (I LIM_th) is set by **OC_config_03** [5-0] bit for H-bridge 1 and **OC_config_07** [5-0] bit for H-Bridge 2. Hence, channel 3 is no longer used for OC detection in H-Bridge 1, but it activates the current limitation. The same function is implemented on channel 7 in H-Bridge 2.

Figure 17. **Current limitation timing diagram**



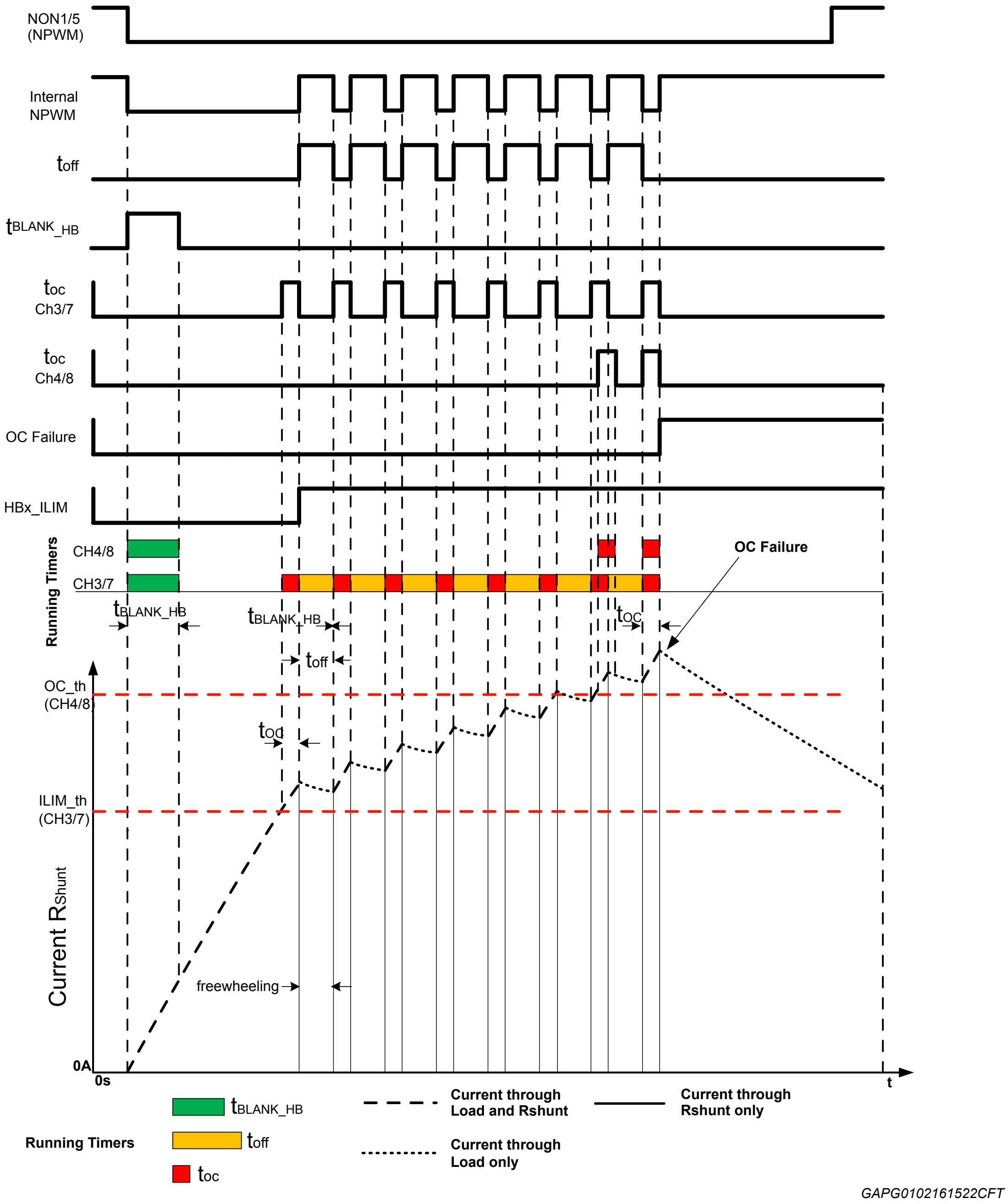
If the current stays above the programmed threshold (I_{LIM_th}) longer than t_{OC}, the H-bridge is driven into freewheeling phase (active freewheeling or not, depending on HBx_AFW bit) for a programmable OFF time (t_{OFF}). During t_{OFF}, high-side outputs are actively OFF but low-side outputs remain controlled according to DIR and HBx_AFW values, performing a freewheeling action on the low-side.

Once t_{OFF} expires, load current is compared against ILIM_th threshold:

- In case load current is below I_{LIM_th}, normal operation can continue (refer to Figure 17. Current limitation timing diagram).
- In case current is not below I_{LIM_th}, the high-side channel is turned on for a t_{FIL_ON} + t_{OC} period and then turned off for another t_{OFF} time. Such operation continues until either the current decreases below I_{LIM_th} or the current reaches the overcurrent threshold and H-Bridge is three-stated (all FETs actively OFF, load floating) (refer to Figure 18. Current limitation iterations (until OC failure)).

Note: *since current limitation makes use of shunt sensing, the blanking time programmed for CH3/CH7 has no effect in detection timings. The blanking time has only effect on FETs using DSM.*

Figure 18. **Current limitation iterations (until OC failure)**



When current limitation threshold is reached for the first time, a dedicated HBx_ILIM latch is set, indicating that current limitation function has been activated. This latch is cleared on SPI readout.

The OFF time interval for current limitation (t_{OFF}) is selectable via SPI according to HBx_toff bit:

Table 22. **t_{OFF} selection**

HBx_toff [1-0]	Min t_{OFF} value	Typical t_{OFF} value	Max t_{OFF} value	Unit
00	28	31	34	µs

HBx_toff [1-0]	Min t_{OFF} value	Typical t_{OFF} value	Max t_{OFF} value	Unit
01	42	48	52	µs
10	56	62.5	70	µs
11	110	125	140	µs

5.5.7 H-Bridge OFF state diagnostic timings

The device offers the possibility to select the OFF state diagnostic filter times t_{DIAG} among two different strategies, selectable via **HBx_tdiag_ext_config** bit (refer to Table 23. OFF state diagnostic timings for H-Bridge):

- When **HBx_tdiag_ext_config** = 0, the diagnostic filter time t_{DIAG} selected for CH1 (CH5) is automatically extended to all channels member of the bridge;
- When **HBx_tdiag_ext_config** = 1, the diagnostic filter time t_{DIAG} must be set individually for each channel member of the bridge.

Regardless of the strategy selected, the t_{DIAG} filter time can be programmed via **tdiag_config_xx** bit.

Table 23. **OFF state diagnostic timings for H-Bridge**

Symbol	tdiag_config_xx	Parameter	Min.	Typ.	Max.	Unit	Comment
$T_{HB\_diag\_1}$	00	H-Bridge Diag Time 1	10	11.2	12.4	µs	HBx_tdiag_ext_config = 0 (all channels set as CH1/CH5)
$T_{HB\_diag\_2}$	01	H-Bridge Diag Time 2	26	28.9	31.8	µs	
$T_{HB\_diag\_3}$	10	H-Bridge Diag Time 3	36	40	44	µs	
$T_{HB\_diag\_4}$	11	H-Bridge Diag Time 4	46	51.2	56.4	µs	
$T_{DIAG\_HB\_100}$	00	H-Bridge Diag Time 1	23	25.6	28.2	µs	HBx_tdiag_ext_config = 1 (channels to be set individually)
$T_{DIAG\_HB\_101}$	01	H-Bridge Diag Time 2	55	61.2	67.4	µs	
$T_{DIAG\_HB\_110}$	10	H-Bridge Diag Time 3	95	105.6	116.2	µs	
$T_{DIAG\_HB\_111}$	11	H-Bridge Diag Time 4	135	150	165	µs	

5.6 Peak & Hold

The pre-drivers can be configured into two independent peak & hold blocks. In this configuration Channels 1,4 are used for Peak & Hold 1, while Channels 2,3 are used for Peak & Hold 2.

The device can handle up to two Peak & Hold branches. There are two possible configurations which can co-exist:

- **Peak & Hold 1**: it involves channels 1 (HS) and 4 (LS) and can be activated by setting PH1_config = 1;
- **Peak & Hold 2**: it involves channels 2 (HS) and 3 (LS) and can be activated by setting PH2_config = 1.

Configurations above are automatically applied once the **PHx_config** bit is set.

The **N_P_config_xx** bit set the MOSFET type (NMOS, PMOS) used in the Peak & Hold high-side.

5.6.1 Peak & Hold driving mode

All channels involved in the peak & hold configuration can be driven independently either via the corresponding **NONx** pin or via SPI, depending on **SPI_INPUT_SEL_xx** bit. An external microcontroller shall close the control loop in order to guarantee the desired current profile in the load. The device does not feature any internal current control capability while in peak & hold configuration.

5.6.2 Peak & Hold diagnostics

When in peak & hold configuration, diagnostic is performed independently on each channel, as if a low-side or high-side configuration was applied. The external microcontroller monitoring the device must properly combine the diagnostic information of the high-side channel to the one read on the low-side channel in order to determine the eventual fault type. Refer to Table 36. Diagnostic codes for the diagnostic codes.

5.6.3 ON state diagnostics

ON state diagnostic latches are updated only when both channels are switched ON, that is, only when the current is supposed to actually flow in the load. In case an OC event occurs on a channel while the other is switched OFF, OC protection is triggered and the external FET is protected, but the diagnostic code of that channel is not updated. OC event will be eventually confirmed once both channels are switched ON (OC or OC pin will be reported).

When in peak & hold configuration, the device protects the external FET against overcurrent as in the HS/LS configuration. However, an additional diagnostic code is available for this configuration:

- If an overcurrent event occurs while the output is switching ON (tblank_oc timer still running), an OC pin failure is stored in the diagnostic latches → code "000"
- If an overcurrent event occurs while the output is fully ON (tblank_oc timer expired), an OC failure is stored in the diagnostic latches → code "001"

In order to detect **a short across the load** (SCL) failure, when an OC/OC pin event occurs simultaneously on HS and LS, an OC pin failure is latched for both sides.

5.6.4 OFF state diagnostics

When both HS and LS are commanded OFF by the control signal, an intentional open load occurs on both load pins (refer to Section 6.4.3: Internal regulator for open load (OL) detection). In order to avoid false OL detection, OL fault is masked in this condition. The diagnostic code reported in such case can be selected by programming the **PHx_diag_strategy** bit:

- **If PHx_diag_strategy = 0, "No OL/STG/STB failure"** is reported → code "110";
- **If PHx_diag_strategy = 1, "No diagnostic done"** is reported → code "111".

OL detection is guaranteed in case HS and LS have different states. In normal HS/LS configuration, the OFF diagnostic filter timer t_{DIAG} is started every time a channel is switched OFF. In peak & hold configuration, two additional events generate a start condition for t_{DIAG}:

- HS OFF, LS OFF → ON;
- LS OFF, HS OFF → ON.

Therefore, an eventual OL fault is detected as soon as one of the two transistor is switched ON (after t_{DIAG})

While HS is in the OFF state, if the voltage on the load node rises above VOL, the fast discharge current is activated to prevent false STB detection (refer to Section 6.4: OFF state diagnostics and Section 6.4.4: Fast charge/discharge currents). Referring to Figure 19. Possible faults in peak & hold configuration, Table 24. Diagnostic strategy for peak & hold configuration shows the possible faults in peak & hold configuration, along with the diagnostic strategy. Refer to Table 36. Diagnostic codes for the diagnostic codes.

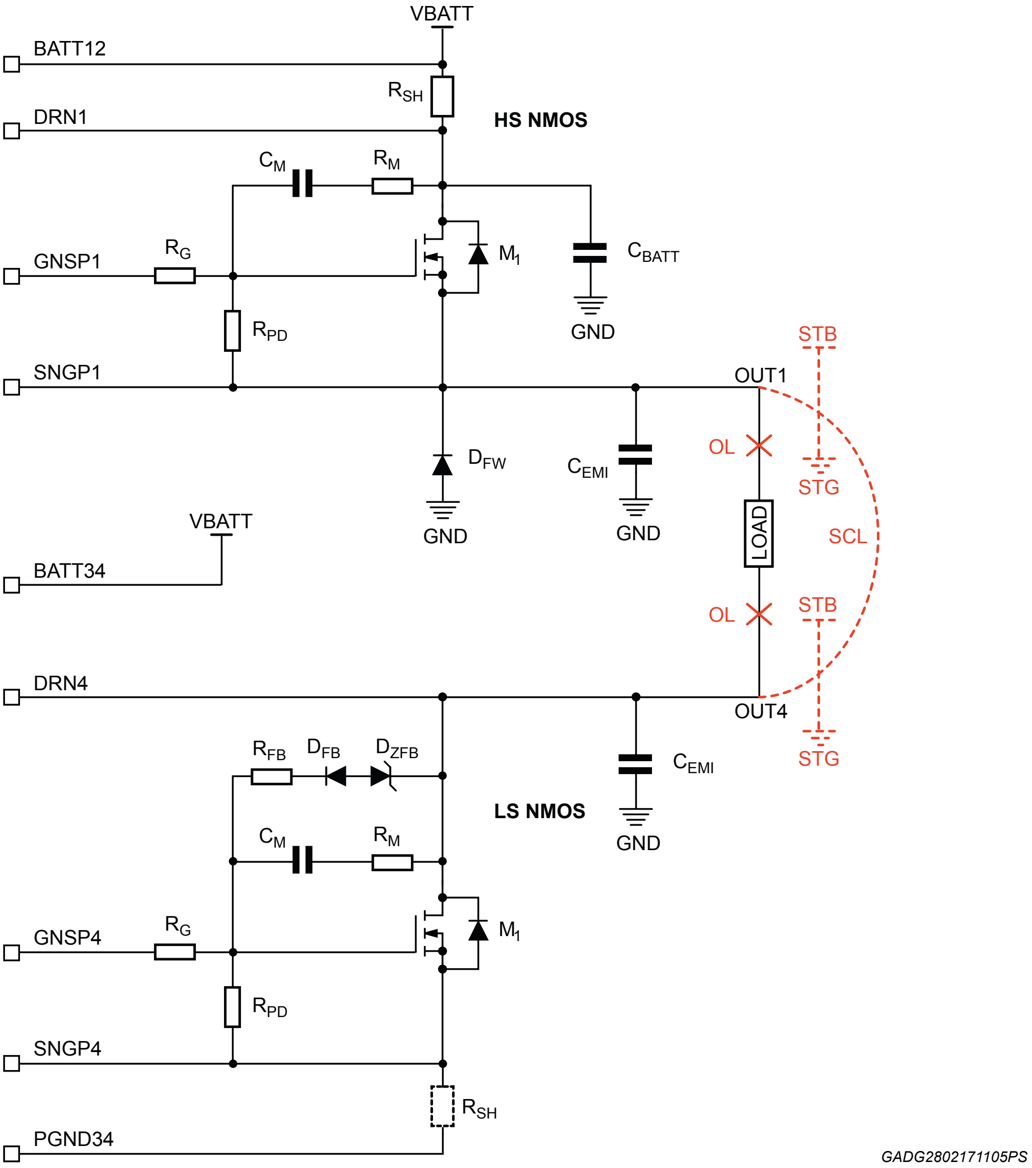
Note: Table 24. Diagnostic strategy for peak & hold configuration has been compiled under the assumption of all channels starting from "No failure" state (100). Such state is reached during normal operation of the circuit when no failure has been detected by both OFF and ON state diagnostics. Therefore, the diagnostic strategy can be applied if at least one ON/OFF switching cycle has been completed without failures. In case the starting state was "No diagnostic done", the "No failure" state can be replaced with "No OL/STG/STB failure" (110) for OFF state diagnostics and with "No OC failure" (101) for ON state diagnostics. Diagnostic codes follow a priority concept. Diagnostic latches are reset in case of NRES/POR assertion or in case of SPI readout. Refer to Section 6.2: Diagnostics overview to understand priority and FSM algorithm.

Table 24. Diagnostic strategy for peak & hold configuration

Fault type	Circuit state							
	HS OFF LS OFF		HS ON LS OFF		HS OFF LS ON		HS ON LS ON	
	HS	LS	HS	LS	HS	LS	HS	LS
OUT1 STB	STB	No fail	No fail	No fail	STB	No fail(1)	No fail(2)	No fail(1)
						OC(1)		OC(1)
OUT1 STG	No fail	STG	OC	STG	No fail	No fail	OC	No fail (2)
			OC pin(3)				OC pin(3)	
OUT1 OL	No diag(4)	No diag(4)	No fail	OL	OL	No fail	No fail (2)	No fail (2)
	No STB/STG/OL(4)	No STB/STG/OL(4)						
OUT4 STB	STB	No fail	No fail(2)	No fail	STB	OC	No fail	OC
						OC pin(3)		OC pin(3)
OUT4 STG	No fail	STG	No fail(1)	STG	No fail	No fail(2)	No fail(1)	No fail(1)
			OC(1)				OC(1)	
OUT4 OL	No diag(4)	No diag(4)	No fail	OL	OL	No fail	No fail (1)	No fail(1)
	No STB/STG/OL(4)	No STB/STG/OL(4)						
OUT1-OUT4 short (SCL)	No diag(4)	No diag(4)	No fail	No fail	No fail	No fail	OC pin(3)	OC pin(3)
	No STB/STG/OL(4)	No STB/STG/OL(4)						

1. *Current limited by the load. In case current is greater than the OC threshold, protection is triggered and external FET is shut OFF. However, diagnostic latches are not updated.*
2. *Current in the shunt resistor is 0 mA. Micro may monitor.*
3. *Depending on transistor switch ON delay and configured tblank_oc.*
4. *Depending on* ***PHx_diag_strategy****.*

Figure 19. **Possible faults in peak & hold configuration**



5.7 Internal oscillator

The device has an internal oscillator providing the timing and control for all device operating functions. The nominal clock frequency is 10 MHz. The oscillator is functional when VDD5 > VPOR.

5.7.1 Spread spectrum

In order to minimize the noise generated by the internal clock signal, the device offers the spread spectrum functionality. Such feature is disabled by default and can be activated by programming the **spread_spectrum** bit.

5.7.2 Internal oscillator electrical characteristics

The table below reports the detailed electrical characteristics of the internal oscillator.

Note: *$T_j = T_{j\_op}$; $V_{VPS\_UV} < V_{VPS} < 60$ V, all supplies are independent; 4.5 V < VDD5 < 5.5 V; 3.0 V < VIO < 5.5 V, unless otherwise noted.*

Table 25. **Internal oscillator electrical characteristics**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
f_{MAIN_CLK1}	Clock Frequency	-	-	10	-	MHz
tol_{MAIN_CLK}	Tolerance of frequency of internal clock oscillator	Spread spectrum disabled; $4.5\ V < V_{VDD5} \leq 36\ V$	-7.7	f_{MAIN_CLK1}	7.7	%
$f_{MOD\_range\_MAIN}$	Clock frequency modulation range spread spectrum enabled	-	-4	-	4	%
f_{MOD_MAIN}	Spread spectrum modulation frequency	-	-	80	-	kHz

5.8 Digital I/Os

Table 1. Pin list reports each pin functionality, along with the pull-up/pull-down implementation. Back supply current into any digital pin is not allowed.

For detailed information about the functionality of the SPI related pins (SCK, SDI, SDO, NCS), refer to Section 5.9: Serial Peripheral Interface (SPI). For the electrical characteristics of the SDO output refer to Section 5.2.5: VIO supply pin & SDO pin characteristics.

For detailed information about the functionality of the reset pin (NRES), refer to Section 5.3: Reset.

For detailed information about the functionality of the channel control pins (NONx and EN6), refer to Section 5.4: Output pre-drivers.

For detailed information about the functionality of the device disable pins (DIS and NDIS), refer to Section 6.1: Disable sources.

5.8.1 Digital I/Os electrical characteristics

The table below lists the electrical characteristics for the digital pins.

Note: *$T_j = T_{j\_op}$; $V_{VPS\_UV} < V_{VPS} < 60\ V$, all supplies are independent; $4.5\ V < VDD5 < 5.5\ V$; $3.0\ V < VIO < 5.5\ V$, unless otherwise noted.*

Table 26. **Digital I/Os electrical characteristics**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{IN_L}	Low input level	-	-	-	0.75	V
V_{IN_H}	High input level	-	1.75	-	-	V
V_{IN_HYS}	Hysteresis	-	0.1	-	0.5	V
I_{PU}	Input pull-up current source	NONx, NRES, DIS, NCS, SDI, SCK	-30	-	-100	μA
I_{PD}	Input pull-down current sink	NDIS, EN6	30	-	100	μA
t_{FIL_a}	Filter time	Applies to NRES, DIS, NDIS	0.5	-	5.0	μs
V_{NDISL}	Low output level for NDIS bidirectional pin	VDD5 > VPOR; I_{NDIS} = 5 mA	-	-	0.4	V

Note: *The NDIS bidirectional pin features internal protection against overvoltage when used as output. Such electrical characteristics are listed in the Section 6.1.1: DIS & NDIS pins paragraph.*

5.9 Serial Peripheral Interface (SPI)

The device is equipped with a Serial Peripheral Interface implementing a 32-bit, synchronous, full duplex, serial protocol. The interface is used to configure the device by programming its internal registers. Device status and diagnostic information can also be read via SPI.

5.9.1 SPI Quick Look

Table 27. **SPI quick look**

Parameter	Value
Frame length	32 bit or multiple
SPI Mode	Mode 1 (CPOL = 0 & CPHA = 1)
Max Frequency	5 MHz
Protocol	Out of frame
Chip Select Signal Active State	Active Low
Endianess	MSB first

The SPI can work in two different ways: parallel operation and daisy chain. These two methods can co-exist, as shown in Figure 20. Daisy chain and parallel operation, where a parallel communication is implemented between a master device and three sub-blocks. Two of them are daisy chains while the last one is made of a single device. In the example, three Chip Select (CS) wires are used for communicating with 6 devices.

5.9.2 Parallel operation

In parallel operation the communication is performed between a device, named master and one or more devices, named slaves. The master can start/stop the communication and generates the clock signal. Each slave device has a dedicated chip select (CS) signal, used to address the communication between the master and the selected slave.

5.9.3 Daisy chain

In daisy chain configuration, master device can communicate with several slaves using only one wire for chip select (CS). All the slaves in the daisy chain are selected when the CS is in the active state. The serial output line of every slave is connected to the serial input line of the following device. This means that data shifted out by a device is shifted in the following one. For instance, after each 32 clock chunk, an entire frame is transferred from a slave to another. Example given, if a three devices chain is implemented, after 96 clock pulses, the master will program the slaves by shifting out three different frames (each one made up of 32 bits). The first frame shifted out of the master will reach the last device of the chain, the second frame will reach the mid device while the third frame will be shifted into the first member of the chain (refer to Figure 21. Data transfer in daisy chain operation).

Figure 20. **Daisy chain and parallel operation**

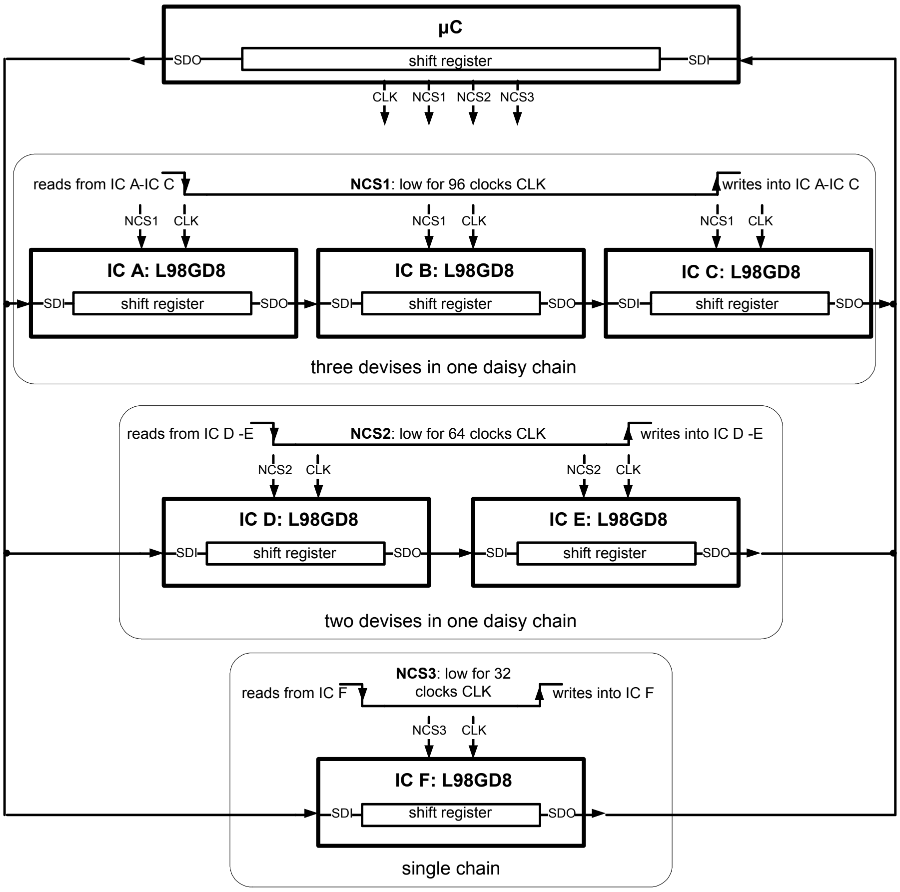
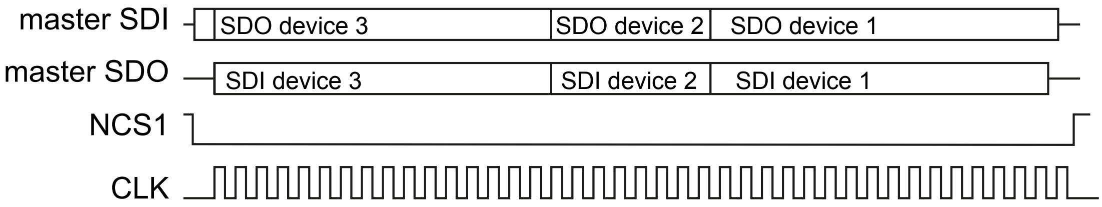


Figure 21. **Data transfer in daisy chain operation**



GADG2802171135PS

5.9.4 SPI electrical characteristics signal and the timing diagram

This section contains the electrical characteristics of the SPI signal and the timing diagram.

Note: *$T_j = T_{j\_op}$; $V_{VPS\_UV} < V_{VPS} < 60$ V, all supplies are independent; 4.5 V < VDD5 < 5.5 V; 3.0 V < VIO < 5.5 V, unless otherwise noted.*

Table 28. **SPI electrical characteristics**

Symbol	Parameter	Comment	Min.	Max.	Unit
f_{SCK}	Clock frequency (50% duty cycle)	SPI works for all frequencies	0	5	MHz
t_{sdo_trans}	SDO Rise and Fall time	20 pF to 150 pF load	5	35	ns
t_{clh}	Minimum time SCLK=HIGH	-	75	-	ns

Symbol	Parameter	Comment	Min.	Max.	Unit
t_{cll}	Minimum time SCLK=LOW	-	75	-	ns
t_{pcld}	Propagation delay – incl. Rise/Fall time (SCLK to data at SDO active)	150 pF load	-	50	ns
t_{csdv}	NCS = LOW to output SDO active	150 pF load	-	90	ns
t_{sclch}	SCLK low before NCS low (setup time SCLK to NCS change H/L)	-	75	-	ns
SCLK change L/H after NCS = low					
t_{hclcl_app}	SCLK change L/H after NCS = low	-	600	-	ns
t_{scld}	SDI input setup time (SCLK change H/L after SDI data valid)	-	15	-	ns
t_{hcld}	SDI input hold time (SDI data hold after SCLK change H/L)	-	15	-	ns
t_{sclcl}	SCLK low before NCS high	-	100	-	ns
t_{hclch}	SCLK high after NCS high	-	100	-	ns
t_{pchdz}	NCS L/H to SDO @ high impedance	-	-	75	ns
t_{onNCS}	NCS min. high time	Minimum high time between two consecutive commands	400	-	ns
C_{IN_SPI}	Input capacitance at SDI; SDO; SCLK; NCS	-	-	10	pF
t_{fNCS}	NCS Filter time (Pulses ≤ t_{fNCS} will be ignored)	-	10	40	ns
V_{SDOH}	High output level	ISDO = -2 mA	VIO - 0.4 V	-	V
V_{SDOL}	Low output level	ISDO = 3.2 mA	-	0.4	V
I_{SDO_Leak}	Three state leakage current	NCS = HIGH; $0 < V_{SDO} \leq V_{IO} - 0.3$ V	-5	15	µA
		NCS = HIGH; $V_{SDO} = V_{IO}$	2	30	µA
SDO protection; 0 V < VIO < 36 V; 0 < VSDO < 36 V; all voltages are independent					
V_{OV_SDO}	Over voltage detection threshold at SDO output	-	VIO + 0.05	VIO + 0.2	V
$t_{OV\_SDO\_fil}$	Overvoltage detection analog filter time	-	100	700	ns
$t_{OFF\_PROT\_OV}$	Overvoltage detection HS turn OFF/ON time at SDO	-	0.5	5	µs
$I_{OVpeak\_SDO\_HS}$	Maximum possible peak reverse current at SDO HS before protection Turn Off	VSDO = 36 V; VIO = 3 V; limited by R_{DSON} only	90	250	mA
Communication Check					
t_{CC}	Communication Timeout	DIS/NDIS released after NRES release.	55	85	ms
t_{CC_INIT}	Deadline for the first communication engagement	DIS/NDIS released before NRES release.	110	165	ms

Figure 22. SPI timing diagram

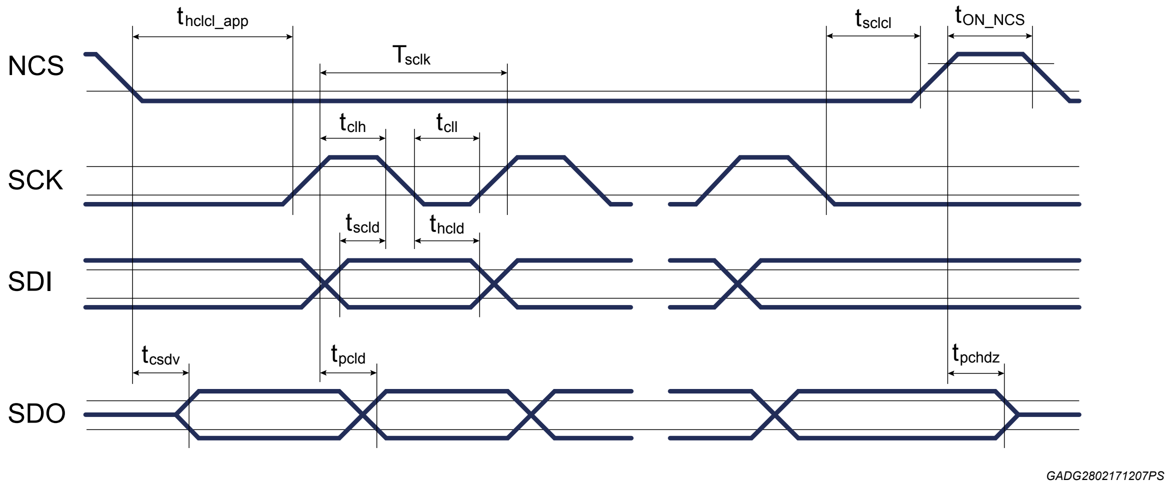


Figure 22. SPI timing diagram shows that the device has CPOL = 0 and CPHA = 1. During Reset, SDO is forced into a high impedance state and any inputs from SCLK and SDI are ignored.

5.9.5 SPI protocol

The SPI protocol features frames structured as follows:

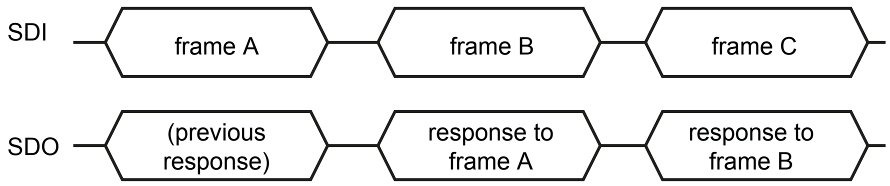
Table 29. SPI protocol

	Command				Data												
	MSB																LSB
MOSI	C3	C2	C1	C0	R/W	D26	D25	D24	D23	D22	D21	D20	….	D3	D2	D1	P
MISO	C3	C2	C1	C0	R/W	R26	R25	R24	R23	R22	R21	R20	….	R3	R2	R1	P

The MSB of each frame will be shifted in/out first. Each frame is equipped with an odd parity bit (LSB).

The response is out of frame, so the response to Nth frame will be received when sending the (N+1)th frame.

Figure 23. Out of frame response



The response frame **0x00000000** will be issued in the following cases:

- After a reset event (POR or NRES assertion)
- Invalid command received (see Table 30. SPI MOSI list for the list of available commands)
- Number of SCK pulses not multiple of 32
- Parity error on the received command

Chip select (NCS) assertion without any following SCK pulse is ignored and doesn't generate any error. In order to ignore spurious transitions, NCS input is equipped with a deglitch filter t_{fNCS}.

5.10 SPI MOSI/MISO list

The following paragraph contains the SPI MOSI and MISO list. Each frame consists of 32 bits with odd parity. Protocol is out of frame. The following table contains links to SPI commands that can be sent on MOSI line, along with their description. The corresponding answers issued by the device on MISO line are also described and linked on the right columns.

Note: All MISO default values have been scanned performing read only requests ("R/W" = 1).

Table 30. **SPI MOSI list**

MOSI	Request	Answer	MISO
COMMAND 0	Spread spectrum and diagnostic enable,OUT1-8 control, input selection and protection disable	Spread spectrum and diagnostic enable, input selection, protection disable and output voltage status	RESPONSE 0
COMMAND 1	OUT1 configuration and H-Bridge 1 diagnostic time	OUT1 configuration and H-Bridge 1 diagnostic time	RESPONSE 1
COMMAND 2	OUT2 configuration, H-Bridge 1 current limitation timing, BCF selection	OUT2 configuration, H-Bridge 1 current limitation timing, BCF selection	RESPONSE 2
COMMAND 3	OUT3 configuration, H-Bridge 1 current limitation enable and active freewheeling, gate charge/ discharge current override	OUT3 configuration, H-Bridge 1 current limitation enable and active freewheeling, gate charge/ discharge current override	RESPONSE 3
COMMAND 4	OUT4 configuration, P&H1 configuration, H-Bridge 1 enable	OUT4 configuration, P&H1 configuration, H-Bridge 1 enable	RESPONSE 4
COMMAND 5	OUT 5 configuration and H-Bridge 2 diagnostic time	OUT 5 configuration and H-Bridge 2 diagnostic time	RESPONSE 5
COMMAND 6	OUT6 configuration, H-Bridge 2 current limitation timing	OUT6 configuration, H-Bridge 2 current limitation timing	RESPONSE 6
COMMAND 7	OUT7 configuration, H-Bridge 2 current limitation enable and active freewheeling	OUT7 configuration, H-Bridge 2 current limitation enable and active freewheeling	RESPONSE 7
COMMAND 8	OUT8 configuration, P&H2 configuration, H-Bridge 2 enable	OUT8 configuration, P&H2 configuration, H-Bridge 2 enable	RESPONSE 8
COMMAND 9	Diagnostic read and diagnostic pulses	H-Bridge1-2 current limitation latches and channels diagnostic status	RESPONSE 9
COMMAND 10	BIST request and CC enable	BIST & HWSC result and device status	RESPONSE 10
COMMAND 11	Channel 1-4 control signal integrity	Channel 1-4 control signal integrity	RESPONSE 11
COMMAND 12	Channel 5-8 control signal integrity	Channel 5-8 control signal integrity	RESPONSE 12
COMMAND 13	Device status, battery and temperature monitor	Device status, battery and temperature monitor	RESPONSE 13

Note: $\Delta T = T_{jFET}$: T_j

T_{jFET} = *junction temperature of the external FET*

T_j = *junction temperature of the device.*

5.10.1 COMMAND X frame partitioning

COMMAND 0

Frame partitioning

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C				R/$\overline{W}$	SPREAD_SPECTRUM	ENABLE_DIAGNOSTIC	SPI_INPUT_SEL_08	SPI_INPUT_SEL_07	SPI_INPUT_SEL_06	SPI_INPUT_SEL_05	SPI_INPUT_SEL_04	SPI_INPUT_SEL_03	SPI_INPUT_SEL_02	SPI_INPUT_SEL_01	PROT_DISABLE_08	PROT_DISABLE_07	PROT_DISABLE_06	PROT_DISABLE_05	PROT_DISABLE_04	PROT_DISABLE_03	PROT_DISABLE_02	PROT_DISABLE_01	SPI_ON_OUT_08	SPI_ON_OUT_07	SPI_ON_OUT_06	SPI_ON_OUT_05	SPI_ON_OUT_04	SPI_ON_OUT_03	SPI_ON_OUT_02	SPI_ON_OUT_01	PARITY

Description Spread spectrum and diagnostic enable,OUT1-8 control, input selection and protection disable

[31:28] **C**: Command 0

0000

[27] **R/$\overline{W}$**: Bit to read/write configuration

0: Write & request read

1: Request read only

[26] **SPREAD_SPECTRUM**: Activates or deactivates the spread spectrum functionality

0: Deactivated

1: Activated

[25] **ENABLE_DIAGNOSTIC**: Enables or disables the diagnostics for all outputs. When set to "0" diagnostics for all outputs is "No diagnostic done".

0: Diagnostic disable

1: Diagnostic enable

[24] **SPI_INPUT_SEL_08**: Driving mode selection bit (output driven by SPI or NON)

0: Output controlled via NONx

1: Output controlled via SPI

[23] **SPI_INPUT_SEL_07**: Driving mode selection bit (output driven by SPI or NON)

0: Output controlled via NONx

1: Output controlled via SPI

[22] **SPI_INPUT_SEL_06**: Driving mode selection bit (output driven by SPI or NON)

0: Output controlled via NONx

1: Output controlled via SPI

[21] **SPI_INPUT_SEL_05**: Driving mode selection bit (output driven by SPI or NON)

0: Output controlled via NONx

1: Output controlled via SPI

[20] **SPI_INPUT_SEL_04**: Driving mode selection bit (output driven by SPI or NON)

0: Output controlled via NONx

1: Output controlled via SPI

[19] **SPI_INPUT_SEL_03**: Driving mode selection bit (output driven by SPI or NON)

0: Output controlled via NONx

1: Output controlled via SPI

[18] **SPI_INPUT_SEL_02**: Driving mode selection bit (output driven by SPI or NON)
0: Output controlled via NONx
1: Output controlled via SPI

[17] **SPI_INPUT_SEL_01**: Driving mode selection bit (output driven by SPI or NON)
0: Output controlled via NONx
1: Output controlled via SPI

[16] **PROT_DISABLE_08**: Protection disable for CH8. As long as the bit is set, CH8 is kept actively OFF
0: Output enabled
1: Output OFF

[15] **PROT_DISABLE_07**: Protection disable for CH7. As long as the bit is set, CH7 is kept actively OFF
0: Output enabled
1: Output OFF

[14] **PROT_DISABLE_06**: Protection disable for CH6. As long as the bit is set, CH6is kept actively OFF
0: Output enabled
1: Output OFF

[13] **PROT_DISABLE_05**: Protection disable for CH5. As long as the bit is set, CH5 is kept actively OFF
0: Output enabled
1: Output OFF

[12] **PROT_DISABLE_04**: Protection disable for CH4. As long as the bit is set, CH4 is kept actively OFF
0: Output enabled
1: Output OFF

[11] **PROT_DISABLE_03**: Protection disable for CH3. As long as the bit is set, CH3 is kept actively OFF
0: Output enabled
1: Output OFF

[10] **PROT_DISABLE_02**: Protection disable for CH2. As long as the bit is set, CH2 is kept actively OFF
0: Output enabled
1: Output OFF

[9] **PROT_DISABLE_01**: Protection disable for CH1. As long as the bit is set, CH1 is kept actively OFF
0: Output enabled
1: Output OFF

[8] **SPI_ON_OUT_08**: SPI output control bit (switches ON/OFF the output)
0: Output OFF
1: Output ON

[7] **SPI_ON_OUT_07**: SPI output control bit (switches ON/OFF the output)
0: Output OFF
1: Output ON

[6] **SPI_ON_OUT_06**: SPI output control bit (switches ON/OFF the output)
0: Output OFF
1: Output ON

[5] **SPI_ON_OUT_05**: SPI output control bit (switches ON/OFF the output)
0: Output OFF
1: Output ON

[4] **SPI_ON_OUT_04**: SPI output control bit (switches ON/OFF the output)
0: Output OFF
1: Output ON

[3] **SPI_ON_OUT_03**: SPI output control bit (switches ON/OFF the output)

0: Output OFF

1: Output ON

[2] **SPI_ON_OUT_02**: SPI output control bit (switches ON/OFF the output)

0: Output OFF
1: Output ON

[1] **SPI_ON_OUT_01**: SPI output control bit (switches ON/OFF the output)

0: Output OFF

1: Output ON

[0] **PARITY**: Parity bit, based on even parity calculation

0: If the number of 1 is odd

1: If the number of 1 is even

COMMAND 1

Frame partitioning

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C				$R/\overline{W}$	HB1_DEAD_TIME		HB1_TDIAG_EXT_CONFIG	TDIAG_CONFIG_01		OC_READ_01	OC_CONFIG_01						OC_TEMP_COMP_01		OC_BATT_COMP_01	TBLANK_OC_01			PROT_CONFIG_01	OC_DS_SHUNT_01	DIAG_I_CONFIG_01	GCC_CONFIG_01		N_P_CONFIG_01	LS_HS_CONFIG_01	EN_OUT_01	PARITY

Description: OUT1 configuration and H-Bridge 1 diagnostic time

[31:28] **C**: Command 1

0001

[27] **$R/\overline{W}$**: Bit to read/write configuration

0: Write & request read

1: Request read only

[25:26] **HB1_DEAD_TIME**: H-bridge1 dead time to avoid cross conduction

00: 1 µs

01: 2 µs

10: 4 µs

11: 8 µs

[24] **HB1_TDIAG_EXT_CONFIG**: Selection of tdiag timers for H-bridge 1. This function only applies when HB1_config = 1

0: H-bridge tdiag timers for HB1. The programmed TDIAG_CONFIG_01 will be extended to CH2. CH3 and CH4.

1: Standard tdiag timers for HB1. The programmed TDIAG_CONFIG_01 is valid only for CH1, while CH2, CH3 and CH4 must be set individually.

[23:22] **TDIAG_CONFIG_01**:

H-bridge 1 OFF state diagnostic blanking/filter timer. This values are valid only when HB1_tdiag_ext_config = 0 & HB1_config = 1.

00: 11.2 µs

01: 28.9 µs

10: 40 µs

11: 51.2 µs

OFF state diagnostic blanking/filter timer for CH1. It is valid for HB1 only when HB1_tdiag_ext_config = 1 & HB1_config = 1

00: 25.6 µs

01: 61.2 µs

10: 105.6 µs

11: 150 µs

[21] **OC_READ_01**: Selection of the OC threshold to read. Fixed threshold or actual threshold.

0: Read fixed OC threshold

1: Read actual OC threshold

[20:15] **OC_CONFIG_01**: Selection of over current detection threshold. 6 bit to code for the OC detection threshold

See Table 40. OC threshold selection

[14:13] **OC_TEMP_COMP_01**: Over current detection with temperature compensation (see note of Table 30. SPI MOSI list)

00: No OC compensation

01: ΔT < 60 °C

10: ΔT < 40 °C

11: ΔT < 25 °C

[12] **OC_BATT_COMP_01**: Over current detection with battery compensation.

0: Battery compensation de-activated

1: Battery compensation activated

[11:9] **TBLANK_OC_01**: When DSM is selected, it specifies the OC blanking time to allow VDS settling. When Rshunt is selected, it only determines the assertion of the 'No OC failure' diagnostic code (once expired).

000: 11.1 µs

001: 15.6 µs

010: 20 µs

011: 31.1 µs

100: 42.2 µs

101: 53.3 µs

110: 97.8 µs

111: 142.2 µs

[8] **PROT_CONFIG_01**: Output re-engagement strategy. Specifies how channel reactivation must be performed following an OC event. This bit has no effect for H-Bridge configuration. Behavior in case of HB is always as PROT_CONFIG_01 = '1'. Diagnostics latches have to be cleared in case of OC in order to re-activate the bridge.

0: output re-engagement with control signal switching event

1: output re-engagement after diagnostic readout and control signal switching event

[7] **OC_DS_SHUNT_01**: Configures the output measure OC with shunt or by DSM

0: OC with DSM

1: OC with Shunt

[6] **DIAG_I_CONFIG_01**: CH1 OL regulator output current capability

0: 100 µA capability

1: 1 mA capability

[5:4] **GCC_CONFIG_01**: Selection of gate charge/discharge currents

00: Lim by ext resistor

01: 20 mA

10: 5 mA

11: 1 mA

[3] **N_P_CONFIG_01**: NMOS or PMOS option for HS configuration

0: Output configured for NMOS

1: Output configured for PMOS

[2] **LS_HS_CONFIG_01**: Configures the channel as LS or HS

0: LS configuration

1: HS configuration

[1] **EN_OUT_01**: Enable output 01

0: Output disabled

1: Output enabled

[0] **PARITY**: Parity bit, based on even parity calculation

0: If the number of 1 is odd

1: If the number of 1 is even

COMMAND 2

Frame partitioning

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C				R/$\overline{W}$	HB1_TOFF		BATT_FACT_CONFIG	TDIAG_CONFIG_02		OC_READ_02	OC_CONFIG_02						OC_TEMP_COMP_02		OC_BATT_COMP_02	TBLANK_OC_02			PROT_CONFIG_02	OC_DS_SHUNT_02	DIAG_I_CONFIG_02	GCC_CONFIG_02		N_P_CONFIG_02	LS_HS_CONFIG_02	EN_OUT_02	PARITY

Description: Output configuration OUT2

[31:28] **C**: Command 2

0010

[27] **R/$\overline{W}$**: Bit to read/write configuration

0: Write & request read

1: Request read only

[26:25] **HB1_TOFF**: H-bridge1 off timer during current limitation

00: 31 µs

01: 48 µs

10: 62.5 µs

11: 125 µs

[24] **BATT_FACT_CONFIG**: Selection of the factor used in battery compensation

0: Factor for CV

1: Factor for PV

[23:22] **TDIAG_CONFIG_02**: OFF state diagnostic blanking/filter timer for output 02. It has no effect if HB1_config =1 & HB1_tdiag_ext_config = 0

00: 25.6 µs

01: 61.2 µs

10: 105.6 µs

11: 150 µs

[21] **OC_READ_02**: Selection of the OC threshold to read. Fixed threshold or actual threshold.

0: Read fixed OC threshold

1: Read actual OC threshold

[20:15] **OC_CONFIG_02**: Selection of over current detection threshold. 6 bit to code for the OC detection threshold

See Table 40. OC threshold selection

[14:13] **OC_TEMP_COMP_02**: Over current detection with temperature compensation (see note of Table 30. SPI MOSI list)

00: No OC compensation

01: ΔT < 60 °C

10: ΔT < 40 °C

11: ΔT < 25 °C

[12] **OC_BATT_COMP_02**: Over current detection with battery compensation

0: Battery compensation de-activated

1: Battery compensation activated

[11:9] **TBLANK_OC_02**: When DSM is selected, it specifies the OC blanking time to allow VDS settling. When Rshunt is selected, it only determines the assertion of the 'No OC failure' diagnostic code (once expired).

000: 11.1 µs

001: 15.6 µs

010: 20 µs

011: 31.1 µs

100: 42.2 µs

101: 53.3 µs

110: 97.8 µs

111: 142.2 µs

[8] **PROT_CONFIG_02**: Output re-engagement strategy. Specifies how channel reactivation must be performed following an OC event. This bit has no effect for H-Bridge configuration. Behavior in case of HB is always as PROT_CONFIG_02 = '1'. Diagnostics latches have to be cleared in case of OC in order to re-activate the bridge.

0: output re-engagement with control signal switching event

1: output re-engagement after diagnostic readout and control signal switching event

[7] **OC_DS_SHUNT_02**: Configures the output measure OC with shunt or by DSM

0: OC with DSM

1: OC with Shunt

[6] **DIAG_I_CONFIG_02**: CH2 OL regulator output current capability

0: 100 µA capability

1: 1 mA capability

[5:4] **GCC_CONFIG_02**: Selection of gate charge/discharge currents

00: Lim by ext resistor

01: 20 mA

10: 5 mA

11: 1 mA

[3] **N_P_CONFIG_02**: NMOS or PMOS option for HS configuration

0: Output configured for NMOS

1: Output configured for PMOS

[2] **LS_HS_CONFIG_02**: Configures the channel as LS or HS

0: LS configuration

1: HS configuration

[1] **EN_OUT_02**: Enable output 02

0: Output disabled

1: Output enabled

[0] **PARITY**: Parity bit, based on even parity calculation

0: If the number of 1 is odd

1: If the number of 1 is even

COMMAND 3

Frame partitioning

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C				$R/\overline{W}$	HB1_ILIM_EN	HB1_AFW	GCC_OVERRIDE_CONFIG	TDIAG_CONFIG_03		OC_READ_03	OC_CONFIG_03						OC_TEMP_COMP_03		OC_BATT_COMP_03	TBLANK_OC_03			PROT_CONFIG_03	OC_DS_SHUNT_03	DIAG_I_CONFIG_03	GCC_CONFIG_03		N_P_CONFIG_03	LS_HS_CONFIG_03	EN_OUT_03	PARITY

Description: Output configuration OUT2

[31:28] **C**: Command 3

0011

[27] **$R/\overline{W}$**: Bit to read/write configuration

0: Write & request read

1: Request read only

[26] **HB1_ILIM_EN**: H-bridge1 current limit activation. CH3 OC threshold is used for current limitation, it is only valid for Shunt measurement

0: Current limitation not active

1: Current limitation active

[25] **HB1_AFW**: H-bridge1 active freewheel configuration on LS

0: Passive freewheeling

1: Active freewheeling

[24] **GCC_OVERRIDE_CONFIG**: Selection of the GCC override configuration upon OC detection. It has no effect if GCC[1:0] = '00' (current limited by external resistor)

0: Selective override:

1 mA --> 5 mA

5 mA --> 20 mA

1: Global override:

1 mA --> 20 mA

5 mA --> 20 mA

[23:22] **TDIAG_CONFIG_03**: OFF state diagnostic blanking/filter timer for output 03. It has no effect if HB1_config =1 & HB1_tdiag_ext_config = 0

00: 25.6 µs

01: 61.2 µs

10: 105.6 µs

11: 150 µs

[21] **OC_READ_03**: Selection of the OC threshold to read. Fixed threshold or actual threshold.

0: Read fixed OC threshold

1: Read actual OC threshold

[20:15] **OC_CONFIG_03**: Selection of over current detection threshold. 6 bit to code for the OC detection threshold

See Table 40. OC threshold selection

[14:13] **OC_TEMP_COMP_03**: Over current detection with temperature compensation (see note of Table 30. SPI MOSI list)

00: No OC compensation

01: ΔT < 60 °C

10: ΔT < 40 °C

11: ΔT < 25 °C

[12] **OC_BATT_COMP_03**: Over current detection with battery compensation

0: Battery compensation de-activated

1: Battery compensation activated

[11:9] **TBLANK_OC_03**: When DSM is selected, it specifies the OC blanking time to allow VDS settling. When Rshunt is selected, it only determines the assertion of the 'No OC failure' diagnostic code (once expired).

000: 11.1 μs

001: 15.6 μs

010: 20 μs

011: 31.1 μs

100: 42.2 μs

101: 53.3 μs

110: 97.8 μs

111: 142.2 μs

[8] **PROT_CONFIG_03**: Output re-engagement strategy. Specifies how channel reactivation must be performed following an OC event. This bit has no effect for H-Bridge configuration. Behavior in case of HB is always as PROT_CONFIG_03 = '1'. Diagnostics latches have to be cleared in case of OC in order to re-activate the bridge.

0: output re-engagement with control signal switching event

1: output re-engagement after diagnostic readout and control signal switching event

[7] **OC_DS_SHUNT_03**: Configures the output measure OC with shunt or by DSM

0: OC with DSM

1: OC with Shunt

[6] **DIAG_I_CONFIG_03**: CH3 OL regulator output current capability

0: 100 μA capability

1: 1 mA capability

[5:4] **GCC_CONFIG_03**: Selection of gate charge/discharge currents

00: Lim by ext resistor

01: 20 mA

10: 5 mA

11: 1 mA

[3] **N_P_CONFIG_03**: NMOS or PMOS option for HS configuration

0: Output configured for NMOS

1: Output configured for PMOS

[2] **LS_HS_CONFIG_03**: Configures the channel as LS or HS

0: LS configuration

1: HS configuration

[1] **EN_OUT_03**: Enable output 03

0: Output disabled

1: Output enabled

[0] **PARITY**: Parity bit, based on even parity calculation

0: If the number of 1 is odd

1: If the number of 1 is even

COMMAND 4

Frame partitioning

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C				R/$\overline{W}$	HB1_CONFIG	PH1_diag_strategy	PH1_CONFIG	TDIAG_CONFIG_04		OC_READ_04	OC_CONFIG_04						OC_TEMP_COMP_04		OC_BATT_COMP_04	TBLANK_OC_04			PROT_CONFIG_04	OC_DS_SHUNT_04	DIAG_I_CONFIG_04	GCC_CONFIG_04		N_P_CONFIG_04	LS_HS_CONFIG_04	EN_OUT_04	PARITY

Description: OUT4 configuration, P&H1 configuration, H-Bridge 1 enable

[31:28] **C**: Command 4

0100

[27] **R/$\overline{W}$**: Bit to read/write configuration

0: Write & request read

1: Request read only

[26] **HB1_CONFIG**: Configures CH1-CH2-CH3-CH4 for H-bridge1 operation

0: H-bridge not configured

1: CH1-CH4 configured as H-bridge

[25] **PH1_DIAG_STRATEGY**: OL masking strategy to prevent false OL assertion in P&H1 configuration

0: "No OL/STG /STB" failure reported

1: "No diagnostic done" reported

[24] **PH1_CONFIG**: Configures CH1-CH4 for Peak and Hold1 operation

0: Peak and Hold1 not configured

1: Peak and Hold1 configured

[23:22] **TDIAG_CONFIG_04**: OFF state diagnostic blanking/filter timer for output 04. It has no effect if HB1_config =1 & HB1_tdiag_ext_config = 0

00: 25.6 µs

01: 61.2 µs

10: 105.6 µs

11: 150 µs

[21] **OC_READ_04**: Selection of the OC threshold to read. Fixed threshold or actual threshold.

0: Read fixed OC threshold

1: Read actual OC threshold

[20:15] **OC_CONFIG_04**: Selection of over current detection threshold. 6 bit to code for the OC detection threshold

See Table 40. OC threshold selection

[14:13] **OC_TEMP_COMP_04**: Over current detection with temperature compensation (see note of Table 30. SPI MOSI list)

00: No OC compensation

01: ΔT < 60 °C

10: ΔT < 40 °C

11: ΔT < 25 °C

[12] **OC_BATT_COMP_04**: Over current detection with battery compensation

0: Battery compensation de-activated

1: Battery compensation activated

[11:9] **TBLANK_OC_04**: When DSM is selected, it specifies the OC blanking time to allow VDS settling. When Rshunt is selected, it only determines the assertion of the 'No OC failure' diagnostic code (once expired).

000: 11.1 µs

001: 15.6 µs

010: 20 µs

011: 31.1 µs

100: 42.2 µs

101: 53.3 µs

110: 97.8 µs

111: 142.2 µs

[8] **PROT_CONFIG_04**: Output re-engagement strategy. Specifies how channel reactivation must be performed following an OC event. This bit has no effect for H-Bridge configuration. Behavior in case of HB is always as PROT_CONFIG_04 = '1'. Diagnostics latches have to be cleared in case of OC in order to re-activate the bridge.

0: output re-engagement with control signal switching event

1: output re-engagement after diagnostic readout and control signal switching event

[7] **OC_DS_SHUNT_04**: Configures the output measure OC with shunt or by DSM

0: OC with DSM

1: OC with Shunt

[6] **DIAG_I_CONFIG_04**: CH4 OL regulator output current capability

0: 100 µA capability

1: 1 mA capability

[5:4] **GCC_CONFIG_04**: Selection of gate charge/discharge currents

00: Lim by ext resistor

01: 20 mA

10: 5 mA

11: 1 mA

[3] **N_P_CONFIG_04**: NMOS or PMOS option for HS configuration

0: Output configured for NMOS

1: Output configured for PMOS

[2] **LS_HS_CONFIG_04**: Configures the channel as LS or HS

0: LS configuration

1: HS configuration

[1] **EN_OUT_04**: Enable output 04

0: Output disabled

1: Output enabled

[0] **PARITY**: Parity bit, based on even parity calculation

0: If the number of 1 is odd

1: If the number of 1 is even

COMMAND 5

Frame partitioning

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">C</td><td>R/W̄</td><td colspan="2">HB2_DEAD_TIME</td><td>HB2_TDIAG_EXT_CONFIG</td><td colspan="2">TDIAG_CONFIG_05</td><td>OC_READ_05</td><td colspan="6">OC_CONFIG_05</td><td colspan="2">OC_TEMP_COMP_05</td><td>OC_BATT_COMP_05</td><td colspan="3">TBLANK_OC_05</td><td>PROT_CONFIG_05</td><td>OC_DS_SHUNT_05</td><td>DIAG_I_CONFIG_05</td><td colspan="2">GCC_CONFIG_05</td><td>N_P_CONFIG_05</td><td>LS_HS_CONFIG_05</td><td>EN_OUT_05</td><td>PARITY</td></tr>
</table>

Description OUT 5 configuration and H-Bridge 2 diagnostic time

[31:28] **C**: Command 5

0100

[27] **R/$\overline{W}$**: Bit to read/write configuration

0: Write & request read

1: Request read only

[26:25] **HB2_DEAD_TIME**: CH-bridge2 dead time to avoid cross conduction

00: 1 µs

01: 2 µs

10: 4 µs

11: 8 µs

[24] **HB2_TDIAG_EXT_CONFIG**: Selection of tdiag timers for H-bridge 2. This function only applies when HB2_config = 1 (command 8)

0: H-bridge tdiag timers for HB2. The programmed TDIAG_CONFIG_05 will be extended to

CH6, CH7 and CH8.

1: Standard tdiag timers for HB2. The programmed TDIAG_CONFIG_05 is valid only for CH5,

while CH6, CH7 and CH8 must be set individually.

[23:22] **TDIAG_CONFIG_05**:

H-bridge 2 OFF state diagnostic blanking/filter timer. This values are valid only when HB2_tdiag_ext_config = 0 & HB2_config = 1

00: 11.2 µs

01: 28.9 µs

10: 40 µs

11: 51.2 µs

OFF state diagnostic blanking/filter timer for output 05. It has no effect if HB2_config = 1 & HB2_tdiag_ext_config = 1

00: 25.6 µs

01: 61.2 µs

10: 105.6 µs

11: 150 µs

[21] **OC_READ_05**: Selection of the OC threshold to read. Fixed threshold or actual threshold.

0: Read fixed OC threshold

1: Read actual OC threshold

[20:15] **OC_CONFIG_05**: Selection of over current detection threshold. 6 bit to code for the OC detection threshold

See Table 40. OC threshold selection

[14:13] **OC_TEMP_COMP_05**: Over current detection with temperature compensation (see note of Table 30. SPI MOSI list)

00: No OC compensation

01: ΔT < 60 °C

10: ΔT < 40 °C

11: ΔT < 25 °C

[12] **OC_BATT_COMP_05**: Over current detection with battery compensation

0: Battery compensation de-activated

1: Battery compensation activated

[11:9] **TBLANK_OC_05**: When DSM is selected, it specifies the OC blanking time to allow VDS settling. When Rshunt is selected, it only determines the assertion of the 'No OC failure' diagnostic code (once expired).

000: 11.1 µs

001: 15.6 µs

010: 20 µs

011: 31.1 µs

100: 42.2 µs

101: 53.3 µs

110: 97.8 µs

111: 142.2 µs

[8] **PROT_CONFIG_05**: Output re-engagement strategy. Specifies how channel reactivation must be performed following an OC event. This bit has no effect for H-Bridge configuration. Behavior in case of HB is always as PROT_CONFIG_05 = '1'. Diagnostics latches have to be cleared in case of OC in order to re-activate the bridge.

0: output re-engagement with control signal switching event

1: output re-engagement after diagnostic readout and control signal switching event

[7] **OC_DS_SHUNT_05**: Configures the output measure OC with shunt or by DSM

0: OC with DSM

1: OC with Shunt

[6] **DIAG_I_CONFIG_05**: CH5 OL regulator output current capability

0: 100 µA capability

1: 1 mA capability

[5:4] **GCC_CONFIG_05**: Selection of gate charge/discharge currents

00: Lim by ext resistor

01: 20 mA

10: 5 mA

11: 1 mA

[3] **N_P_CONFIG_05**: NMOS or PMOS option for HS configuration

0: Output configured for NMOS

1: Output configured for PMOS

[2] **LS_HS_CONFIG_05**: Configures the channel as LS or HS

0: LS configuration

1: HS configuration

[1] **EN_OUT_05**: Enable output 05

0: Output disabled

1: Output enabled

[0] **PARITY**: Parity bit, based on even parity calculation

0: If the number of 1 is odd

1: If the number of 1 is even

COMMAND 6

Frame partitioning

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C				$R/\overline{W}$	HB2_TOFF		NOT_USED_FIXED_PATTERN	TDIAG_CONFIG_06		OC_READ_06	OC_CONFIG_06						OC_TEMP_COMP_06		OC_BATT_COMP_06	TBLANK_OC_06			PROT_CONFIG_06	OC_DS_SHUNT_06	DIAG_I_CONFIG_06	GCC_CONFIG_06		N_P_CONFIG_06	LS_HS_CONFIG_06	EN_OUT_06	PARITY

Description OUT2 configuration, H-Bridge 2 current limitation timing

[31:28] **C**: Command 6

0110

[27] **$R/\overline{W}$**: Bit to read/write configuration

0: Write & request read

1: Request read only

[26:25] **HB2_TOFF**: H-bridge2 off timer during current limitation

00: 31 µs

01: 48 µs

10: 62.5 µs

11: 125 µs

[24] **FIXED_PATTERN**

0

[23:22] **TDIAG_CONFIG_06**: OFF state diagnostic blanking/filter timer for output 06. It has no effect if HB2_config =1 & HB2_tdiag_ext_config = 0.

00: 25.6 µs

01: 61.2 µs

10: 105.6 µs

11: 150 µs

[21] **OC_READ_06**: Selection of the OC threshold to read. Fixed threshold or actual threshold.

0: Read fixed OC threshold

1: Read actual OC threshold

[20:15] **OC_CONFIG_06**: Selection of over current detection threshold. 6 bit to code for the OC detection threshold

See Table 40. OC threshold selection

[14:13] **OC_TEMP_COMP_06**: Over current detection with temperature compensation (see note of Table 30. SPI MOSI list)

00: No OC compensation

01: ΔT < 60 °C

10: ΔT < 40 °C

11: ΔT < 25 °C

[12] **OC_BATT_COMP_06**: Over current detection with battery compensation

0: Battery compensation de-activated

1: Battery compensation activated

[11:9] **TBLANK_OC_06**: When DSM is selected, it specifies the OC blanking time to allow VDS settling. When Rshunt is selected, it only determines the assertion of the 'No OC failure' diagnostic code (once expired).

000: 11.1 µs

001: 15.6 µs

010: 20 µs

011: 31.1 µs

100: 42.2 µs

101: 53.3 µs

110: 97.8 µs

111: 142.2 µs

[8] **PROT_CONFIG_06**: Output re-engagement strategy. Specifies how channel reactivation must be performed following an OC event. This bit has no effect for H-Bridge configuration. Behavior in case of HB is always as PROT_CONFIG_06 = '1'. Diagnostics latches have to be cleared in case of OC in order to re-activate the bridge.

0: output re-engagement with control signal switching event

1: output re-engagement after diagnostic readout and control signal switching event

[7] **OC_DS_SHUNT_06**: Configures the output measure OC with shunt or by DSM

0: OC with DSM

1: OC with Shunt

[6] **DIAG_I_CONFIG_06**: CH6 OL regulator output current capability

0: 100 µA capability

1: 1 mA capability

[5:4] **GCC_CONFIG_06**: Selection of gate charge/discharge currents

00: Lim by ext resistor

01: 20 mA

10: 5 mA

11: 1 mA

[3] **N_P_CONFIG_06**: NMOS or PMOS option for HS configuration

0: Output configured for NMOS

1: Output configured for PMOS

[2] **LS_HS_CONFIG_06**: Configures the channel as LS or HS

0: LS configuration

1: HS configuration

[1] **EN_OUT_06**: Enable output 06

0: Output disabled

1: Output enabled

[0] **PARITY**: Parity bit, based on even parity calculation

0: If the number of 1 is odd

1: If the number of 1 is even

COMMAND 7

Frame partitioning

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C				R/$\overline{W}$	HB2_ILIM_EN	HB2_AFW	FIXED_PATTERN	TDIAG_CONFIG_07		OC_READ_07	OC_CONFIG_07						OC_TEMP_COMP_07		OC_BATT_COMP_07	TBLANK_OC_07			PROT_CONFIG_07	OC_DS_SHUNT_07	DIAG_I_CONFIG_07	GCC_CONFIG_07		N_P_CONFIG_07	LS_HS_CONFIG_07	EN_OUT_07	PARITY

Description OUT7 configuration, H-Bridge 2 current limitation enable and active freewheeling

[31:28] **C**: Command 7

0111

[27] **R/$\overline{W}$**: Bit to read/write configuration

0: Write & request read

1: Request read only

[26] **HB2_ILIM_EN**: H-bridge2 current limit activation. CH7 OC threshold is used for current limitation, only valid with Shunt measurement

0: Current limitation not active

1: Current limitation active

[25] **HB2_AFW**: H-bridge2 active freewheel configuration on LS

0: Passive freewheeling

1: Active freewheeling

[24] **FIXED_PATTERN**

0

[23:22] **TDIAG_CONFIG_07**: OFF state diagnostic blanking/filter timer for output 07. It has no effect if HB2_config =1 & HB2_tdiag_ext_config = 0.

00: 25.6 µs

01: 61.2 µs

10: 105.6 µs

11: 150 µs

[21] **OC_READ_07**: Selection of the OC threshold to read. Fixed threshold or actual threshold.

0: Read fixed OC threshold

1: Read actual OC threshold

[20:15] **OC_CONFIG_07**: Selection of over current detection threshold. 6 bit to code for the OC detection threshold

See Table 40. OC threshold selection

[14:13] **OC_TEMP_COMP_07**: Over current detection with temperature compensation (see note of Table 30. SPI MOSI list)

00: No OC compensation

01: ΔT < 60 °C

10: ΔT < 40 °C

11: ΔT < 25 °C

[12] **OC_BATT_COMP_07**: Over current detection with battery compensation

0: Battery compensation de-activated

1: Battery compensation activated

[11:9] **TBLANK_OC_07**: When DSM is selected, it specifies the OC blanking time to allow VDS settling. When Rshunt is selected, it only determines the assertion of the 'No OC failure' diagnostic code (once expired).

000: 11.1 µs

001: 15.6 µs

010: 20 µs

011: 31.1 µs

100: 42.2 µs

101: 53.3 µs

110: 97.8 µs

111: 142.2 µs

[8] **PROT_CONFIG_07**: Output re-engagement strategy. Specifies how channel reactivation must be performed following an OC event. This bit has no effect for H-Bridge configuration. Behavior in case of HB is always as PROT_CONFIG_07 = '1'. Diagnostics latches have to be cleared in case of OC in order to re-activate the bridge.

0: output re-engagement with control signal switching event

1: output re-engagement after diagnostic readout and control signal switching event

[7] **OC_DS_SHUNT_07**: Configures the output measure OC with shunt or by DSM

0: OC with DSM

1: OC with Shunt

[6] **DIAG_I_CONFIG_07**: CH7 OL regulator output current capability

0: 100 µA capability

1: 1 mA capability

[5:4] **GCC_CONFIG_07**: Selection of gate charge/discharge currents

00: Lim by ext resistor

01: 20 mA

10: 5 mA

11: 1 mA

[3] **N_P_CONFIG_07**: NMOS or PMOS option for HS configuration

0: Output configured for NMOS

1: Output configured for PMOS

[2] **LS_HS_CONFIG_07**: Configures the channel as LS or HS

0: LS configuration

1: HS configuration

[1] **EN_OUT_07**: Enable output 07

0: Output disabled

1: Output enabled

[0] **PARITY**: Parity bit, based on even parity calculation

0: If the number of 1 is odd

1: If the number of 1 is even

COMMAND 8

Frame partitioning

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C				R/$\overline{W}$	HB2_CONFIG	PH2_diag_strategy	PH2_CONFIG	TDIAG_CONFIG_08		OC_READ_08	OC_CONFIG_08						OC_TEMP_COMP_08		OC_BATT_COMP_08	TBLANK_OC_08			PROT_CONFIG_08	OC_DS_SHUNT_08	DIAG_I_CONFIG_08	GCC_CONFIG_08		N_P_CONFIG_08	LS_HS_CONFIG_08	EN_OUT_08	PARITY

Description: OUT8 configuration, P&H2 configuration, H-Bridge 2 enable

[31:28] **C**: Command 8

1000

[27] **R/$\overline{W}$**: Bit to read/write configuration

0: Write & request read

1: Request read only

[26] **HB2_CONFIG**: Configures CH5-CH6-CH7-CH8 for H-bridge2 operation

0: Not H-bridge configured

1: CH5-CH8 configured as H-bridge

[25] **PH2_DIAG_STRATEGY**: OL masking strategy to prevent false OL assertion in P&H2 configuration

0: "No OL/STG /STB" failure reported

1: "No diagnostic done" reported

[24] **PH2_CONFIG**: Configures CH2-CH3 for Peak and Hold2 operation

0: Peak and Hold2 not configured

1: Peak and Hold2 configured

[23:22] **TDIAG_CONFIG_08**: OFF state diagnostic blanking/filter timer for output 08. It has no effect if HB2_config =1 & HB2_tdiag_ext_config = 0.

00: 25.6 µs

01: 61.2 µs

10: 105.6 µs

11: 150 µs

[21] **OC_READ_08**: Selection of the OC threshold to read. Fixed threshold or actual threshold.

0: Read fixed OC threshold

1: Read actual OC threshold

[20:15] **OC_CONFIG_08**: Selection of over current detection threshold. 6 bit to code for the OC detection threshold

See Table 40. OC threshold selection

[14:13] **OC_TEMP_COMP_08**: Over current detection with temperature compensation (see note of Table 30. SPI MOSI list)

00: No OC compensation

01: ΔT < 60 °C

10: ΔT < 40 °C

11: ΔT < 25 °C

[12] **OC_BATT_COMP_08**: Over current detection with battery compensation

0: Battery compensation de-activated

1: Battery compensation activated

[11:9] **TBLANK_OC_08**: When DSM is selected, it specifies the OC blanking time to allow VDS settling. When Rshunt is selected, it only determines the assertion of the 'No OC failure' diagnostic code (once expired).

000: 11.1 µs

001: 15.6 µs

010: 20 µs

011: 31.1 µs

100: 42.2 µs

101: 53.3 µs

110: 97.8 µs

111: 142.2 µs

[8] **PROT_CONFIG_08**: Output re-engagement strategy. Specifies how channel reactivation must be performed following an OC event. This bit has no effect for H-Bridge configuration. Behavior in case of HB is always as PROT_CONFIG_08 = '1'. Diagnostics latches have to be cleared in case of OC in order to re-activate the bridge.

0: output re-engagement with control signal switching event

1: output re-engagement after diagnostic readout and control signal switching event

[7] **OC_DS_SHUNT_08**: Configures the output measure OC with shunt or by DSM

0: OC with DSM

1: OC with Shunt

[6] **DIAG_I_CONFIG_08**: CH8 OL regulator output current capability

0: 100 µA capability

1: 1 mA capability

[5:4] **GCC_CONFIG_08**: Selection of gate charge/discharge currents

00: Lim by ext resistor

01: 20 mA

10: 5 mA

11: 1 mA

[3] **N_P_CONFIG_08**: NMOS or PMOS option for HS configuration

0: Output configured for NMOS

1: Output configured for PMOS

[2] **LS_HS_CONFIG_08**: Configures the channel as LS or HS

0: LS configuration

1: HS configuration

[1] **EN_OUT_08**: Enable output 08

0: Output disabled

1: Output enabled

[0] **PARITY**: Parity bit, based on even parity calculation

0: If the number of 1 is odd

1: If the number of 1 is even

COMMAND 9

Frame partitioning

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C				R/$\overline{W}$	FIXED_PATTERN										DIAG_OFF_PULSE_08	DIAG_OFF_PULSE_07	DIAG_OFF_PULSE_06	DIAG_OFF_PULSE_05	DIAG_OFF_PULSE_04	DIAG_OFF_PULSE_03	DIAG_OFF_PULSE_02	DIAG_OFF_PULSE_01	DIAG_ON_PULSE_08	DIAG_ON_PULSE_07	DIAG_ON_PULSE_06	DIAG_ON_PULSE_05	DIAG_ON_PULSE_04	DIAG_ON_PULSE_03	DIAG_ON_PULSE_02	DIAG_ON_PULSE_01	PARITY

Description: Diagnostic pulses

[31:28] **C**: Command 9
1001

[27] **R/$\overline{W}$**: Bit to read/write configuration
0: Write & request read
1: Request read only

[26:17] **FIXED_PATTERN**
0101010101

[16] **DIAG_OFF_PULSE_08**: Diagnostic OFF pulse request on CH8
0: no pulse
1: OFF pulse

[15] **DIAG_OFF_PULSE_07**: Diagnostic OFF pulse request on CH7
0: no pulse
1: OFF pulse

[14] **DIAG_OFF_PULSE_06**: Diagnostic OFF pulse request on CH6
0: no pulse
1: OFF pulse

[13] **DIAG_OFF_PULSE_05**: Diagnostic OFF pulse request on CH5
0: no pulse
1: OFF pulse

[12] **DIAG_OFF_PULSE_04**: Diagnostic OFF pulse request on CH4
0: no pulse
1: OFF pulse

[11] **DIAG_OFF_PULSE_03**: Diagnostic OFF pulse request on CH3
0: no pulse
1: OFF pulse

[10] **DIAG_OFF_PULSE_02**: Diagnostic OFF pulse request on CH2
0: no pulse
1: OFF pulse

[9] **DIAG_OFF_PULSE_01**: Diagnostic OFF pulse request on CH1
0: no pulse
1: OFF pulse

[8] **DIAG_ON_PULSE_08**: Diagnostic ON pulse request on CH8
0: no pulse
1: ON pulse

[7] **DIAG_ON_PULSE_07**: Diagnostic ON pulse request on CH7
0: no pulse
1: ON pulse

[6] **DIAG_ON_PULSE_06**: Diagnostic ON pulse request on CH6
0: no pulse
1: ON pulse

[5] **DIAG_ON_PULSE_05**: Diagnostic ON pulse request on CH5
0: no pulse
1: ON pulse

[4] **DIAG_ON_PULSE_04**: Diagnostic ON pulse request on CH4
0: no pulse
1: ON pulse

[3] **DIAG_ON_PULSE_03**: Diagnostic ON pulse request on CH3
0: no pulse
1: ON pulse

[2] **DIAG_ON_PULSE_02**: Diagnostic ON pulse request on CH2
0: no pulse
1: ON pulse

[1] **DIAG_ON_PULSE_01**: Diagnostic ON pulse request on CH1
0: no pulse
1: ON pulse

[0] **PARITY**: Parity bit, based on even parity calculation
0: If the number of 1 is odd
1: If the number of 1 is even

COMMAND 10

Frame partitioning

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C				R/$\overline{\text{W}}$	FIXED_PATTERN																				BIST_RQ		CONFIG_CC		FIXED_PATTERN		PARITY

Description: BIST request and CC enable

[31:28] **C**: Command 10
1010

[27] **R/$\overline{\text{W}}$**: Bit to read/write configuration
0: Write & request read
1: Request read only

[26:7] **FIXED_PATTERN**: Not used
01010101010101010101

[6:5] **BIST_RQ**: Request for BIST and HWSC sequence
00: not allowed => behavior as for "no request"
01: request
10: no request
11: not allowed => behavior as for "no request"

[4:3] **CONFIG_CC**: Activation or deactivation of communication check
00: not allowed => previous configuration will be maintained
01: CC active
10: CC inactive
11: not allowed => previous configuration will be maintained

[2:1] **FIXED_PATTERN**
10

[0] **PARITY**: Parity bit, based on even parity calculation
0: If the number of 1 is odd
1: If the number of 1 is even

COMMAND 11

Fixed frame

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xBAAAAAAA																															

Description: Channel 1-4 control signal integrity

COMMAND 12

Fixed frame

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xCAAAAAAB																															

Description: Channel 5-8 control signal integrity

COMMAND 13

Fixed frame

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0xDAAAAAAA																															

Description: Device status, battery and temperature monitor

5.10.2 RESPONSE X frame partitioning

RESPONSE 0

Frame partitioning

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C				R/$\overline{W}$	SPREAD_SPECTRUM	ENABLE_DIAGNOSTIC	SPI_INPUT_SEL_08	SPI_INPUT_SEL_07	SPI_INPUT_SEL_06	SPI_INPUT_SEL_05	SPI_INPUT_SEL_04	SPI_INPUT_SEL_03	SPI_INPUT_SEL_02	SPI_INPUT_SEL_01	PROT_DISABLE_08	PROT_DISABLE_07	PROT_DISABLE_06	PROT_DISABLE_05	PROT_DISABLE_04	PROT_DISABLE_03	PROT_DISABLE_02	PROT_DISABLE_01	OUTPUT_VOLTAGE[8:1]								PARITY

Description Spread spectrum and diagnostic enable, input selection, protection disable and output voltage status. Initial OUTPUT_VOLTAGE field value depends on load.

[31:28] **C**: Response to command 0

Reset: 0000

Reset Condition: -

[27] **R/$\overline{W}$**: Bit to read/write configuration

0: Write & request read

1: Request read only

Reset: 1

Reset Condition: POR, NRES

[26] **SPREAD_SPECTRUM**: Active or deactive the spread spectrum functionality

0: Inactive

1: Active

Reset: 0

Reset Condition: POR, NRES

[25] **ENABLE_DIAGNOSTIC**: Enable or disable the diagnostics for all outputs. When i to "0" diagnostics for all outputs is "Not Diag Done"

0: Diagnostic disable

1: Diagnostic enable

Reset: 0

Reset Condition: POR, NRES

[24] **SPI_INPUT_SEL_08**: Driving mode selection bit (output driven by SPI or NON)

0: Output control by NONx

1: Output control by SPI

Reset: 0

Reset Condition: POR, NRES

[23] **SPI_INPUT_SEL_07**: Driving mode selection bit (output driven by SPI or NON)

0: Output control by NONx

1: Output control by SPI

Reset: 0

Reset Condition: POR, NRES

[22] **SPI_INPUT_SEL_06**: Driving mode selection bit (output driven by SPI or NON)
0: Output control by NONx
1: Output control by SPI
Reset: 0
Reset Condition: POR, NRES

[21] **SPI_INPUT_SEL_05**: Driving mode selection bit (output driven by SPI or NON)
0: Output control by NONx
1: Output control by SPI
Reset: 0
Reset Condition: POR, NRES

[20] **SPI_INPUT_SEL_04**: Driving mode selection bit (output driven by SPI or NON)
0: Output control by NONx
1: Output control by SPI
Reset: 0
Reset Condition: POR, NRES

[19] **SPI_INPUT_SEL_03**: Driving mode selection bit (output driven by SPI or NON)
0: Output control by NONx
1: Output control by SPI
Reset: 0
Reset Condition: POR, NRES

[18] **SPI_INPUT_SEL_02**: Driving mode selection bit (output driven by SPI or NON)
0: Output control by NONx
1: Output control by SPI
Reset: 0
Reset Condition: POR, NRES

[17] **SPI_INPUT_SEL_01**: Driving mode selection bit (output driven by SPI or NON)
0: Output control by NONx
1: Output control by SPI
Reset: 0
Reset Condition: POR, NRES

[16] **PROT_DISABLE_08**: Protection disable for CH8. As long as the bit is set, CH8 is kept actively OFF
0: Output enabled
1: Output OFF
Reset: 0
Reset Condition: POR, NRES

[15] **PROT_DISABLE_07**: Protection disable for CH7. As long as the bit is set, CH7 is kept actively OFF
0: Output enabled
1: Output OFF
Reset: 0
Reset Condition: POR, NRES

[14] **PROT_DISABLE_06**: Protection disable for CH6. As long as the bit is set, CH6 is kept actively OFF
0: Output enabled
1: Output OFF
Reset: 0
Reset Condition: POR, NRES

[13] **PROT_DISABLE_05**: Protection disable for CH5. As long as the bit is set, CH5 is kept actively OFF

0: Output enabled

1: Output OFF

Reset: 0

Reset Condition: POR, NRES

[12] **PROT_DISABLE_04**: Protection disable for CH4. As long as the bit is set, CH4 is kept actively OFF

0: Output enabled

1: Output OFF

Reset: 0

Reset Condition: POR, NRES

[11] **PROT_DISABLE_03**: Protection disable for CH3. As long as the bit is set, CH3 is kept actively OFF

0: Output enabled

1: Output OFF

Reset: 0

Reset Condition: POR, NRES

[10] **PROT_DISABLE_02**: Protection disable for CH2. As long as the bit is set, CH2 is kept actively OFF

0: Output enabled

1: Output OFF

Reset: 0

Reset Condition: POR, NRES

[9] **PROT_DISABLE_01**: Protection disable for CH1. As long as the bit is set, CH1 is kept actively OFF

0: Output enabled

1: Output OFF

Reset: 0

Reset Condition: POR, NRES

[8:1] **OUTPUT_VOLTAGE**:

Output voltage compared to LVT threshold **(Low-Side**)

0: $V_{OUT} < V_{LVT}$ output ON

1: $V_{OUT} > V_{LVT}$ output OFF

Reset: Initial OUTPUT_VOLTAGE field value depends on load

Reset Condition: POR, NRES

Output voltage compared to VOL threshold (**High-Side**)

0: VOUT < VOL output OFF

1: VOUT > VOL output ON

Reset: Initial OUTPUT_VOLTAGE field value depends on load

Reset Condition: POR, NRES

Note: The OUTPUT_VOLTAGE[8:1] field value depends on external HW configuration. By default, all channels are configured as LS NMOS. Hence, the default value of this field follows such interpretation.

[0] **PARITY**: Parity bit, based on even parity calculation

0: If the number of 1 is odd

1: If the number of 1 is even

RESPONSE 1

Frame partitioning

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C				R/$\overline{W}$	HB1_DEAD_TIME		HB1_TDIAG_EXT_CONFIG	TDIAG_CONFIG_01		OC_READ_01	OC_CONFIG_01						OC_TEMP_COMP_01		OC_BATT_COMP_01	T_BLANK_OC_01			PROT_CONFIG_01	OC_DS_SHUNT_01	DIAG_I_CONFIG_01	GCC_CONFIG_01		N_P_CONFIG_01	LS_HS_CONFIG_01	EN_OUT_01	PARITY

Description:	OUT1 configuration and H-Bridge 1 diagnostic time
Reset:	0x1EC00001

[31:28] **C**: Response to command 1

Reset: 0001

Reset Condition: -

[27] **R/$\overline{W}$**: Bit to read/write configuration

0: Write & request read

1: Request read only

Reset: 1

Reset Condition: POR, NRES

[26:25] **HB1_DEAD_TIME**: H-bridge 1 dead time to avoid cross conduction

00: 1 µs

01: 2 µs

10: 4 µs

11: 8 µs

Reset: 11

Reset Condition: POR, NRES

[24] **HB1_TDIAG_EXT_CONFIG**: Selection of tdiag timers for H-bridge 1. This function only applies when HB1_config = 1

0: H-bridge tdiag timers for HB1. The programmed TDIAG_CONFIG_01 will be extended to

CH2, CH3 and CH4

1: Standard tdiag timers for HB1. The programmed TDIAG_CONFIG_01 is valid only for CH1,

while CH2, CH3 and CH4 must be set individually.

Reset: 0

Reset Condition: POR, NRES

[23:22] **TDIAG_CONFIG_01:**

H-bridge 1 OFF state diagnostic blanking/filter timer. This values are valid only when HB1_tdiag_ext_config = 0 & HB1_config = 1

00: 11.2 µs

01: 28.9 µs

10: 40 µs

11: 51.2 µs

OFF state diagnostic blanking/filter timer for CH1. It is valid for HB1 only when HB1_tdiag_ext_config = 1 & HB1_config = 1

00: 25.6 µs

01: 61.2 µs

10: 105.6 µs

11: 150 µs

Reset: 11

Reset Condition: POR, NRES

[21] **OC_READ_01**: Selection of the OC threshold to read. Fixed threshold or actual threshold

0: Read fixed OC threshold

1: Read actual OC threshold

Reset: 0

Reset Condition: POR, NRES

[20:15] **OC_CONFIG_01**: Selection of over current detection threshold. 6 bit to code for the OC detection threshold

See Table 40. OC threshold selection

Reset: 000000

Reset Condition: POR, NRES

[14:13] **OC_TEMP_COMP_01**: Over current detection with temperature compensation (see note of Table 30. SPI MOSI list)

00: No OC compensation

01: ΔT < 60 °C

10: ΔT < 40 °C

11: ΔT < 25 °C

Reset: 00

Reset Condition: POR, NRES

[12] **OC_BATT_COMP_01**: Over current detection with battery compensation

0: Battery compensation de-activated

1: Battery compensation activated

Reset: 0

Reset Condition: POR, NRES

[11:9] **TBLANK_OC_01**: When DSM is selected, it specifies the OC blanking time to allow VDS settling. When Rshunt is selected, it only determines the assertion of the 'No OC failure' diagnostic code (once expired).

000: 11.1 µs

001: 15.6 µs

010: 20 µs

011: 31.1 µs

100: 42.2 µs

101: 53.3 µs

110: 97.8 µs

111: 142.2 µs

Reset: 000

Reset Condition: POR, NRES

[8] **PROT_CONFIG_01**: Output re-engagement strategy. Specifies how channel reactivation must be performed following an OC event

0: output re-engagement with control signal switching event

1: output re-engagement after diagnostic readout and control signal switching event

Reset: 0

Reset Condition: POR, NRES

[7] **OC_DS_SHUNT_01**: Configures the output measure OC with shunt or by DSM

0: OC with DSM

1: OC with Shunt

Reset: 0

Reset Condition: POR, NRES

[6] **DIAG_I_CONFIG_01**: CH1 OL regulator output current capability

0: 100 µA capability

1: 1 mA capability

Reset: 0

Reset Condition: POR, NRES

[5:4] **GCC_CONFIG_01**: Selection of gate charge/discharge currents

00: Lim by ext resistor

01: 20 mA

10: 5 mA

11: 1 mA

Reset: 00

Reset Condition: POR, NRES

[3] **N_P_CONFIG_01**: NMOS or PMOS option for HS configuration

0: LS configuration

1: HS configuration

Reset: 0

Reset Condition: POR, NRES

[2] **LS_HS_CONFIG_01**: Configures the channel as LS or HS

0: LS configuration

1: HS configuration

Reset: 0

Reset Condition: POR, NRES

[1] **EN_OUT_01**: Enable output 01

0: Output disabled

1: Output enabled

Reset: 0

Reset Condition: POR, NRES

[0] **PARITY**: Parity bit, based on even parity calculation

0: If the number of 1 is odd

1: If the number of 1 is even

Reset: 1

Reset Condition: -

RESPONSE 2

Frame partitioning

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C				$R/\overline{W}$	HB1_TOFF		BATT_FACT_CONFIG	TDIAG_CONFIG_02		OC_READ_02	OC_CONFIG_02						OC_TEMP_COMP_02		OC_BATT_COMP_02	T_BLANK_OC_02			PROT_CONFIG_02	OC_DS_SHUNT_02	DIAG_I_CONFIG_02	GCC_CONFIG_02		N_P_CONFIG_02	LS_HS_CONFIG_02	EN_OUT_02	PARITY

Description: OUT2 configuration, H-Bridge 1 current limitation timing, BCF selection

Reset: 0x2EC00001

[31:28] **C**: Response to command 2
Reset: 0010
Reset Condition: -

[27] **$R/\overline{W}$**: Bit to read/write configuration
0: Write & request read
1: Request read only
Reset: 1
Reset Condition: POR, NRES

[26:25] **HB1_TOFF**: H-bridge1 off timer during current limitation
00: 31 µs
01: 48 µs
10: 62.5 µs
11: 125 µs
Reset: 11
Reset Condition: POR, NRES

[24] **BATT_FACT_CONFIG**: Selection of the factor used in battery compensation
0: Factor for CV
1: Factor for PV
Reset: 0
Reset Condition: POR, NRES

[23:22] **TDIAG_CONFIG_02**: OFF state diagnostic blanking/filter timer for output 02. It has no effect if HB1_config =1 & HB1_tdiag_ext_config = 0
00: 25.6 µs
01: 61.2 µs
10: 105.6 µs
11: 150 µs
Reset: 11
Reset Condition: POR, NRES

[21] **OC_READ_02**: Selection of the OC threshold to read. Fixed threshold or actual threshold
0: Read fixed OC threshold
1: Read actual OC threshold
Reset: 0
Reset Condition: POR, NRES

[20:15] **OC_CONFIG_02**: Selection of over current detection threshold. 6 bit to code for the OC detection threshold

See Table 40. OC threshold selection

Reset: 000000

Reset Condition: POR, NRES

[14:13] **OC_TEMP_COMP_02**: Over current detection with temperature compensation (see note of Table 30. SPI MOSI list)

00: No OC compensation

01: ΔT < 60 °C

10: ΔT < 40 °C

11: ΔT < 25 °C

Reset: 00

Reset Condition: POR, NRES

[12] **OC_BATT_COMP_02**: Over current detection with battery compensation

0: Battery compensation de-activated

1: Battery compensation activated

Reset: 0

Reset Condition: POR, NRES

[11:9] **TBLANK_OC_02**: When DSM is selected, it specifies the OC blanking time to allow VDS settling. When Rshunt is selected, it only determines the assertion of the 'No OC failure' diagnostic code (once expired).

000: 11.1 µs

001: 15.6 µs

010: 20 µs

011: 31.1 µs

100: 42.2 µs

101: 53.3 µs

110: 97.8 µs

111: 142.2 µs

Reset: 000

Reset Condition: POR, NRES

[8] **PROT_CONFIG_02**: Output re-engagement strategy. Specifies how channel reactivation must be performed following an OC event

0: output re-engagement with control signal switching event

1: output re-engagement after diagnostic readout and control signal switching event

Reset: 0

Reset Condition: POR, NRES

[7] **OC_DS_SHUNT_02**: Configures the output measure OC with shunt or by DSM

0: OC with DSM

1: OC with Shunt

Reset: 0

Reset Condition: POR, NRES

[6] **DIAG_I_CONFIG_02**: CH2 OL regulator output current capability

0: 100 µA capability

1: 1 mA capability

Reset: 0

Reset Condition: POR, NRES

[5:4] **GCC_CONFIG_02**: Selection of gate charge/discharge currents
00: Lim by ext resistor
01: 20 mA
10: 5 mA
11: 1 mA
Reset: 00
Reset Condition: POR, NRES

[3] **N_P_CONFIG_02**: NMOS or PMOS option for HS configuration
0: LS configuration
1: HS configuration
Reset: 0
Reset Condition: POR, NRES

[2] **LS_HS_CONFIG_02**: Configures the channel as LS or HS
0: LS configuration
1: HS configuration
Reset: 0
Reset Condition: POR, NRES

[1] **EN_OUT_02**: Enable output 02
0: Output disabled
1: Output enabled
Reset: 0
Reset Condition: POR, NRES

[0] **PARITY**: Parity bit, based on even parity calculation
0: If the number of 1 is odd
1: If the number of 1 is even
Reset: 1
Reset Condition: -

RESPONSE 3

Frame partitioning

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C				R/$\overline{W}$	HB1_ILIM_EN	HB1_AFW	GCC_OVERRIDE_CONFIG	TDIAG_CONFIG_03		OC_READ_03	OC_CONFIG_03						OC_TEMP_COMP_03		OC_BATT_COMP_03	T_BLANK_OC_03			PROT_CONFIG_03	OC_DS_SHUNT_03	DIAG_I_CONFIG_03	GCC_CONFIG_03		N_P_CONFIG_03	LS_HS_CONFIG_03	EN_OUT_03	PARITY

Description:	OUT3 configuration, H-Bridge 1 current limitation enable and active freewheeling, gate charge/ discharge current override
Reset	0x3BC00000

[31:28] **C**: Reponse to command 3

Reset: 0011

Reset Condition: POR, NRES

[27] **R/$\overline{W}$**: Bit to read/write configuration

0: Write & request read

1: Request read only

Reset: 1

Reset Condition: POR, NRES

[26] **HB1_ILIM_EN**: H-bridge1 current limit activation. CH3 OC threshold is used for current limitation, it is only valid for Shunt measurement

0: Current limitation not active

1: Current limitation active

Reset: 0

Reset Condition: POR, NRES

[25] **HB1_AFW**: H-bridge1 active freewheel configuration on LS

0: Freewheel low

1: Active freewheeling

Reset: 1

Reset Condition: POR, NRES

[24] **GCC_OVERRIDE_CONFIG**: GCC configuration of the channel, regardless of its channels configuration (LS.HS,H-bridge) must be override to a higher GCC configuration upon OC detection. GCC configuration will remain active until next (NON+SPI) internal turn off transition, in which case the override will be cleared

0: GCC override function upon OC detection:

1 mA → 5 mA

5 mA → 20 mA

1: GCC override function upon OC detection:

1 mA → 20 mA

5 mA → 20 mA

Reset: 1

Reset Condition: POR, NRES

[23:22] **TDIAG_CONFIG_03**: OFF state diagnostic blanking/filter timer for output 03. It has no effect if HB1_config =1 & HB1_tdiag_ext_config = 0

00: 25.6 µs

01: 61.2 µs

10: 105.6 µs

11: 150 µs

Reset: 11

Reset Condition: POR, NRES

[21] **OC_READ_03**: Selection of the OC threshold to read. Fixed threshold or actual threshold

0: Read fixed OC threshold

1: Read actual OC threshold

Reset: 0

Reset Condition: POR, NRES

[20:15] **OC_CONFIG_03**: Selection of over current detection threshold. 6 bit to code for the OC detection threshold

See Table 40. OC threshold selection

Reset: 000000

Reset Condition: POR, NRES

[14:13] **OC_TEMP_COMP_03**: Over current detection with temperature compensation (see note of Table 30. SPI MOSI list)

00: No OC compensation

01: ΔT < 60 °C

10: ΔT < 40 °C

11: ΔT < 25 °C

Reset: 00

Reset Condition: POR, NRES

[12] **OC_BATT_COMP_03**: Over current detection with battery compensation

0: Battery compensation de-activated

1: Battery compensation activated

Reset: 0

Reset Condition: POR, NRES

[11:9] **TBLANK_OC_03**: When DSM is selected, it specifies the OC blanking time to allow VDS settling. When Rshunt is selected, it only determines the assertion of the 'No OC failure' diagnostic code (once expired).

000: 11.1 µs

001: 15.6 µs

010: 20 µs

011: 31.1 µs

100: 42.2 µs

101: 53.3 µs

110: 97.8 µs

111: 142.2 µs

Reset: 000

Reset Condition: POR, NRES

[8] **PROT_CONFIG_03**: Output re-engagement strategy. Specifies how channel reactivation must be performed following an OC event

0: output re-engagement with control signal switching event

1: output re-engagement after diagnostic readout and control signal switching event

Reset: 0

Reset Condition: POR, NRES

[7] **OC_DS_SHUNT_03**: Configures the output measure OC with shunt or by DSM

0: OC with DSM

1: OC with Shunt

Reset: 0

Reset Condition: POR, NRES

[6] **DIAG_I_CONFIG_03**: CH3 OL regulator output current capability

0: 100 µA capability

1: 1 mA capability

Reset: 0

Reset Condition: POR, NRES

[5:4] **GCC_CONFIG_03**: Selection of gate charge/discharge currents

00: Lim by ext resistor

01: 20 mA

10: 5 mA

11: 1 mA

Reset: 00

Reset Condition: POR, NRES

[3] **N_P_CONFIG_03**: NMOS or PMOS option for HS configuration

0: LS configuration

1: HS configuration

Reset: 0

Reset Condition: POR, NRES

[2] **LS_HS_CONFIG_03**: Configures the channel as LS or HS

0: LS configuration

1: HS configuration

Reset: 0

Reset Condition: POR, NRES

[1] **EN_OUT_03**: Enable output 03

0: Output disabled

1: Output enabled

Reset: 0

Reset Condition: POR, NRES

[0] **PARITY**: Parity bit, based on even parity calculation

0: If the number of 1 is odd

1: If the number of 1 is even

Reset: 0

Reset Condition: -

RESPONSE 4

Frame partitioning

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C				$R/\overline{W}$	HB1_CONFIG	PH1_DIAG_STRATEGY	PH1_CONFIG	TDIAG_CONFIG_04		OC_READ_04	OC_CONFIG_04						OC_TEMP_COMP_04		OC_BATT_COMP_04	T_BLANK_OC_04			PROT_CONFIG_04	OC_DS_SHUNT_04	DIAG_I_CONFIG_04	GCC_CONFIG_04		N_P_CONFIG_04	LS_HS_CONFIG_04	EN_OUT_04	PARITY

Description: OUT4 configuration, P&H1 configuration, H-Bridge 1 enable

Reset: 0x48C00001

[31:28] **C**: Response to command 4
Reset: 0100
Reset Condition: POR, NRES

[27] **$R/\overline{W}$**: Bit to read/write configuration
0: Write & request read
1: Request read only
Reset: 1
Reset Condition: POR, NRES

[26] **HB1_CONFIG**: Configures CH1-CH2-CH3-CH4 for H-bridge1 operation
0: Not H-bridge configured
1: CH1-CH4 configured as H-bridge
Reset: 0
Reset Condition: POR, NRES

[25] **PH1_DIAG_STRATEGY**: OL masking strategy to prevent false OL assertion in P&H1 configuration
0: "No OL/STG /STB" failure reported
1: "No diagnostic done" reported
Reset: 0
Reset Condition: POR, NRES

[24] **PH1_CONFIG**: Configures CH1-CH4 for Peak and Hold1 configuration
0: Peak and Hold1 not configured
1: Peak and Hold1 configured
Reset: 0
Reset Condition: POR, NRES

[23:22] **TDIAG_CONFIG_04**: OFF state diagnostic blanking/filter timer for output 04. It has no effect if HB1_config =1 & HB1_tdiag_ext_config = 0
00: 25.6 µs
01: 61.2 µs
10: 105.6 µs
11: 150 µs
Reset: 11
Reset Condition: POR, NRES

[21] **OC_READ_04**: Selection of the OC threshold to read. Fixed threshold or actual threshold

0: Read fixed OC threshold

1: Read actual OC threshold

Reset: 0

Reset Condition: POR, NRES

[20:15] **OC_CONFIG_04**: Selection of over current detection threshold. 6 bit to code for the OC detection threshold

See Table 40. OC threshold selection

Reset: 000000

Reset Condition: POR, NRES

[14:13] **OC_TEMP_COMP_04**: Over current detection with temperature compensation (see note of Table 30. SPI MOSI list)

00: No OC compensation

01: ΔT < 60 °C

10: ΔT < 40 °C

11: ΔT < 25 °C

Reset: 00

Reset Condition: POR, NRES

[12] **OC_BATT_COMP_04**: Over current detection with battery compensation

0: Battery compensation de-activated

1: Battery compensation activated

Reset: 0

Reset Condition: POR, NRES

[11:9] **TBLANK_OC_04**: When DSM is selected, it specifies the OC blanking time to allow VDS settling. When Rshunt is selected, it only determines the assertion of the 'No OC failure' diagnostic code (once expired).

000: 11.1 µs

001: 15.6 µs

010: 20 µs

011: 31.1 µs

100: 42.2 µs

101: 53.3 µs

110: 97.8 µs

111: 142.2 µs

Reset: 000

Reset Condition: POR, NRES

[8] **PROT_CONFIG_04**: Output re-engagement strategy. Specifies how channel reactivation must be performed following an OC event

0: output re-engagement with control signal switching event

1: output re-engagement after diagnostic readout and control signal switching event

Reset: 0

Reset Condition: POR, NRES

[7] **OC_DS_SHUNT_04**: Configures the output measure OC with shunt or by DSM

0: OC with DSM

1: OC with Shunt

Reset: 0

Reset Condition: POR, NRES

[6] **DIAG_I_CONFIG_04**: CH4 OL regulator output current capability

0: 100 µA capability

1: 1 mA capability

Reset: 0

Reset Condition: POR, NRES

[5:4] **GCC_CONFIG_04**: Selection of gate charge/discharge currents

00: Lim by ext resistor

01: 20 mA

10: 5 mA

11: 1 mA

Reset: 00

Reset Condition: POR, NRES

[3] **N_P_CONFIG_04**: NMOS or PMOS option for HS configuration

0: LS configuration

1: HS configuration

Reset: 0

Reset Condition: POR, NRES

[2] **LS_HS_CONFIG_04**: Configures the channel as LS or HS

0: LS configuration

1: HS configuration

Reset: 0

Reset Condition: POR, NRES

[1] **EN_OUT_04**: Enable output 04

0: Output disabled

1: Output enabled

Reset: 0

Reset Condition: POR, NRES

[0] **PARITY**: Parity bit, based on even parity calculation

0: If the number of 1 is odd

1: If the number of 1 is even

Reset: 0

Reset Condition: -

RESPONSE 5

Frame partitioning

<table>
<tr><td>31</td><td>30</td><td>29</td><td>28</td><td>27</td><td>26</td><td>25</td><td>24</td><td>23</td><td>22</td><td>21</td><td>20</td><td>19</td><td>18</td><td>17</td><td>16</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>9</td><td>8</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td colspan="4">C</td><td>R/$\overline{\text{W}}$</td><td colspan="2">HB2_DEAD_TIME</td><td>HB2_TDIAG_EXT_CONFIG</td><td colspan="2">TDIAG_CONFIG_05</td><td>OC_READ_05</td><td colspan="6">OC_CONFIG_05</td><td colspan="2">OC_TEMP_COMP_05</td><td>OC_BATT_COMP_05</td><td colspan="3">T_BLANK_OC_05</td><td>PROT_CONFIG_05</td><td>OC_DS_SHUNT_05</td><td>DIAG_I_CONFIG_05</td><td colspan="2">GCC_CONFIG_05</td><td>N_P_CONFIG_05</td><td>LS_HS_CONFIG_05</td><td>EN_OUT_05</td><td>PARITY</td></tr>
</table>

Description	OUT 5 configuration and H-Bridge 2 diagnostic time
Reset:	0x5EC00000

[31:28] **C**: Response to command 5

Reset: 0101

Reset Condition: POR, NRES

[27] **R/$\overline{\text{W}}$**: Bit to read/write configuration

0: Write & request read

1: Request read only

Reset: 1

Reset Condition: POR, NRES

[26:25] **HB2_DEAD_TIME**: H-bridge2 dead time to avoid cross conduction

00: 1 µs

01: 2 µs

10: 4 µs

11: 8 µs

Reset: 11

Reset Condition: POR, NRES

[24] **HB2_TDIAG_EXT_CONFIG**: Selection of tdiag timers for H-bridge 2. This function only applies when HB2_config = 1 (command 8)

0: H-bridge tdiag timers for HB2. The programmed TDIAG_CONFIG_05 will be extended to

CH6, CH7 and CH8.

1: Standard tdiag timers for HB2. The programmed TDIAG_CONFIG_05 is valid only for CH5,

while CH6, CH7 and CH8 must be set individually

Reset: 0

Reset Condition: POR, NRES

[23:22] **TDIAG_CONFIG_05**:

H-bridge 2 OFF state diagnostic blanking/filter timer. This values are valid only when HB2_tdiag_ext_config = 0 & HB2_config = 1

00: 11.2 µs

01: 28.9 µs

10: 40 µs

11: 51.2 µs

OFF state diagnostic blanking/filter timer for CH5. It is valid for HB1 only when HB2_tdiag_ext_config = 1 & HB2_config = 1

00: 25.6 µs

01: 61.2 µs

10: 105.6 µs

11: 150 µs

Reset: 11

Reset Condition: POR, NRES

[21] **OC_READ_05**: Selection of the OC threshold to read. Fixed threshold or actual threshold

0: Read fixed OC threshold

1: Read actual OC threshold

Reset: 0

Reset Condition: POR, NRES

[20:15] **OC_CONFIG_05**: Selection of over current detection threshold. 6 bit to code for the OC detection threshold

See Table 40. OC threshold selection

Reset: 000000

Reset Condition: POR, NRES

[14:13] **OC_TEMP_COMP_05**: Over current detection with temperature compensation (see note of Table 30. SPI MOSI list)

00: No OC compensation

01: ΔT < 60 °C

10: ΔT < 40 °C

11: ΔT < 25 °C

Reset: 00

Reset Condition: POR, NRES

[12] **OC_BATT_COMP_05**: Over current detection with battery compensation

0: Battery compensation de-activated

1: Battery compensation activated

Reset: 0

Reset Condition: POR, NRES

[11:9] **TBLANK_OC_05**: When DSM is selected, it specifies the OC blanking time to allow VDS settling. When Rshunt is selected, it only determines the assertion of the 'No OC failure' diagnostic code (once expired).

000: 11.1 µs

001: 15.6 µs

010: 20 µs

011: 31.1 µs

100: 42.2 µs

101: 53.3 µs

110: 97.8 µs

111: 142.2 µs

Reset: 000

Reset Condition: POR, NRES

[8] **PROT_CONFIG_05**: Output re-engagement strategy. Specifies how channel reactivation must be performed following an OC event

0: output re-engagement with control signal switching event

1: output re-engagement after diagnostic readout and control signal switching event

Reset: 0

Reset Condition: POR, NRES

[7] **OC_DS_SHUNT_05**: Configures the output measure OC with shunt or by DSM

0: OC with DSM

1: OC with Shunt

Reset: 0

Reset Condition: POR, NRES

[6] **DIAG_I_CONFIG_05**: CH5 OL regulator output current capability

0: 100 µA capability

1: 1 mA capability

Reset: 0

Reset Condition: POR, NRES

[5:4] **GCC_CONFIG_05**: Selection of gate charge/discharge currents

00: Lim by ext resistor

01: 20 mA

10: 5 mA

11: 1 mA

Reset: 00

Reset Condition: POR, NRES

[3] **N_P_CONFIG_05**: NMOS or PMOS option for HS configuration

0: LS configuration

1: HS configuration

Reset: 0

Reset Condition: POR, NRES

[2] **LS_HS_CONFIG_05**: Configures the channel as LS or HS

0: LS configuration

1: HS configuration

Reset: 0

Reset Condition: POR, NRES

[1] **EN_OUT_05**: Enable output 05

0: Output disabled

1: Output enabled

Reset: 0

Reset Condition: POR, NRES

[0] **PARITY**: Parity bit, based on even parity calculation

0: If the number of 1 is odd

1: If the number of 1 is even

Reset: 0

Reset Condition: -

RESPONSE 6

Frame partitioning

<table>
<tr><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="4">C</td><td>R/$\overline{W}$</td><td colspan="2">HB2_TOFF</td><td>FIXED_PATTERN</td><td colspan="2">TDIAG_CONFIG_06</td><td>OC_READ_06</td><td colspan="6">OC_CONFIG_06</td><td colspan="2">OC_TEMP_COMP_06</td><td>OC_BATT_COMP_06</td><td colspan="3">T_BLANK_OC_06</td><td>PROT_CONFIG_06</td><td>OC_DS_SHUNT_06</td><td>DIAG_I_CONFIG_06</td><td colspan="2">GCC_CONFIG_06</td><td>N_P_CONFIG_06</td><td>LS_HS_CONFIG_06</td><td>EN_OUT_06</td><td>PARITY</td></tr>
</table>

Description: OUT6 configuration, H-Bridge 2 current limitation timing

Reset: 0x6EC00000

[31:28] **C**: Response to command 6
Reset: 0101
Reset Condition: POR, NRES

[27] **R/$\overline{W}$**: Bit to read/write configuration
0: Write & request read
1: Request read only
Reset: 1
Reset Condition: POR, NRES

[26:25] **HB2_TOFF**: H-bridge2 off timer during current limitation
00: 31 µs
01: 48 µs
10: 62.5 µs
11: 125 µs
Reset: 11
Reset Condition: POR, NRES

[24] **FIXED_PATTERN**
Reset: 0
Reset Condition: POR, NRES

[23:22] **TDIAG_CONFIG_06**: OFF state diagnostic blanking/filter timer for CH6. It is valid for HB1 only when HB2_tdiag_ext_config = 1 & HB2_config = 1
00: 25.6 µs
01: 61.2 µs
10: 105.6 µs
11: 150 µs
Reset: 11
Reset Condition: POR, NRES

[21] **OC_READ_06**: Selection of the OC threshold to read. Fixed threshold or actual threshold
0: Read fixed OC threshold
1: Read actual OC threshold
Reset: 0
Reset Condition: POR, NRES

[20:15] **OC_CONFIG_06**: Selection of over current detection threshold. 6 bit to code for the OC detection threshold

See Table 40. OC threshold selection

Reset: 000000

Reset Condition: POR, NRES

[14:13] **OC_TEMP_COMP_06**: Over current detection with temperature compensation (see note of Table 30. SPI MOSI list)

00: No OC compensation

01: ΔT < 60 °C

10: ΔT < 40 °C

11: ΔT < 25 °C

Reset: 00

Reset Condition: POR, NRES

[12] **OC_BATT_COMP_06**: Over current detection with battery compensation

0: Battery compensation de-activated

1: Battery compensation activated

Reset: 0

Reset Condition: POR, NRES

[11:9] **TBLANK_OC_06**: When DSM is selected, it specifies the OC blanking time to allow VDS settling. When Rshunt is selected, it only determines the assertion of the 'No OC failure' diagnostic code (once expired).

000: 11.1 µs

001: 15.6 µs

010: 20 µs

011: 31.1 µs

100: 42.2 µs

101: 53.3 µs

110: 97.8 µs

111: 142.2 µs

Reset: 000

Reset Condition: POR, NRES

[8] **PROT_CONFIG_06**: Output re-engagement strategy. Specifies how channel reactivation must be performed following an OC event

0: output re-engagement with control signal switching event

1: output re-engagement after diagnostic readout and control signal switching event

Reset: 0

Reset Condition: POR, NRES

[7] **OC_DS_SHUNT_06**: Configures the output measure OC with shunt or by DSM

0: OC with DSM

1: OC with Shunt

Reset: 0

Reset Condition: POR, NRES

[6] **DIAG_I_CONFIG_06**: CH6 OL regulator output current capability

0: 100 µA capability

1: 1 mA capability

Reset: 0

Reset Condition: POR, NRES

[5:4] **GCC_CONFIG_06**: Selection of gate charge/discharge currents
00: Lim by ext resistor
01: 20 mA
10: 5 mA
11: 1 mA
Reset: 00
Reset Condition: POR, NRES

[3] **N_P_CONFIG_06**: NMOS or PMOS option for HS configuration
0: LS configuration
1: HS configuration
Reset: 0
Reset Condition: POR, NRES

[2] **LS_HS_CONFIG_06**: Configures the channel as LS or HS
0: LS configuration
1: HS configuration
Reset: 0
Reset Condition: POR, NRES

[1] **EN_OUT_06**: Enable output 06
0: Output disabled
1: Output enabled
Reset: 0
Reset Condition: POR, NRES

[0] **PARITY**: Parity bit, based on even parity calculation
0: If the number of 1 is odd
1: If the number of 1 is even
Reset: 0
Reset Condition: -

RESPONSE 7

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C				$R/\overline{W}$	HB2_ILIM_EN	HB2_AFW	FIXED_PATTERN	TDIAG_CONFIG_07		OC_READ_07	OC_CONFIG_07						OC_TEMP_COMP_07		OC_BATT_COMP_07	T_BLANK_OC_07			PROT_CONFIG_07	OC_DS_SHUNT_07	DIAG_I_CONFIG_07	GCC_CONFIG_07		N_P_CONFIG_07	LS_HS_CONFIG_07	EN_OUT_07	PARITY

Description: OUT7 configuration, H-Bridge 2 current limitation enable and active freewheeling

Reset: 0x7AC00000

[31:28] **C**: Response to command 7

Reset: 0111

Reset Condition: POR, NRES

[27] **$R/\overline{W}$**: Bit to read/write configuration

0: Write & request read

1: Request read only

Reset: 1

Reset Condition: POR, NRES

[26] **HB1_ILIM_EN**: H-bridge2 current limit activation. CH7 OC threshold is used for current limitation, it is only valid for Shunt measurement

0: Current limitation not active

1: Current limitation active

Reset: 0

Reset Condition: POR, NRES

[25] **HB2_AFW**: H-bridge2 active freewheel configuration on LS

0: Freewheel low

1: Active freewheeling

Reset: 1

Reset Condition: POR, NRES

[24] **FIXED_PATTERN**

Reset: 0

Reset Condition: POR, NRES

[23:22] **TDIAG_CONFIG_07**: OFF state diagnostic blanking/filter timer for output 07. It has no effect if HB2_config =1 & HB2_tdiag_ext_config = 0

00: 25.6 µs

01: 61.2 µs

10: 105.6 µs

11: 150 µs

Reset: 11

Reset Condition: POR, NRES

[21] **OC_READ_07**: Selection of the OC threshold to read. Fixed threshold or actual threshold

0: Read fixed OC threshold

1: Read actual OC threshold

Reset: 0

Reset Condition: POR, NRES

[20:15] **OC_CONFIG_07**: Selection of over current detection threshold. 6 bit to code for the OC detection threshold

See Table 40. OC threshold selection

Reset: 000000

Reset Condition: POR, NRES

[14:13] **OC_TEMP_COMP_07**: Over current detection with temperature compensation (see note of Table 30. SPI MOSI list)

00: No OC compensation

01: ΔT < 60 °C

10: ΔT < 40 °C

11: ΔT < 25 °C

Reset: 00

Reset Condition: POR, NRES

[12] **OC_BATT_COMP_07**: Over current detection with battery compensation

0: Battery compensation de-activated

1: Battery compensation activated

Reset: 0

Reset Condition: POR, NRES

[11:9] **TBLANK_OC_07**: When DSM is selected, it specifies the OC blanking time to allow VDS settling. When Rshunt is selected, it only determines the assertion of the 'No OC failure' diagnostic code (once expired).

000: 11.1 µs

001: 15.6 µs

010: 20 µs

011: 31.1 µs

100: 42.2 µs

101: 53.3 µs

110: 97.8 µs

111: 142.2 µs

Reset: 000

Reset Condition: POR, NRES

[8] **PROT_CONFIG_07**: Output re-engagement strategy. Specifies how channel reactivation must be performed following an OC event

0: output re-engagement with control signal switching event

1: output re-engagement after diagnostic readout and control signal switching event

Reset: 0

Reset Condition: POR, NRES

[7] **OC_DS_SHUNT_07**: Configures the output measure OC with shunt or by DSM

0: OC with DSM

1: OC with Shunt

Reset: 0

Reset Condition: POR, NRES

[6] **DIAG_I_CONFIG_07**: CH7 OL regulator output current capability

0: 100 µA capability

1: 1 mA capability

Reset: 0

Reset Condition: POR, NRES

[5:4] **GCC_CONFIG_07**: Selection of gate charge/discharge currents

00: Lim by ext resistor

01: 20 mA

10: 5 mA

11: 1 mA

Reset: 00

Reset Condition: POR, NRES

[3] **N_P_CONFIG_07**: NMOS or PMOS option for HS configuration

0: LS configuration

1: HS configuration

Reset: 0

Reset Condition: POR, NRES

[2] **LS_HS_CONFIG_07**: Configures the channel as LS or HS

0: LS configuration

1: HS configuration

Reset: 0

Reset Condition: POR, NRES

[1] **EN_OUT_07**: Enable output 07

0: Output disabled

1: Output enabled

Reset: 0

Reset Condition: POR, NRES

[0] **PARITY**: Parity bit, based on even parity calculation

0: If the number of 1 is odd

1: If the number of 1 is even

Reset: 0

Reset Condition: -

RESPONSE 8

Frame partitioning

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C				R/$\overline{W}$	HB2_CONFIG	PH2_DIAG_STRATEGY	PH2_CONFIG	TDIAG_CONFIG_08		OC_READ_08	OC_CONFIG_08						OC_TEMP_COMP_08		OC_BATT_COMP_08	T_BLANK_OC_08			PROT_CONFIG_08	OC_DS_SHUNT_08	DIAG_I_CONFIG_08	GCC_CONFIG_08		N_P_CONFIG_08	LS_HS_CONFIG_08	EN_OUT_08	PARITY

Description	OUT8 configuration, P&H2 configuration, H-Bridge 2 enable
Reset:	0x88C00001

[31:28] **C**: Response to command 8

Reset: 1000

Reset Condition: POR, NRES

[27] **R/$\overline{W}$**: Bit to read/write configuration

0: Write & request read

1: Request read only

Reset: 1

Reset Condition: POR, NRES

[26] **HB2_CONFIG**: Configures CH5-CH6-CH7-CH8 for H-bridge2 operation

0: Not H-bridge configured

1: CH5-CH8 configured as H-bridge

Reset: 0

Reset Condition: POR, NRES

[25] **PH2_DIAG_STRATEGY**: OL masking strategy to prevent false OL assertion in P&H2 configuration

0: "No OL/STG /STB" failure reported

1: "No diagnostic done" reported

Reset: 0

Reset Condition: POR, NRES

[24] **PH2_CONFIG**: Configures CH5-CH8 for Peak and Hold2 configuration

0: Peak and Hold2 not configured

1: Peak and Hold2 configured

Reset: 0

Reset Condition: POR, NRES

[23:22] **TDIAG_CONFIG_08**: OFF state diagnostic blanking/filter timer for output 02. It has no effect if HB1_config =1 & HB1_tdiag_ext_config = 0

00: 25.6 µs

01: 61.2 µs

10: 105.6 µs

11: 150 µs

Reset: 11

Reset Condition: POR, NRES

[21] **OC_READ_08**: Selection of the OC threshold to read. Fixed threshold or actual threshold

0: Read fixed OC threshold

1: Read actual OC threshold

Reset: 0

Reset Condition: POR, NRES

[20:15] **OC_CONFIG_08**: Selection of over current detection threshold. 6 bit to code for the OC detection threshold

See Table 40. OC threshold selection

Reset: 000000

Reset Condition: POR, NRES

[14:13] **OC_TEMP_COMP_08**: Over current detection with temperature compensation (see note of Table 30. SPI MOSI list)

00: No OC compensation

01: ΔT < 60 °C

10: ΔT < 40 °C

11: ΔT < 25 °C

Reset: 00

Reset Condition: POR, NRES

[12] **OC_BATT_COMP_08**: Over current detection with battery compensation

0: Battery compensation de-activated

1: Battery compensation activated

Reset: 0

Reset Condition: POR, NRES

[11:9] **TBLANK_OC_08**: When DSM is selected, it specifies the OC blanking time to allow VDS settling. When Rshunt is selected, it only determines the assertion of the 'No OC failure' diagnostic code (once expired).

000: 11.1 µs

001: 15.6 µs

010: 20 µs

011: 31.1 µs

100: 42.2 µs

101: 53.3 µs

110: 97.8 µs

111: 142.2 µs

Reset: 000

Reset Condition: POR, NRES

[8] **PROT_CONFIG_08**: Output re-engagement strategy. Specifies how channel reactivation must be performed following an OC event

0: output re-engagement with control signal switching event

1: output re-engagement after diagnostic readout and control signal switching event

Reset: 0

Reset Condition: POR, NRES

[7] **OC_DS_SHUNT_08**: Configures the output measure OC with shunt or by DSM

0: OC with DSM

1: OC with Shunt

Reset: 0

Reset Condition: POR, NRES

[6] **DIAG_I_CONFIG_08**: CH8 OL regulator output current capability

0: 100 μA capability

1: 1 mA capability

Reset: 0

Reset Condition: POR, NRES

[5:4] **GCC_CONFIG_08**: Selection of gate charge/discharge currents

00: Lim by ext resistor

01: 20 mA

10: 5 mA

11: 1 mA

Reset: 00

Reset Condition: POR, NRES

[3] **N_P_CONFIG_08**: NMOS or PMOS option for HS configuration

0: LS configuration

1: HS configuration

Reset: 0

Reset Condition: POR, NRES

[2] **LS_HS_CONFIG_08**: Configures the channel as LS or HS

0: LS configuration

1: HS configuration

Reset: 0

Reset Condition: POR, NRES

[1] **EN_OUT_08**: Enable output 08

0: Output disabled

1: Output enabled

Reset: 0

Reset Condition: POR, NRES

[0] **PARITY**: Parity bit, based on even parity calculation

0: If the number of 1 is odd

1: If the number of 1 is even

Reset: 0

Reset Condition: -

RESPONSE 9

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C				R/$\overline{W}$	HB2_ILIM	HB1_ILIM	DIAG_08_2	DIAG_07_2	DIAG_06_2	DIAG_05_2	DIAG_04_2	DIAG_03_2	DIAG_02_2	DIAG_01_2	DIAG_08_1	DIAG_07_1	DIAG_06_1	DIAG_05_1	DIAG_04_1	DIAG_03_1	DIAG_02_1	DIAG_01_1	DIAG_08_0	DIAG_07_0	DIAG_06_0	DIAG_05_0	DIAG_04_0	DIAG_03_0	DIAG_02_0	DIAG_01_0	PARITY

Description: OUT8 configuration, P&H2 configuration, H-Bridge 2 enable

Reset: 0x99FFFFFE

[31:28] **C**: Response to command 9

Reset: 1001

Reset Condition: POR, NRES

[27] **R/$\overline{W}$**: Bit to read/write configuration

0: Write & request read

1: Request read only

Reset: 1

Reset Condition: POR, NRES

[26] **HB2_ILIM**: H-bridge 2 Current limitation latch

0: No current limitation active

1: Current limitation active

Reset: 0

Reset Condition: Read out POR, NRES

[25] **HB1_ILIM**: H-bridge 1 Current limitation latch

0: No current limitation active

1: Current limitation active

Reset: 0

Reset Condition: Read out POR, NRES

[24, 16, 8] **DIAG_08**: Diagnostic information for CH8

diag_8[2] diag_8[1] diag_8[0]:

0 0 0: OC pin failure

0 0 1: OC failure

0 1 0: STG/STB failure

0 1 1: OL failure

1 0 0: no failure

1 0 1: No OC failure

1 1 0: No OL/STG/STB failure

1 1 1: no diagnostic done

Reset: 111

Reset Condition: Read out POR, NRES

[23, 15, 7]	**DIAG_07**: Diagnostic information for CH7 diag_7[2] diag_7[1] diag_7[0]: 0 0 0: OC pin failure 0 0 1: OC failure 0 1 0: STG/STB failure 0 1 1: OL failure 1 0 0: no failure 1 0 1: No OC failure 1 1 0: No OL/STG/STB failure 1 1 1: no diagnostic done Reset: 111 Reset Condition: Read out POR, NRES
[22, 14, 6]	**DIAG_06**: Diagnostic information for CH6 diag_6[2] diag_6[1] diag_6[0]: 0 0 0: OC pin failure 0 0 1: OC failure 0 1 0: STG/STB failure 0 1 1: OL failure 1 0 0: no failure 1 0 1: No OC failure 1 1 0: No OL/STG/STB failure 1 1 1: no diagnostic done Reset: 111 Reset Condition: Read out POR, NRES
[21, 13, 5]	**DIAG_05**: Diagnostic information for CH5 diag_5[2] diag_5[1] diag_5[0]: 0 0 0: OC pin failure 0 0 1: OC failure 0 1 0: STG/STB failure 0 1 1: OL failure 1 0 0: no failure 1 0 1: No OC failure 1 1 0: No OL/STG/STB failure 1 1 1: no diagnostic done Reset: 111 Reset Condition: Read out POR, NRES

[20, 12, 4]	**DIAG_04**: Diagnostic information for CH4 diag_4[2] diag_4[1] diag_4[0]: 0 0 0: OC pin failure 0 0 1: OC failure 0 1 0: STG/STB failure 0 1 1: OL failure 1 0 0: no failure 1 0 1: No OC failure 1 1 0: No OL/STG/STB failure 1 1 1: no diagnostic done Reset: 111 Reset Condition: Read out POR, NRES
[19, 11, 3]	**DIAG_03**: Diagnostic information for CH3 diag_3[2] diag_3[1] diag_3[0]: 0 0 0: OC pin failure 0 0 1: OC failure 0 1 0: STG/STB failure 0 1 1: OL failure 1 0 0: no failure 1 0 1: No OC failure 1 1 0: No OL/STG/STB failure 1 1 1: no diagnostic done Reset: 111 Reset Condition: Read out POR, NRES
[18, 10, 2]	**DIAG_02**: Diagnostic information for CH2 diag_2[2] diag_2[1] diag_2[0]: 0 0 0: OC pin failure 0 0 1: OC failure 0 1 0: STG/STB failure 0 1 1: OL failure 1 0 0: no failure 1 0 1: No OC failure 1 1 0: No OL/STG/STB failure 1 1 1: no diagnostic done Reset: 111 Reset Condition: Read out POR, NRES

[17, 9, 1]	**DIAG_01**: Diagnostic information for CH1 diag_1[2] diag_1[1] diag_1[0]: 0 0 0: OC pin failure 0 0 1: OC failure 0 1 0: STG/STB failure 0 1 1: OL failure 1 0 0: no failure 1 0 1: No OC failure 1 1 0: No OL/STG/STB failure 1 1 1: no diagnostic done Reset: 111 Reset Condition: Read out POR, NRES
[0]	**PARITY**: Parity bit, based on even parity calculation 0: If the number of 1 is odd 1: If the number of 1 is even Reset: 0 Reset Condition: -

RESPONSE 10

Frame partitioning

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C				R/$\overline{W}$	EN6_LATCH	EN6_STATE	OV_DIS_LATCH	UV_DIS_STATE	UV_DIS_LATCH	DIS_STATE	DIS_LATCH	NDIS_STATE	NDIS_LATCH	NDIS_OUT_LATCH	CONFIG_CC_STATE	CC_LATCH	BIST_DONE	BIST_DIS	HWSC_DONE	HWSC_DIS	OV_VDD5_STATE	OV_VDD5_LATCH	UV_VDD5_STATE	UV_VDD5_LATCH	N_POR_LATCH	NRES_LATCH	VCP_UV_STATE	VCP_UV_LATCH	VPS_STATE	VPS_LATCH	PARITY

Description: BIST & HWSC result and device status

Note: the value of DIS, NDIS and EN6 related bit depends on how the microcontroller drives such pins. The value of POR and NRES related bit depends on which event caused the logic reset. The value of BIST and HWSC related bit depends on which event caused the logic reset: self test sequence is not performed in case of POR. In addition, the value of BIST_DONE and HWSC_DONE bit depends on the status of self test sequence at the time instant where the read event occurs. The CC_LATCH is set in case the first SPI communication occurs after the watchdog timer expired. The UV_DIS_LATCH and UV_VDD5_LATCH might be set at startup, depending on the VDD5 ramp slope. It is strongly recommended to perform two consecutive SPI read via COMMAND 10 in order to verify that the relevant faults (eventually latched during startup) are cleared.

[31:28] **C**: Response to command 10

Reset: 1010

Reset Condition: -

[27] **R/$\overline{\mathbf{W}}$**: Bit to read/write configuration

0: Write & request read

1: Request read only

Reset: 1

Reset Condition: POR, NRES

[26] **EN6_LATCH**: Shows if a deactivation via EN6 pin was detected since last read out (EN6 = LOW)

0: no disable via EN6 detected

1: disable via EN6 detected

Reset: X

Reset Condition: Read out POR

[25] **EN6_STATE**: Shows if channel 6 is currently disabled by the EN6 input

0: EN disabled

1: EN enabled

Reset: 0

Reset Condition: -

[24] **OV_DIS_LATCH**: Bit set to 1 (OV filtering expired) if VDD5 overvoltage disable was triggered since last read out (shows also if OV occurs during Reset)

0: no OV disable condition detected

1: OV disable condition detected

Reset: 0

Reset Condition: -

[23] **UV_DIS_STATE**: Shows if the device is currently in VDD5 under voltage disable
0: Currently no UV condition
1: UV condition active
Reset: 0
Reset Condition: Read out POR, NRES

[22] **UV_DIS_LATCH**: Bit set to 1 (UV filter expired) if VDD5 under voltage disable was triggered
0: no UV condition detected
1: UV condition detected
Reset: 0
Reset Condition: Read out POR

[21] **DIS_STATE**: Shows if the device is currently disabled by the DIS input signal
0: DIS inactive
1: DIS active
Reset: X
Reset Condition: -

[20] **DIS_LATCH**: Shows if DIS was applied since last read out. Bit set to 1 by DIS input set HIGH
0: No DIS detected
1: DIS detected
Reset: X
Reset Condition: Read out POR

[19] **NDIS_STATE**: Shows if the device is currently disabled by the NDIS input signal
0: NDIS active
1: NDIS inactive
Reset: X
Reset Condition: -

[18] **NDIS_LATCH**: Shows if NDIS was applied since last read out. Bit set to 1 by NDIS input = LOW
0: No NDIS detected
1: NDIS detected
Reset: X
Reset Condition: Read out POR

[17] **NDIS_OUT_LATCH**: Shows NDIS was used as output and internally pulled down.
0: No internal NDIS activation
1: Internal NDIS activation
Reset: X
Reset Condition: Read out POR

[16] **CONFIG_CC_STATE**: Shows if communication check functionality is activated or deactivated
0: CC inactive
1: CC active
Reset: X
Reset Condition: Read out POR

[15] **CC_LATCH**: Shows if CC failed since last read out. Bit set to 1 if communication check failed
0: no CC failure detected
1: CC failure detected
Reset: X
Reset Condition: Read out POR

[14] **BIST_DONE**: BIST status

0: not done/ongoing

1: BIST finished

Reset: X

Reset Condition: POR, NRES

[13] **BIST_DIS**: BIST disable event latch

0: BIST passed

1: BIST failed

Reset: X

Reset Condition: POR, NRES

[12] **HWSC_DONE**: HWSC status

0: not done/ongoing

1: HWSC finished

Reset: X

Reset Condition: POR, NRES

[11] **HWSC_DIS**: HWSC disable event latch

0: HWSC passed

1: HWSC failed

Reset: X

Reset Condition: POR, NRES

[10] **OV_VDD5_STATE**: Current state of the VDD5 over voltage comparator output, no digital filter

0: currently no OV condition on VDD5

1: OV condition active on VDD5

Reset: 0

Reset Condition: -

[9] **OV_VDD5_LATCH**: Bit set to 1 if a VDD5 over voltage was detected by OV VDD5 comparator (even if OV filter not expired)

0: no VDD5 fast transient OV detected

1: fast VDD5 transient OV detected

Reset: 0

Reset Condition: Read out POR, NRES

[8] **UV_VDD5_STATE**: Current state of the VDD5 under voltage comparator output, no digital filter

0: currently no UV condition on VDD5

1: UV condition active on VDD5

Reset: 0

Reset Condition: -

[7] **UV_VDD5_LATCH**: Bit set to 1 if a VDD5 under voltage was detected by UV VDD5 comparator (even if UV filter not expired)

0: no fast VDD5 UV transient detected

1: fast VDD5 UV transient detected

Reset: 0

Reset Condition: Read out POR, NRES

[6] **N_POR_LATCH**: Shows if a POR_VDD5 on the int. 5V supply for channel occurred since last read out

0: No POR on VDD5 detected (state after readout)

Reset: X

Reset Condition: Cleared: Read out

1: POR on VDD5 detected (state after event)

Reset: X

Reset Condition: Set to default: POR

[5] **NRES_LATCH**: Shows if NRES was applied since last readout bit set to 1 by NRES input is LOW

0: No NRES detected

1: NRES detected

Reset: X

Reset Condition: Read out POR, NRES

[4] **VCP_UV_STATE**: Returns the output status of the VGBHI undervoltage comparator

0: VPS > VVPS_UV outputs enabled

1: VPS < VVPS_UV outputs disabled

Reset: 0

Reset Condition: -

[3] **VCP_UV_LATCH**: Returns if a VCP_UV was detected since last read out

0: No VCP_UV detected

1: VCP_UV detected

Reset: 0

Reset Condition: Read out POR, NRES

[2] **VPS_STATE**: Feedback of the voltage at the VPS pin: if VPS pin smaller VVPS_UV the external MOSFETs are disabled

0: VPS > VVPS_UV outputs enabled

1: VPS < VVPS_UV outputs disabled

Reset: 0

Reset Condition: -

[1] **VPS_LATCH**: Returns if a low VPS voltage was detected since last read out

0: No VPS low detected

1: VPS low detected

Reset: 0

Reset Condition: Read out POR, NRES

[0] **PARITY**: Parity bit, based on even parity calculation

0: If the number of 1 is odd

1: If the number of 1 is even

Reset: 0

Reset Condition: -

RESPONSE 11

Frame partitioning

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C				$R/\overline{W}$	FIXED_PATTERN						V4	V3	V2	V1	C4	C3	C2	C1	PUPD4			PUPD3			PUPD2			PUPD1			PARITY

Description: Channel 1-4 control signal integrity

Reset: 0xBABE0000

[31:28] **C**: Response to command 11

Reset: 1011

Reset Condition: -

[27] **$R/\overline{W}$**: Bit to read/write configuration

0: Write & request read

1: Request read only

Reset: 1

Reset Condition: POR, NRES

[26:21] **FIXED_PATTERN**: Fixed pattern

Reset: 010101

Reset Condition: POR, NRES

[20:17] **V4…1**: This bit monitors the external FET drain voltage by exploiting the internal diagnostic comparators. It is useful for obtaining the status of the output during normal operation

The value of this bit depends on the channel configuration:

0: Drain voltage low ($V_{DRAIN} < V_{LVT}$) -> transistor ON

1: Drain voltage high ($V_{DRAIN} > V_{LVT}$) -> transistor OFF

(Low-Side with NFET)

0: Drain voltage low ($V_{DRAIN} < V_{OL}$) -> transistor OFF

1: Drain voltage high ($V_{DRAIN} > V_{OL}$) -> transistor ON

(High-Side with NFET/PFET)

Reset: 1111

Reset Condition: POR, NRES

[16:13] **C4…1**: This bit combines the control signals SPI_ON_OUTxx, NONx and SPI_input_sel_xx to determine if the x-th channel is commanded ON or OFF

0: output commanded OFF

1: output commanded ON

Reset: 0000

Reset Condition: POR, NRES

[12:10]
[9:7]
[6:4]
[3-1]

PUPD4...1: Pull up / Pull down status of CHx

This field consists of 3 bit encoding the current status of the gate charge / discharge current sources for the x-th channel. The code depends on the output configuration:

High-Side with PFET:

- 100: I_{PD} ON and I_{PU} OFF -> transistor ON
- 010: I_{PD} OFF and I_{PU} ON -> transistor OFF
- 000: I_{PD} OFF and I_{PU} OFF -> output in three-state
- Others: integrity of the output control is compromised

High-Side/Low-Side with NFET:

- 010: I_{PD} ON and I_{PU} OFF -> transistor OFF
- 001: I_{PD} OFF and I_{PU} ON -> transistor ON
- 000: I_{PD} OFF and I_{PU} OFF -> output in three-state
- Others: integrity of the output control is compromised

Reset: 0000

Reset Condition: -

[0] **PARITY**: Parity bit, based on even parity calculation

0: If the number of 1 is odd

1: If the number of 1 is even

Reset: 0

Reset Condition: -

RESPONSE 12

Frame partitioning

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C				$R/\overline{W}$	FIXED_PATTERN						V8	V7	V6	V5	C8	C7	C6	C5	PUPD8			PUPD7			PUPD6			PUPD5			PARITY

Description:	Channel 5-8 control signal integrity
Reset	0xCABE0001

[31:28] **C**: Response to command 12

Reset: 1100

Reset Condition: -

[27] **$R/\overline{W}$**: Bit to read/write configuration

0: Write & request read

1: Request read only

Reset: 1

Reset Condition: POR, NRES

[26:21] **FIXED_PATTERN**: Fixed pattern

Reset: 010101

Reset Condition: POR, NRES

[20:17] **V8…5**: This bit monitors the external FET drain voltage by exploiting the internal diagnostic comparators. It is useful for obtaining the status of the output during normal operation

The value of this bit depends on the channel configuration:

0: Drain voltage low ($V_{DRAIN} < V_{LVT}$) -> transistor ON

1: Drain voltage high ($V_{DRAIN} > V_{LVT}$) -> transistor OFF

(Low-Side with NFET)

0: Drain voltage low ($V_{DRAIN} < V_{OL}$) -> transistor OFF

1: Drain voltage high ($V_{DRAIN} > V_{OL}$) -> transistor ON

(High-Side with NFET/PFET)

Reset: 1111

Reset Condition: POR, NRES

[16:13] **C8…5**: This bit combines the control signals SPI_ON_OUTxx, NONx and SPI_input_sel_xx to determine if the x-th channel is commanded ON or OFF

0: output commanded OFF

1: output commanded ON

Reset: 0000

Reset Condition: POR, NRES

[10:12] **PUPD8...5**: Pull up / Pull down status of CHx

[9:7]
[6:4]
[3-1]

This field consists of 3 bit encoding the current status of the gate charge / discharge current sources for the x-th channel. The code depends on the output configuration:

High-Side with PFET:

- 100: I_{PD} ON and I_{PU} OFF -> transistor ON
- 010: I_{PD} OFF and I_{PU} ON -> transistor OFF
- 000: I_{PD} OFF and I_{PU} OFF -> output in three-state
- Others: integrity of the output control is compromised

High-Side/Low-Side with NFET:

- 010: I_{PD} ON and I_{PU} OFF -> transistor OFF
- 001: I_{PD} OFF and I_{PU} ON -> transistor ON
- 000: I_{PD} OFF and I_{PU} OFF -> output in three-state
- Others: integrity of the output control is compromised

Reset: 0000

Reset Condition: POR, NRES

[0] **PARITY**: Parity bit, based on even parity calculation

0: If the number of 1 is odd

1: If the number of 1 is even

Reset: 0

Reset Condition: -

RESPONSE 13

Frame partitioning

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C				R/$\overline{\text{W}}$	FIXED_PATTERN			NDIS_PROT_LATCH	OT_STATE	SDO_OV_LATCH	TEMP_ADC										VPS_ADC										PARITY

Description Device status, battery and temperature monitor

Reset X

[31:28] **C**: Response to command 12

Reset: 1101

Reset Condition: -

[27] **R/$\overline{\text{W}}$**: Bit to read/write configuration

0: Write & request read

1: Request read only

Reset: 1

Reset Condition: POR, NRES

[26:24] **FIXED_PATTERN:** Fixed pattern

Reset: 010

Reset Condition: -

[23] **NDIS_PROT_LATCH**: Bit set to 1 if the protection on NDIS pin was activated while NDIS was being internally pulled down, reactivation with control change

0: no OV condition on NDIS

1: OV condition on NDIS detected

Reset: 0

Reset Condition: Read out POR

[22] **OT_STATE**: Current state of OT comparator output

0: no OV condition on SDO detected

1: OV condition on SDO detected

Reset: 0

Reset Condition: -

[21] **SDO_OV_LATCH**: Shows if an OV in SDO pin was detected since last read out

0: no OV condition on SDO detected

1: OV condition on SDO detected

Reset: 0

Reset Condition: Read out POR

[20:11] **TEMP_ADC**: Returns the actual temperature measured by the internal temperature sensor of the device. 10 bit to code for the actual temperature of the device

See Temperature ADC.

Reset: X

Reset Condition: POR, NRES

[10:1]	**VPS_ADC**: Returns the actual VPS voltage measured by the internal voltage sensor of the device. 10 bit to code for the actual VPS voltage See VPS ADC Reset: X Reset Condition: POR, NRES
[0]	**PARITY**: Parity bit, based on even parity calculation 0: If the number of 1 is odd 1: If the number of 1 is even Reset: X Reset Condition: -

6 Safety & diagnostics

This chapter contains all the information regarding safety and diagnostic features. All the external and internal disable sources are described. The Built-In Self-Test (BIST), HardWare Self-Check (HWSC) and the Communication Check (CC) watchdog are also explained. The diagnostics implemented for monitoring the output status and protecting the external FETs are described.

All the information regarding the effects of disable sources and diagnostics on the output pre-drivers is summarized in Summary of disable sources and faults.

6.1 Disable sources

There are several disable sources implemented in order to guarantee safety and correct functionality of the output pre-drivers.

6.1.1 DIS & NDIS pins

For safety purposes, the device features two disable pins that can be driven by an external microcontroller:

- **DIS:** is a positive asserted disable input with internal pull up. When DIS is asserted, all channels except 7 and 8 are actively turned off. DIS status can be monitored reading **DIS_STATE** bit via SPI. If DIS has been asserted, the event is latched in the **DIS_LATCH**, cleared on SPI readout. Outputs are automatically re-engaged when DIS is released.
- **NDIS**: is a negative asserted disable input/output with internal pull down. Refer to Figure 24. NDIS structure.
  - When used as **input**, a negative assertion implies an active shut off of all the outputs except channels 7 and 8. NDIS status can be monitored reading **NDIS_STATE** bit via SPI. If NDIS has been asserted, the event is latched in the **NDIS_LATCH**, cleared on SPI readout. Outputs are automatically re-engaged when NDIS is released.
  - This device uses this pin as **output** every time an over/under voltage is detected on VDD5 supply. The purpose is to provide a feedback on the VDD5 status to the external microcontroller. This functionality is enabled only if NRES is set high. If NDIS is internally pulled down, the event is latched in **NDIS_out_LATCH**, cleared on SPI readout.

In case of overvoltage (VDD5 > V_{VDD5_OV} for t > t_{VDD5_OV}) NDIS is pulled-down immediately.

In case of undervoltage (VDD5 < V_{VDD5_UV} for t > t_{VDD5_UV1}) NDIS is pulled-down after tVDD5_UV2.

Note: *For timings and electrical characteristics related to VDD5 refer to Table 8. VDD5 supply block electrical characteristics.*

When configured as H-Bridge, channels 7 and 8 are handled like other channels and are disabled in case of DIS/NDIS assetion.

When used as output, NDIS is protected against overvoltage. In case NDIS is internally activated low and the voltage at NDIS pin exceeds VNDIS_OV, for a time longer than tNDIS_OV + tNDIS_OV_react, the protection is activated by switching OFF the pull down structure on NDIS pin. Once the protection is activated it will stay active until the next NDIS internal activation event. NDIS overvoltage event is latched into **NDIS_PROT_LATCH**, cleared via SPI readout.

Figure 24. **NDIS structure**

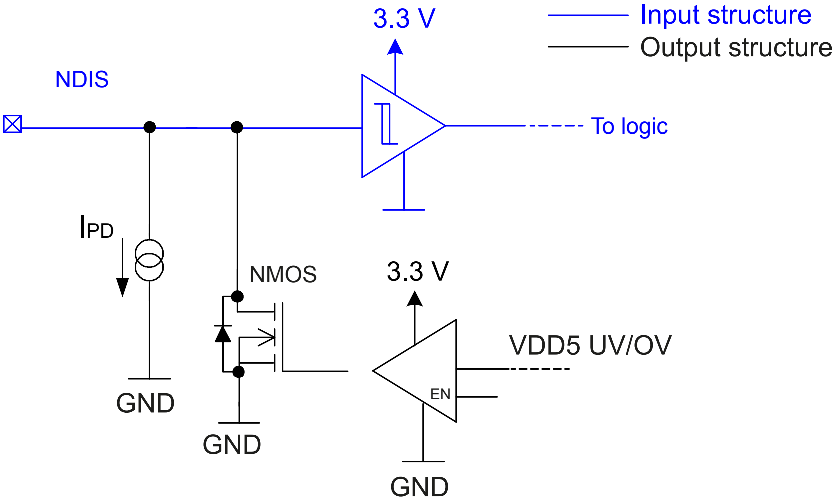


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Table 31. **NDIS OV protection electrical characteristics**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{NDIS_OV}	NDIS OV disable threshold	Low Side ON	0.8	-	1.0	V
t_{NDIS_OV}	NDIS OV deglitch filter time	-	2.2	2.5	2.7	µs
$t_{NDIS\_OV\_react}$	NDIS OV Comparator reaction time	-	100	-	700	ns

6.1.2 VDD5 Overvoltage/Undervoltage

VDD5 is internally monitored to detect overvoltage/undervoltage conditions:

- In case VDD5 ≥ V_{VDD5_OV}, an internal OV disable is generated after the filter time t_{VDD5_OV}. Such an event is latched in **OV_DIS_LATCH**, cleared on SPI readout. In case of overvoltage all outputs except channel 7 and 8 are actively turned off until the next SPI diagnostic readout. Overvoltage comparator status can be monitored reading **OV_VDD5_STATE** bit via SPI. If the comparator output goes high due to a transient overvoltage, the **OV_VDD5_LATCH** is set, even if the filter time tVDD5_OV hasn't expired. This latch is cleared on SPI readout and doesn't imply an output disable.
- In case V_{POR} ≤ VDD5 ≤ V_{VDD5_UV}, an internal UV disable is generated after the filter time t_{VDD5_UV1}. Such an event is latched in **UV_DIS_LATCH**, cleared on SPI readout. Once UV disable is activated it will stay active at least for tVDD5_UV1 after UV condition disappears. In case of undervoltage all outputs except channel 7 and 8 are actively turned off. If UV condition disappears, outputs are automatically re-engaged. Undervoltage comparator output can be monitored by reading **UV_DIS_STATE** via SPI.

In case VDD5 ≤ V_{POR} an internal POR is generated and the device is reset. Such an event is latched in **n_POR_LATCH** and can be cleared via SPI readout.

Note: *Refer to Table 8. VDD5 supply block electrical characteristics for the electrical characteristics and the parameters regarding VDD5 overvoltage and undervoltage detection.*

When configured as H-Bridge, channels 7 and 8 are handled like other channels and are disabled in case of VDD5 UV/OV.

6.1.3 BIST & HWSC

The device features a Built-In Self-Test (BIST) and a HardWare Self-Check (HWSC).

For functional safety considerations, internal disable structures must operate always correctly and reliably. To accomplish this, the disable sources paths and the VDD5 overvoltage detection block are self-checked by the device:

- BIST covers the digital domain of disable-related functions;
- HWSC covers the analog domain of the VDD5 overvoltage comparator.

In case of BIST or HWSC failure, all channels except 7 and 8 are disabled. BIST is always followed by HWSC to ensure full coverage of digital and analog domains. The sequence is performed in less than 3 ms, and is run:

- After each NRES release (POR assertion does not imply BIST & HWSC sequence execution);
- On demand, programming the **BIST_RQ** bit via SPI.

Note: Due to device configuration reset during BIST, the procedure must be executed prior to channel configuration applied.

The procedure starts with BIST. During BIST execution:

- The **BIST_DONE** latch is set low;
- All output drivers (including 7 and 8) are three-stated;
- All the device registers are reset, except SPI latches (UV/OV events, disable events, etc.).

BIST checks the correct function of the disable logic to the gate drive of the outputs:

- Switch OFF paths from DIS, NDIS, EN6, including the bidirectional NDIS output;
- Switch OFF path from Communication Check;
- Switch OFF path from HWSC/BIST;
- Switch OFF path from OV/UV detection block.

BIST also checks that the implemented timers can be stopped (e.g. communication check timeout).

The BIST_DONE latch is set high once BIST has terminated.

- In case the procedure detects an error, the **BIST_DIS** latch is set and all outputs, except 7 and 8, are kept actively turned off. Channels 7 and 8 are kept in three-state.
- In case BIST detected no error, the outputs are kept in three-state

HWSC follows BIST and checks the functionality of VDD5 overvoltage detection mechanism. HWSC lasts t_{HWSC_DUR}. During such interval, the outputs 1-6 are kept OFF actively by asserting the **HWSC_DIS** internal signal; channels 7-8 are still in three-state, since the BIST executed previously. After t_{HWSC_DUR} has expired, the **HWSC_DONE** latch is set high and the self check result will be available via SPI reading the HWSC_DIS signal status. Two cases can occur:

- HWSC failed: the signal HWSC_DIS is kept high and disables (actively) all the outputs except 7 and 8;
- HWSC passed: the signal HWSC_DIS is set low and the disable is released.

If both BIST and HWSC are successful, BIST_DIS and HWSC_DIS disable signals are released and the outputs can be configured and enabled normally. If one among BIST and HWSC failed, channels 1-6 are kept disabled, regardless of the configuration applied; channels 7-8 can still be enabled.

BIST and HWSC sequence is stopped in case of a reset condition:

- NRES set low;
- POR.

Note: When configured as H-Bridge, channels 7 and 8 are handled like other channels and are disabled in case of BIST/HWSC failure.

Figure 25. **BIST & HWSC sequence**

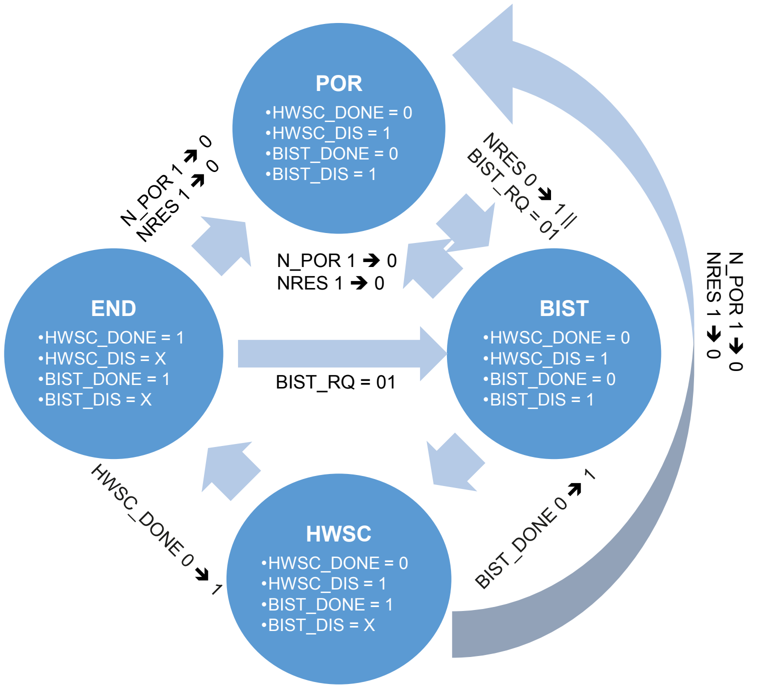

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Table 32. **HWSC timing characteristics**

Symbol	Parameter	Min.	Max.	Unit
t_{HWSC_DUR}	HWSC duration time	100	160	µs

6.1.4 VPS undervoltage

In case **VPS** is lower than V_{VPS_UV} for $t_{VPS\_react} + t_{LBD\_FIL}$, a battery undervoltage is detected, all outputs are actively turned off and the **VPS_LATCH** is set high (cleared on SPI readout). The undervoltage comparator output can be monitored by reading **VPS_STATE** bit via SPI. Outputs are re-engaged when undervoltage condition disappears.

Table 33. **VPS UV detection electrical characteristics**

Symbol	Parameter	Min.	Max.	Unit
V_{VPS_UV}	VPS low battery detection threshold	3.5	3.8	V
t_{VPS_react}	VPS Comparator output reaction time for L->H and H->L transition	100	700	ns
t_{LBD_FIL}	Filter time for VPS low battery detection	0.5	5	µs

6.1.5 Charge pump undervoltage

In case **VGBHI** is lower than V_{CP_UV} for t_{CP_UV}, a charge pump undervoltage is detected, all outputs are actively turned off and the **VCP_UV_LATCH** is set high (cleared on SPI readout). The undervoltage comparator output can be monitored by reading **VCP_UV_STATE** bit via SPI. Outputs are re-engaged when undervoltage condition disappears.

Table 34. **Charge pump undervoltage detection electrical characteristics**

Symbol	Parameter	Test condition	Min.	Max.	Unit
V_{CP_UV}	Under voltage threshold	Referenced to VVPS	VVPS + 3.9	VVPS + 5.1	V

Symbol	Parameter	Test condition	Min.	Max.	Unit
Vh_{CP_UV}	Under voltage hysteresis	Referenced to VVPS	250	-	mV
t_{CP_UV}	Digital filter of UV shutdown	-	10	30	µs

6.1.6 SPI enable bit

Each channel can be enabled/disabled independently by programming the **en_OUT_xx** SPI bit. If such bit is set low, the corresponding channel is three-stated. By default, all channels are three-stated and must be enabled setting en_OUT_xx high after having properly configured them in the same SPI register. Output control signal is ignored as long as en_OUT_xx is low.

6.1.7 Protection disable bit

The device offers additional SPI bit for disabling channels via SPI: **prot_disable_xx**. Although such bit can disable each channel separately, the main purpose of prot_disable_xx is to allow a fast disabling of all channels through a single SPI frame. In fact, all prot_disable_xx bit are part of the same SPI command. In case prot_disable_xx is set high, the corresponding channel is actively turned off. Output control signal is ignored as long as prot_disable_xx is low.

6.1.8 EN6 input

Channel 6 is designed for being used in safety relevant applications. For such reason, an additional enable input, EN6, has been provided. If EN6 is set low, channel 6 is actively turned off and the **EN6_LATCH** is set high (cleared on SPI readout). Channel 6 control signal is ignored as long as EN6 is low.

6.1.9 NRES assertion

In case of NRES assertion, all outputs are actively turned off and the **NRES_LATCH** is set (cleared on SPI readout). Since channel configuration is reset, output re-engagement must be executed manually.

6.1.10 Communication Check (CC)

Communication Check (CC) starts to work as soon as the disable inputs NDIS/DIS are released. With this condition the CC timer is started. Depending on the status of NDIS/DIS at the release of NRES, two possible scenarios can occur:

- NDIS/DIS are released after NRES release, once the external microcontroller power-up routine is completed. In this case, CC starts with t_{CC} time frame (see Figure 26. NDIS/DIS release after NRES release: t_{CC} is selected as watchdog starting timer value)
- NDIS/DIS are released before NRES release. In this case, once NRES is deasserted, CC starts with t_{CC_INIT} time frame, in order to allow the external microcontroller completing the power-up routine. Then, it switches to t_{CC} (see Figure 27. NDIS/DIS release before NRES release: t_{CC} is selected as watchdog starting timer value. Then, CC timer switches to t_{CC}.)

Figure 26. **NDIS/DIS release after NRES release: t_{CC} is selected as watchdog starting timer value**

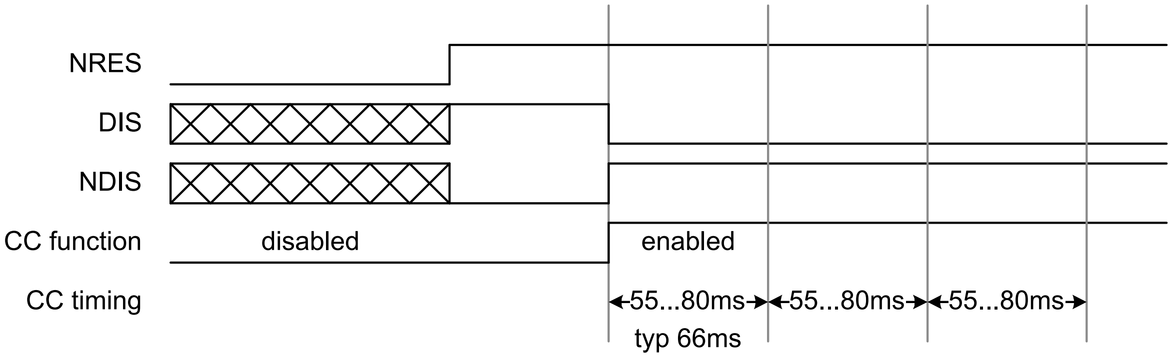

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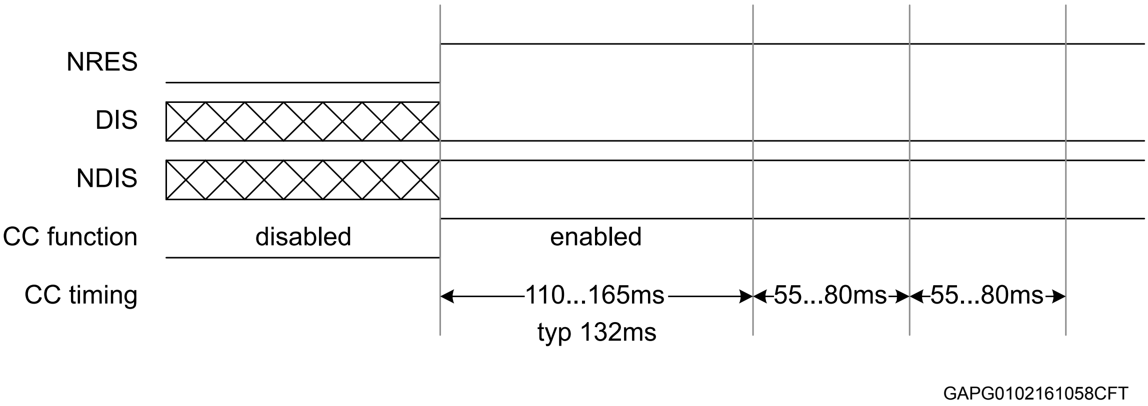
Figure 27. **NDIS/DIS release before NRES release: t_{CC} is selected as watchdog starting timer value. Then, CC timer switches to t_{CC}.**



The distinction between t_{CC} and t_{CC_INIT} applies only at the beginning of CC. After the first valid SPI frame, CC always operates with t_{CC} deadline.

In case of no valid communication the CC timer will expire and disable all related outputs. With the next valid communication the outputs are enabled. Each correct communication restarts the CC timer. If a CC failure is detected, all channels except 7 and 8 are actively turned off and the **CC_LATCH** is set high (cleared on SPI readout).

The CC can be deactivated by programming the **CONFIG_CC** field via SPI. By default CC is active. CC status can be monitored by reading the **config_CC_STATE** SPI bit.

Note: When configured as H-Bridge, channels 7 and 8 are handled like other channels and are disabled in case of CC failure.

Table 35. **CC timings**

Symbol	Parameter	Min.	Max.	Unit
t_{CC}	Communication Timeout	55	85	ms
t_{CC_INIT}	Deadline for the first communication engagement in case DIS/NDIS are released before NRES release.	110	165	ms

6.2 Diagnostics overview

The device performs two types of diagnostics for each output channel:

- ON state diagnostics: overcurrent (OC) detection;
- OFF state diagnostics: open load (OL), short to ground (STG), and short to battery (STB) detection.

Diagnostic can be enabled/disabled by programming the **ENABLE_DIAGNOSTIC** bit.

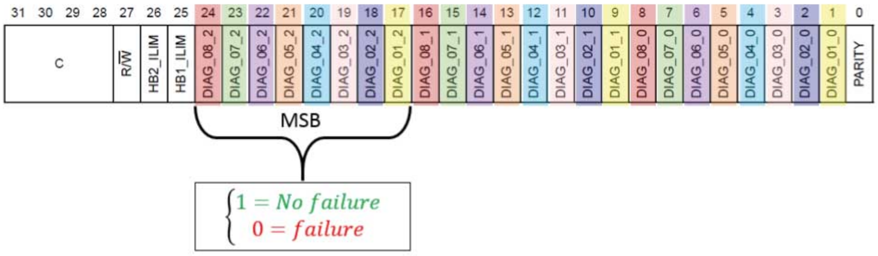
Diagnostic report for all channels is readable via SPI, after having issued the **0x9AAA0001** frame. The diagnostic status of each channel is encoded in 3 bit (**diag_xx**[2-0]), as shown in the table below.

Table 36. **Diagnostic codes**

Channel Status	diag_xx[2-0]	Priority
OC pin failure (see note below)	000	1
OC failure	001	2
STG/STB failure	010	3
OL failure	011	4
No failure	100	5
No OC failure	101	6
No OL/STG/STB failure	110	7
No diagnostic done	111	8

Note: *The OC pin failure, corresponding to the code "000" is available only for channels operating in Peak & Hold. This code is unused in other configurations. Refer to Section 5.6.2: Peak & Hold diagnostics in order to understand how this diagnostic is performed.*

Figure 28. **Diagnostic codes quick look**



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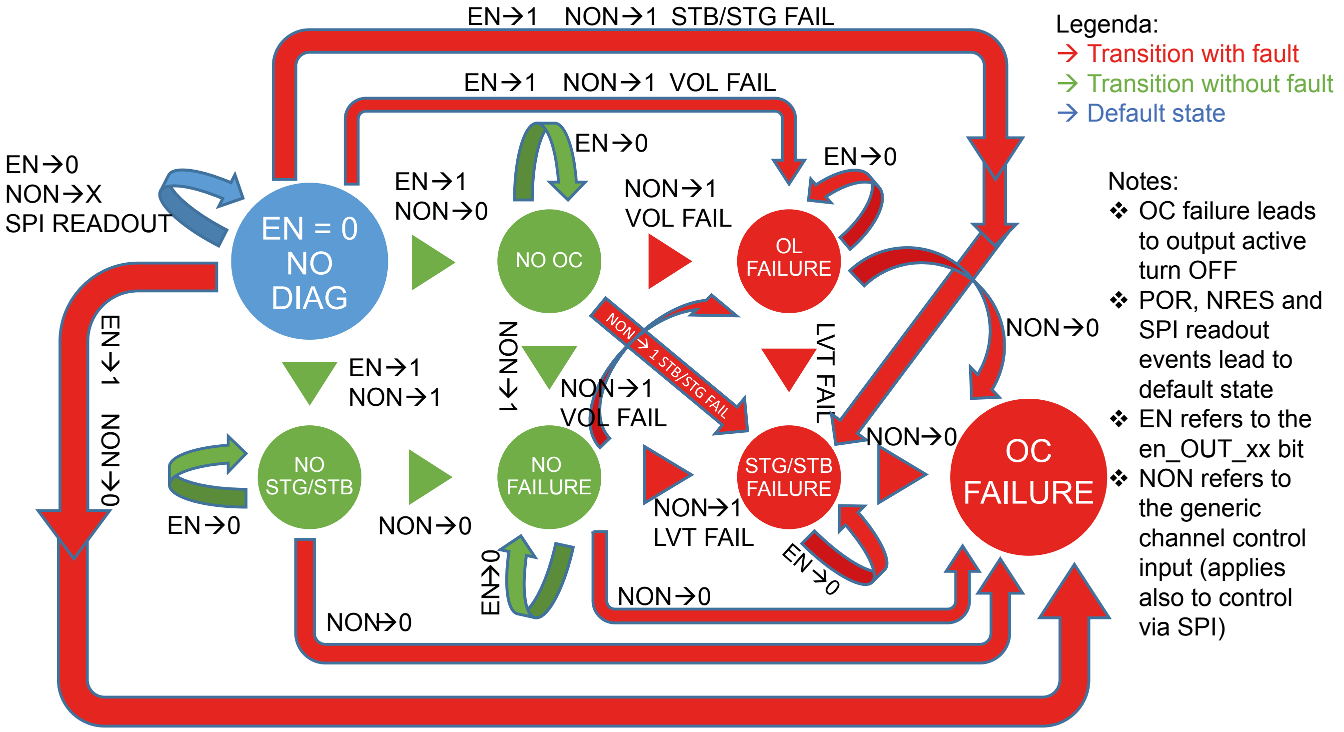
For an immediate fault detection, the MSB of the diagnostic code can be evaluated, as shown in Figure 28. Diagnostic codes quick look. An MSB equal to zero indicates that a failure occurred.

By default, all channels will report the "No diagnostic done" message. Such message is also reported in case diagnostic has been disabled. The diagnostic status follows a priority concept: if more than one event occurs on a channel, only the one with the highest priority will be encoded in the diag_xx[2-0] bit. Priority codes are related to the severity of the fault. OC failures have the highest priority.

The diagnostic latches are reset in case of SPI readout, POR or NRES. After a reset event, diagnostic filters are reset to prevent false detection.

Figure 29. FSM describing diagnostic priority shows an equivalent Finite State Machine (FSM) that helps understanding diagnostic priority.

Figure 29. **FSM describing diagnostic priority**



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Note: *In case a diagnostic event occurs during SPI readout, such event is latched and provided with the next diagnostic request.*

6.3 ON state diagnostics

The following diagnostic codes can be set during the output ON state:

- The diagnostic code corresponding to normal operation while in ON state is "No OC failure" (101);
- The "No failure" (100) code will be reported only once, after an OFF->ON transition, assuming that "No OL/STG/STB failure" latch was set while in OFF state and "No OC failure" is detected;
- The "OC failure" (001) or "OC pin failure" (000) codes will be reported in case of overcurrent detection.

This device protects the external FET against overcurrent (OC) during the ON phase. The device features an analog comparator with a programmable overcurrent threshold. Sensing is performed measuring the voltage drop on an external element and comparing it to the programmed threshold. Such threshold can be compensated against battery and temperature variations for specific applications.

6.3.1 Behavior in case of OC detection

If an OC event is detected, the output is actively shut off and the "OC failure" message is encoded in the diag_xx[2-0] bit. To prevent FET damage, in case the normal operation gate charge/discharge currents are low (1 mA or 5 mA), the device selects a higher shut off current among the ones available through **GCC_config_xx**. By programming the **GCC_override_config**, it is possible to select the entity of current increase in case of OC, as shown in the table below. These settings are in common between all channels.

Table 37. **Selection of fast shutdown currents in case of OC detection**

GCC_override_config	I_{PU} or I_{PD} [mA]
0	1 → 5 5 → 20

GCC_override_config	I_{PU} or I_{PD} [mA]
1	1 → 20 5 → 20

Note: I_{PU} is used to shut down PMOS, while IPD shuts down NMOS.

The GCC override configuration is applied as soon as an OC event is detected. The original GCC configuration is restored once diagnostics have been read.

6.3.2 Output re-engagement strategy after an OC event

After an OC event, the affected output must be manually re-engaged. There are two reactivation strategies, configurable via SPI bit **prot_config_xx**:

- Output re-engagement with control signal switching event (default);
- Output re-engagement after diagnostic readout and control signal switching event.

In case of H-Bridge configuration, the prot_config_xx has no effect. Re-engagement is always performed after diagnostic readout.

Note: Control signal can be either NONx or SPI_ON_OUTxx, depending on SPI_INPUT_SEL_xx bit

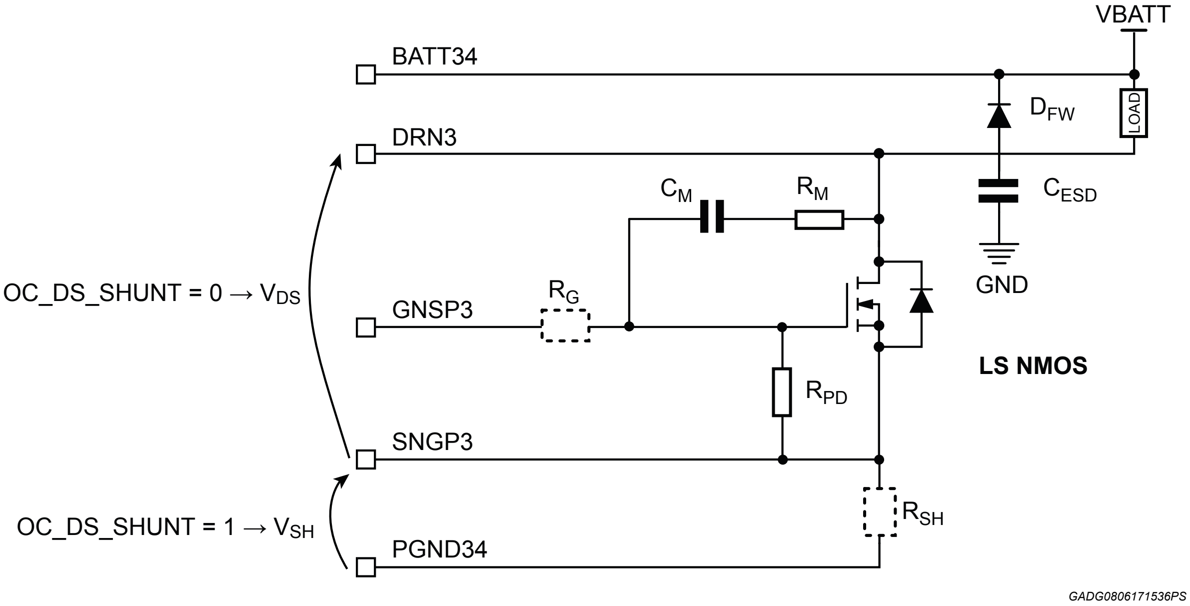
6.3.3 OC sensing strategy

OC detection is performed by sensing the voltage either on an external shunt resistor or between the drain and the source of the external FET. Detection strategy can be selected on each channel independently by programming the **OC_DS_Shunt_xx** bit as follows:

Table 38. **OC sensing strategy**

OC_DS_Shunt_xx	OC sensing strategy
0	Drain To Source Measurement (DSM)
1	Shunt Measurement

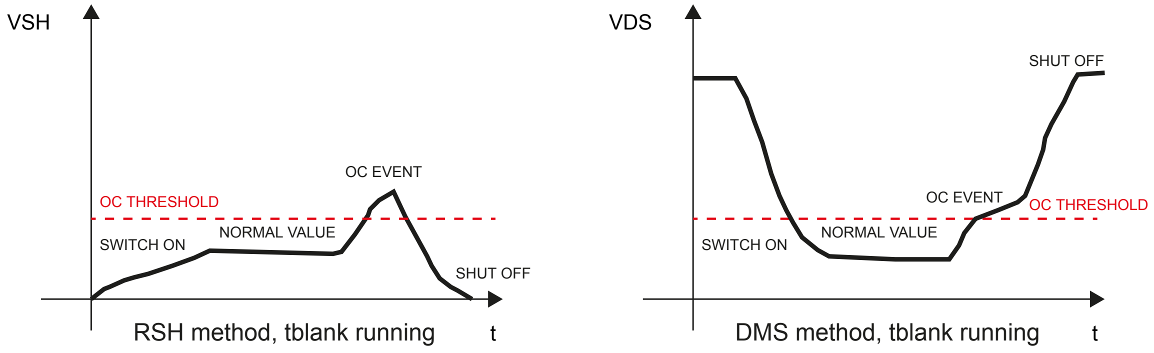
Figure 30. **Overcurrent sensing method (example on a LS NMOS)**



The following behaviors correspond to the different sensing methods (refer to Figure 31. Rshunt and DSM method diagram):

- In case Rshunt is selected, the V_{sense} behavior during the OFF==>ON transition corresponds to an ascending transient. In case the FET current crosses the OC threshold with a positive slope, t_{BLANK_OC} is stopped and t_{OC} is started. The OC detection will be mainly based on t_{FIL_ON} and t_{OC} parameters. The former is a deglitch filter to avoid small overshoots on the shunt resistor due to inductive effects, while the latter represents the actual OC blanking time. An OC event lasting $t_{FIL\_ON}+t_{OC}$ will be detected and the output switched OFF: the programmed t_{BLANK_OC} will have no effect on the OC reaction time. Only in case Peak & Hold configuration is selected and the OC event occurs while t_{BLANK_OC} is still running, an **'OC pin failure' (000)** will be reported instead of simple 'OC failure' (001). However, reaction time won't be affected.
- In case DSM is selected, the V_{sense} behavior during the OFF==>ON transition corresponds to a falling transient. Once t_{BLANK_OC} has expired, the VDS will be compared to the OC threshold and, if greater, the output will be shut OFF. Hence, t_{BLANK_OC} must be sized to allow VDS settling. In order to ensure maximum FET protection against critical OC events during blanking time, an OC threshold crossing with a positive slope will stop the tblank_oc and engage the t_{OC} filter.

Figure 31. **Rshunt and DSM method diagram**



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6.3.4 OC threshold selection

The voltage corresponding to the OC threshold can be selected independently for each channel programming the **OC_config_xx** bit. Such threshold is highly flexible: it is encoded on 6 bits (64 available values) and falls in the [50 - 1000] mV range.

Table 39. **Overcurrent threshold selection electrical parameters**

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OC_RANGE}	Range	50	-	1000	mV
OC_RES	Resolution	-	6	-	Bit
$t_{SETTLING}$	Threshold settling Time	5	-	18	µs

Refer to Table 40. OC threshold selection for the encoding tables for LS and HS configurations. Overcurrent threshold must be programmed according to the Eq. (3):

Eq. (3): Overcurrent threshold

$$V_{OC} = R_{OC} \times I_{OC} \tag{3}$$

where V_{OC} is the value programmed in the **OC_config_xx** bit, IOC is the maximum current for the given application and R_{OC} can be either R_{SH} (shunt resistor) or R_{DSon} (DSM).

Note: For H-Bridge configuration, refer to Overcurrent detection strategies for H-Bridge and Current limitation for H-Bridge to understand how OC thresholds can be programmed and exploited also for current limitation feature.

Table 40. **OC threshold selection**

OC_config_xx[5-0]	LS		HS		Unit
	Min.	Max.	Min.	Max.	
0	53	67	53	69	mV
1	68	82	68	85	mV
2	83	97	83	101	mV
3	97	113	99	117	mV
4	113	128	113	133	mV
5	128	143	129	150	mV
6	142	158	144	166	mV
7	157	173	159	182	mV
8	172	188	172	198	mV
9	186	204	189	214	mV
10	201	220	204	231	mV
11	216	235	219	247	mV
12	231	250	234	263	mV
13	246	266	248	279	mV
14	261	281	264	295	mV
15	275	296	278	311	mV
16	290	311	290	326	mV
17	305	327	305	341	mV
18	320	343	320	356	mV
19	334	358	338	375	mV
20	349	374	351	391	mV
21	364	389	367	407	mV
22	379	405	382	423	mV
23	393	420	397	439	mV
24	408	436	412	455	mV
25	423	451	427	471	mV
26	438	467	442	488	mV
27	453	482	456	504	mV
28	467	498	472	520	mV
29	482	513	486	536	mV
30	497	529	501	552	mV
31	512	544	515	568	mV
32	526	559	525	579	mV
33	541	575	545	595	mV
34	556	590	560	612	mV
35	570	606	575	628	mV
36	585	621	590	644	mV
37	600	637	604	660	mV
38	614	653	619	676	mV

OC_config_xx[5-0]	LS		HS		Unit
	Min.	Max.	Min.	Max.	
39	629	668	634	693	mV
40	644	684	649	708	mV
41	658	699	663	724	mV
42	673	715	679	740	mV
43	688	730	693	756	mV
44	702	746	708	772	mV
45	717	761	723	788	mV
46	732	777	738	804	mV
47	746	792	753	821	mV
48	761	808	767	836	mV
49	776	823	782	852	mV
50	791	839	797	868	mV
51	806	854	812	885	mV
52	820	870	827	900	mV
53	835	885	842	916	mV
54	849	900	856	933	mV
55	864	916	871	949	mV
56	878	931	886	964	mV
57	893	947	900	981	mV
58	908	962	916	997	mV
59	922	977	930	1013	mV
60	937	992	946	1029	mV
61	951	1008	960	1045	mV
62	967	1023	975	1061	mV
63	982	1038	987	1078	mV

6.3.5 OC detection timings

ON state diagnostics timings are listed in the following table.

Table 41. **OC detection timings**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{BLANK_OC}	OC blanking filter: It doesn't mask the OC failure. It only determines the assertion of the "No OC failure" diagnostic code.	tblank_oc = 000	10	11.1	12.2	µs
		tblank_oc = 001	14	15.6	17.1	µs
		tblank_oc = 010	18	20	22	µs
		tblank_oc = 011	28	31.1	34.2	µs
		tblank_oc = 100	39	42.2	46.5	µs
		tblank_oc = 101	48	53.3	58.7	µs
		tblank_oc = 110	88	97.8	107.6	µs
		tblank_oc = 111	128	142.2	156.5	µs
t_{FIL_ON}	OC deglitch filter time	-	0.6	-	1	µs

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{OC}	OC Detection filter time	-	2	-	3	µs

6.3.6 Temperature compensation for OC threshold

The device offers the possibility to compensate the OC threshold against temperature variations. Such feature can be enabled independently on each channel.

The device is able to monitor the internal junction temperature T_j through on board Table 6. Temperature ADC electrical characteristics. Given the estimated temperature variation between the device junction and the external FET junction.

Eq. (4): Estimated temperature variation for the compensation algorithm

$$\Delta T = T_{jFET} - T_j \tag{4}$$

An internal algorithm measures T_j and is able to compensate V_{OC} against RDSon variations induced by T_{jFET}. The latter can be estimated according to the given application and operating scenario.

Temperature compensation can be enabled by programming the **OC_Temp_comp_xx** bit according to the following table:

Table 42. **Temperature compensation**

OC_Temp_comp_xx	Function
00	Temperature compensation deactivated
01	Temperature compensation active for estimated ΔT < 60 °C. TCF is saturated at '1' for $T_j \geq T_{j\_SAT}$ = 83 °C.
10	Temperature compensation active for estimated ΔT < 40 °C. TCF is saturated at '1' for $T_j \geq T_{j\_SAT}$ = 96 °C.
11	Temperature compensation active for estimated ΔT < 25 °C. TCF is saturated at '1' for $T_j \geq T_{j\_SAT}$ = 108 °C.

In case temperature compensation is enabled, the overcurrent threshold must be programmed according to Eq. (3), where R_{OC} is the RDSon of the external FET evaluated for T_{jFET} = 150 °C.

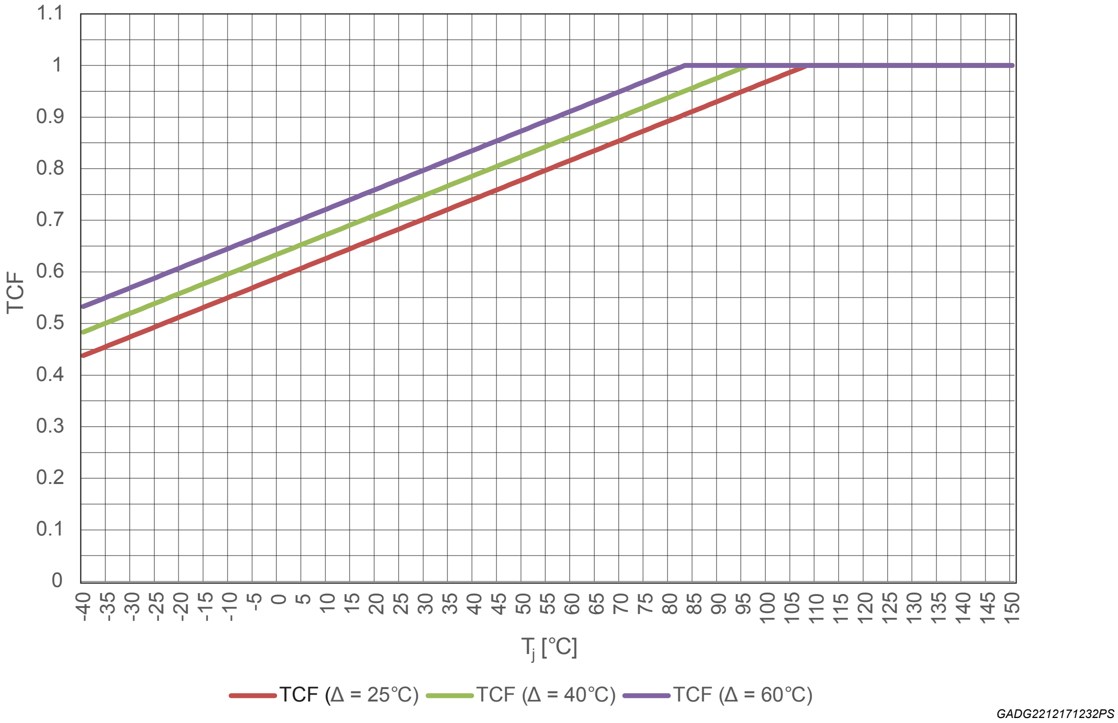
The internal algorithm compensates the OC threshold based on a multiplicative factor:

Eq. (5): Temperature Compensation Factor (TCF)

$$V_{OC\_comp} = TCF \times V_{OC} \tag{5}$$

TCF = 1 when $T_j \geq T_{j\_SAT}$, and it's decremented with a constant slope of 0.38 %/°C for $T_j < T_{j\_SAT}$.

Figure 32. **TCF vs. T_j**



Note: This feature is recommended only in case of DSM, because the compensation algorithm is based on RDSon variations. The external FET must have a characteristic RDSon vs. T_{jFET} that matches the 0.38 %/°C slope. In case of shunt measurement, the algorithm may show performances worse than the uncompensated strategy.

6.3.7 Battery compensation for OC threshold

The device offers the possibility to compensate the OC threshold against battery variations. This feature can be enabled when driving a resistive output load R_L, and helps preventing the load resistance from dropping below a minimum threshold R_{Lmin}. Given Eq. (3), the I_{OC} can be evaluated as the current flowing when the battery is at its maximum operating value (18 V for passenger vehicles or 36 V for commercial vehicles) and the load resistance assumes its minimum allowed value R_{Lmin}:

Eq. (6): Overcurrent detection in case of resistive load

$$I_{OC} \cong \frac{V_{BATT\max}}{R_{L\min}} \rightarrow V_{OC} = R_{OC} \times \frac{V_{BATT\max}}{R_{L\min}} \tag{6}$$

Eq. (6) assumes that $R_L >> R_{OC}$. The sensing resistance ROC can be either the shunt resistor or the R_{DSon}. Referring to Figure 34. OC detection through DSM or shunt measurement in Low side configuration and Figure 35. OC detection through DSM or shunt measurement in high side configuration with PMOS, the device measures:

Eq. (7): Overcurrent sensing in case of resistive load

$$V_{SENSE} = R_{OC} \times I_{LOAD} = R_{OC} \times \frac{V_{BATT}}{R_L} \tag{7}$$

The device is able to monitor the battery voltage on the VPS pin through the on board **VPS** ADC. This information can be used to compensate the VOC with respect to V_{BATT} variations. Therefore, the OC detection occurs only when $V_{SENSE} = V_{OC}$ due to a R_L variation.

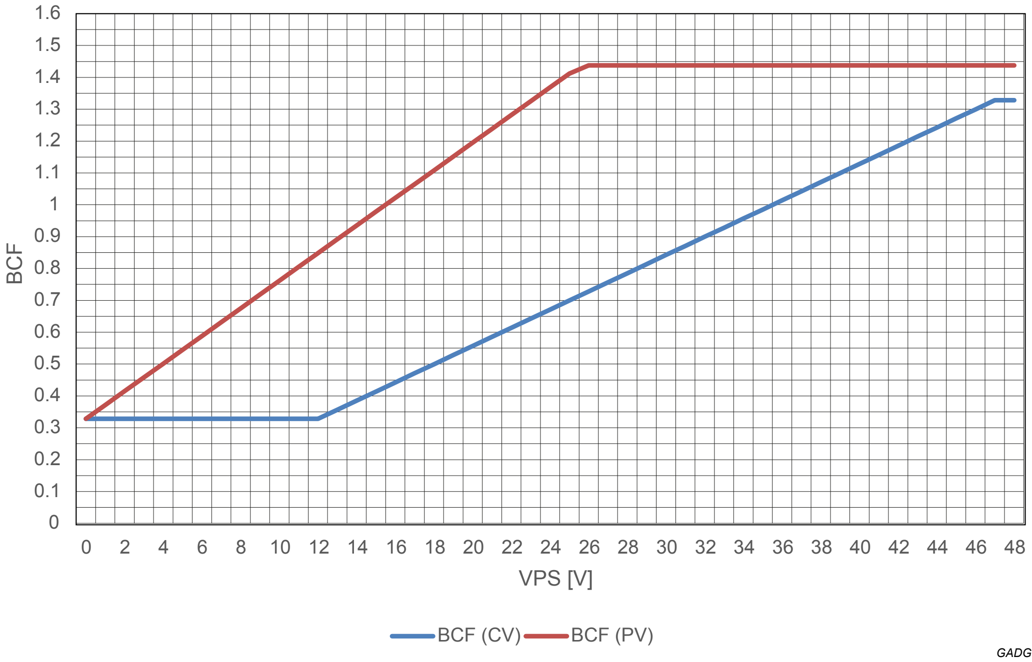
The internal algorithm compensates the OC threshold based on a multiplicative factor:

Eq. (8): Battery Compensation Factor (BCF)

$$V_{OCcomp} = BCF \times V_{OC} \tag{8}$$

The battery compensation feature can be activated independently on each channel by programming the **OC_Batt_comp_xx** bit. Two different BCF have been implemented for Passenger Vehicle (PV) and Commercial Vehicle (CV) applications. The BCF can be selected by programming the **Batt_fact_config** bit (refer to Figure 33. BCF vs.VPS).

Figure 33. BCF vs.VPS



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Note: *Because the algorithm is based on the assumption made for Eq. (6), the battery compensation feature is recommended only in case of resistive load. Usage either in case of different load types or in case of small resistive loads may lead to performances worse than the uncompensated strategy.*

6.3.8 Reading the compensated OC threshold

In general, the overcurrent threshold can be evaluated as follows:

Eq. (9): Overcurrent threshold compensation formula

$$V_{OCcomp} = BCF \times TCF \times V_{OC} \tag{9}$$

Where V_{OC} is the value programmed in the **OC_config_xx** bit, BCF is the battery compensation factor and TCF is the temperature compensation factor. When a compensation feature is disabled, its compensation factor is set to 1 (no effect on V_{OC}).

Note: *It is recommended to enable battery and temperature compensation simultaneously only in case of resistive load with DSM. Different usage may lead to performances worse than the uncompensated strategy.*

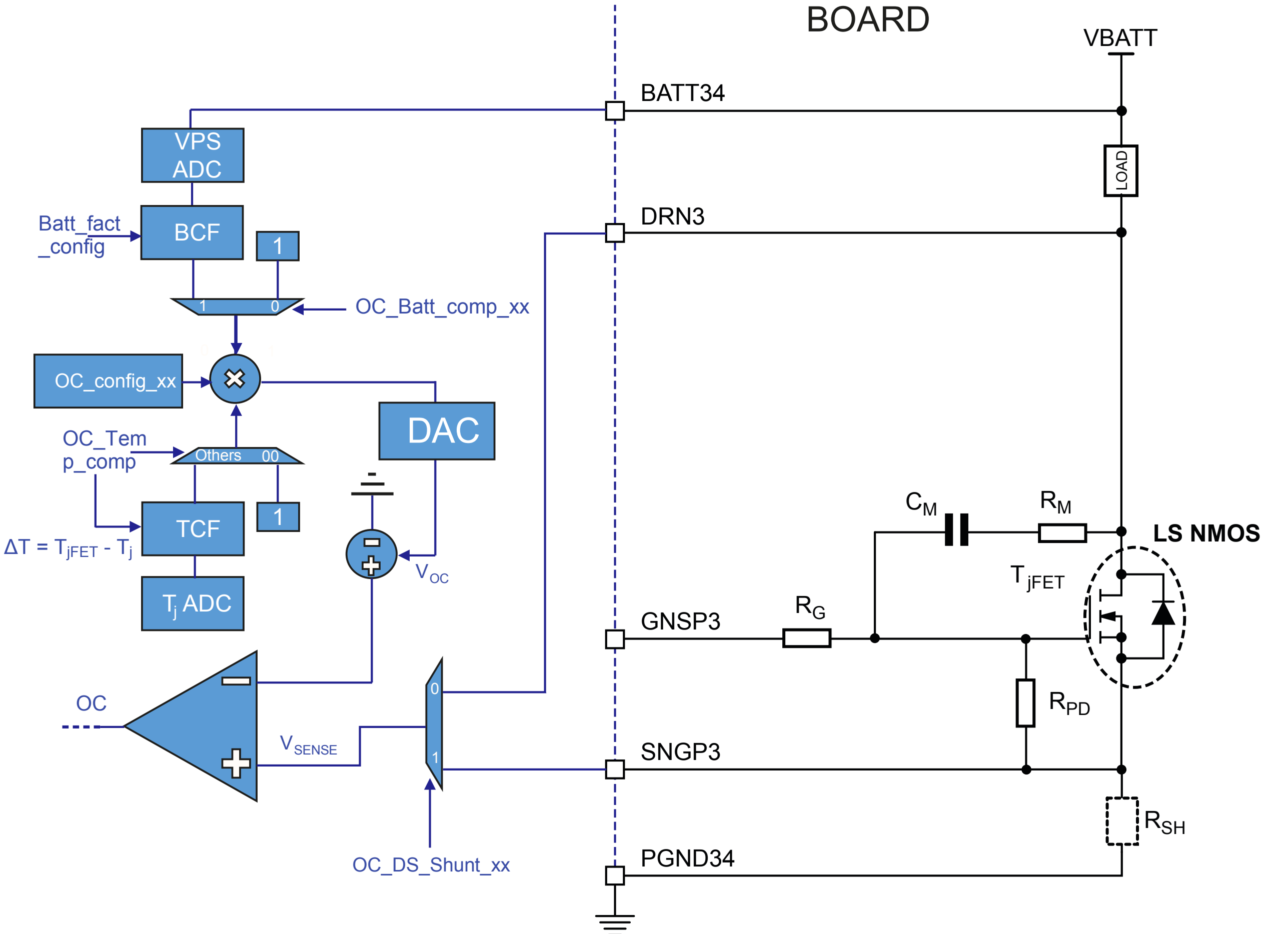
When configuring the device, the **OC_read_xx** can be used to select whether reading the programmed threshold VOC or the compensated one V_{OCcomp}.

6.3.9 OC detection schematics

Figure 34. OC detection through DSM or shunt measurement in Low side configuration shows the OC detection implementation in case of LS configuration. It can also be applied to the HS scenario with NFET (see description). In case DSM is selected RSH must not be mounted and the pins SNGPx and PGNDxx must be shorted.

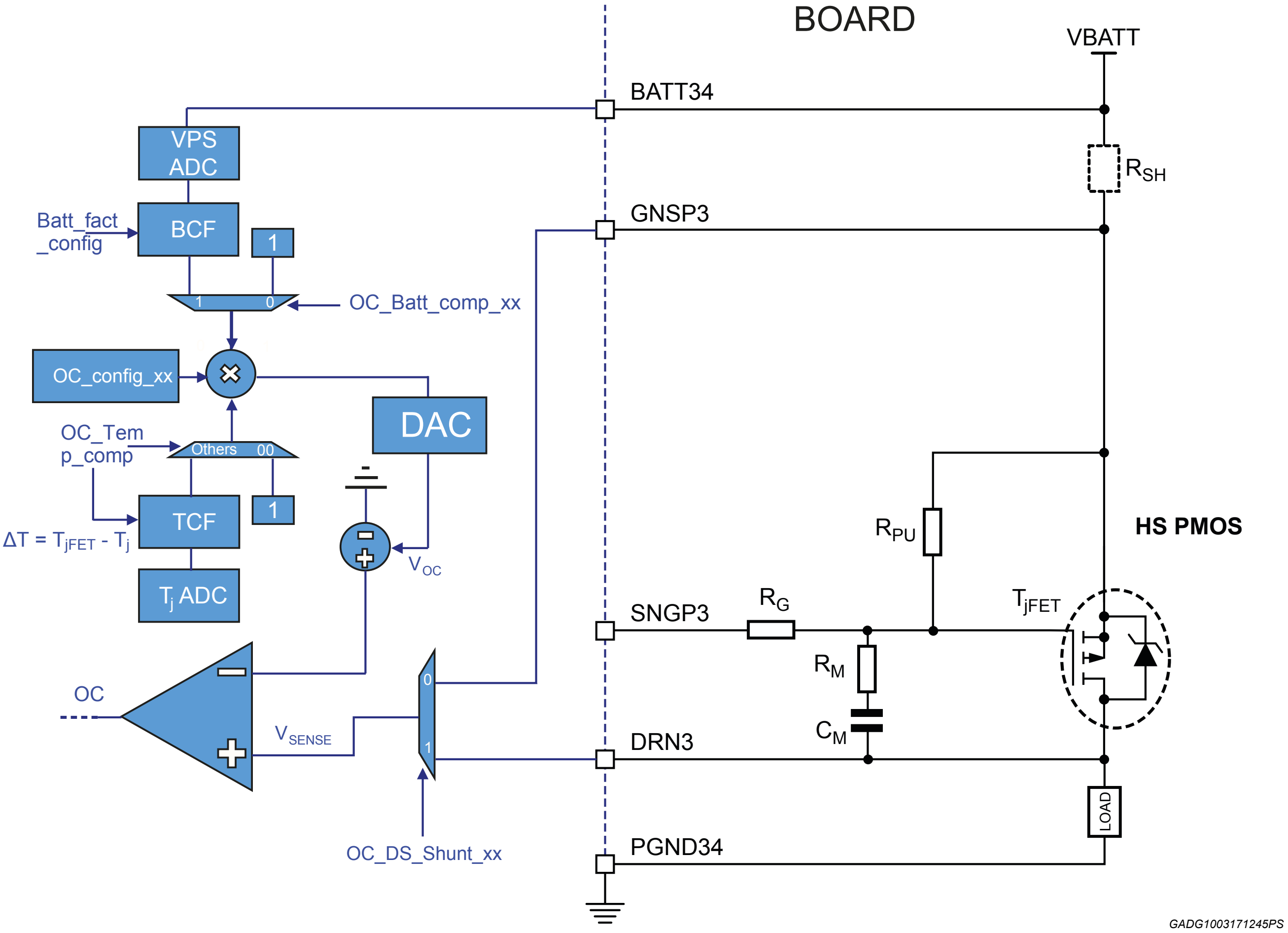
Figure 35. OC detection through DSM or shunt measurement in high side configuration with PMOS shows the OC detection implementation in case of HS configuration with PMOS. In case DSM is selected RSH must not be mounted and the pins GNSPx and BATTxx must be shorted.

Figure 34. **OC detection through DSM or shunt measurement in Low side configuration**



Note: *V_{OC} compensation against temperature and battery variations is shown in Figure 34. OC detection through DSM or shunt measurement in Low side configuration. In case of high side configuration with NMOS, RSH and the LOAD must be swapped, and the OC_DS_Shunt_xx signal is negated.*

Figure 35. **OC detection through DSM or shunt measurement in high side configuration with PMOS**



Note: *V_{OC} compensation against temperature and battery variations is shown in Figure 35. OC detection through DSM or shunt measurement in high side configuration with PMOS.*

6.4 OFF state diagnostics

The following diagnostic codes can be set to the output OFF state:

- The diagnostic code corresponding to normal operation while in OFF state is "No OL/STG/STB failure" (110);
- The "No failure" (100) code will be reported only once, after an ON->OFF transition, assuming that the "No OC failure" latch was set while in ON state;
- The "OL failure" (011) or "STG/STB failure" (010) codes are reported respectively in case of open load and short to ground/battery failures.

Short To Battery (**STB**), Open Load (**OL**) and Short To Ground (**STG**) are part of the OFF state diagnostics. This device measures the voltage on the output node V_{out} to determine if the output is shorted to battery/ground (respectively for HS/LS configurations) or if the output node is floating (open load). Depending on channel configuration, different faults can be detected:

- LS diagnostics
  - $V_{out} < V_{LVT}$ indicates a STG (see Figure 36. Deglitch and settling filter times for OFF state diagnostics: (left) STG detection on LS; (right) STB detection on HS)
  - $V_{LVT} < V_{out} < V_{OL}$ indicates an OL
  - $V_{out} > V_{OL}$ is a normal condition for LS configuration

- HS diagnostics
  - $V_{out} > V_{OL}$ indicates a STB (see Figure 36. Deglitch and settling filter times for OFF state diagnostics: (left) STG detection on LS; (right) STB detection on HS)
  - $V_{LVT} < V_{out} < V_{OL}$ indicates an OL
  - $V_{out} < V_{LVT}$ is a normal condition for HS configuration

Refer to Table 36. Diagnostic codes for the diagnostic codes corresponding to the STB/STG and OL faults.

Refer to Section 6.4.2: Diagnostic thresholds for the V_{OL} and V_{LVT} thresholds value.

When an OL or STB/STG fault is detected, the corresponding diagnostic code is latched, but no action is taken on the outputs.

Note: *V_{out} corresponds to DRNx pin for LS NMOS and HS PMOS configurations, while it is SNGPx pin for HS NMOS configuration.*

6.4.1 Settling and deglitch filter times

A filter time t_{DIAG} has been implemented to allow settling of the output node voltage (V_{out}) before the comparison to the diagnostic thresholds.

When an output is switched OFF, the t_{DIAG} filter time is started. When the filter expires, V_{out} is compared to the V_{LVT} and V_{OL} thresholds to determine the output diagnostic status (see Figure 36. Deglitch and settling filter times for OFF state diagnostics: (left) STG detection on LS; (right) STB detection on HS).

The filter time t_{DIAG} can be programmed as follows:

Table 43. Diagnostic filter time selection for OFF state

tdiag_config_xx	Value	Unit
Values available for all configurations		
00	25.6	µs
01	61.2	µs
10	105.6	µs
11	150	µs
Additional values available for H-Bridge configuration (refer to H-Bridge OFF state diagnostic timings**)**		
00	11.2	µs
01	28.9	µs
10	40	µs
11	51.2	µs

While in the OFF state, the t_{DIAG} filter is reset and restarts if one of the following condition occurs:

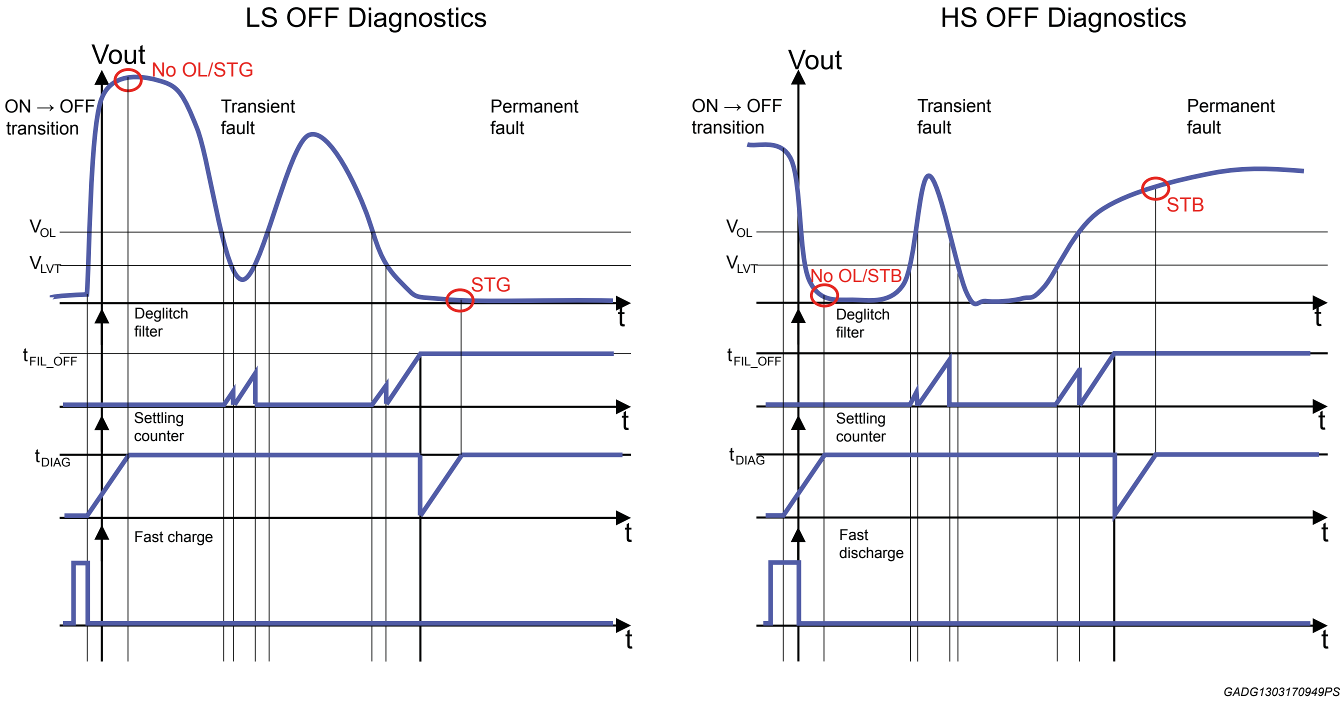
- LS configuration
  - V_{LVT} crossed with a negative slope (possible STG),
  - V_{OL} crossed with a negative slope (possible OL),
- HS configuration
  - V_{LVT} crossed with a positive slope (possible OL),
  - V_{OL} crossed with a positive slope (possible STB).

To avoid glitches on threshold crossing, a deglitch filter with t_{FIL_OFF} timeout has been implemented. The deglitch filter time t_{FIL_OFF} is fixed (see Figure 36. Deglitch and settling filter times for OFF state diagnostics: (left) STG detection on LS; (right) STB detection on HS):

Table 44. **Deglitch filter time for OFF state diagnostics**

Symbol	Parameter	Min.	Max.	Unit
t_{FIL_OFF}	Deglitch filter time for OFF state diagnostics	0.3	0.5	µs

Figure 36. **Deglitch and settling filter times for OFF state diagnostics: (left) STG detection on LS; (right) STB detection on HS**



Note: *V_{out} corresponds to DRNx pin for LS NMOS and HS PMOS configurations, while it's SNGPx pin for HS NMOS configuration.*

6.4.2 Diagnostic thresholds

The diagnostic thresholds are fixed, as shown in the table below. They have been designed in tracking, thus both spreading in the same direction.

Table 45. **OFF state diagnostic thresholds**

Symbol	Parameter	Min.	Max.	Unit
V_{LVT}	Threshold for: • STG detection in LS config ($V_{out} < V_{LVT}$) • OL detection in HS/LS config ($V_{LVT} < V_{out} < V_{OL}$)	1.9	2.3	V
V_{OL}	Threshold for: • STB detection in HS config ($V_{out} > V_{OL}$) • OL detection in HS/LS config ($V_{LVT} < V_{out} < V_{OL}$)	2.8	3.4	V

Note: *V_{out} corresponds to DRNx pin for LS NMOS and HS PMOS configurations, while it's SNGPx pin for HS NMOS configuration.*

6.4.3 Internal regulator for open load (OL) detection

Each channel features an internal regulator with limited current capability that regulates the output node voltage V_{out} around V_{OUT_OL}, which falls in the middle of the [V_{LVT}; V_{OL}] range. OL regulators are always ON, independently on the ENABLE_DIAGNOSTIC bit value.

Table 46. **Open Load output voltage**

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OUT_OL}	V_{out} node voltage in case of open load	2.25	2.5	2.75	V

Note: *V_{out} corresponds to DRNx pin for LS NMOS and HS PMOS configurations, while it's SNGPx pin for HS NMOS configuration.*

Regulator current capability IDIAG can be programmed via **diag_i_config_xx** bit as follows:

Table 47. **V_{out} regulator current capability I_{DIAG}**

diag_i_config_xx	Min.	Max.	Unit
0	60	100	µA
1	0.6	1	mA

A higher current capability allows compensating the leakage of external devices (FET, recirculation diodes, etc.) The current limitation feature allows distinguishing between OL and STB/STG faults:

- In case of open load, the regulator is able to drive V_{out} around V_{OUT_OL} and the OL fault is flagged;
- In case of STB/STG fault, due to the limited current capability, the regulator has no effect on V_{out}. Therefore, output node voltage stays below V_{LVT} (STG on LS) or above V_{OL} (STB on HS).

Refer to Figure 37. OFF state output regulator for OL detection. Example of operation on HS and Figure 39. Fast charge/discharge currents for OL detection: (left) OL detection on LS; (right) OL detection on HS for OL regulator operation in HS configuration.

Refer to Figure 38. OFF state output regulator for OL detection. Example of operation on LS and Figure 39. Fast charge/discharge currents for OL detection: (left) OL detection on LS; (right) OL detection on HS for OL regulator operation in LS configuration.

6.4.4 Fast charge/discharge currents

To reliably detect a fault, the V_{out} voltage must be stable before the settling time t_{DIAG} expires.

In case of STB/STG faults, high current capability of battery and ground supplies guarantee fast V_{out} settling.

In case of open load, Vout must be brought in the [V_{LVT}; V_{OL}] range before t_{DIAG} expires to guarantee fault detection. The device implements internal fast charge/discharge currents to allow settling of V_{out} in a time suitable for detection:

- When the HS transistor is switched OFF, a fast discharge current I_{FAST_DIS} rapidly decreases V_{out} down to V_{OL} to help the OL regulator detect an eventual open load fault (see Figure 37. OFF state output regulator for OL detection. Example of operation on HS and Figure 39. Fast charge/discharge currents for OL detection: (left) OL detection on LS; (right) OL detection on HS). I_{FAST_DIS} is enabled in the case:
  - The HS channel has been just switched OFF;
  - The settling time t_{DIAG} is still running;
  - V_{out} is above V_{OL}.

- When LS transistor is switched OFF, a fast charge current I_{FAST_CHG} rapidly increases V_{out} up to V_{LVT} to help the OL regulator detect an eventual open load fault (see Figure 37. OFF state output regulator for OL detection. Example of operation on HS and Figure 39. Fast charge/discharge currents for OL detection: (left) OL detection on LS; (right) OL detection on HS). I_{FAST_CHG} is enabled in the case:
  - The LS channel has been just switched OFF;
  - The settling time t_{DIAG} is still running;
  - Vout is below V_{LVT}.

Figure 37. **OFF state output regulator for OL detection. Example of operation on HS**

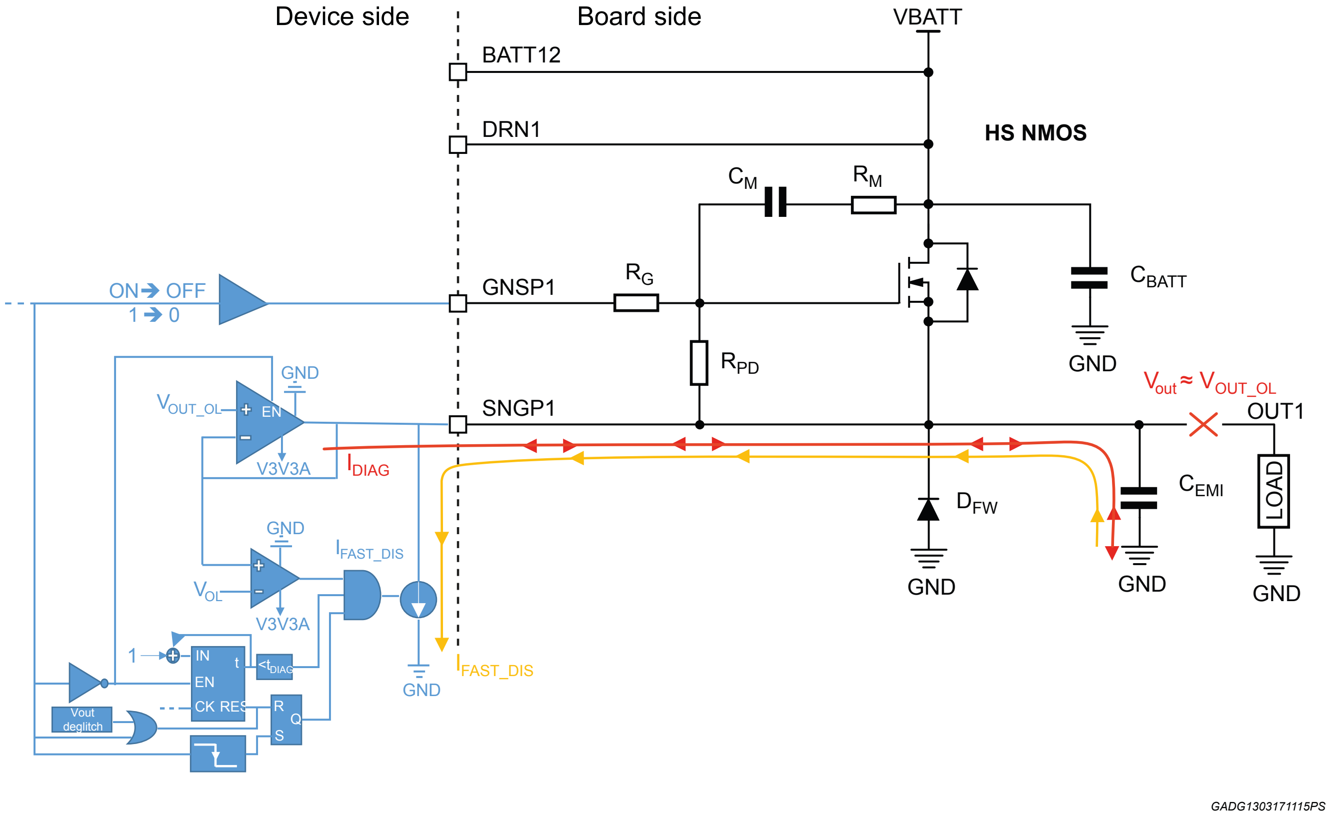


Figure 38. **OFF state output regulator for OL detection. Example of operation on LS**

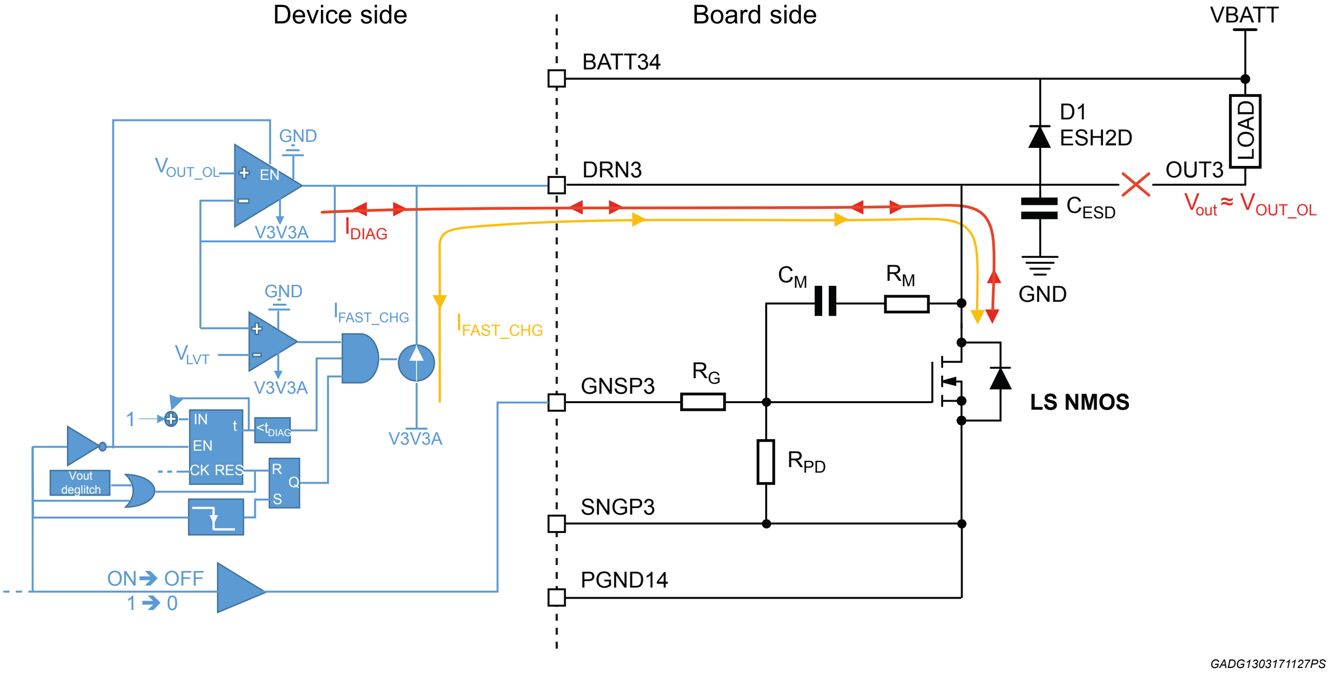
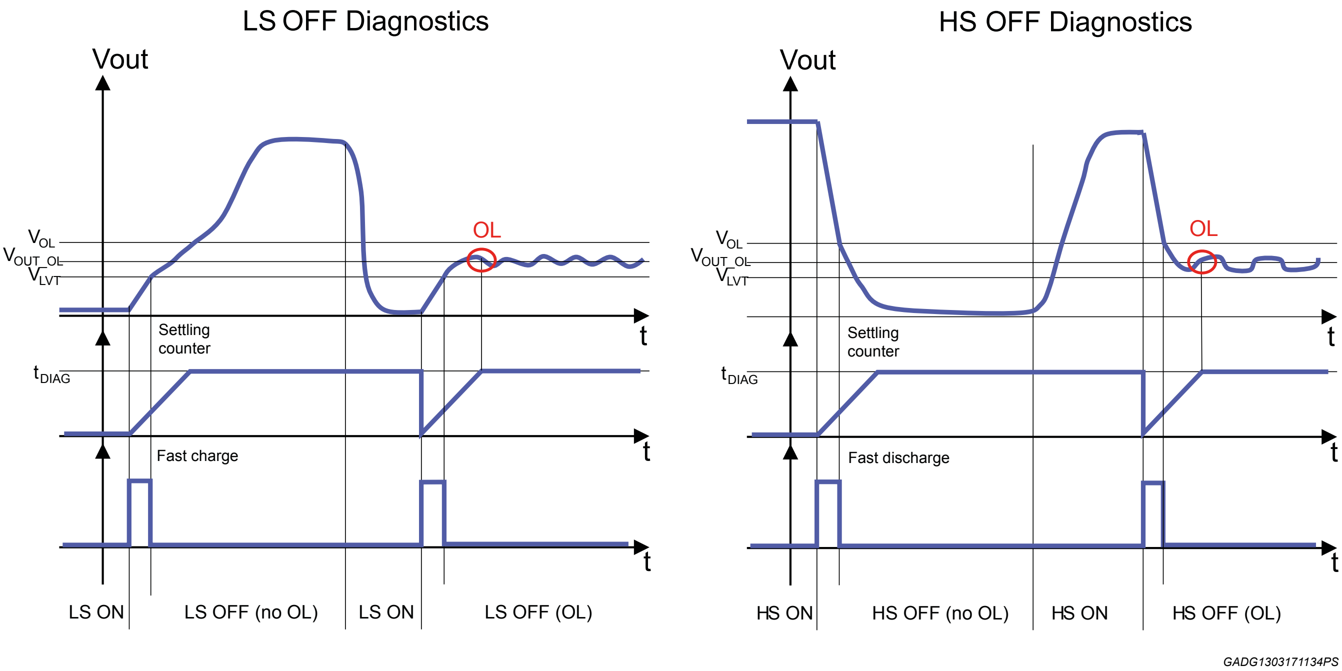


Figure 39. **Fast charge/discharge currents for OL detection: (left) OL detection on LS; (right) OL detection on HS**



The table below reports the electrical characteristics of the fast charge/discharge current generators.

Table 48. **Fast charge/discharge current generator electrical characteristics**

Symbol	Parameter	Min.	Max.	Unit
I_{FAST_CHG}	V_{out} node fast charge current used in case of LS NMOS	2.4	3.8	mA

Symbol	Parameter	Min.	Max.	Unit
$I_{FAST\_DIS\_P}$	$\mathbf{V_{out}}$ node fast discharge current used in case of HS PMOS	8	13	mA
$I_{FAST\_DIS\_N}$	$\mathbf{V_{out}}$ node fast discharge current used in case of HS NMOS	9	15	mA

Note: *V_{out} corresponds to DRNx pin for LS NMOS and HS PMOS configurations, while it is SNGPx pin for HS NMOS configuration.*

6.5 Silent diagnostic pulses for static loads

The device features ON/OFF diagnostic pulses of fixed duration for monitoring channels that are in a steady state. Two type of pulses are available:

- **OFF pulse**: turns off the selected channel for a t_{PULSE_OFF} interval. To be used for OL and STG/STB detection. It is effective only if T_{diag} < 100 µs.
- **ON pulse**: turns on the selected channel for a t_{PULSE_ON} interval. To be used for OC detection. It is effective only if T_{blank_oc} < 80 µs.

Once a diagnostic pulse is over, the output control is released and channel can be driven either by NONx pins or SPI (as programmed).

Diagnostic pulses can be sent by programming the **DIAG_ON_PULSE_xx** and **DIAG_OFF_PULSE_xx** bit in the COMMAND 9 frame. Pulse requests are latched and are reset once pulse execution is completed.

For each channel:

- A diagnostic pulse request must not be sent until the previous one is completed. If a pulse request incomes when pulse latches are still set, it will be ignored.
- If both OFF and ON pulses are requested in the same SPI frame, the behavior depends on the output state:
  - If the output is currently being kept OFF, an ON pulse will be generated
  - If the output is currently being kept ON, an OFF pulse will be generated

Diagnostic pulses requests are ignored in case of H-Bridge configuration.

The table below lists the diagnostic pulses related timings.

Table 49. **Diagnostic pulses timings**

Symbol	Parameter	Min.	Max.	Unit
t_{PULSE_ON}	ON pulse duration	80	120	µs
t_{PULSE_OFF}	OFF pulse duration	100	150	µs

6.6 Summary of disable sources and faults

The table below gathers all the disable sources and the fault events and summarizes their effects on the outputs.

Table 50. **Summary of disable sources and faults**

Event	CH1 – CH5	CH6	CH7 – CH8
DIS assertion (Section 6.1.1: DIS & NDIS pins)	Actively OFF^{A}	Actively OFF^{A}	No Effect
NDIS assertion (Section 6.1.1: DIS & NDIS pins)	Actively OFF^{A}	Actively OFF^{A}	No Effect
VDD5 overvoltage (Section 6.1.2: VDD5 Overvoltage/Undervoltage)	Actively OFF^{M}	Actively OFF^{M}	No Effect
VDD5 undervoltage (Section 6.1.2: VDD5 Overvoltage/Undervoltage)	Actively OFF^{A}	Actively OFF^{A}	No Effect
BIST on going (Section 6.1.3: BIST & HWSC)	Three-State	Three-State	Three-State
BIST failed (Section 6.1.3: BIST & HWSC)	Actively OFF^{M}	Actively OFF^{M}	Three-State^{M}
HWSC on going (Section 6.1.3: BIST & HWSC)	Actively OFF	Actively OFF	Three-State
HWSC failed (Section 6.1.3: BIST & HWSC)	Actively OFF^{M}	Actively OFF^{M}	Three-State^{M}

Event	CH1 – CH5	CH6	CH7 – CH8
VPS undervoltage (Section 6.1.4: VPS undervoltage)	Actively OFF^{A}	Actively OFF^{A}	Actively OFF^{A}
Charge Pump undervoltage (Section 6.1.5: Charge pump undervoltage)	Actively OFF^{A}	Actively OFF^{A}	Actively OFF^{A}
Disable via SPI (en_OUT_xx) (Section 6.1.6: SPI enable bit)	Three-State^{M}	Three-State^{M}	Three-State^{M}
Disable via SPI (prot_disable_xx) (Section 6.1.7: Protection disable bit)	Actively OFF^{M}	Actively OFF^{M}	Actively OFF^{M}
EN6 set low (Section 6.1.8: EN6 input)	No Effect	Actively OFF^{A}	No Effect
NRES assertion (Section 6.1.9: NRES assertion)	Actively OFF^{M}	Actively OFF^{M}	Actively OFF^{M}
CC failed (Section 6.1.10: Communication Check (CC))	Actively OFF^{M}	Actively OFF^{M}	No Effect
OC failure (Section 6.3.1: Behavior in case of OC detection)	Actively OFF^{M}	Actively OFF^{M}	Actively OFF^{M}
STG failure (Section 6.4: OFF state diagnostics)	No Effect	No Effect	No Effect
STB failure (Section 6.4: OFF state diagnostics)	No Effect	No Effect	No Effect
OL failure (Section 6.4: OFF state diagnostics)	No Effect	No Effect	No Effect
ON pulse request (Section 6.5: Silent diagnostic pulses for static loads)	Actively ON^{A}	Actively ON^{A}	Actively ON^{A}
OFF pulse request (Section 6.5: Silent diagnostic pulses for static loads)	Actively OFF^{A}	Actively OFF^{A}	Actively OFF^{A}

Syntax: A = Automatic Re-Engagement, M = Manual Re-Engagement

Note: *When configured as H-Bridge, CH7 and CH8 are treated like CH1-CH5.*

6.7 Signal integrity check

For signal integrity purposes, the device offers the possibility of verifying the correct propagation and effects of the control signals. The integrity of the output signals can be monitored via SPI issuing the following frames:

- **Frame 1 = 0xBAAAAAAA**: channels 1 to 4 integrity report
- **Frame 2 = 0xCAAAAAAB**: channels 5 to 8 integrity report

The response frame consists of 32 bit containing the following fields:

Table 51. **Response frames to signal integrity requests**

		Response Frame															
		31-28	27	26-21	20	19	18	17	16	15	14	13	12-10	9-7	6-4	3-1	0
Frame issued	Fr1	1011	1	010101	V4	V3	V2	V1	C4	C3	C2	C1	PUPD4	PUPD3	PUPD2	PUPD1	P
	Fr2	1100	1	010101	V8	V7	V6	V5	C8	C7	C6	C5	PUPD8	PUPD7	PUPD6	PUPD5	P

Note: *The SPI protocol is out of frame, meaning that the response to the current message will be issued on the following frame.*

Field description of Table 51. Response frames to signal integrity requests is listed below:

- **P**: Parity bit, based on even parity calculation
- **PUPDx**: Pull up / Pull down status. This field consists of 3 bit encoding the current status of the gate charge / discharge current sources (IPU and IPD in Figure 12. Output pre-driver control) for the x$^{\text{th}}$ channel. The code depends on the output configuration:

High-Side with PFET

- 100 : IPD ON and IPU OFF→ transistor ON
- 010 : IPD OFF and IPU ON → transistor OFF
- 000 : IPD OFF and IPU OFF → output in three-state
- Others : integrity of the output control is compromised

High-Side/Low-Side with NFET

- 010 : IPD ON and IPU OFF → transistor OFF

- 001 : IPD OFF and IPU ON → transistor ON
- 000: IPD OFF and IPU OFF → output in three-state
- Others : integrity of the output control is compromised
- **Cx**: Output control signal. This flag combines the control signals SPI_ON_OUTxx, NONx and SPI_input_sel_xx to feedback if the xth channel is commanded ON or OFF
  - 1 : output commanded ON
  - 0 : output commanded OFF
- **Vx**: Channel status. This flag provides feedback about the external FET output voltage (DRNx pin in case of LS NMOS or HS PMOS, SNGPx pin in case of HS NMOS) through the internal diagnostic comparators (refer to Section 6.4: OFF state diagnostics for further information about diagnostics). The value of this bit depends on the channel configuration:

High-Side with NFET/PFET

- 1 : Output voltage high (Vout > VOL) → transistor ON
- 0 : Output voltage low (Vout < VOL) → transistor OFF

Low-Side with NFET

- 1 : Drain voltage high (Vout > VLVT) → transistor OFF
- 0 : Drain voltage low (Vout < VLVT) → transistor ON

Note: *This information is not intended to replace diagnostics and must be used only to verify the control signal integrity. Refer to Section 6.2: Diagnostics overview in order to understand how output diagnostic is performed and which are the fault codes.*

7 Ordering information

Table 52. **Order codes**

Order code	Package	Package marking	Packaging
L98GD8-TR	TQFP64 (exposed pad down)	L98GD8	Tape and reel

8 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 TQFP64 (10x10x1 mm exp. pad down) package information

Figure 40. **TQFP64 (10x10x1 mm exp. pad down) package outline**

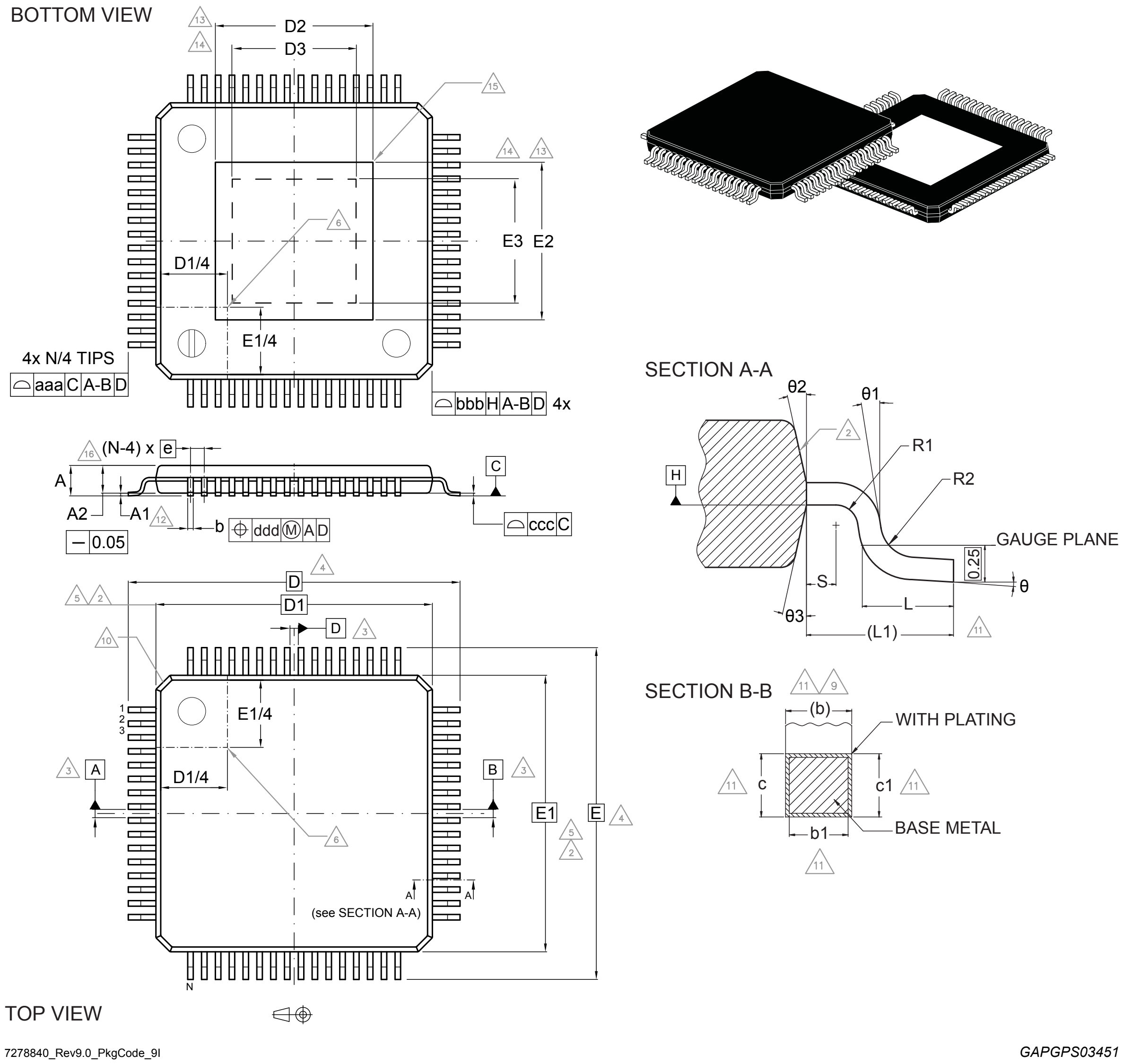


Table 53. TQFP64 (10x10x1 mm exp. pad down) package mechanical data

Ref	Min.	Typ.	Max.	Note (see # in Notes below)
Θ	0°	3.5°	7°	-
Θ1	0°	-	-	-
Θ2	11°	12°	13°	-
Θ3	11°	12°	13°	-
A	-	-	1.2	15
A1	0.05	-	0.15	12
A2	0.95	1	1.05	15
b	0.17	0.22	0.27	9, 11
b1	0.17	0.2	0.23	11
c	0.09	-	0.2	11
c1	0.09	-	0.16	11
D	-	12.00 BSC	-	4
D1	-	10.00 BSC	-	5, 2
D2	-	-	6.4	13
D3	4.8	-	-	14
e	-	0.50 BSC	-	-
E	-	12.00 BSC	-	4
E1(*)	-	10.00 BSC	-	5, 2
E2	-	-	6.4	13
E3	4.8	-	-	14
L	0.45	0.6	0.75	-
L1	-	1.00 REF	-	-
N	-	64	-	16
R1	0.08	-	-	-
R2	0.08	-	0.2	-
S	0.2	-	-	-
Tolerance of form and position				
aaa	-	0.2	-	1, 7
bbb	-	0.2	-	
ccc	-	0.08	-	
ddd	-	0.08	-	

Notes

1. Dimensioning and tolerancing schemes conform to ASME Y14.5M-1994.
2. The Top package body size may be smaller than the bottom package size up to 0.15 mm.
3. Datum A-B and D to be determined at datum plane H.
4. To be determined at seating datum plane C.
5. Dimensions D1 and E1 do not include mold flash or protrusions. Allowable mold flash or protrusions is “0.25 mm” per side. D1 and E1 are Maximum plastic body size dimensions including mold mismatch.
6. Details of pin 1 identifier are optional but must be located within the zone indicated.
7. All Dimensions are in millimeters.

8. No intrusion allowed inwards the leads.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum “b” dimension by more than 0.08 mm. Dambar cannot be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm for 0.4 mm and 0.5 mm pitch packages.
10. Exact shape of each corner is optional.
11. These dimensions apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
12. A1 is defined as the distance from the seating plane to the lowest point on the package body.
13. Dimensions D2 and E2 show the maximum exposed metal area on the package surface where the exposed pad is located (if present). It includes all metal protrusions from exposed pad itself.
14. Dimensions D3 and E3 show the minimum solderable area, defined as the portion of exposed pad which is guaranteed to be free from resin flashes/bleeds, bordered by internal edge of inner groove.
15. The optional exposed pad is generally coincident with the top or bottom side of the package and not allowed to protrude beyond that surface.
16. “N” is the number of terminal positions for the specified body size.

Revision history

Table 54. **Document revision history**

Date	Revision	Changes
03-Sep-2024	1	Initial release.
08-May-2025	2	Front page: updated package image, edit change in Features list, added Applications list; removed tray option from product summary table. Minor text changes in the Description text. Features and Description. Changed name of chapter 2 (form Application to Output configurations). Pinout chapter: deleted the sentence "All pins, except the ground ones, can withstand at least 40 V to GND.". Moved parameter I_{PS_leak} from table 2 to table 9. Table 7: specified extended range up to 58V and specified operational range up to 48V (due to voltage sense ADC saturation). Chapter 5.4.4: removed the reference to the obsolete application note. Table 15: changed the test conditions of I_{LEAK_S} parameter with V_SNGPx up to 52V. Table 24: fixed typos of row OUT1 STG / column HS ON-LS OFF; row OUT4 STB column HS OFF-LS ON; row OUT4 STG column HS ON-LS OFF. Added ordering information chapter.

Contents

List of tables

List of figures

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