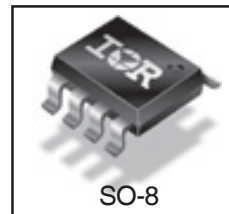
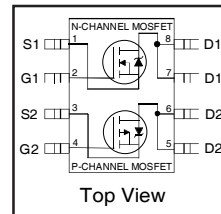


	N-CH	P-CH	
V_{DS}	30	-30	V
$R_{DS(on) \max}$	27	64	mΩ
Q_g (typical)	6.8	8.1	nC
I_D (@ $T_A = 25^\circ\text{C}$)	6.8	-4.6	A

HEXFET® Power MOSFET



Applications

- High and Low Side Switches for Inverter
- High and Low Side Switches for Generic Half-Bridge

Features

High and low-side MOSFETs in a single package
High-side P-Channel MOSFET
Industry-standard pinout
Compatible with existing surface mount techniques
RoHS compliant containing no Lead, no Bromide and no Halogen
MSL1, Consumer qualification

results in
⇒

Benefits

Increased power density
Easier drive circuitry
Multi-vendor compatibility
Easier manufacturing
Environmentally friendlier
Increased reliability

Base Part Number	Package Type	Standard Pack		Orderable part number
		Form	Quantity	
IRF9389PbF	SO-8	Tube/Bulk	95	IRF9389PbF
		Tape and Reel	4000	IRF9389TRPbF

Absolute Maximum Ratings

	Parameter	Max.		Units
		N-Channel	P-Channel	
V _{GS}	Gate-to-Source Voltage	±20	±20	V
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V	6.8	-4.6	A
I _D @ T _A = 70°C	Continuous Drain Current, V _{GS} @ 10V	5.4	-3.7	
I _{DM}	Pulsed Drain Current ①	34	-23	
P _D @T _A = 25°C	Power Dissipation	2.0		W
P _D @T _A = 70°C	Power Dissipation	1.3		
	Linear Derating Factor	0.016		W/°C
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance

	Parameter	Typ.	Max	Units
$R_{\theta JL}$	Junction-to-Drain Lead ④	—	20	°C/W
$R_{\theta JA}$	Junction-to-Ambient ③	—	62.5	

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter		Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	N-Ch	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
		P-Ch	-30	—	—		$V_{GS} = 0V, I_D = -250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	N-Ch	—	0.03	—	$V/^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
		P-Ch	—	0.02	—		Reference to $25^\circ\text{C}, I_D = -1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	N-Ch	—	22	27	$m\Omega$	$V_{GS} = 10V, I_D = 6.8A$ ②
			—	33	40		$V_{GS} = 4.5V, I_D = 5.4A$ ②
		P-Ch	—	51	64	$m\Omega$	$V_{GS} = -10V, I_D = -4.6A$ ②
			—	82	103		$V_{GS} = -4.5V, I_D = -3.7A$ ②
$V_{GS(th)}$	Gate Threshold Voltage	N-Ch	1.3	1.8	2.3	V	$V_{DS} = V_{GS}, I_D = 10\mu A$
		P-Ch	-1.3	-1.8	-2.3		$V_{DS} = V_{GS}, I_D = -10\mu A$
I_{DSS}	Drain-to-Source Leakage Current	N-Ch	—	—	1.0	μA	$V_{DS} = 24V, V_{GS} = 0V$
		P-Ch	—	—	-1.0		$V_{DS} = -24V, V_{GS} = 0V$
		N-Ch	—	—	150		$V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
		P-Ch	—	—	-150		$V_{DS} = -24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	N-Ch	—	—	100	nA	$V_{GS} = 20V$
		P-Ch	—	—	-100		$V_{GS} = -20V$
	Gate-to-Source Reverse Leakage	N-Ch	—	—	-100		$V_{GS} = -20V$
		P-Ch	—	—	100		$V_{GS} = 20V$
g_{fs}	Forward Transconductance	N-Ch	8.2	—	—	S	$V_{DS} = 15V, I_D = 5.4A$
		P-Ch	4.1	—	—		$V_{DS} = -15V, I_D = -3.7A$
Q_g	Total Gate Charge	N-Ch	—	6.8	14	nC	N-Channel $V_{GS} = 10V, V_{DS} = 15V, I_D = 6.8A$
		P-Ch	—	8.1	16		
Q_{gs}	Gate-to-Source Charge	N-Ch	—	1.4	—		
		P-Ch	—	1.3	—		P-Channel $V_{GS} = -10V, V_{DS} = -15V, I_D = -4.6A$
Q_{gd}	Gate-to-Drain ("Miller") Charge	N-Ch	—	0.98	—		
		P-Ch	—	2.1	—		
R_G	Gate Resistance	N-Ch	—	2.2	4.4	Ω	
		P-Ch	—	9.4	19		
$t_{d(on)}$	Turn-On Delay Time	N-Ch	—	5.1	—	ns	N-Channel $V_{DD} = 15V, V_{GS} = 4.5V$ ② $I_D = 1.0A, R_G = 6.2\Omega$
		P-Ch	—	8.0	—		
t_r	Rise Time	N-Ch	—	4.8	—		
		P-Ch	—	14	—		
$t_{d(off)}$	Turn-Off Delay Time	N-Ch	—	4.9	—		P-Channel $V_{DD} = -15V, V_{GS} = -4.5V$ ② $I_D = -1.0A, R_G = 6.8\Omega$
		P-Ch	—	17	—		
t_f	Fall Time	N-Ch	—	3.9	—	pF	
		P-Ch	—	15	—		
C_{iss}	Input Capacitance	N-Ch	—	398	—		N-Channel $V_{GS} = 0V, V_{DS} = 15V, f = 1.0\text{MHz}$
		P-Ch	—	383	—		
C_{oss}	Output Capacitance	N-Ch	—	82	—		
		P-Ch	—	104	—		P-Channel $V_{GS} = 0V, V_{DS} = -15V, f = 1.0\text{KHz}$
C_{rss}	Reverse Transfer Capacitance	N-Ch	—	36	—		
		P-Ch	—	64	—		

Diode Characteristics

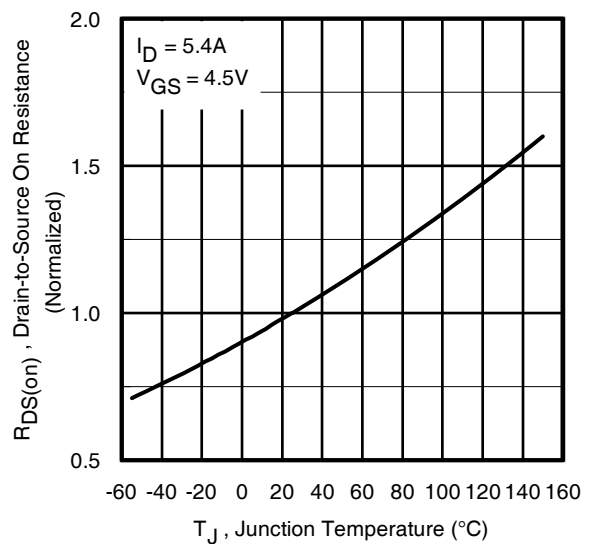
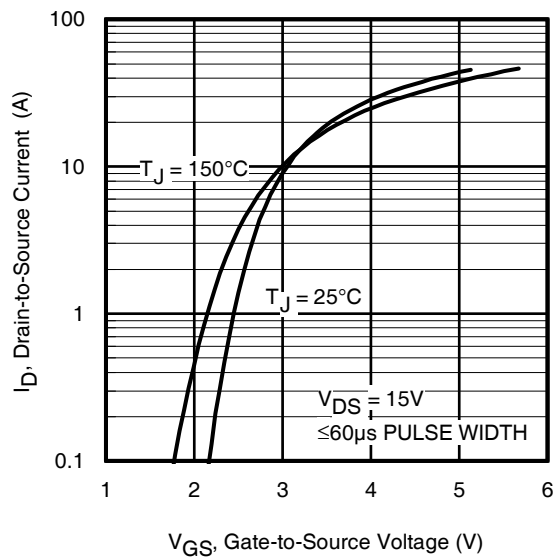
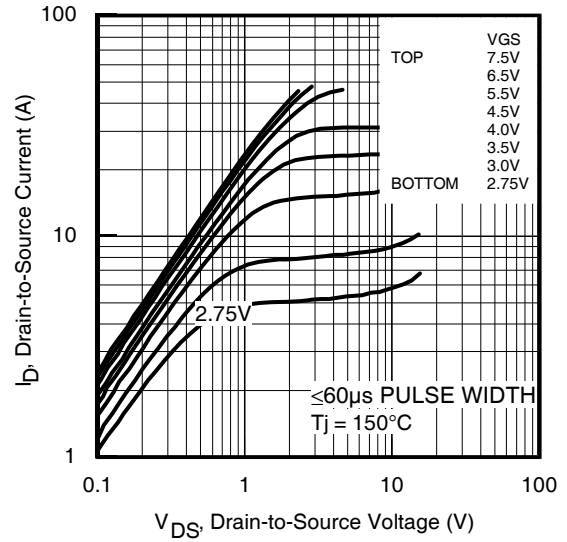
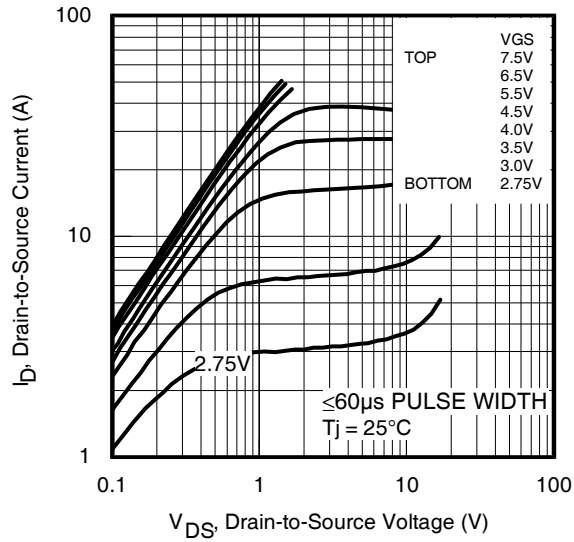
	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	N-Ch	—	—	2.0	A	
		P-Ch	—	—	-2.0		
I_{SM}	Pulsed Source Current (Body Diode)	N-Ch	—	—	34		
		P-Ch	—	—	-23		
V_{SD}	Diode Forward Voltage	N-Ch	—	—	1.2	V	$T_J = 25^\circ\text{C}, I_S = 2.0A, V_{GS} = 0V$ ②
		P-Ch	—	—	-1.2		$T_J = 25^\circ\text{C}, I_S = -2.0A, V_{GS} = 0V$ ②
t_{rr}	Reverse Recovery Time	N-Ch	—	8.4	13	ns	N-Channel: $T_J = 25^\circ\text{C}, I_F = 2.0A,$ $V_{DD} = 15V, di/dt = 102/\mu s$ ②
		P-Ch	—	11	17		
Q_{rr}	Reverse Recovery Charge	N-Ch	—	2.3	3.5	nC	P-Channel: $T_J = 25^\circ\text{C}, I_F = -2.0A,$ $V_{DD} = -15V, di/dt = 102/\mu s$ ②
		P-Ch	—	4.8	7.2		

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 16)
 ② Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.

- ③ Surface mounted on 1 in square Cu board
 ④ R_θ is measured at T_J approximately 90°C

N-Channel



N-Channel

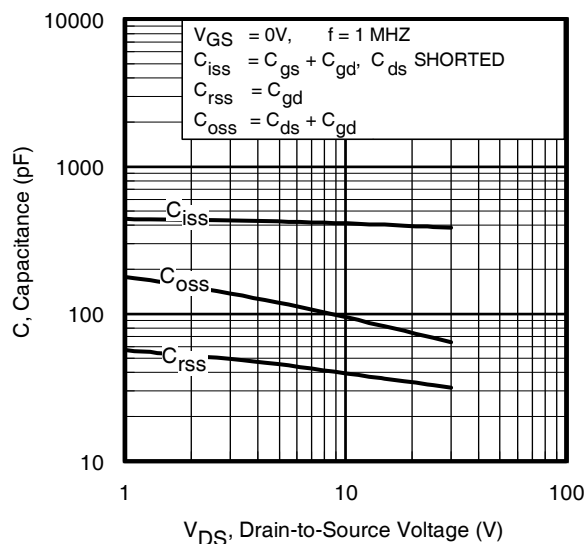


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

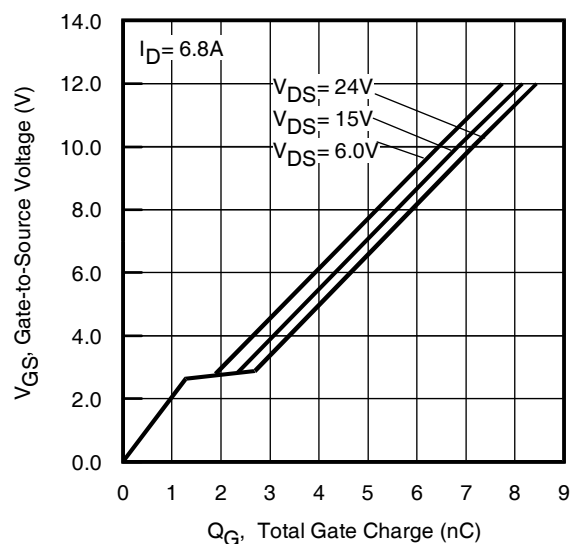


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

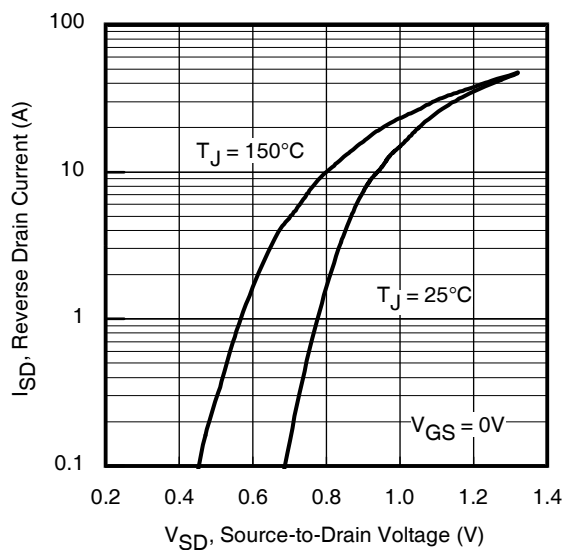


Fig 7. Typical Source-Drain Diode Forward Voltage

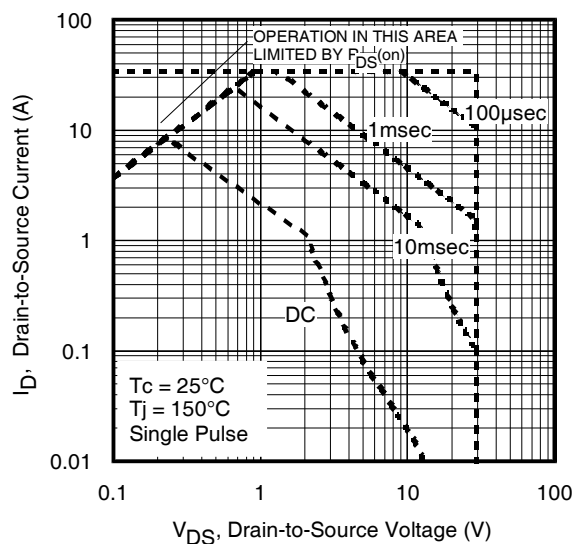


Fig 8. Maximum Safe Operating Area

N-Channel

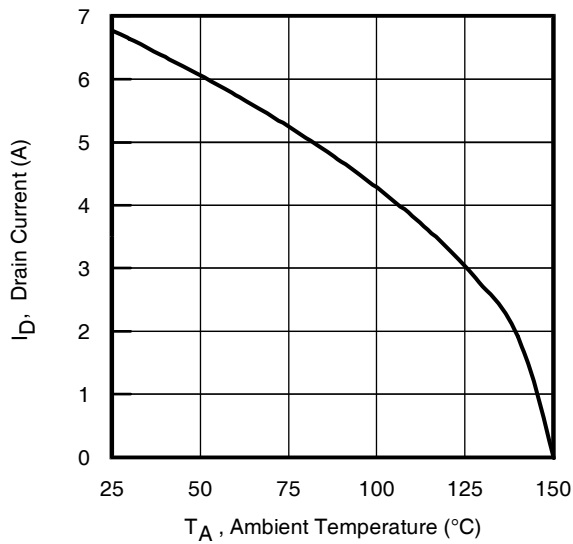


Fig 9. Maximum Drain Current vs. Ambient Temperature

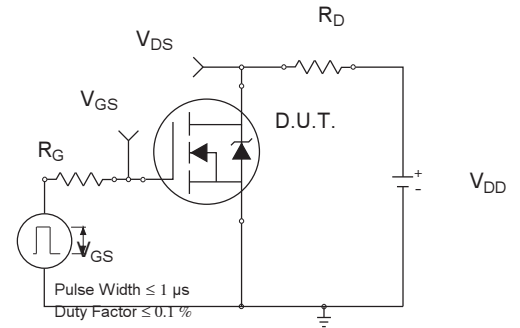


Fig 10a. Switching Time Test Circuit

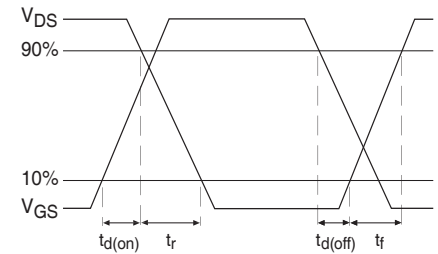


Fig 10b. Switching Time Waveforms

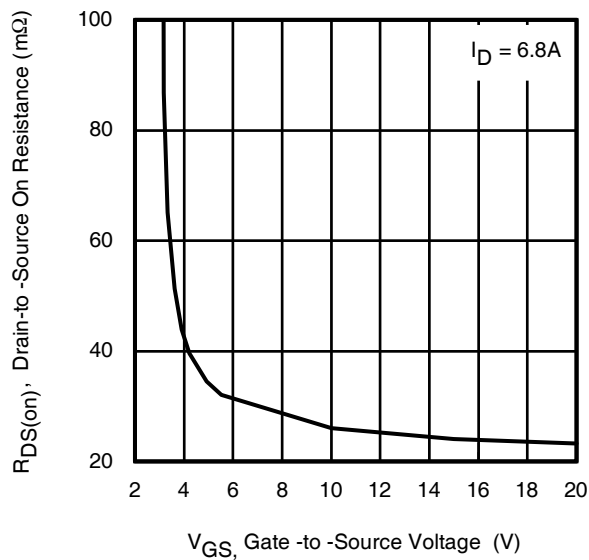


Fig 11. Typical On-Resistance vs. Gate Voltage

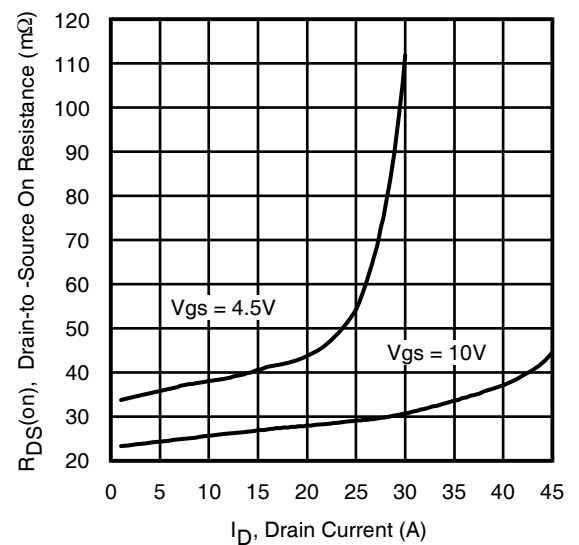


Fig 12. Typical On-Resistance vs. Drain Current

N-Channel

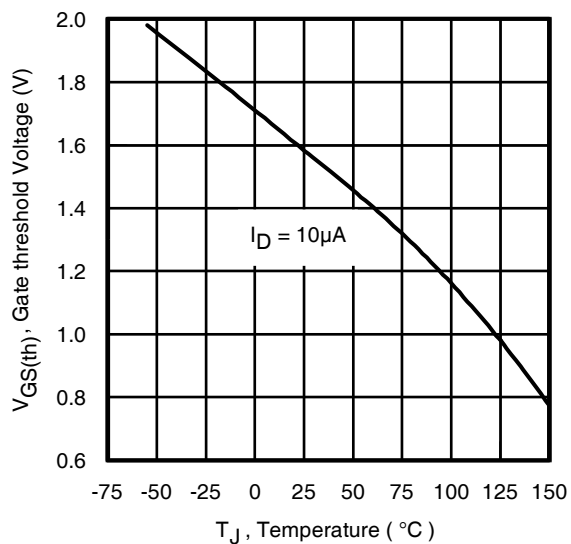


Fig 13. Threshold Voltage vs. Temperature

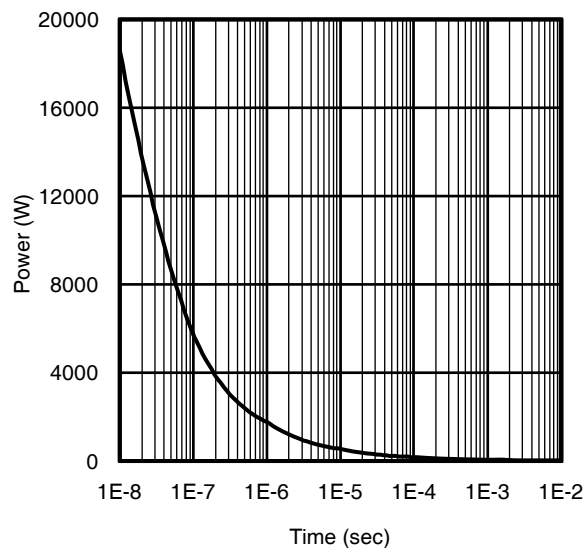


Fig 14. Typical Power vs. Time

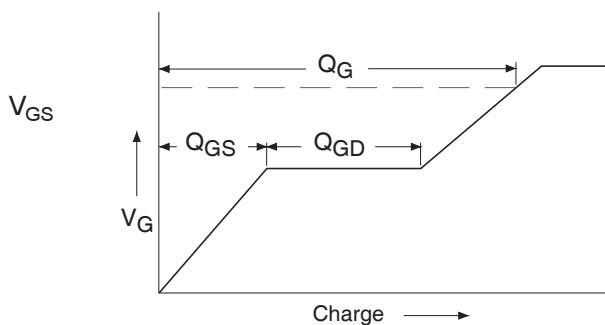


Fig 15a. Basic Gate Charge Waveform

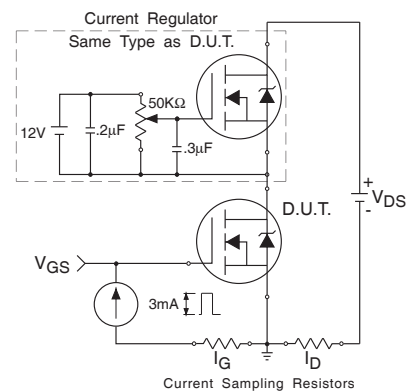


Fig 15b. Gate Charge Test Circuit

N and P-Channel

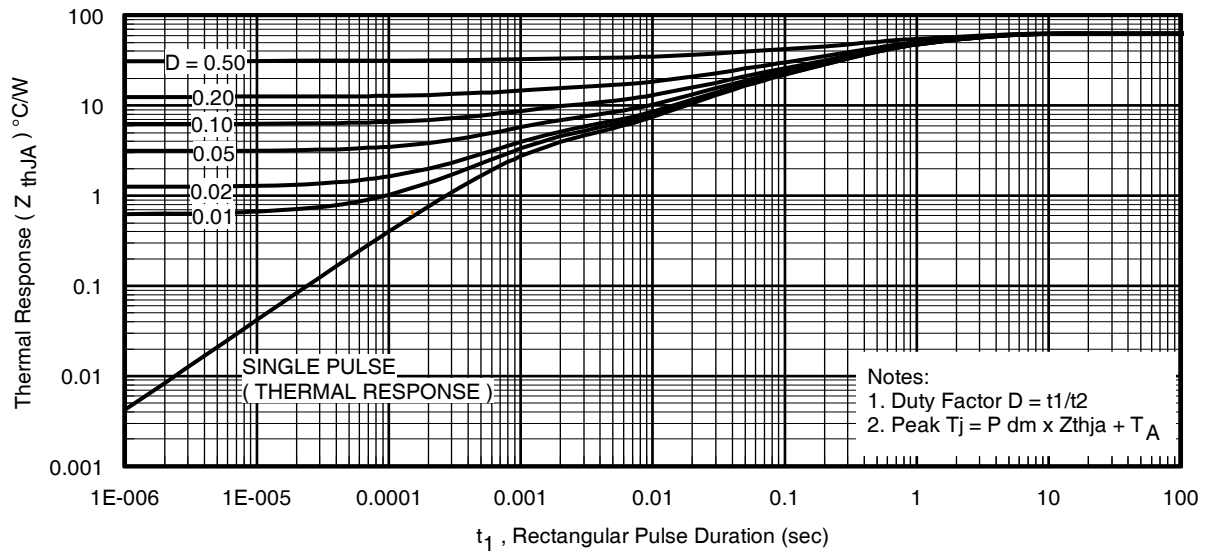


Fig 16. Typical Effective Transient Thermal Impedance, Junction-to-Ambient

P-Channel

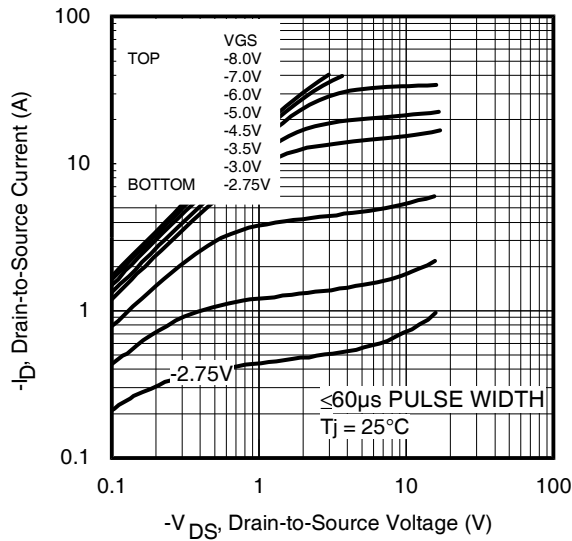


Fig 17. Typical Output Characteristics

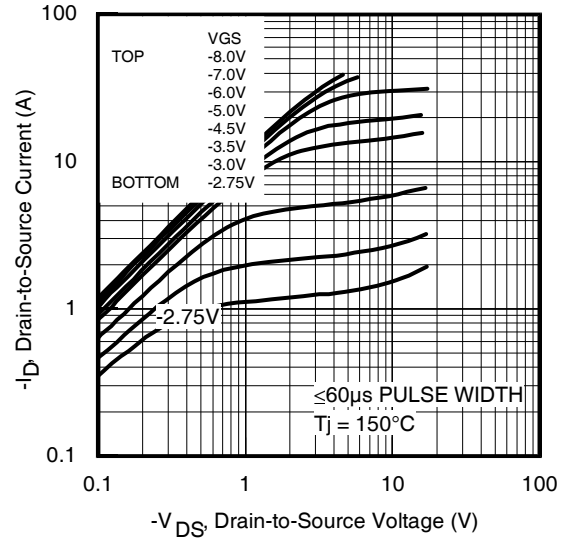


Fig 18. Typical Output Characteristics

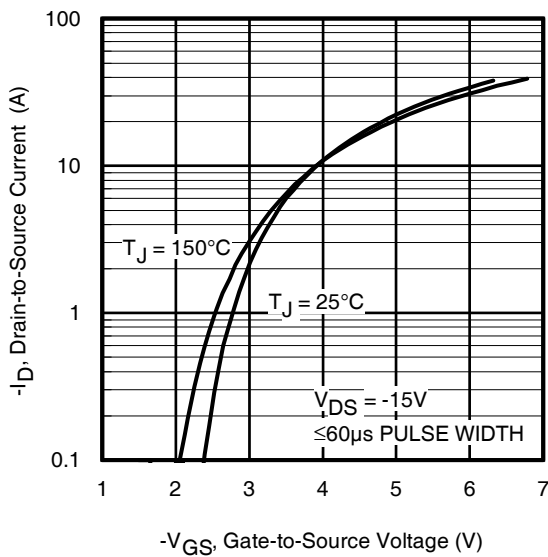


Fig 19. Typical Transfer Characteristics

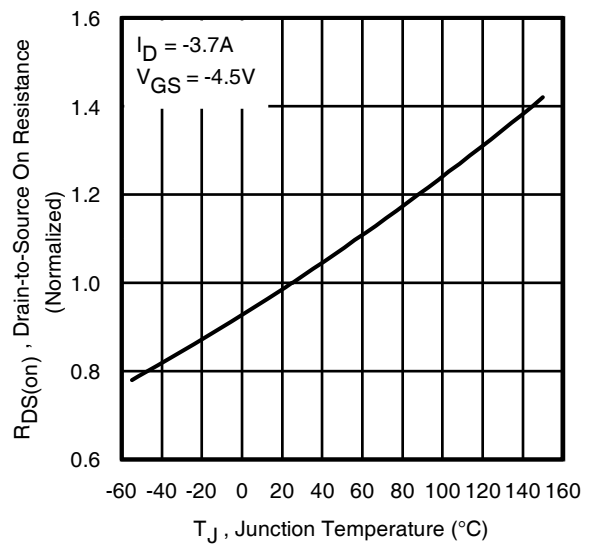


Fig 20. Normalized On-Resistance vs. Temperature

P-Channel

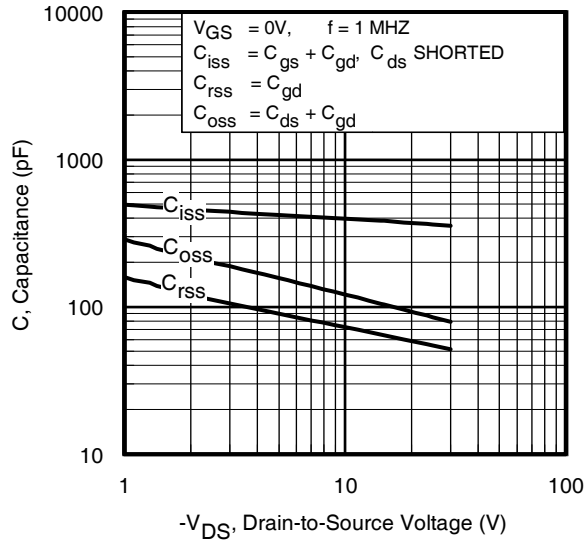


Fig 21. Typical Capacitance vs. Drain-to-Source Voltage

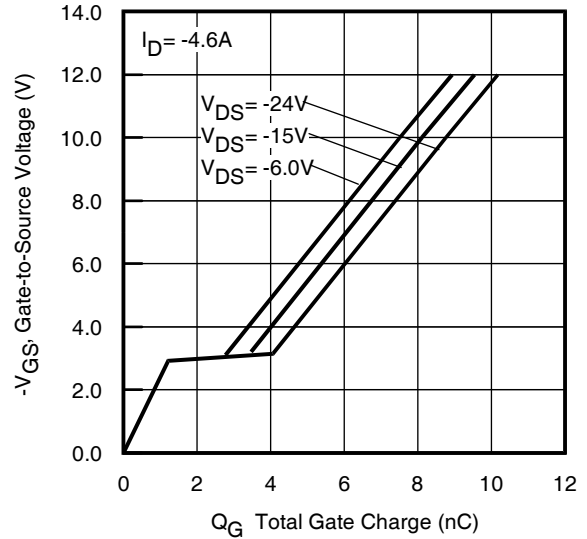


Fig 22. Typical Gate Charge vs. Gate-to-Source Voltage

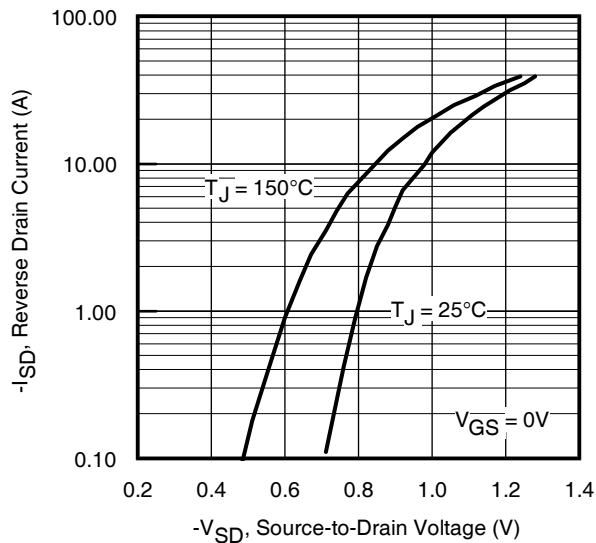


Fig 23. Typical Source-Drain Diode Forward Voltage

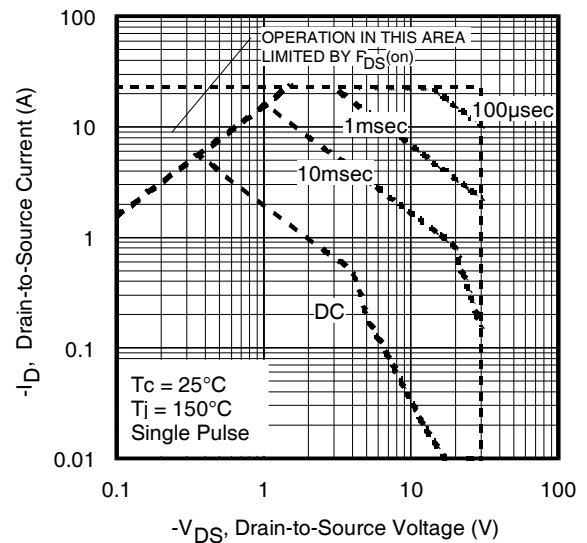


Fig 24. Maximum Safe Operating Area

P-Channel

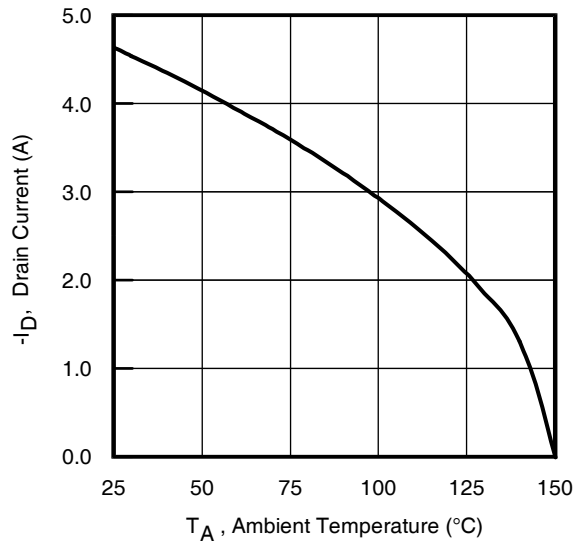


Fig 25. Maximum Drain Current vs. Ambient Temperature

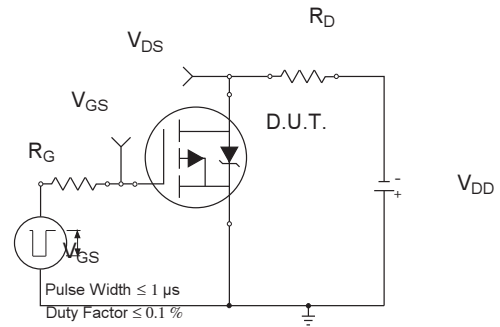


Fig 26a. Switching Time Test Circuit

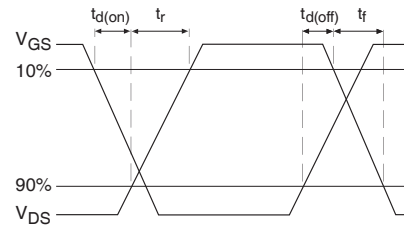


Fig 26b. Switching Time Waveforms

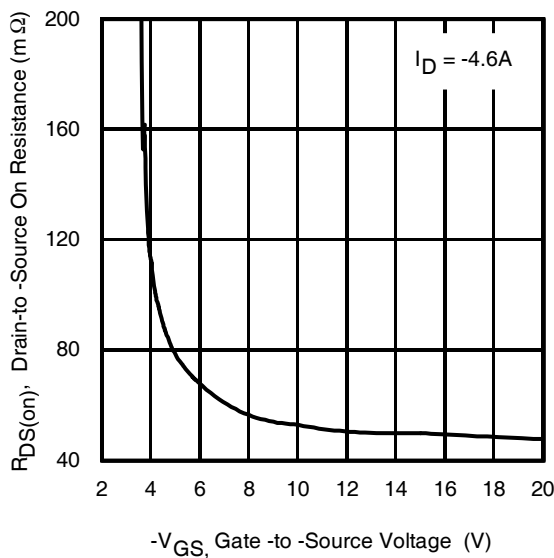


Fig 27. Typical On-Resistance vs. Gate Voltage

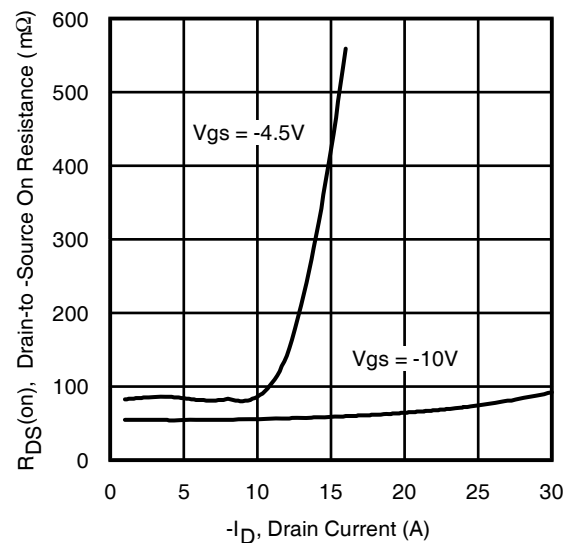


Fig 28. Typical On-Resistance vs. Drain Current

P-Channel

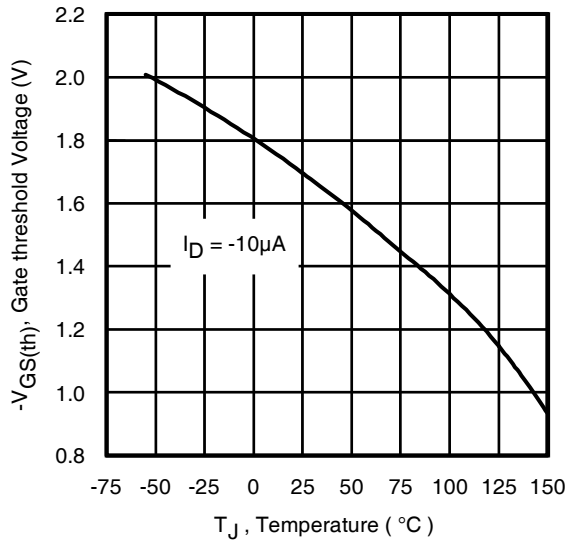


Fig 29. Threshold Voltage vs. Temperature

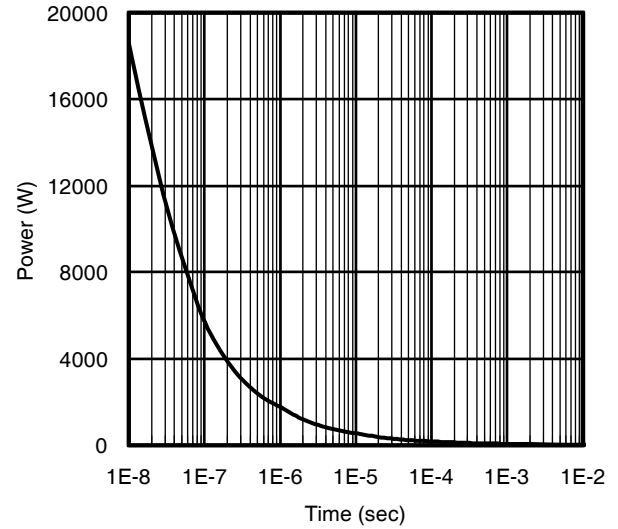


Fig 30. Typical Power vs. Time

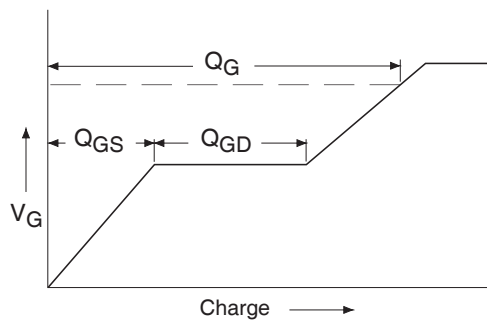


Fig 31a. Basic Gate Charge Waveform

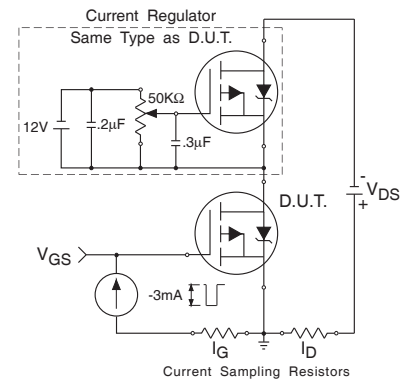
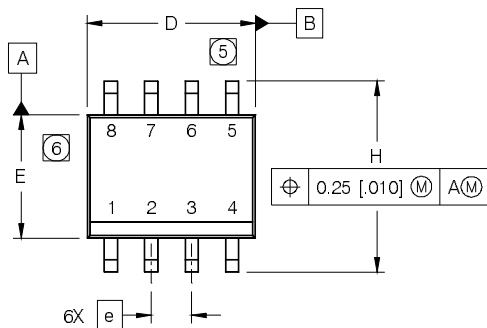
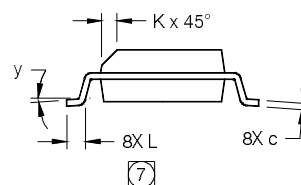
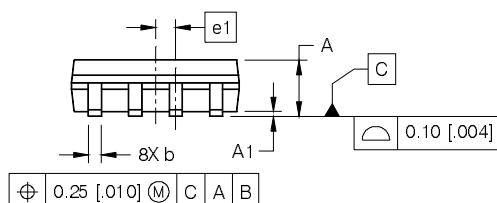


Fig 31b. Gate Charge Test Circuit

SO-8 Package Details



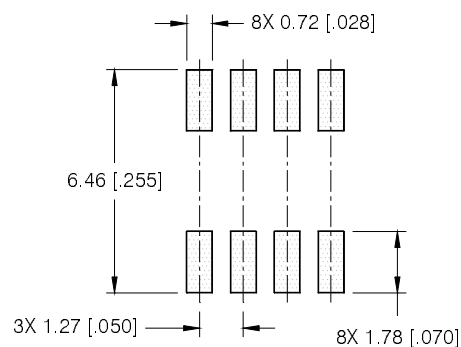
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



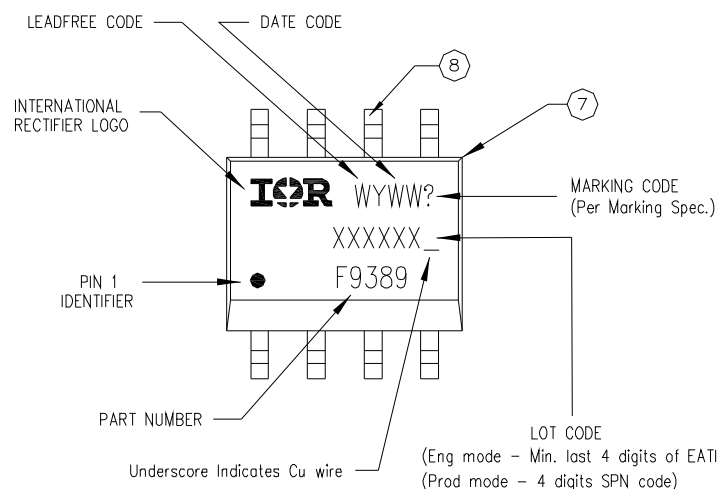
NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [0.006].
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [0.010].
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

FOOTPRINT

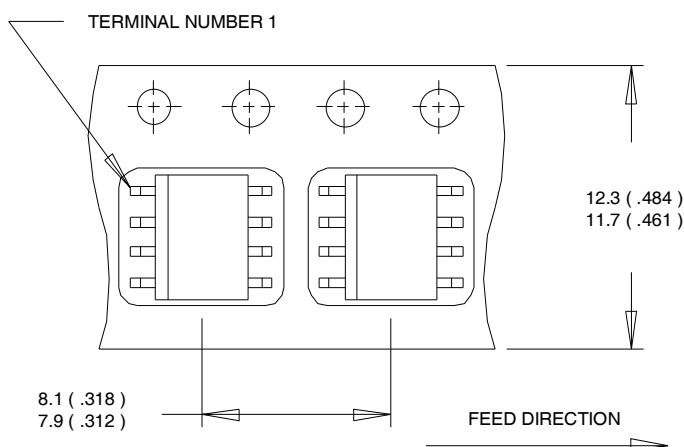


SO-8 Part Marking



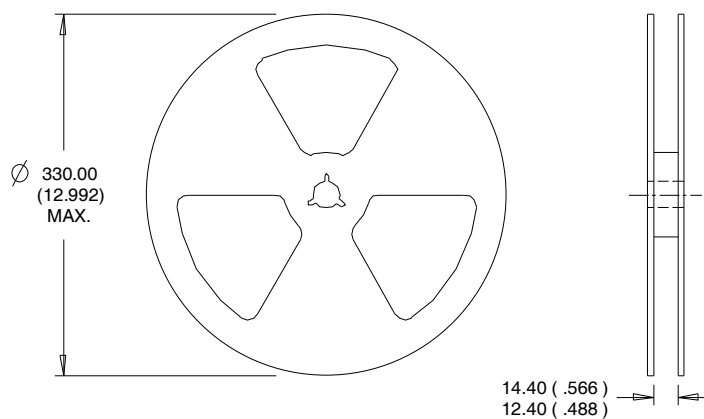
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Tape and Reel



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Qualification information[†]

Qualification level	Consumer (per JEDEC JESD47F ^{††} guidelines)	
Moisture Sensitivity Level	SO-8	MSL1 (per JEDEC J-STD-020D ^{††})
RoHS compliant	Yes	

[†] Qualification standards can be found at International Rectifier's web site:

<http://www.irf.com/product-info/reliability/>

^{††} Applicable version of JEDEC standard at the time of product release.

International
 Rectifier

IR WORLD HEADQUARTERS: 101 N. Sepulveda Blvd., El Segundo, California 90245
 To contact International Rectifier, please visit <http://www.irf.com/who-to-call/>