

Document Title**512Kx8 bit Low Power CMOS Static RAM****Revision History**

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>
0.0	Initial Draft	October 26, 1993	Advance
0.1	Revise	December 9, 1994	Preliminary
0.2	Revise - Changed Operating current Icc2; 80mA → 90mA	June 5, 1995	Preliminary
1.0	Finalize - Change datasheet format ; One datasheet for commercial and industrial product.	April 15, 1996	Final
2.0	Revise - Change datasheet format - Remove low power product from TSOP package product - Remove 100ns part form product	February 25, 1998	Final

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512K x8 bit Low Power CMOS Static RAM

FEATURES

- Process Technology : TFT
- Organization : 512Kx8
- Power Supply Voltage : 4.5~5.5V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : 32-DIP-600, 32-SOP-525, 32-TSOP2-400F/R

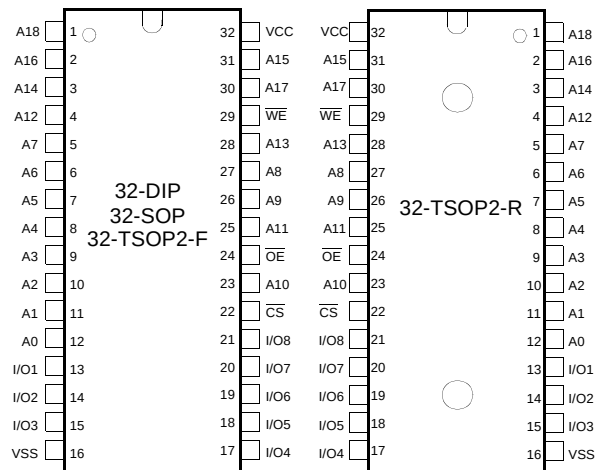
GENERAL DESCRIPTION

The KM684000A families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and have various package types for user flexibility of system design. The families also supports low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

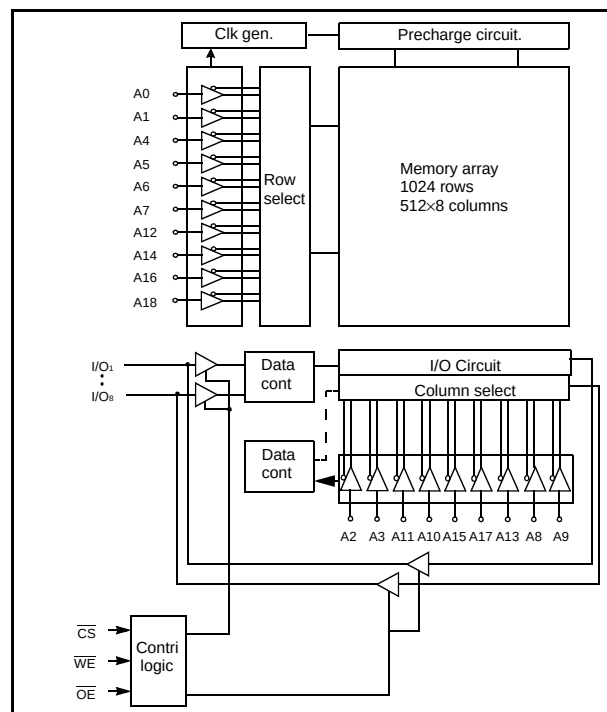
Product Family	Operating Temperature	Vcc Range(V)	Speed(ns)	Power Dissipation		PKG Type
				Standby (Isb1, Max)	Operating (icc2, Max)	
KM684000AL KM684000AL-L	Commercial(0~70°C)	4.5~5.5	55/70ns	100µA 20µA	90mA	32-DIP, 32-SOP 32-TSOP2-F/R
KM684000ALI KM684000ALI-L	Industrial(-40~85°C)	4.5~5.5	70ns	100µA 50µA		32-SOP 32-TSOP2-F/R

PIN DESCRIPTION



Pin Name	Function
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
A0~A18	Address Inputs
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power
Vss	Ground

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Commercial Temperature Products(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	Function	Part Name	Function
KM684000ALP-5	32-DIP, 55ns, L-pwr	KM684000ALGI-7	32-SOP, 70ns, L-pwr
KM684000ALP-5L	32-DIP, 55ns, LL-pwr	KM684000ALGI-7L	32-SOP, 70ns, LL-pwr
KM684000ALP-7	32-DIP, 70ns, L-pwr	KM684000ALTI-7L	32-TSOP2-F, 70ns, LL-pwr
KM684000ALP-7L	32-DIP, 70ns, LL-pwr	KM684000ALRI-7L	32-TSOP2-R, 70ns, LL-pwr
KM684000ALG-5	32-SOP, 55ns, L-pwr		
KM684000ALG-5L	32-SOP, 55ns, LL-pwr		
KM684000ALG-7	32-SOP, 70ns, L-pwr		
KM684000ALG-7L	32-SOP, 70ns, LL-pwr		
KM684000ALT-5L	32-TSOP2-F, 55ns, LL-pwr		
KM684000ALT-7L	32-TSOP2-F, 70ns, LL-pwr		
KM684000ALR-5L	32-TSOP2-R, 55ns, LL-pwr		
KM684000ALR-7L	32-TSOP2-R, 70ns, LL-pwr		

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O Pin	Mode	Power
H	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
L	H	H	High-Z	Output disbaled	Active
L	L	H	Dout	Read	Active
L	X ¹⁾	L	Din	Write	Active

1. X means don't care.(Must be high or low state.)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	V _{CC}	-0.5 to 7.0	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	0 to 70	°C	KM684000AL/L-L
		-40 to 85	°C	KM684000ALI/LI-L
Soldering temperature and time	T _{SOLDER}	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.2	-	V _{CC} +0.5V ²⁾	V
Input low voltage	V _{IL}	-0.5 ³⁾	-	0.8	V

Note:

1. Commercial Product : T_A=0 to 70°C, otherwise specifiedIndustrial Product : T_A=-40 to 85°C, otherwise specified2. Overshoot : V_{CC}+3.0V in case of pulse width ≤ 30ns

3. Undershoot : -3.0V in case of pulse width ≤ 30ns

4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾(f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA
Output leakage current	I _{LO}	$\overline{CS}$ =V _{IH} or $\overline{OE}$ =V _{IH} or $\overline{WE}$ =V _{IL} , V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA
Operating power supply current	I _{CC}	I _{IO} =0mA, $\overline{CS}$ =V _{IL} , V _{IN} =V _{IL} or V _{IH} , Read	-	-	15	mA
Average operating current	I _{CC1}	Cycle time=1μs, 100% duty, I _{IO} =0mA $\overline{CS}$ ≤0.2V, V _{IN} ≥0.2V or V _{IN} ≥V _{CC} -0.2V	Read	-	15	mA
			Write	-	35	
	I _{CC2}	Cycle time=Min, 100% duty, I _{IO} =0mA, $\overline{CS}$ =V _{IL} , V _{IN} =V _{IH} or V _{IL}	-	-	90	mA
Output low voltage	V _{OL}	I _{OL} =2.1mA	-	-	0.4	V
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.4	-	-	V
Standby Current(TTL)	I _{SB}	$\overline{CS}$ =V _{IH} , Other inputs=V _{IL} or V _{IH}	-	-	3	mA
Standby Current(CMOS)	I _{SB1}	$\overline{CS}$ ≥V _{CC} -0.2V, Other inputs=0~V _{CC}	KM684000AL	-	100	μA
			KM684000AL-L	-	20	μA
			KM684000ALI	-	100	μA
			KM684000ALI-L	-	50	μA

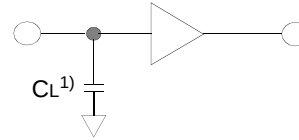
AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level : 0.8 to 2.4V

Input rising and falling time : 5ns

Input and output reference voltage : 1.5V

Output load (See right) : $C_L = 100\text{pF} + 1\text{TTL}$ 

1. Including scope and jig capacitance

AC CHARACTERISTICS ($V_{CC} = 4.5 \sim 5.5\text{V}$, KM684000A Family: $T_A = 0$ to 70°C , KM684000AI Family: $T_A = -40$ to 85°C)

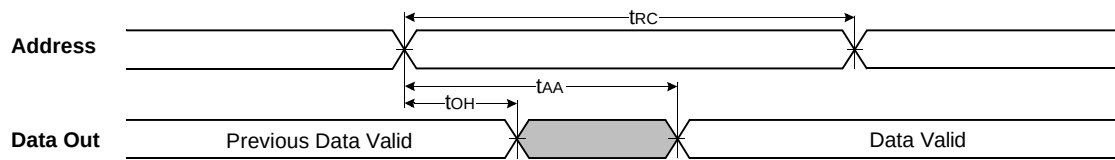
Parameter List		Symbol	Speed Bins				Units
			55ns		70ns		
			Min	Max	Min	Max	
Read	Read cycle time	t _{RC}	55	-	70	-	ns
	Address access time	t _{AA}	-	55	-	70	ns
	Chip select to output	t _{CO}	-	55	-	70	ns
	Output enable to valid output	t _{OE}	-	25	-	35	ns
	Chip select to low-Z output	t _{LZ}	10	-	10	-	ns
	Output enable to low-Z output	t _{OLZ}	5	-	5	-	ns
	Chip disable to high-Z output	t _{HZ}	0	20	0	25	ns
	Output disable to high-Z output	t _{OHZ}	0	20	0	25	ns
	Output hold from address change	t _{OH}	10	-	10	-	ns
Write	Write cycle time	t _{WC}	55	-	70	-	ns
	Chip select to end of write	t _{CW}	45	-	60	-	ns
	Address set-up time	t _{AS}	0	-	0	-	ns
	Address valid to end of write	t _{AW}	45	-	60	-	ns
	Write pulse width	t _{WP}	40	-	50	-	ns
	Write recovery time	t _{WR}	0	-	0	-	ns
	Write to output high-Z	t _{WHZ}	0	20	0	25	ns
	Data to write time overlap	t _{DW}	25	-	30	-	ns
	Data hold from write time	t _{DH}	0	-	0	-	ns
	End write to output low-Z	t _{OW}	5	-	5	-	ns

DATA RETENTION CHARACTERISTICS

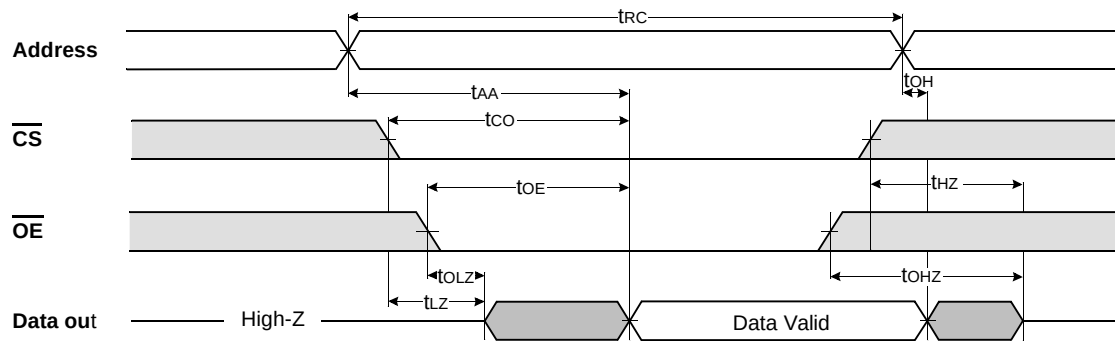
Item	Symbol	Test Condition	Min	Typ	Max	Unit
V _{CC} for data retention	V _{DR}	$\overline{CS} \geq V_{CC} - 0.2\text{V}$	2.0	-	5.5	V
Data retention current	I _{DR}	$V_{CC} = 3.0\text{V}, \overline{CS} \geq V_{CC} - 0.2\text{V}$	KM684000AL	-	-	50
			KM684000AL-L	-	-	15
			KM684000ALI	-	-	50
			KM684000ALI-L	-	-	20
Data retention set-up time	t _{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t _{RDR}		5	-	-	

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$)



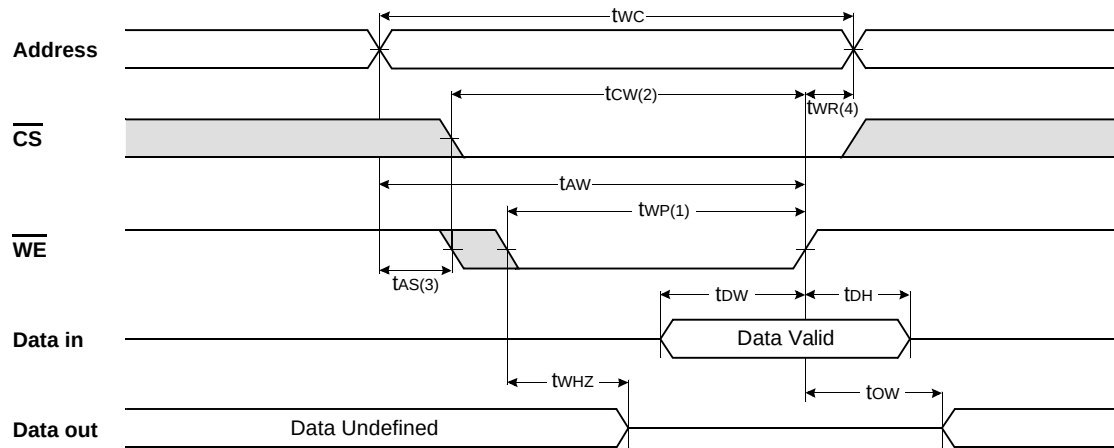
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



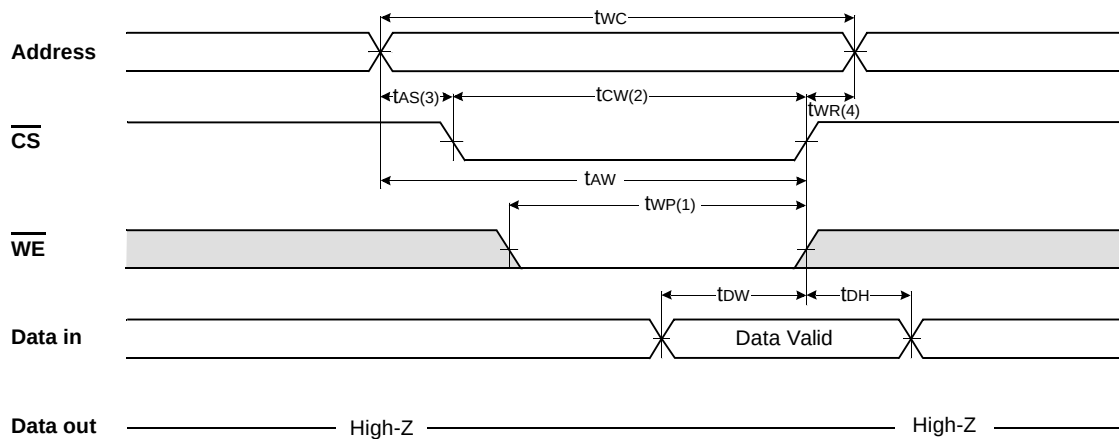
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)

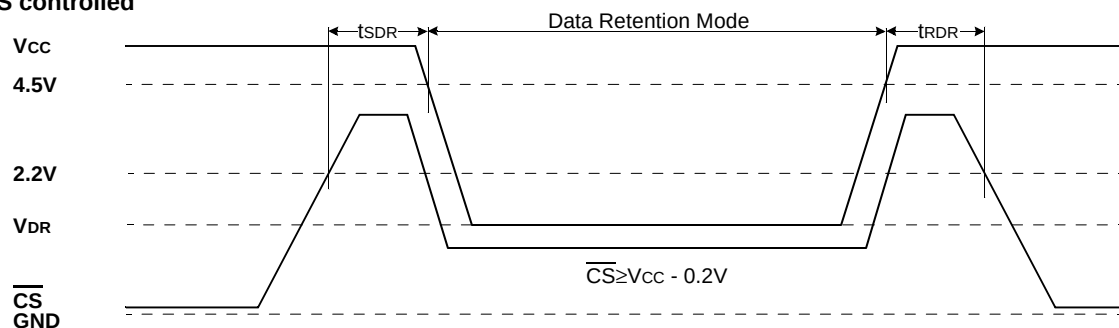


NOTES (WRITE CYCLE)

1. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going Low and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

DATA RETENTION WAVE FORM

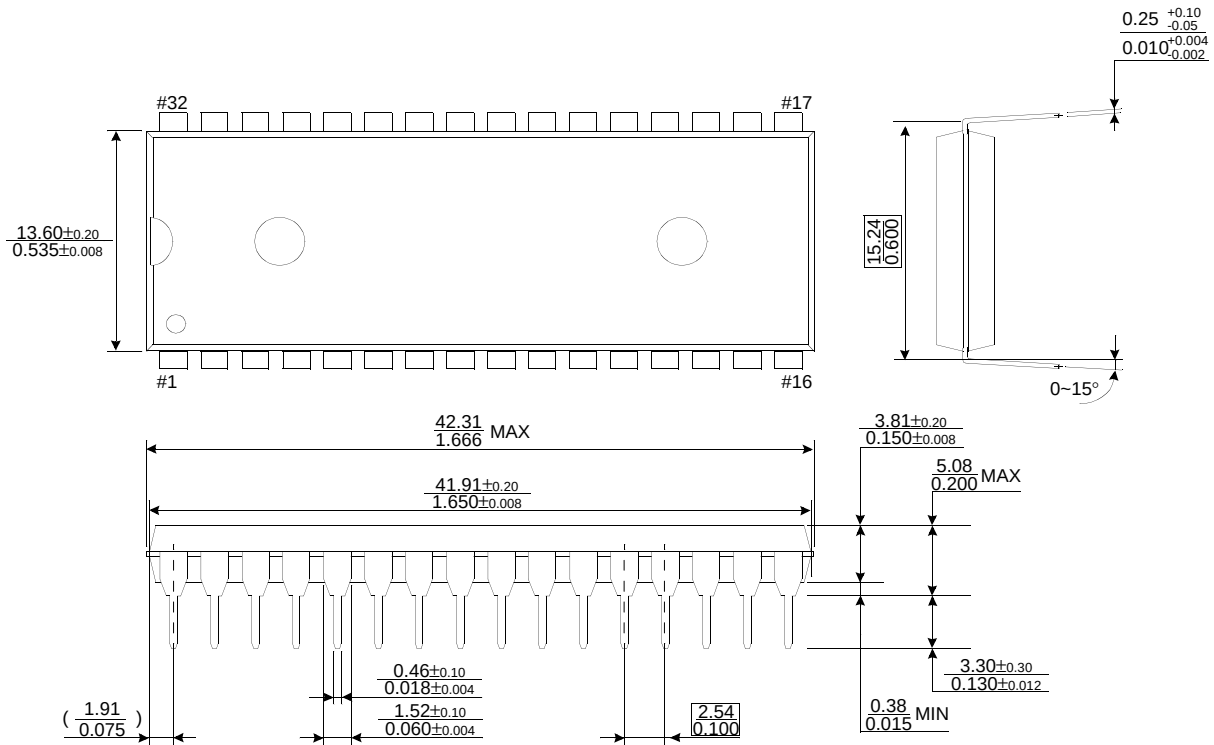
$\overline{CS}$ controlled



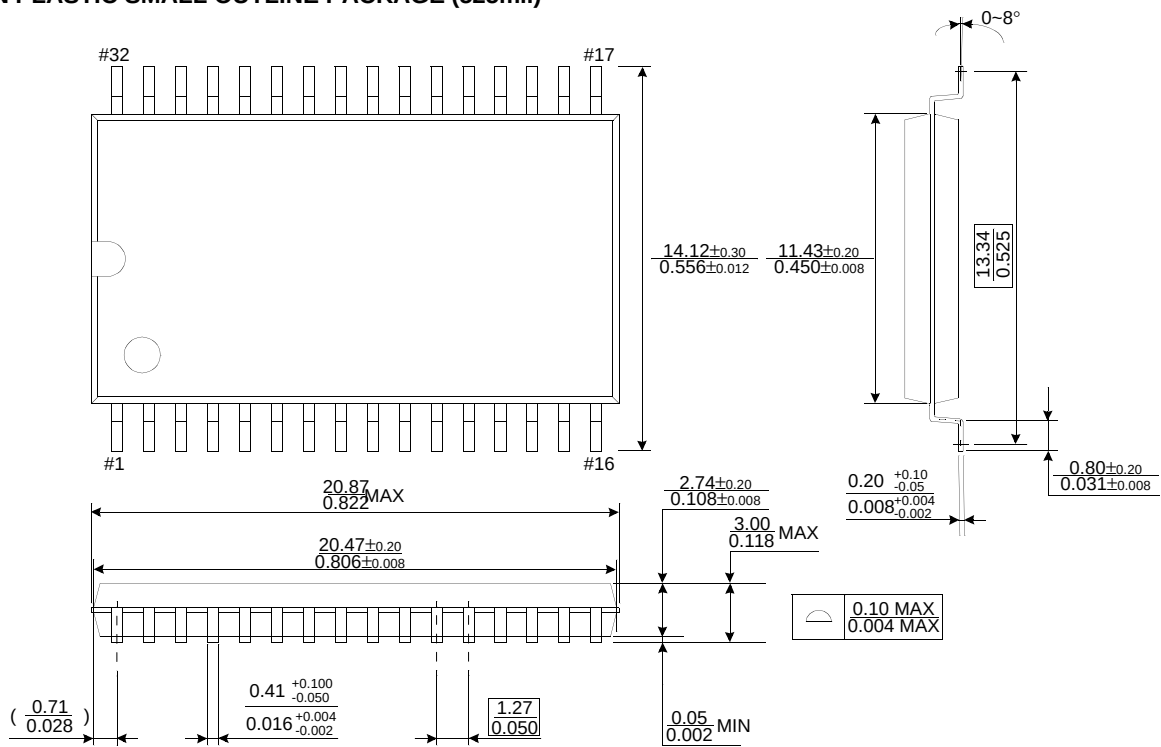
PACKAGE DIMENSIONS

Units : millimeter(inch)

32 PIN DUAL INLINE PACKAGE (600mil)



32 PIN PLASTIC SMALL OUTLINE PACKAGE (525mil)



Units : millimeter(inch)

Top View Dimensions:

- Overall Length: 21.35 MAX
- Overall Width: 11.76 ± 0.20
- Pin Pitch: 0.039 ± 0.004
- Pin Diameter: 0.25 ± 0.010
- Pin Numbering: #1 to #32

Side View Dimensions:

- Overall Height: 10.16 ± 0.400
- Pin Height: $0.45 \sim 0.75$
- Pin Angle: $0 \sim 8^\circ$
- Pin Spacing: $0.018 \sim 0.030$
- Pin Diameter: 0.25 ± 0.010
- Pin Numbering: #1 to #32

PIN THIN SMALL OUTLINE PACKAGE TYPE II (40R)

The drawing illustrates the mechanical specifications for a Pin Thin Small Outline Package Type II (40R). It includes a top view, a side view, and a detail view of the pin profile.

Top View Dimensions:

- Overall width: 21.35 ± 0.841 MAX
- Width of the body: 10.16 ± 0.400
- Width of the pin area: 10.16 ± 0.400
- Pin pitch: 0.50 ± 0.020
- Pin width: 0.15 ± 0.10 / -0.05 / $+0.004$ / -0.002
- Pin thickness: 0.006 ± 0.002
- Pin length: 1.27 ± 0.050
- Pin diameter: 0.05 ± 0.002 MIN

Side View Dimensions:

- Overall height: 11.76 ± 0.20 / 0.463 ± 0.008
- Body height: 10.16 ± 0.400
- Pin height: 1.27 ± 0.050
- Pin thickness: 0.05 ± 0.002 MIN

Detail View Dimensions:

- Pin diameter: 0.10 ± 0.004 MAX
- Pin thickness: 0.004 ± 0.002 MAX