Analog input and output modules

Data sheets

Version: **1.10 (March 2024)**
Order no.: **Analog input and output modules**

Translation of the original documentation

Publishing information

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Analog input modules

Data sheets

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1.1 X20(c)AI1744

This data sheet describes 2 module revisions. The module revision is laser-marked on the side of the module. Select the desired module revision from the following table to view its description.

Module	Revision	Page
X20AI1744	≥H0	4
X20cAI1744	All	
X20AI1744	<H0	35

1.1.1 X20AI1744 with Rev. ≥H0

1.1.1.1 General information

This module works with both 4-wire and 6-wire strain gauge load cells. The concept applied by the module requires compensation in the measurement system. This compensation eliminates the absolute uncertainty in the measurement circuit, such as component tolerances, effective bridge voltage or zero point offset. The measurement precision refers to the absolute (compensated) value, which will only change as a result of changes in the operating temperature.

- 1 full-bridge strain gauge input
- Data output rate configurable from 0.1 Hz to 7.5 kHz
- Special operating modes (synchronous mode and multiple sampling)
- Configurable filter level

1.1.1.1.1 Other applicable documents

For additional and supplementary information, see the following documents.

Other applicable documents

Document name	Title
MAX20	X20 System user's manual
MAEMV	Installation / EMC guide

1.1.1.2 Order data

Order number	Short description	Figure
	Analog inputs	
X20AI1744	X20 analog input module, 1 full-bridge strain gauge input, 24-bit converter resolution, 5 kHz input filter	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 1: X20AI1744 - Order data

1.1.1.3 Technical description

1.1.1.3.1 Technical data

Order number	X20AI1744
Short description	
I/O module	1 full-bridge strain gauge input
General information	
B&R ID code	0x1CDE
Status indicators	Channel status, operating state, module status

Table 2: X20AI1744 - Technical data

Order number	X20AI1744
Diagnostics	
Module run/error	Yes, using LED status indicator and software
Open circuit	Yes, using LED status indicator and software
Input	Yes, using LED status indicator and software
Power consumption	
Bus	0.01 W
Internal I/O	0.5 W
Additional power dissipation caused by actuators (resistive) [W]	Max. +0.36 [1]
Certifications	
CE	Yes
UKCA	Yes
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
EAC	Yes
KC	Yes
Full-bridge strain gauge	
Strain gauge factor	2 to 256 mV/V, configurable using software
Connection	4- or 6-wire connections [2]
Input type	Differential, used to evaluate a full-bridge strain gauge
Digital converter resolution	24-bit
Conversion time	Depends on the configured data output rate
Data output rate	0.1 - 7500 samples per second, configurable using software (f_{DATA})
Input filter	
Cutoff frequency	5 kHz
Order	3
Slope	60 dB
ADC filter characteristics	Sigma-delta, see section "Filter characteristics of the sigma-delta A/D converter"
Operating range / Measurement sensor	85 to 5000 Ω
Influence of cable length [3]	See section "Calculation example".
Input protection	RC protection
Common-mode range	0 to 3 VDC Permissible input voltage range (with regard to the electric potential strain gauge GND) on inputs "Input +" and "Input -"
Insulation voltage between input and bus	500 V_{eff}
Conversion procedure	Sigma-delta
Output of digital value	
Broken bridge supply line	Value approaching 0
Broken sensor line	Value approaching ±end value (status bit "Line monitoring" is set in register "Module status")
Valid range of values	0xFF800001 to 0x007FFFFF (-8,388,607 to 8,388,607)
Strain gauge supply	
Voltage	5.5 VDC / Max. 65 mA
Short-circuit and overload-proof	Yes
Voltage drop for short-circuit protection	Max. 0.2 VDC at 65 mA and 25°C
Quantization [4]	
LSB value (16-bit)	
2 mV/V	336 nV
4 mV/V	671 nV
8 mV/V	1.343 µV
16 mV/V	2.686 µV
32 mV/V	5.371 µV
64 mV/V	10.74 µV
128 mV/V	21.48 µV
256 mV/V	42.97 µV
LSB value (24-bit)	
2 mV/V	1.31 nV
4 mV/V	2.62 nV
8 mV/V	5.25 nV
16 mV/V	10.49 nV
32 mV/V	20.98 nV
64 mV/V	41.96 nV
128 mV/V	83.92 nV
256 mV/V	167.85 nV
Temperature coefficient	
Rev. ≥E0	10 ppm/°C
Rev. <E0	30 ppm/°C
Max. gain drift	12 ppm/°C [5]

Table 2: X20AI1744 - Technical data

Order number	X20AI1744
Max. offset drift	2 ppm/°C [6]
Nonlinearity	<10 ppm [6]
Electrical properties	
Electrical isolation	Bus isolated from analog input and strain gauge supply voltage Channel not isolated from I/O power supply
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	See section "Hardware configuration"
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x terminal block X20TB12 separately. Order 1x bus module X20BM11 separately.
Pitch	12.5$^{+0.2}$ mm

Table 2: X20AI1744 - Technical data

1) Depends on the full-bridge strain gauge being used.
2) With 6-wire connections, line compensation does not function (see section "Connection examples").
3) Sensor cable with twisted and shielded conductors, cable length as short as possible, cable routing separate from load circuits, without intermediate terminal to the sensor.
4) Quantization depends on the strain gauge factor.
5) Based on the current measured value.
6) Based on the entire measurement range.

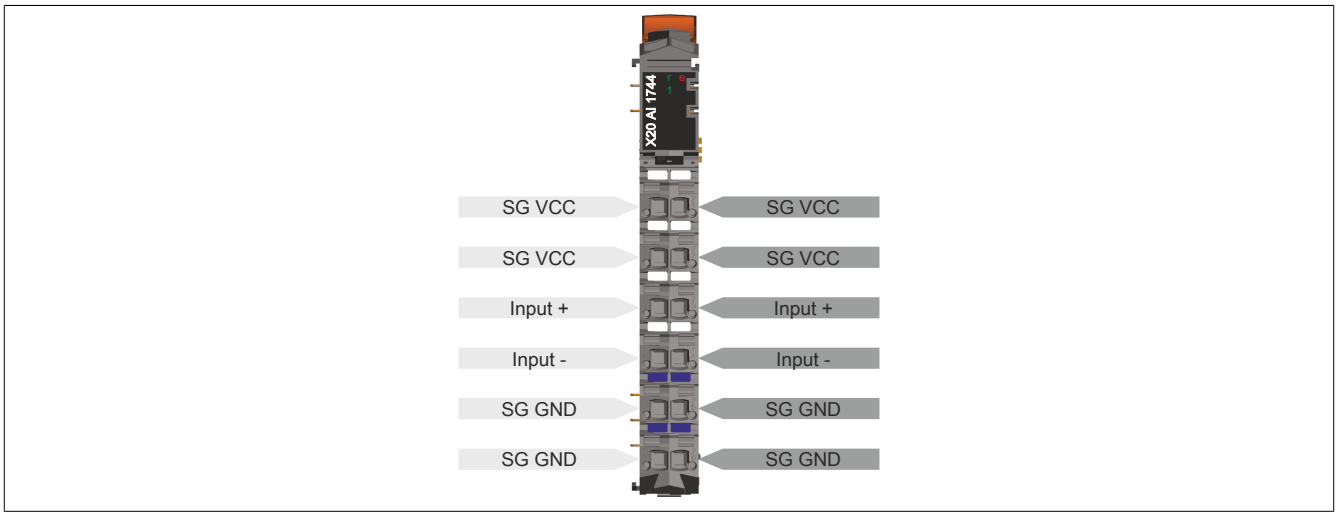
1.1.1.3.2 LED status indicators

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 System user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	1	Green	Off	Possible causes: • Open circuit • Sensor is disconnected • Converter is busy
			On	Analog/digital converter running, value OK

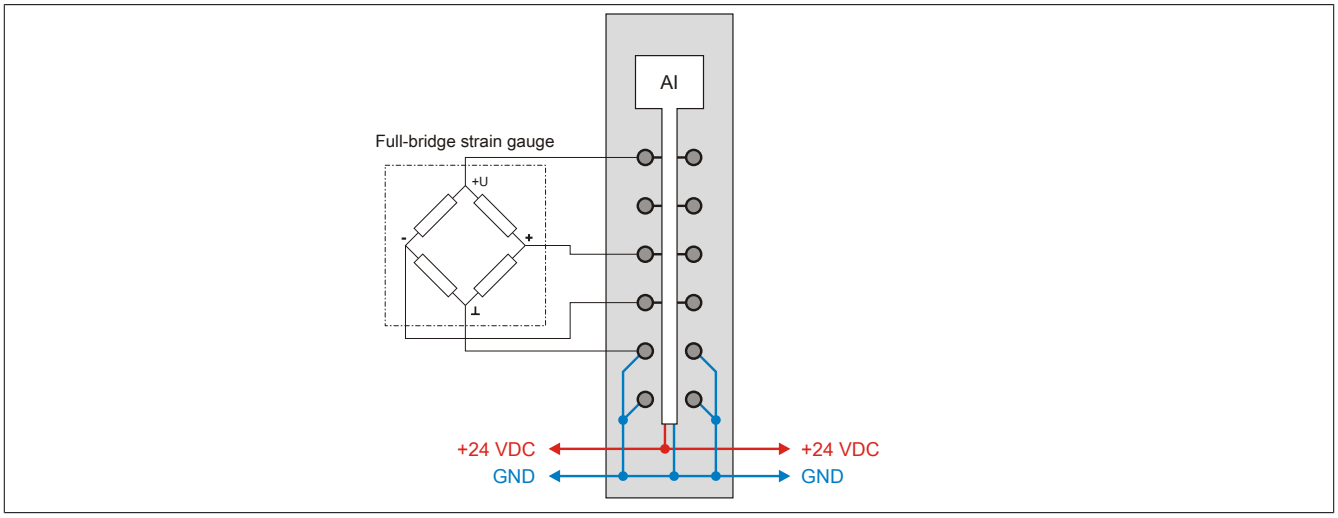
1) Depending on the configuration, a firmware update can take up to several minutes.

1.1.1.3.3 Pinout



1.1.1.3.4 Connection examples

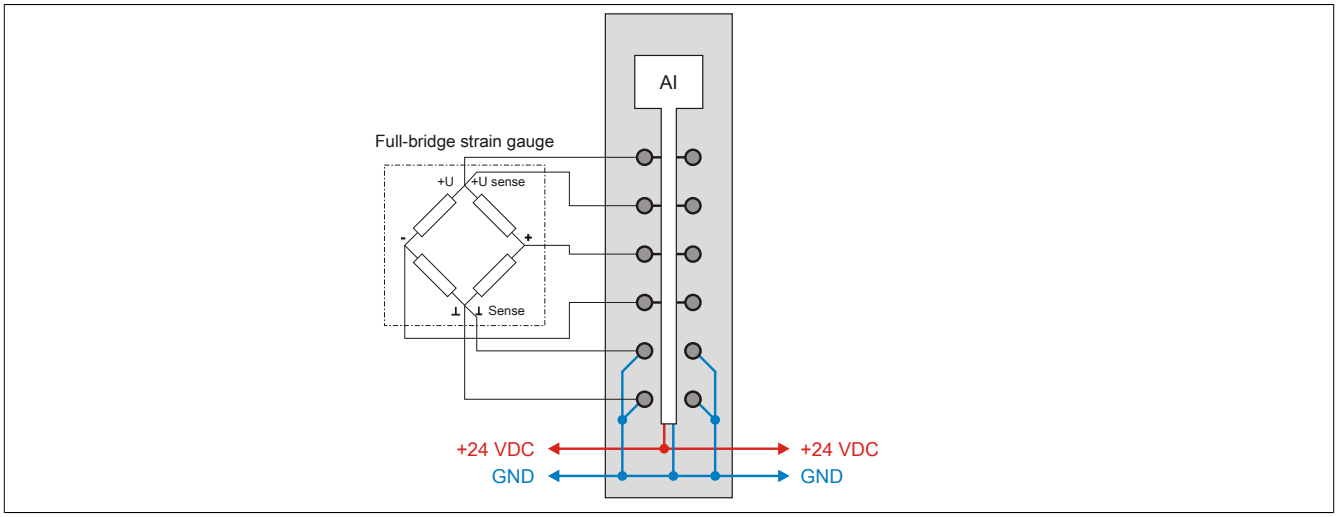
Full-bridge strain gauge with 4-wire connections



Full-bridge strain gauge with 6-wire connections

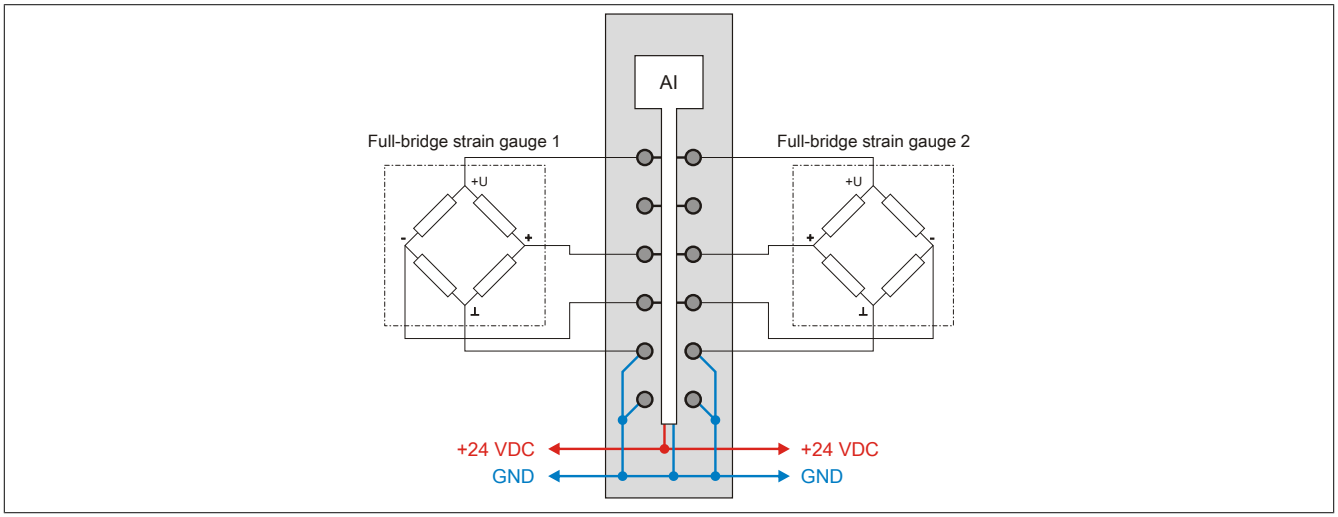
Full-bridge strain gauges can be connected to this module with 6-wire connections. Line compensation is not supported by the module, however. The sense lines are short circuited by the internally connected strain gauge VCC and GND connections (see "Input circuit diagram" on page 9). The measurement precision is therefore affected by changes in operating temperature. Longer cable lengths and smaller cable cross sections also increase the potential for errors in the measurement system.

In order to reduce cable resistance, the sense lines should be connected in parallel with the strain gauge supply lines. Optimal signal quality can be obtained by using a shielded twisted pair cable. The connections for the strain gauge supply lines, the sensor lines and the bridge differential voltage lines should each use one twisted pair cable.



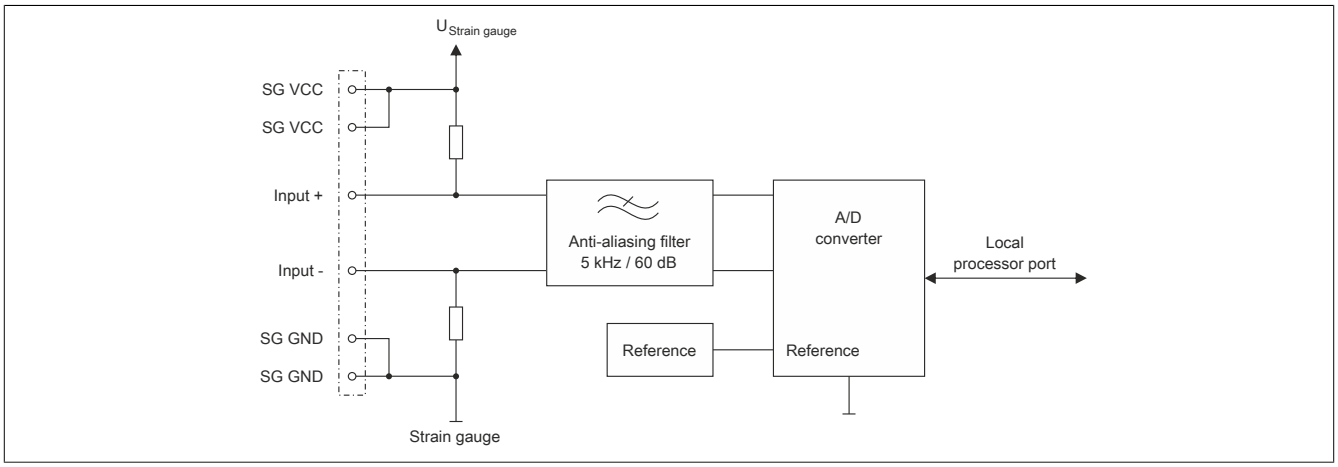
Parallel connection of 2 full-bridge strain gauges (4-wire connections)

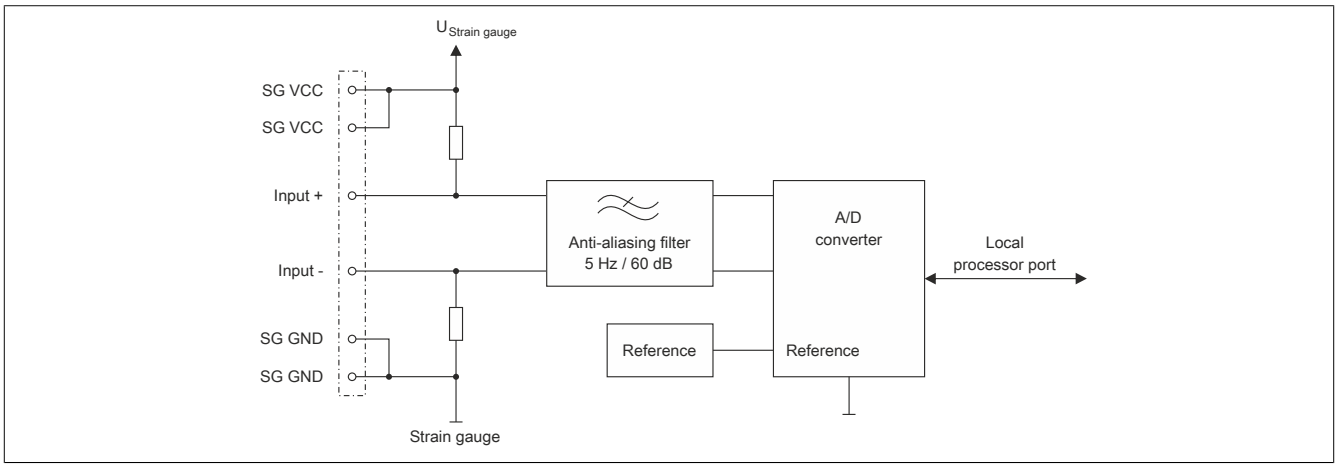
If connecting the full-bridge strain gauges in parallel, the manufacturer's guidelines must be observed.



When connecting 3 or more full-bridge strain gauges in parallel, 2 lines must be connected together in an X20 terminal block.

1.1.1.3.5 Input circuit diagram



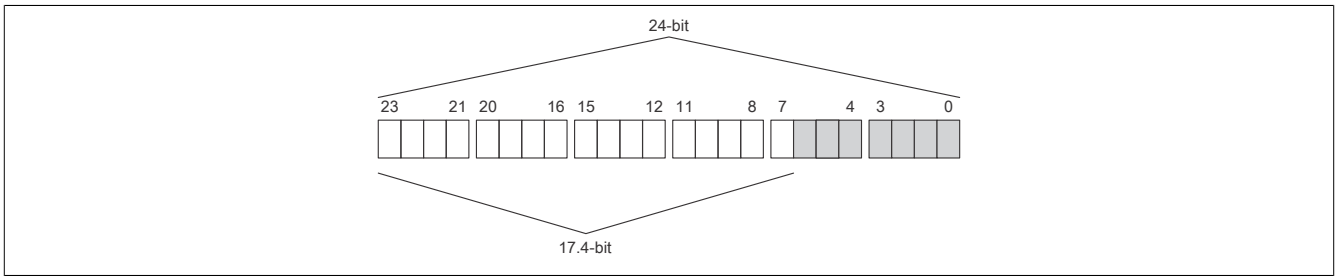


1.1.1.3.6 Effective resolution of the A/D converter

The A/D converter on the module provides a 24-bit measured value. The actual attainable noise-free resolution is always less than 24-bit, however. This "effective resolution" depends on the data rate and measurement range.

Example:

Based on the conversion method, a data rate of 2.5 Hz and a specified measurement range of 2 mV/V result in an effective resolution of17.4 bits:



The low-order bits (grayed out) contain only noise instead of valid values and are therefore not permitted to be evaluated.

With "Function model 1 - Multisampling", only the highest 16 bits are made available.

1.1.1.3.7 Bridge voltage and quantization

The following example shows the influence of the length of the measuring cable on the bridge voltage of the module and the quantization calculated with it.

1.1.1.3.7.1 Bridge voltage

Although the measuring bridge must be adjusted with the module, the line length has an influence on the accuracy of the measurement. The reason for this is the voltage drop on the power supply lines of the measuring bridge. As a result, the bridge supply voltage at the measuring bridge is no longer the full 5.5 V. The reduced bridge voltage also affects the quantization.

Example

Characteristics of the measuring device used:

- Full-bridge strain gauge with 4-wire connection
- Material-dependent conductivity of the line (copper: $12 \frac{m}{\Omega \cdot mm^2}$)
- Cross section of the line: 22 AWG = 0.34 mm²
- Length of the line: 5 m
- Nominal current of the measuring bridge: 15 mA
- Bridge voltage of the module: 5.5 V

Actual bridge voltage taking the voltage drop on the measuring line into account:

$$5.5V - \frac{2 \cdot 5\,m}{12 \frac{m}{\Omega \cdot mm^2} \cdot 0.34\,mm^2} \cdot 0.015A = 5.463\ V$$

The quantization must be calculated using the actual calculated bridge voltage (see "Quantization" on page 11).

1.1.1.3.7.2 Quantization

In a weighing application, the corresponding weight located on the connected load cell should be determined from the value derived from the module.

Example

The characteristics of the strain gauge load cell are as follows:

- Rated load: 1000 kg
- Strain gauge factor: 4 mV/V
- Actual bridge voltage: 5.463 V

Maximum quantization:
Multiplying the bridge factor of the strain gauge load cell with the bridge supply voltage from the module results in the value for the positive full-scale deflection at a specified rated load of 1000 kg:

4 mV/V · 5.5 V = 22 mV

Actual quantization:
Taking the voltage drop on the measuring line into account, the actual bridge voltage is 5.463 V (for the calculation, see section "Bridge voltage" on page 10). If this voltage is multiplied by the strain gauge factor of 4 mV/V, the following actual quantization results:

4 mV/V · 5.463 V = 21.85 mV

These 21.85 mVcorrespond to 99.3% of the maximum possible measurement range.

Information:

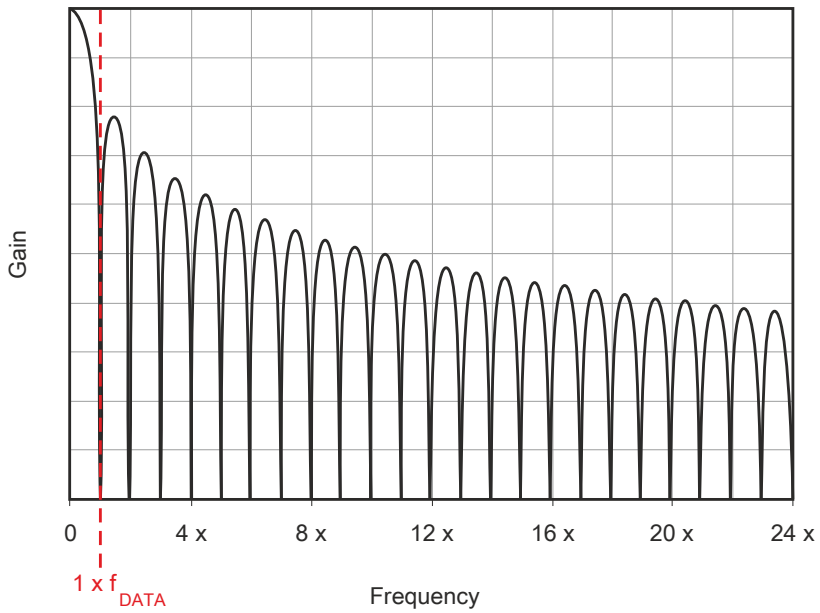
If the quantization decreases, the maximum possible effective resolution also decreases (see "Effective resolution of the A/D converter" on page 9).

With a simple Rule of Three calculation, the corresponding value can be calculated (as seen in the table) from weight to the converter value and vice versa. This simplified theoretical approach is only valid for an ideal measurement system. Calibration of the entire measurement system is recommended because not only the module, but particularly the strain gauge bridges exhibit tolerances (offset, gain). When taring, the gradient offset is recalculated and the gain of the linear equation is determined when normalized. In addition to the calculation displayed in the table, these calculations must also be carried out in the application.

24-bit value of the module		Quantization	Corresponding weight
0x007F FFFF	8,388,607	21.85 mV	1000 kg
0x0000 0001	1	2.61 nV	0.119 g
0x0000 20C3	8387	21.85 µV	1 kg
0x0001 0000	65536	170.7 µV	7.81 kg

The values for 1 LSB are also included in the module's technical data under item "Quantization" (1 LSB each for 16 bits and 24 bits).

1.1.1.3.8 Filter characteristics of the sigma-delta A/D converter

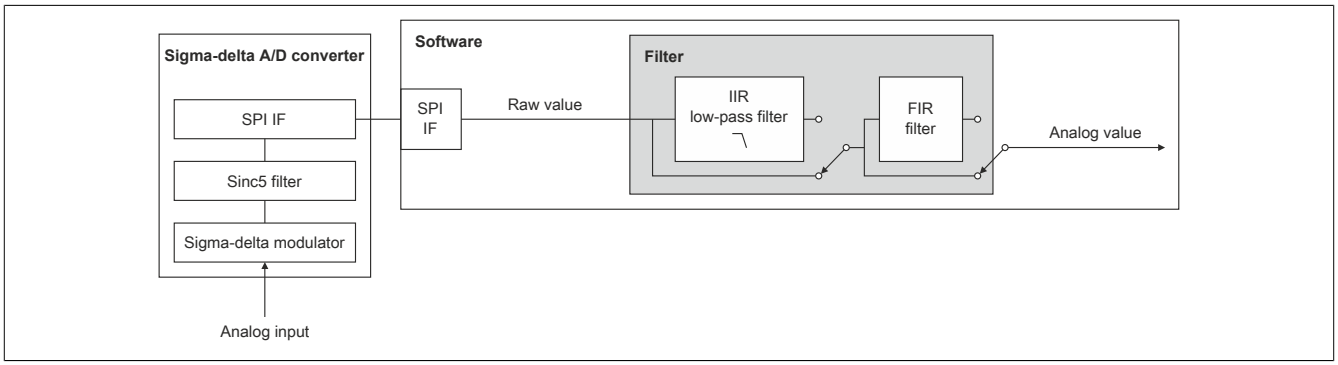


1.1.1.3.9 Software filters

2 filters are available for the analog input. They can be individually enabled and configured at runtime. By default, both filters are disabled when the device is switched on. The filters are controlled and configured using "Function model 2 - Extended filter".

In order to allow the filter behavior to be adapted to the measuring situation or machine cycle (high dynamics and low precision or low dynamics and high precision), the filter characteristics of both the IIR low-pass filter as well as the FIR filter can be changed synchronously at any time.

Filter diagram



1.1.1.3.9.1 IIR low-pass filter

General information

The IIR low-pass filter is used to generally smooth and increase the resolution of the analog value. The filter works according to the following formula:

$$y = y_{Old} + \frac{x - y_{Old}}{2^{Filter\ level}}$$

x ... Current filter input value

y_{Old} ... Old filter output value

y ... New filter output value

Parameter "Filter level" in the formula above is configured using register "ConfigCommonOutput01" on page 32. "Filter level" = 0 if the IIR low-pass filter is disabled.

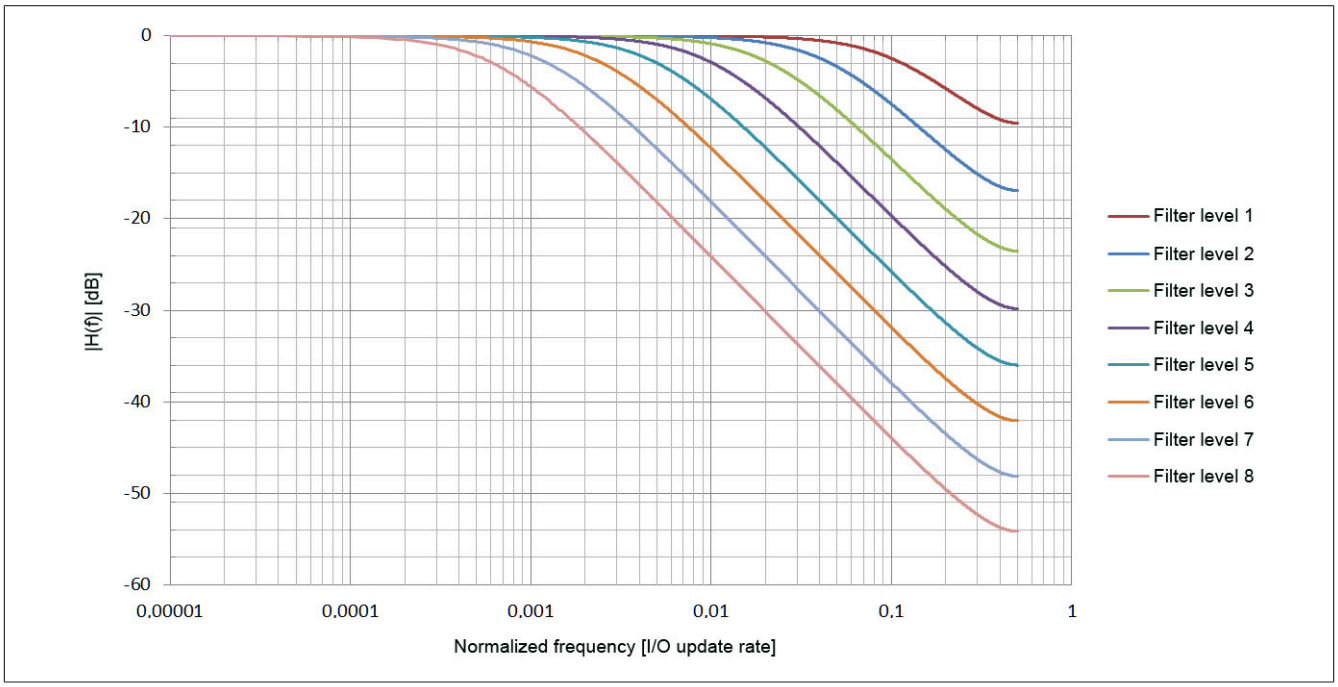
Filter characteristics of the first-order IIR low-pass filter

Limit frequency f_c

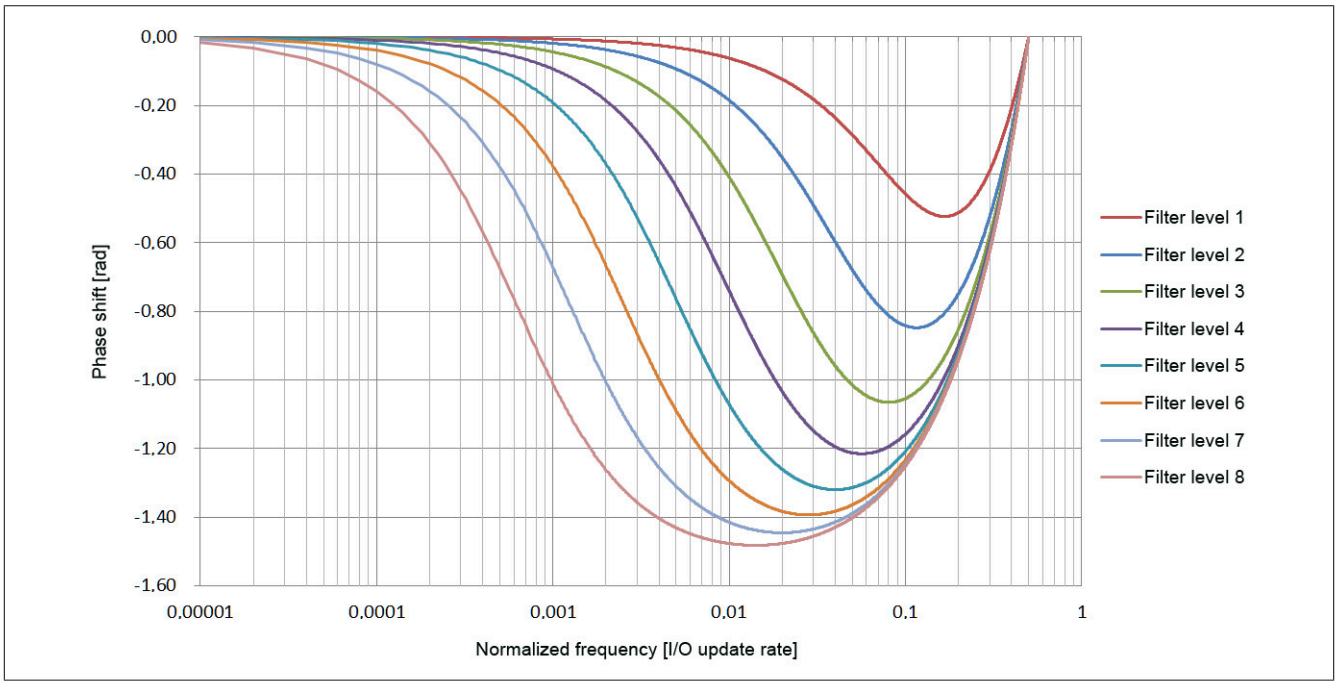
The following table provides an overview of the -3 dB limit frequency f_c depending on the configured filter level.

Filter level	Normalized f_c [I/O update rate]	f_c [Hz] I/O update rate = 15000/s	f_c [Hz] I/O update rate = 20000/s
1	0.11476	1721.4	2295.2
2	0.046	690	920
3	0.02124	318.6	424.8
4	0.01026	153.9	205.2
5	0.00504	75.6	100.8
6	0.0025	37.5	50
7	0.00124	18.6	24.8
8	0.00062	9.3	12.4

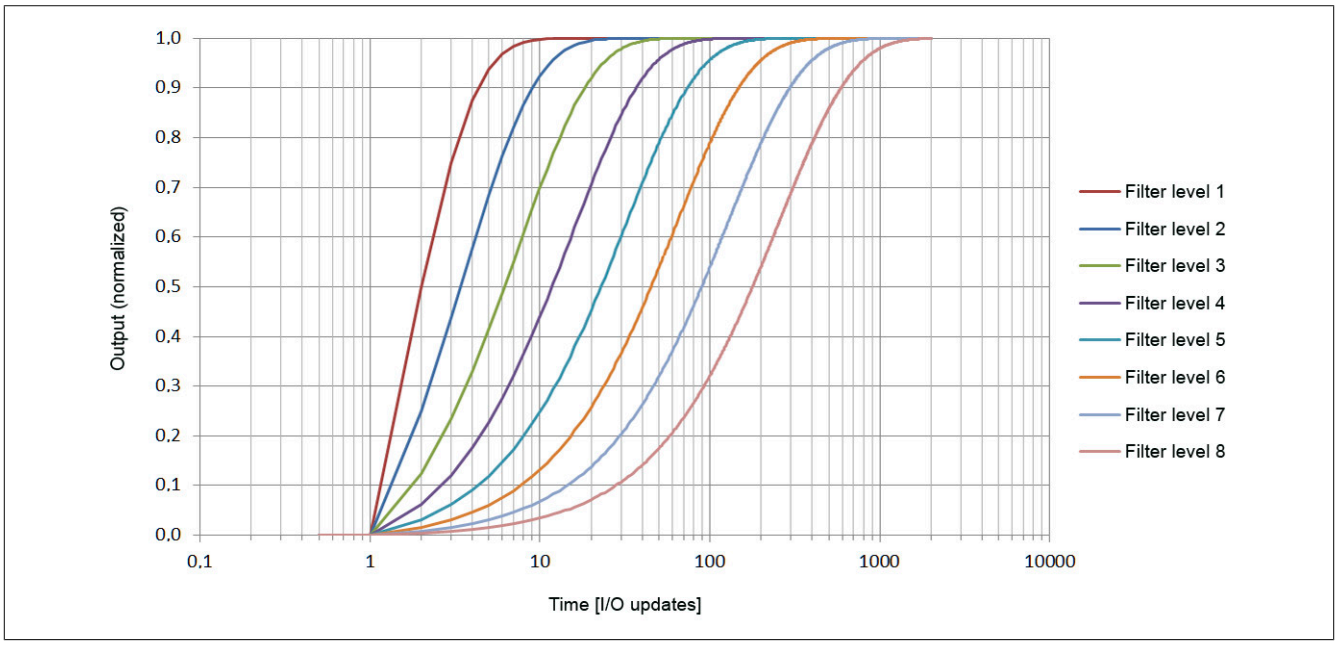
Gain of the IIR low-pass filter



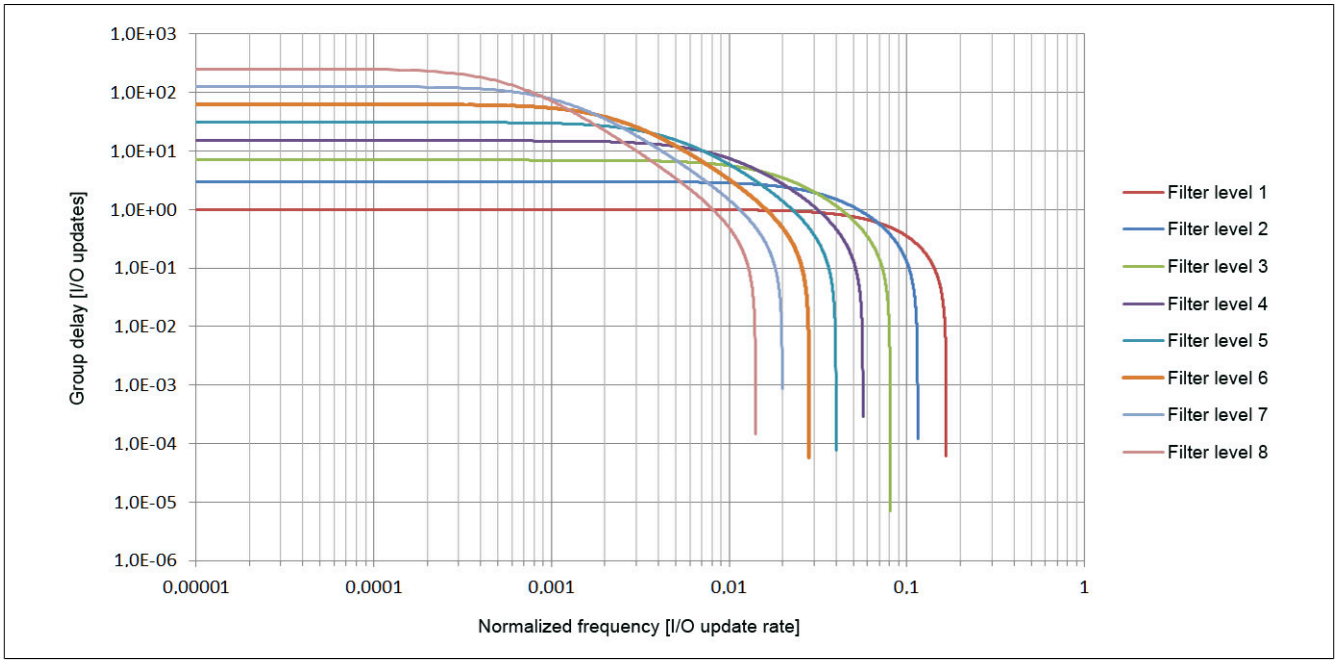
Phase shift of the IIR low-pass filter



Step response of the IIR low-pass filter



Group delay of the IIR low-pass filter



1.1.1.3.9.2 FIR filter

Like the IIR low-pass filter, the FIR filter can also be used to smooth out the signal and increase its resolution. In addition, configuring the filter length accordingly makes it possible to target and efficiently filter out individual interference frequencies. The source of these interference frequencies may be mechanical or electromagnetic. Multiples of these are also filtered out (as long as they are a whole-number factor of the data output rate).

Example:
Data output rate = 15000 samples/s, averaging over 15 values → "Notch" at 1 kHz (2 kHz, etc.)

When reconfiguring the filter, it takes 1/data rate (FIR filter in mode "Selectable data rate") or 1/filter frequency (FIR filter in mode"High-resolution data rate") until the filter is tuned. During tuning, bit 5 is set in register "StatusInput01" on page 33.

Characteristics of the FIR filter in mode "Selectable data rate"

The following table applies to "Function model 0 - Standard" and "Function model 254 - Bus controller" as well as for "Function model 2 - Extended filter" in mode "Selectable data rate".

			I/O update rate [Hz]		I/O update time [ms]	
Set value [1) 2)]	**Data rate (f_{Data}) [Hz]** [3) 4)]	**f_{Notch} [Hz]**	**Function model 0 and 254**	**Function model 2 ("Selectable data rate" mode)**	**Function model 0 and 254**	**Function model 2 ("Selectable data rate" mode)**
0000	2.5	2.5	2.5	15000	400	0.0667
0001	5	5	5	15000	200	0.0667
0010	10	10	10	15000	100	0.0667
0011	15	15	15	15000	66.6667	0.0667
0100	25	25	25	15000	40	0.0667
0101	30	30	30	15000	33.3333	0.0667
0110	50	50	50	15000	20	0.0667
0111	60	60	60	15000	16.6667	0.0667
1000	100	100	100	15000	10	0.0667
1001	500	500	500	15000	2	0.0667
1010	1000	1000	1000	15000	1	0.0667
1011	2000	2000	2000	20000	0.5	0.05
1100	3750	3750	3750	15000	0.2667	0.0667
1101	7500	7500	7500	15000	0.1333	0.0667
1110	Reserved					
1111	Reserved					

1) Function model 0 and 254: Bits 0 to 3 of register "ConfigOutput01" on page 24
2) Function model 2: Bits 0 to 3 of register "ConfigDatarateOutput01" on page 33
3) Function models 0 and 254: Data rate = 1/Filter length [s] (f_{Notch}) = I/O update rate
4) Function model 2: Data rate = 1/Filter length [s] (f_{Notch})

Characteristics of the FIR filter in mode "High-resolution data rate"

The following table applies to "Function model 2 - Extended filter".

Setpoint [0.1 Hz] 1)	Data rate (f_{Data}) [Hz]	f_{Notch} [Hz]	I/O update time [µs]
1 to 65535	Setpoint / 10	= Data rate	≈50 µs 2)

1) Setpoint from register "ConfigHighResolutionOutput01" on page 33
2) The value varies between 42 and 56 µs (see also the next section "I/O update time")

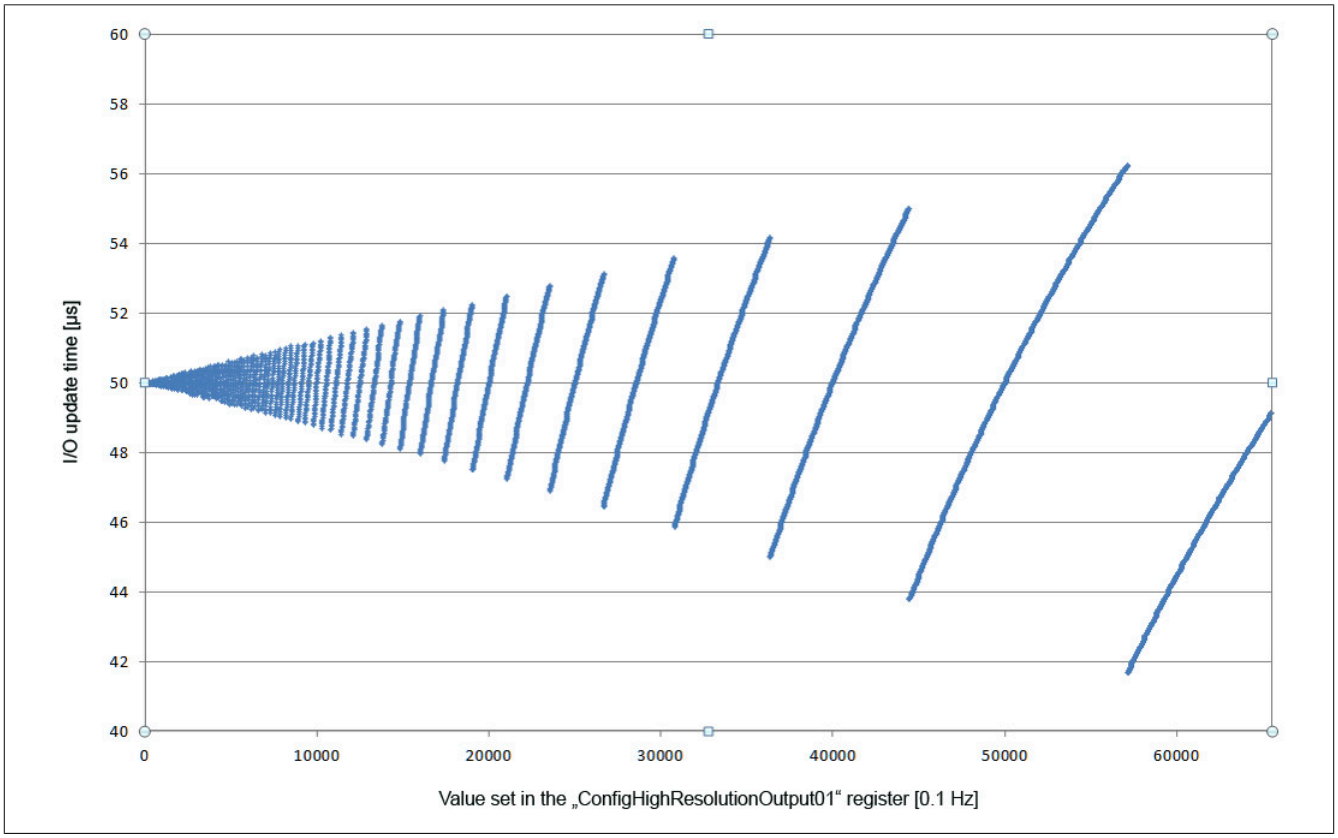
I/O update time

The value of the I/O update time depends on the setpoint and varies between 42 and 56 µs. The following formula can be used to precisely calculate the I/O update time:

I/O update time = 1e6 · (1e-4 - 10 / (Setpoint · [10 / (5e-5 · Setpoint)]))

Legend: The square brackets in the formula above mean that the calculated value must be rounded to a whole number.

The following image shows the I/O update time depending on the setpoint:

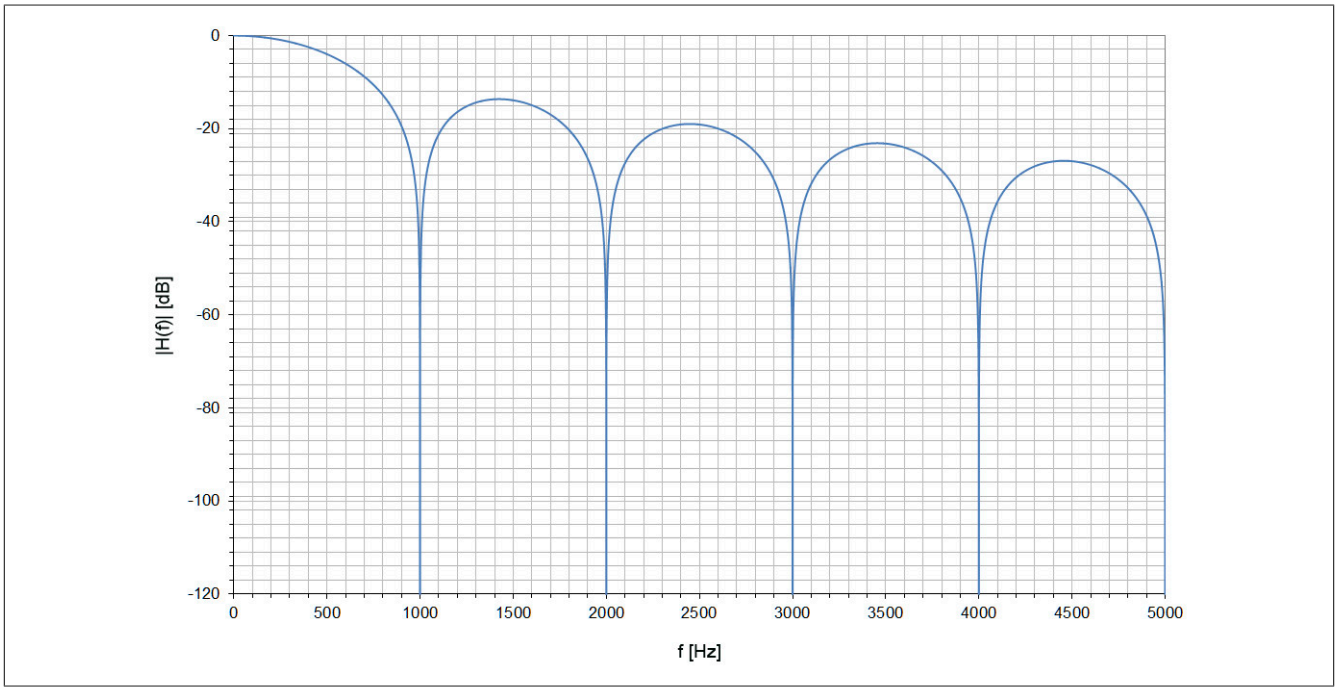


Examples for the gain of the FIR filter

Example 1

Filter setting = 10:

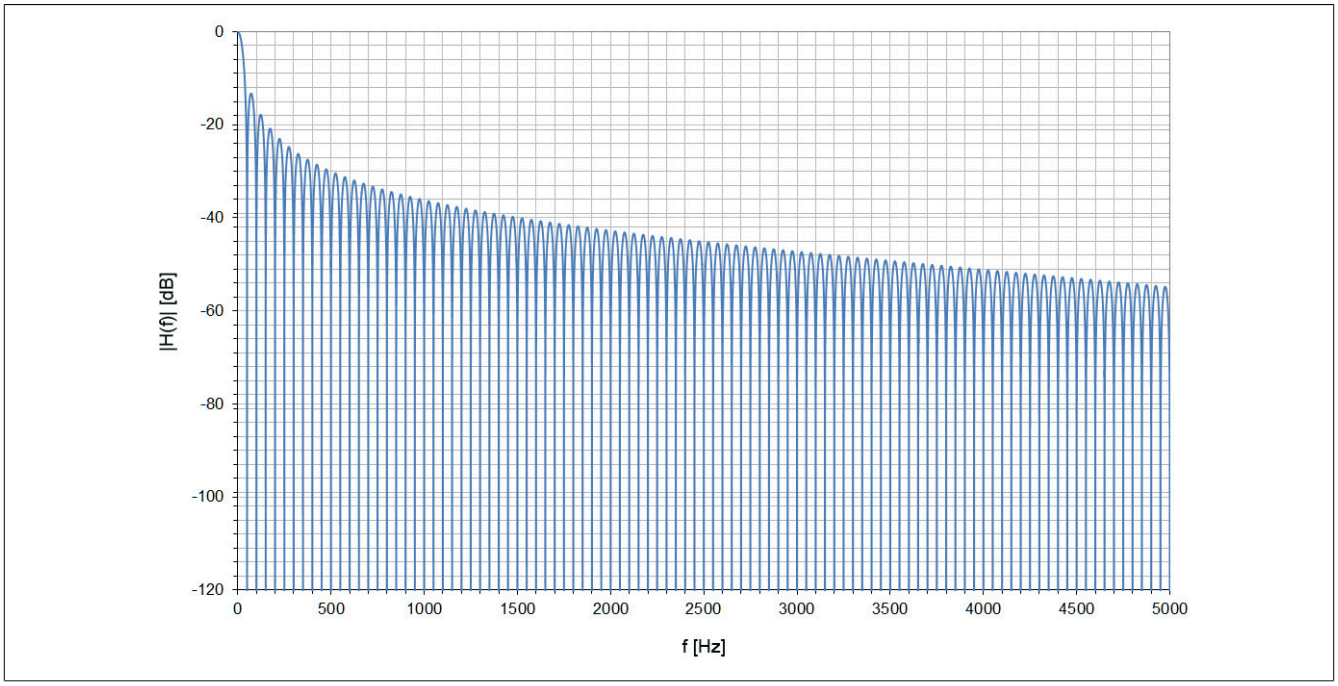
- f_{Notch} = 1000 Hz
- f_c = 439.3 Hz



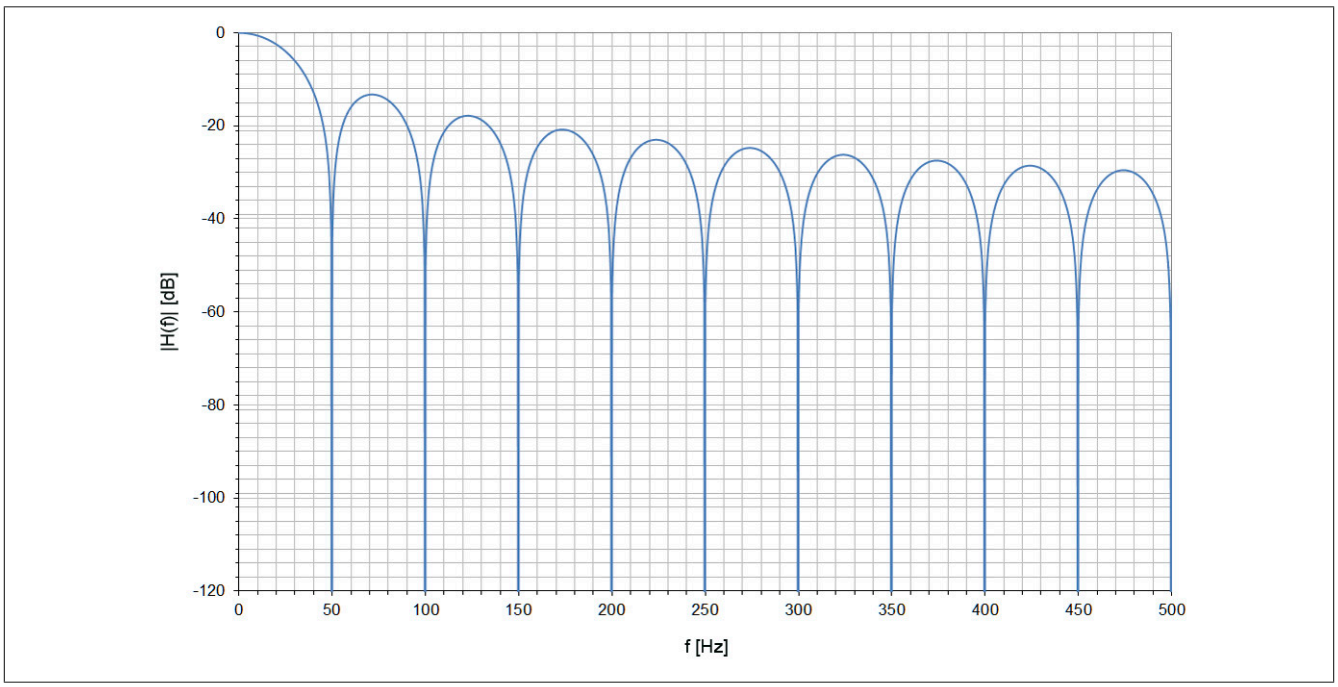
Example 2

Filter setting = 6:

- f_{Notch} = 50 Hz
- f_c = 21.8 Hz



Detailed excerpt from the filter curve shown above:

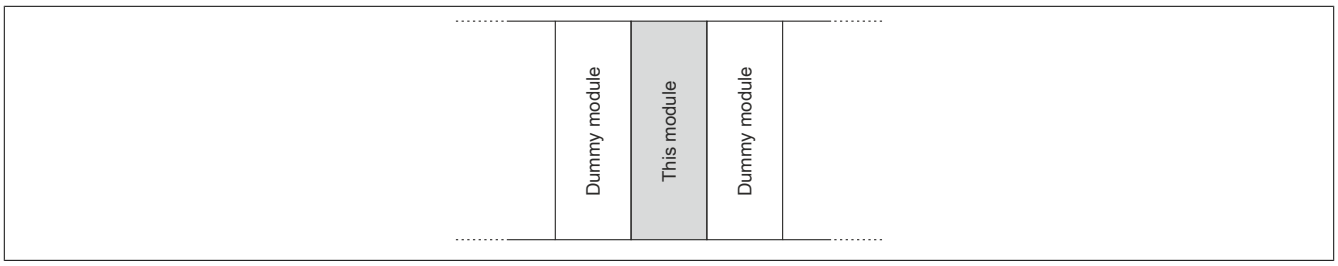


1.1.1.3.10 Hardware configuration

1.1.1.3.10.1 Hardware configuration for horizontal installation starting at 55°C ambient temperature

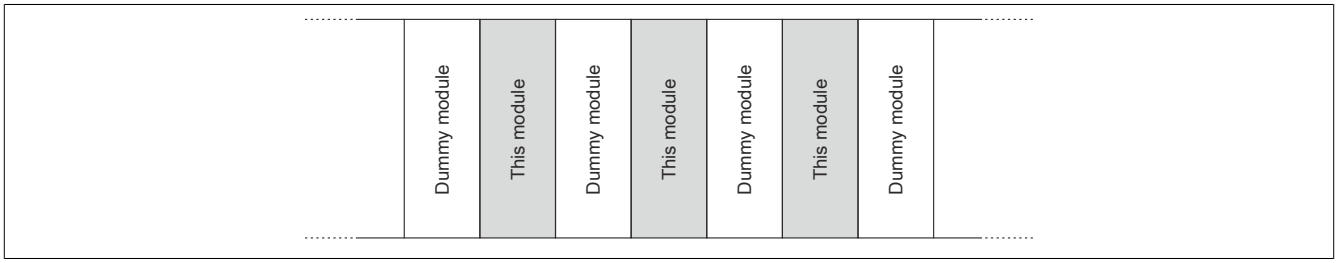
Operating a strain gauge module

Starting at an ambient temperature of 55°C, a dummy module must be connected to the left and right of the strain gauge module in a horizontal mounting orientation.



Operating multiple strain gauge modules side by side

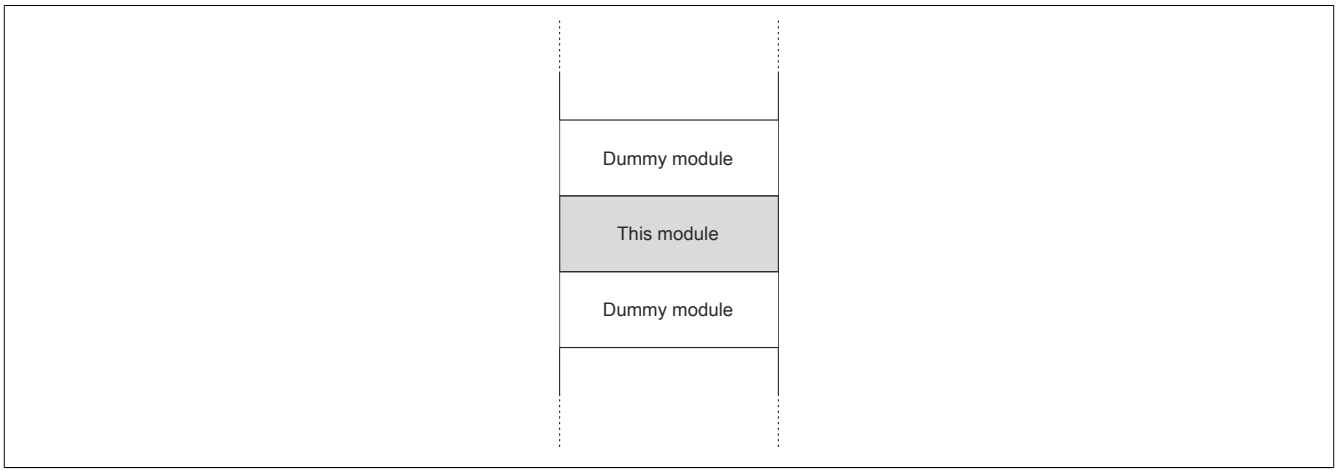
If 2 or more horizontal strain gauge modules are being operated in a cluster, the following arrangement of modules must be observed.



1.1.1.3.10.2 Hardware configuration for vertical installation starting at 45°C ambient temperature

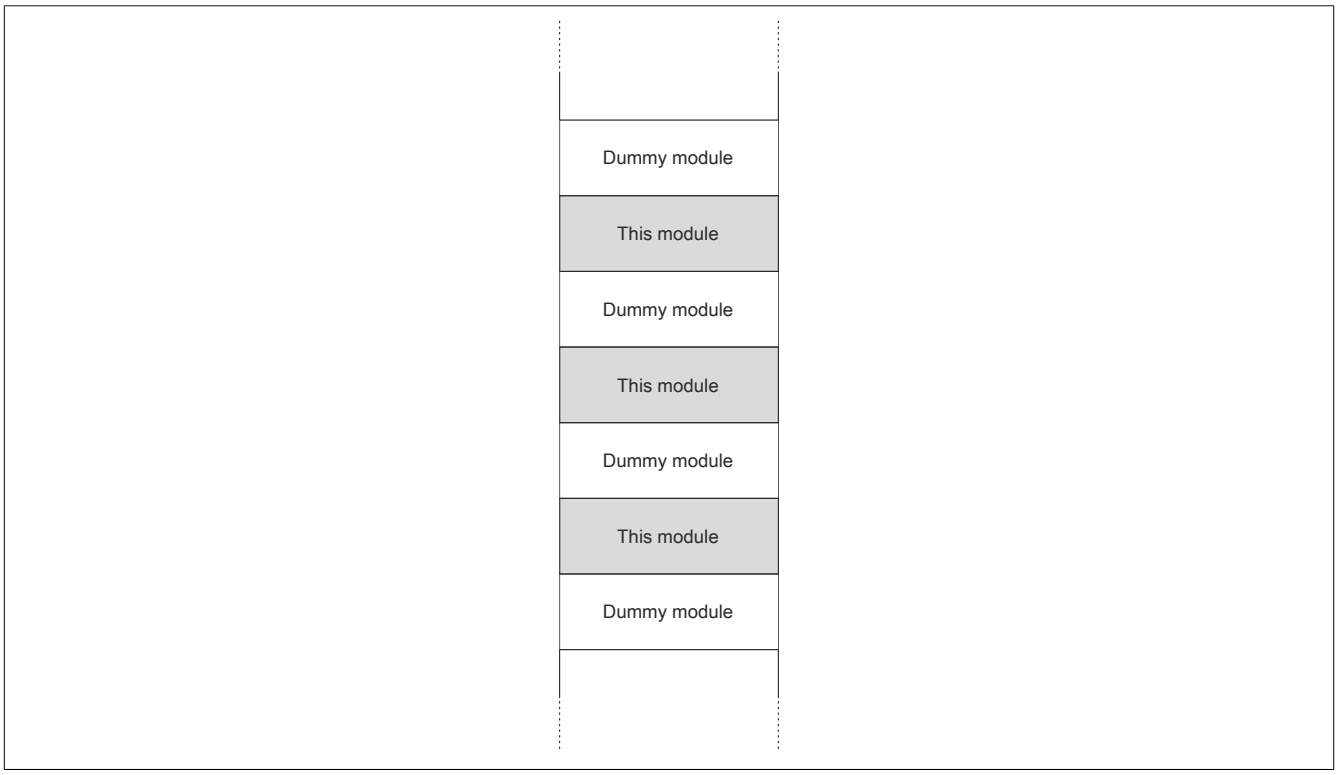
Operating a strain gauge module

Starting at an ambient temperature of 45°C, a dummy module must be connected to the left and right of the strain gauge module in a vertical mounting orientation.



Operating multiple strain gauge modules side by side

If 2 or more vertical strain gauge modules are being operated in a cluster, the following arrangement of modules must be observed.



1.1.1.4 Register description

1.1.1.4.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 System user's manual.

1.1.1.4.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration						
16	ConfigOutput01 (A/D converter configuration)	USINT			•	
18	ConfigCycletime01	UINT				•
32	AdcClkFreqShift01	USINT				•
Analog signal - Communication						
2	StatusInput01	USINT	•			
4	AnalogInput01	DINT	•			

1.1.1.4.3 Function model 1 - Multisampling

In this function model, the A/D converter is operated synchronously to X2X Link with a predefined A/D converter cycle time. The value is configurable as 50 or 100 µs.

The module returns between 3 and 10 measured values per X2X cycle depending on the configuration. With an X2X cycle time of 400 µs and A/D converter cycle time of 50 µs, exactly 8 measurements are performed and the module can return 8 values (strain gauge value 01 to strain gauge value 08).

If a longer cycle time is used, the values returned correspond to the last measurements. If using an X2X cycle time that is not a whole number multiple of the A/D converter cycle time, then the conversion cannot be synchronized with X2X Link. In this case, the module outputs the invalid value 0x8000.

Example 1

If using an X2X cycle time of 800 µs, it is possible to perform 16 measurements per X2X cycle if the A/D converter cycle time equals 50 µs. The first 6 measured values are discarded; the last 10 measured values are provided by the module.

With a shorter X2X cycle time, the number of measured values should not exceed the number of measurements that can actually be made. All other measured values are invalid (0x8000). To minimize the load on the X2X Link network, it is possible in Automation Studio to hide the registers that are not required (AnalogInputXX) and thus disable the transfer.

Example 2

If using an X2X cycle time of 300 µs, it is possible to perform 6 measurements per X2X cycle if the A/D converter cycle time equals 50 µs. For this reason, only the first 6 registers are valid. The registers for the 7th to 10th measured value (AnalogInput07 to AnalogInput10) should be hidden (disabled) by configuring setting "Number of measured values" to "6 measured values" in the I/O configuration in Automation Studio.

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration						
1601	ConfigGain01_MultiSample	USINT			•	
1603	ConfigCycletime01_MultiSample	USINT				•
Analog signal - Communication						
2	StatusInput01	USINT	•			
1534 + N * 4	AnalogInput0N (N = 1 to 10)	INT	•			

1.1.1.4.4 Function model 2 - Extended filter

The IIR low-pass filter and the FIR filter can be enabled in this function model.

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration						
272	ConfigCommonOutput01 (A/D converter and IIR filter configuration)	USINT			•	
288	ConfigFilterOutput01	UINT				•
273	ConfigDatarateOutput01	USINT			•	
274	ConfigHighResolutionOutput01	UINT			•	
Analog signal - Communication						
2	StatusInput01	USINT	•			
4	AnalogInput01	DINT	•			
256	AdcConvTimeStampInput01	DINT	•			

1.1.1.4.5 Function model 254 - Bus controller

In function model "254 - Bus controller", the module behaves as it does in "Function model 0 - Standard" with the exception that it is not synchronized to the X2X Link network even if synchronous mode is enabled in register "ConfigOutput01" on page 24. Instead, the module behaves as if the set A/D converter cycle time is not a factor or multiple of the X2X cycle time and attempts to maintain the set A/D converter cycle time as precisely as possible.

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration							
16	0	ConfigOutput01 (A/D converter configuration)	USINT			•	
18	18	ConfigCycletime01	UINT				•
32	32	AdcClkFreqShift01	USINT				•
Analog signal - Communication							
2	4	StatusInput01	USINT	•			
4	0	AnalogInput01	DINT	•			

1) The offset specifies the position of the register within the CAN object.

1.1.1.4.5.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

1.1.1.4.5.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

1.1.1.4.6 Registers for function models "0 - Standard" and "254 - Bus controller"

1.1.1.4.6.1 A/D converter configuration

Name:
ConfigOutput01

The data rate and measurement range of the A/D converter can be configured in this register.

Data type	Values	Bus controller default setting
USINT	See bit structure.	13

Bit structure:

Bit	Description	Value	Information
0 - 3	Data rate f_{DATA} (samples per second):	0000	2.5
		0001	5
		0010	10
		0011	15
		0100	25
		0101	30
		0110	50
		0111	60
		1000	100
		1001	500
		1010	1000
		1011	2000
		1100	3750
		1101	7500 (bus controller default setting)
		1110	Synchronous mode
		1111	Reserved
4 - 6	Standard measurement range (bit 6 = 0)	000	16 mV/V (bus controller default setting)
		001	8 mV/V
		010	4 mV/V
		011	2 mV/V
	Extended measurement range (bit 6 = 1)	100	256 mV/V
		101	128 mV/V
		110	64 mV/V
		111	32 mV/V
7	Reserved	0	(must be 0)

Synchronous mode

The module's analog/digital converter (A/D converter) can optionally be operated and read synchronously to the X2X Link network. Synchronous mode is enabled by selecting the respective operating mode in register "ConfigOutput01" on page 24. A time between 200 and 2000 µs must be set in register "ConfigCycletime01" on page 25 for this. If this time is a whole number factor or multiple of the configured cycle time of X2X Link, then the A/D converter is read synchronously to X2X Link.

Information:

The A/D converter cycle time must be ≥1/4 of the X2X cycle time!

Bit 2 in *Module status* is set (i.e. A/D converter not running synchronously)...

- ... If the configured A/D converter cycle time cannot be synchronized with X2X Link.
- ... If the module is still in the settling phase.

Jitter, dead time and settling time:

Jitter A/D converter cycle times <1500 µs A/D converter cycle times >1500 µs	 Max. ±1 µs Max. ±4 µs
X2X link dead time	$50\ \mu s + \frac{\text{X2X cycle time}}{128}$
Settling time	150 x X2X cycle time

The settling time corresponds to the time needed until the A/D converter can be operated after enabling synchronous mode or following conversion of the A/D converter cycle time.

1.1.1.4.6.2 A/D converter cycle time

Name:
ConfigCycletime01

This register is only used in Synchronous mode. If synchronous mode is enabled in the A/D converter configuration, then the module attempts to operate the A/D converter as synchronously as possible to the X2X Link network (based on the A/D converter cycle time set in this register). It is of course necessary for the X2X Link cycle time and the A/D converter cycle time to have a certain ratio. The following conditions must be observed:

1) A/D converter cycle time ≥ 1/4 X2X cycle time
2) A/D converter cycle time corresponds to a whole number factor or multiple of the X2X cycle time
3) A/D converter cycle time must be in the range 50 to 2000 µs

Data type	Values	Information
UINT	50 to 2000	Bus controller default setting: 400

1.1.1.4.6.3 A/D converter clock frequency shift

Name:
AdcClkFreqShift01

In rare cases, strain gauge modules connected to neighboring slots can influence one another. This can result in temporary, minimal deviations in measured values. This can only occur if the sigma-delta A/D converters on the neighboring strain gauge modules are operated at exactly the same clock frequency.

In most cases, these clock frequencies vary slightly due to part variances. When they are the same however, this register on the strain gauge module provides a safe way for an application to prevent this type of mutual influence.

Data type	Values	Information
SINT	-128 to 127	Bus controller default setting: 127

This register can be used to vary the clock frequency in increments of 200 ppm. Setting values from -50 to 50 cover a range of -10000 ppm to 10000 ppm. This corresponds with -1% to 1%.

Values beyond this range will cause activation of a default mode. The frequency shift is derived from the last 2 digits of the serial number by the module firmware. This saves time that would otherwise be needed for programming, provided that the last two digits of the serial numbers on the neighboring modules are not the same

Register value	Frequency shift in ppm	Example of a sampling rate[1)]
127	((SerialNo. modulo 100) - 50) * (-200) ppm	Based on the serial number
...	...	...
51	((SerialNo. modulo 100) - 50) * (-200) ppm	Based on the serial number
50	10000	505
49	9800	504.9
...	...	...
2	400	500.2
1	200	500.1
0	0	500
-1	-200	499.9
-2	-400	499.8
...	...	...
-50	-10000	495
-51	((SerialNo. modulo 100) - 50) * (-200) ppm	Based on the serial number
...	...	...
-128	((SerialNo. modulo 100) - 50) * (-200) ppm	Based on the serial number

1) Nominal sampling rate of 500 samples per second

Important:

As shown in the table above, shifting the A/D converter clock frequency will equally shift the A/D converter sampling rate. Shifting the A/D converter clock frequency too much can cause problems with disturbance suppression particularly when a very specific sampling rate has been defined to suppress existing disturbances (e.g. 50 Hz to suppress the 50 Hz hum). See also "Filter characteristics of the sigma-delta A/D converter" on page 12.
It is situations like this where the option to manually shift the frequency in the I/O configuration or ASIOACC library should be utilized rather than relying on the default frequency shift that is based on the serial number.

A frequency shift like the one shown below would be sufficient to prevent modules from influencing one another and would not cause any noticeable difference to the filter characteristics.

Slot	1	2	3	4	5	6	...
A/D converter clock frequency shift	0	2	-1	1	-2	0	...

Information:

- **This register has no effect in synchronous mode because the firmware regulates the A/D converter clock frequency in such a way that the A/D converter cycle is synchronous with the X2X cycle.**
- **When writing to this register using the ASIOACC library, only the lowest value byte of the written value is accepted. For example, the value 256 (=0x100) is identical to the value 0 (=0x00).**

1.1.1.4.6.4 Module status

Name:
StatusInput01

The current state of the module is indicated in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	A/D converter value	0	Valid A/D converter value
		1	Invalid A/D converter value (analog value = 0xFF800000). Possible causes: • Strain gauge supply error • I/O power supply error • A/D converter not (yet) configured
1	Line monitoring	0	Ok
		1	Open circuit
2	Only valid in synchronous mode	0	A/D converter runs synchronous to X2X Link
		1	A/D converter does not run synchronous to X2X Link
3 - 7	Reserved	-	

1.1.1.4.6.5 Strain gauge value

Name:
AnalogInput01

This register contains the raw value determined by the A/D converter for the full-bridge strain gauge with 24-bit resolution.

Data type	Values	Information
DINT	-8,388,608	Negative invalid value
	-8,388,607	Negative full-scale deflection / Underflow
	-8,388,606 to 8388606	Valid range
	8,388,607	Positive full-scale deflection / Overflow / Open circuit

Effective resolution

In principle, the effective resolution of the A/D converter is dependent on the data rate and the measurement range (see "Effective resolution of the A/D converter" on page 9).

The following table shows how the effective resolution (in bits) or effective range of values of the strain gauge value depend on the module configuration (data rate, measurement range):

	Measurement range							
	±16 mV/V		±8 mV/V		±4 mV/V		±2 mV/V	
Data rate f_{DATA} [Hz]	Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
2.5	19.9	±489,000	19.1	±281,000	18.0	±131,000	17.4	±86,500
5	19.4	±346,000	18.2	±151,000	17.5	±92,700	16.4	±43,200
10	18.5	±185,000	17.8	±114,000	16.8	±57,100	15.9	±30,600
15	18.2	±151,000	17.3	±80,700	16.4	±43,200	15.4	±21,600
25	17.8	±114,000	16.9	±61,100	16.0	±32,800	14.9	±15,300
30	17.8	±114,000	16.8	±57,100	15.9	±30,600	14.8	±14,300
50	17.4	±86,500	16.3	±40,300	15.4	±21,600	14.4	±10,800
60	17.4	±86,500	16.2	±37,600	15.3	±20,200	14.1	±8,780
100	16.9	±61,100	15.9	±30,600	14.8	±14,300	13.8	±7,130
500	15.5	±23,200	14.5	±11,600	13.5	±5,790	12.5	±2,900
1000	15.0	±16,400	14.1	±8,780	13.1	±4,390	11.9	±1,910
2000	14.5	±11,600	13.4	±5,400	12.6	±3,100	11.4	±1,350
3750	14.1	±8,780	13.1	±4,390	12.1	±2,190	11.1	±1,100
7500	13.8	±7,130	12.7	±3,330	11.8	±1,780	10.6	±776

Table 3: Effective resolution of the strain gauge value in bits for the measurement range 2 to 16 mV/V

	Measurement range							
	±256 mV/V		±128 mV/V		±64 mV/V		±32 mV/V	
Data rate f_{DATA} [Hz]	Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
2.5	22.0	±2,100,000	22.0	±2,100,000	21.2	±1,200,000	20.5	±741,000
5	21.7	±1,700,000	21.4	±1,380,000	20.8	±913,000	20.3	±645,000
10	20.8	±913,000	20.8	±913,000	20.2	±602,000	19.4	±346,000
15	20.7	±852,000	20.5	±741,000	19.9	±489,000	19.3	±323,000
25	20.1	±562,000	19.9	±489,000	19.7	±426,000	18.9	±245,000
30	19.9	±489,000	19.9	±489,000	19.4	±346,000	18.8	±228,000
50	19.8	±456,000	19.2	±301,000	19.2	±301,000	18.2	±151,000
60	19.5	±371,000	19.2	±301,000	19.0	±262,000	18.2	±151,000
100	19.0	±262,000	18.8	±228,000	18.5	±185,000	17.6	±99,300
500	17.8	±114,000	17.5	±92,700	17.1	±70,200	16.4	±43,200
1000	17.2	±75,300	17.1	±70,200	16.7	±53,200	15.8	±28,500
2000	16.7	±53,200	16.5	±46,300	16.1	±35,100	15.2	±18,800
3750	16.2	±37,600	16.1	±35,100	15.8	±28,500	14.9	±15,300
7500	15.9	±30,600	15.8	±28,500	15.3	±20,200	14.6	±12,400

Table 4: Effective resolution of the strain gauge value in bits for the measurement range 32 to 256 mV/V

1.1.1.4.7 Register for "Function model 1 - Multisampling"

1.1.1.4.7.1 A/D converter configuration

Name:
ConfigGain01_MultiSample

The measurement range for the A/D converter can be configured in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Standard measurement range (bit 2 = 0)	000	16 mV/V
		001	8 mV/V
		010	4 mV/V
		011	2 mV/V
	Extended measurement range (bit 2 = 1)	100	256 mV/V
		101	128 mV/V
		110	64 mV/V
		111	32 mV/V
3 - 7	Reserved	0	(must be 0)

1.1.1.4.7.2 A/D converter cycle time

Name:
ConfigCycletime01_MultiSample

The A/D converter cycle time can be configured in this register.

In order for multisampling to work, the X2X cycle time must be divisible by the A/D converter cycle time to produce a whole number.

Data type	Value	Information
USINT	0	50 µs (default)
	1	100 µs
	2 to 255	Reserved

1.1.1.4.7.3 Recording multiple measured values per X2X cycle

In function model , the A/D converter is operated synchronously to X2X Link with a fixed specified A/D converter cycle time. The value is configurable as 50 or 100 µs.

Information:

"Function model 1 - Multisampling" can only be used on channel 1.

The module returns between 3 and 10 measured values per X2X cycle depending on the configuration. With an X2X cycle time of 400 µs and A/D converter cycle time of 50 µs, exactly 8 measurements are performed and the module can return 8 values (strain gauge value 01 to strain gauge value 08).

If a longer cycle time is used, the values returned correspond to the last measurements. If using an X2X cycle time that is not a whole number multiple of the A/D converter cycle time, then the conversion cannot be synchronized with X2X Link. In this case, the module outputs the invalid value 0x8000.

Example 1

If using an X2X cycle time of 800 µs, it is possible to perform 16 measurements per X2X cycle if the A/D converter cycle time equals 50 µs. The first 6 measured values are discarded; the last 10 measured values are provided by the module.

With a shorter X2X cycle time, the number of measured values should not exceed the number of measurements that can actually be made. All other measured values are invalid (0x8000). To minimize the load on the X2X Link network, it is possible in Automation Studio to hide the registers that are not required (AnalogInputXX) and thus disable the transfer.

Example 2

If using an X2X cycle time of 300 µs, it is possible to perform 6 measurements per X2X cycle if the A/D converter cycle time equals 50 µs. For this reason, only the first 6 registers are valid. The registers for the 7th to 10th measured value (AnalogInput07 to AnalogInput10) should be hidden (disabled) by configuring setting "Number of measured values" to "6 measured values" in the I/O configuration in Automation Studio.

Number of measured values

If the X2X cycle time is too short, then not all 10 measurements can be performed. To reduce the load on X2X Link, it makes sense to only transfer as many values as measurements that can be made. The maximum possible number of measured values to be transferred is determined by selecting the X2X cycle time and the A/D converter cycle time.

To minimize the load on the X2X Link network, it is possible in Automation Studio to hide the registers that are not required (AnalogInputXX) and thus disable the transfer.

Example: A/D converter cycle time = 50 µs

X2X cycle time	Number of measured values to be transferred
250 µs	5
300 µs	6
350 µs	7
400 µs	8
450 µs	9
≥500 µs	10

Example: A/D converter cycle time = 100 µs

X2X cycle time	Number of measured values to be transferred
300 µs	3
400 µs	4
500 µs	5
600 µs	6
700 µs	7
800 µs	8
900 µs	9
≥1 ms	10

1.1.1.4.7.4 Module status

Name:
StatusInput01

This register contains the current state of the module.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	A/D converter values	0	Valid A/D converter value
		1	Invalid A/D converter value
1	Line monitoring	0	OK
		1	Open circuit An open circuit was found during at least one measurement in this X2X cycle. This bit is reset if all measurements are OK after correcting this error, i.e. it does not have to be acknowledged.
2	Synchronous mode	0	A/D converter runs synchronous to X2X Link
		1	A/D converter does not run synchronous to X2X Link
3 - 7	Reserved	-	

1.1.1.4.7.5 Strain gauge value - Multiple

Name:
AnalogInput01 to AnalogInput10

This register contains the raw value determined by the A/D converter for the full-bridge strain gauge with 16-bit resolution. The module returns between 3 and 10 measured values per X2X cycle depending on the configuration.

Effective resolution

In principle, the effective resolution of the A/D converter is dependent on the data rate and measurement range (see "Effective resolution of the A/D converter" on page 9).

The following table shows how the effective resolution (in bits) or effective range of values of the strain gauge value depend on the module configuration (data rate, measurement range):

Measurement range							
±16 mV/V		±8 mV/V		±4 mV/V		±2 mV/V	
Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
13.4	±5,240	12.3	±2,510	11.3	±1,300	10.3	±630

Table 5: Effective resolution of the strain gauge value in bits for the measurement range 2 to 16 mV/V

Measurement range							
±256 mV/V		±128 mV/V		±64 mV/V		±32 mV/V	
Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
15.5	±23,200	15.0	±16,400	15.0	±16,400	14.1	±8,490

Table 6: Effective resolution of the strain gauge value in bits for the measurement range 32 to 256 mV/V

1.1.1.4.8 Register for "Function model 2 - Extended filter"

1.1.1.4.8.1 A/D converter and IIR filter configuration

Name:
ConfigCommonOutput01

The IIR low-pass filter and measurement range of the A/D converter can be configured in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	IIR low-pass filter: Definition of the filter level	0000	IIR low-pass filter switched off
		0001	Filter level 1
		0010	Filter level 2
		0011	Filter level 3
		0100	Filter level 4
		0101	Filter level 5
		0110	Filter level 6
		0111	Filter level 7
		1000	Filter level 8
		1001 - 1111	Not permitted
4 - 6	Default measurement range	000	16 mV/V
		001	8 mV/V
		010	4 mV/V
		011	2 mV/V
	Extended measurement range	100	256 mV/V
		101	128 mV/V
		110	64 mV/V
		111	32 mV/V
7	Reserved	0	(must be 0)

1.1.1.4.8.2 Data rate configuration

Name:
ConfigFilterOutput01

Whether a selectable data rate or a high-resolution data rate is being used for the FIR filter is configured in this register.

Data type	Values	Information
UINT	0	Mode "Selectable data rate": A selectable data rate is used for the FIR filter (default). Configuration takes place in register "ConfigDatarateOutput01" on page 33.
	1	Mode "High-resolution data rate": A high-resolution data rate is used for the FIR filter. Configuration takes place in register "ConfigHighResolutionOutput01" on page 33.

Selectable data rate

Name:
ConfigDatarateOutput01

The data rate of the FIR filter can be configured in mode "Selectable data rate" in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Data rate f_{DATA} (samples per second):	0000	2.5
		0001	5
		0010	10
		0011	15
		0100	25
		0101	30
		0110	50
		0111	60
		1000	100
		1001	500
		1010	1000
		1011	2000
		1100	3750
		1101	7500
		1110 - 1111	The analog input value indicates an invalid range.
4 - 7	Reserved	0	(must be 0)

High-resolution data rate

Name:
ConfigHighResolutionOutput01

The data rate of the FIR filter can be configured in 0.1 Hz steps (0.1 to 6553.5 Hz) in this register.

Data type	Values	Information
UINT	0	Disables the FIR filter
	1 to 65,535	0.1 to 6553.5 Hz

1.1.1.4.8.3 Module status

Name:
StatusInput01

This register contains the current state of the module. If there is a fault in the module power supply or strain gauge supply, the analog input value indicates an invalid range and the buffer of the enabled filter is reset.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	A/D converter values	0	Valid A/D converter value
		1	Invalid A/D converter value
1	Line monitoring	0	OK
		1	Open circuit
2	Reserved	-	
3	Module power supply	0	OK
		1	Error in module power supply
4	Strain gauge supply	0	OK
		1	Error in strain gauge supply
5	FIR filter ready	0	OK
		1	FIR filter not yet ready
6 - 7	Reserved	-	

1.1.1.4.8.4 A/D converter conversion timestamp

Name:
AdcConvTimeStampInput01

This register holds the timestamp of the last analog conversion. This is always the point in time in [µs] at which the conversion of the latest A/D converter raw value is completed.

Data type	Values	Explanation
DINT	-2,147,483,648 to 2,147,483,647	Timestamp [µs] of the last analog conversion

1.1.1.4.9 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
250 µs

1.1.1.4.10 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

For the I/O update times for function models "0 - Standard", "2 - Extended filter" and "254 - Bus controller", see section "Characteristics of the FIR filter in mode "Selectable data rate"" on page 16.

Depending on the setting in register "ConfigCycletime01_MultiSample" on page 29, the I/O update time in "Function model 1 - Multisampling" is 50 or 100 µs.

1.1.2 X20AI1744 - With Rev. <H0

1.1.2.1 General information

This module works with both 4-wire and 6-wire strain gauge load cells. The concept applied by the module requires compensation in the measurement system. This compensation eliminates the absolute uncertainty in the measurement circuit, such as component tolerances, effective bridge voltage or zero point offset. The measurement precision refers to the absolute (compensated) value, which will only change as a result of changes in the operating temperature.

- 1 full-bridge strain gauge input
- Data output rate configurable from 2.5 Hz to 7.5 kHz
- Special operating modes (synchronous mode and multiple sampling)

1.1.2.2 Order data

Model number	Short description	Figure
	Analog inputs	
X20AI1744	X20 analog input module,1 full-bridge strain gauge input,24-bit converter resolution,5 kHz input filter	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply continuous	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 7: X20AI1744 - Order data

1.1.2.3 Technical data

Order number	X20AI1744
Short description	
I/O module	1 full-bridge strain gauge input
General information	
B&R ID code	0x1CDE
Status indicators	Channel status, operating status, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Open circuit	Yes, using status LED and software
Input	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1.25 W
Additional power dissipation caused by actuators (resistive) [W]	Max. +0.36 [1)]
Certifications	
CE	Yes
KC	Yes
EAC	Yes
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
Full-bridge strain gauge	
Strain gauge factor	2 to 256 mV/V, configurable using software
Connection	4- or 6-wire connections [2)]
Input type	Differential, used to evaluate a full-bridge strain gauge
Digital converter resolution	24-bit
Conversion time	Depends on the configured data output rate

Table 8: X20AI1744 - Technical data

Order number	X20AI1744
Data output rate	2.5 - 7500 samples per second, configurable using software (f_{DATA})
Input filter	
Cutoff frequency	5 kHz
Order	3
Slope	60 dB
ADC filter characteristics	Sigma-delta, see section "Filter characteristics of the sigma-delta A/D converter"
Operating range / Measurement sensor	85 to 5000 Ω
Influence of cable length	The shielded twisted pair cable should be as short as possible and run separately to the sensor (isolated from load circuit) without intermediate terminals
Input protection	RC protection
Common-mode range	0 to 3 VDC Permissible input voltage range (with regard to the potential strain gauge GND) on inputs "Input +" and "Input -"
Isolation voltage between input and bus	500 V_{eff}
Conversion procedure	Sigma-delta
Output of digital value	
Broken bridge supply line	Value approaches 0
Broken sensor line	Value approaches ±end value ("open circuit" status bit is set in the *Module status* register)
Valid range of values	0xFF800001 to 0x007FFFFF (-8,388,607 to 8,388,607)
Strain gauge supply	
Voltage	5.5 VDC / max. 65 mA [3]
Short-circuit and overload resistant	Yes
Voltage drop for short-circuit protection	Max. 0.2 VDC at 65 mA
Quantization [4]	
LSB value (16-bit)	
2 mV/V	336 nV
4 mV/V	671 nV
8 mV/V	1.343 µV
16 mV/V	2.686 µV
32 mV/V	5.371 µV
64 mV/V	10.74 µV
128 mV/V	21.48 µV
256 mV/V	42.97 µV
LSB value (24-bit)	
2 mV/V	1.31 nV
4 mV/V	2.62 nV
8 mV/V	5.25 nV
16 mV/V	10.49 nV
32 mV/V	20.98 nV
64 mV/V	41.96 nV
128 mV/V	83.92 nV
256 mV/V	167.85 nV
Temperature coefficient	
Rev. ≥E0	10 ppm/°C
Rev. <E0	30 ppm/°C
Electrical isolation	Bus isolated from analog input and strain gauge supply voltage Channel not isolated from I/O power supply
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	0 to 55°C
Vertical mounting orientation	0 to 50°C
Derating	See section "Hardware configuration"
Storage	-25 to 70°C
Transport	-25 to 70°C

Table 8: X20AI1744 - Technical data

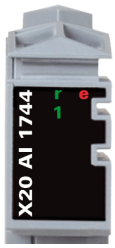
Order number	X20AI1744
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x terminal block X20TB12 separately Order 1x bus module X20BM11 separately
Spacing	12.5$^{+0.2}$ mm

Table 8: X20AI1744 - Technical data

1) Depends on the full-bridge strain gauge being used.
2) With 6-wire connections, line compensation does not function (see section "Connection examples").
3) The maximum current of 90 mA is permitted up to an operating temperature of 45°C.
4) Quantization depends on the strain gauge factor.

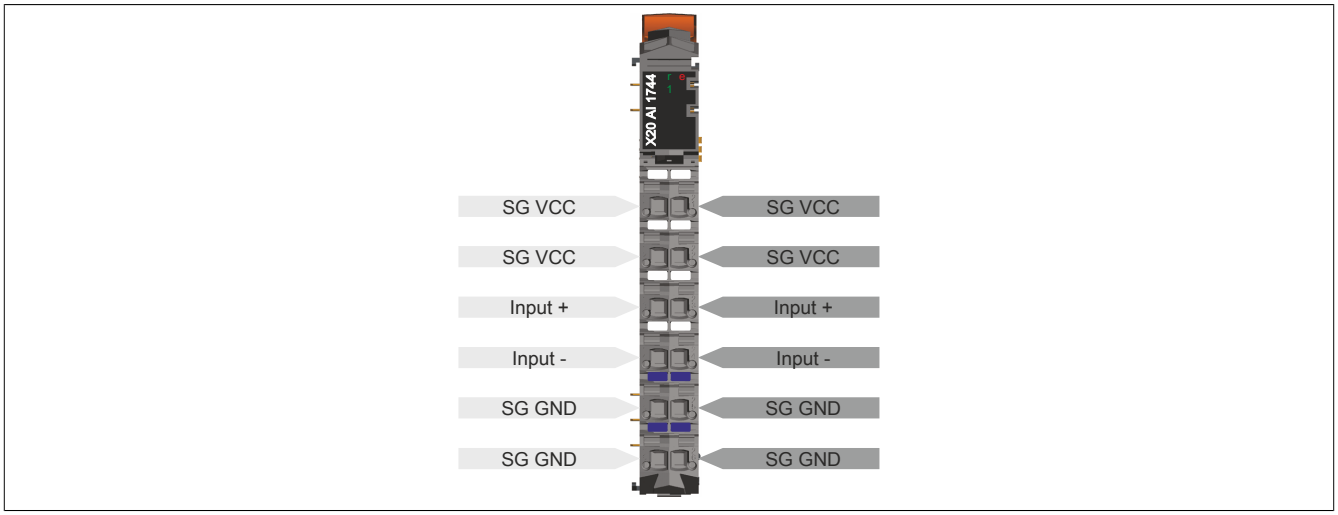
1.1.2.4 LED status indicators

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 System user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	1	Green	Off	Possible causes: • Open circuit • Sensor is disconnected • Converter is busy
			On	Analog/digital converter running, value OK

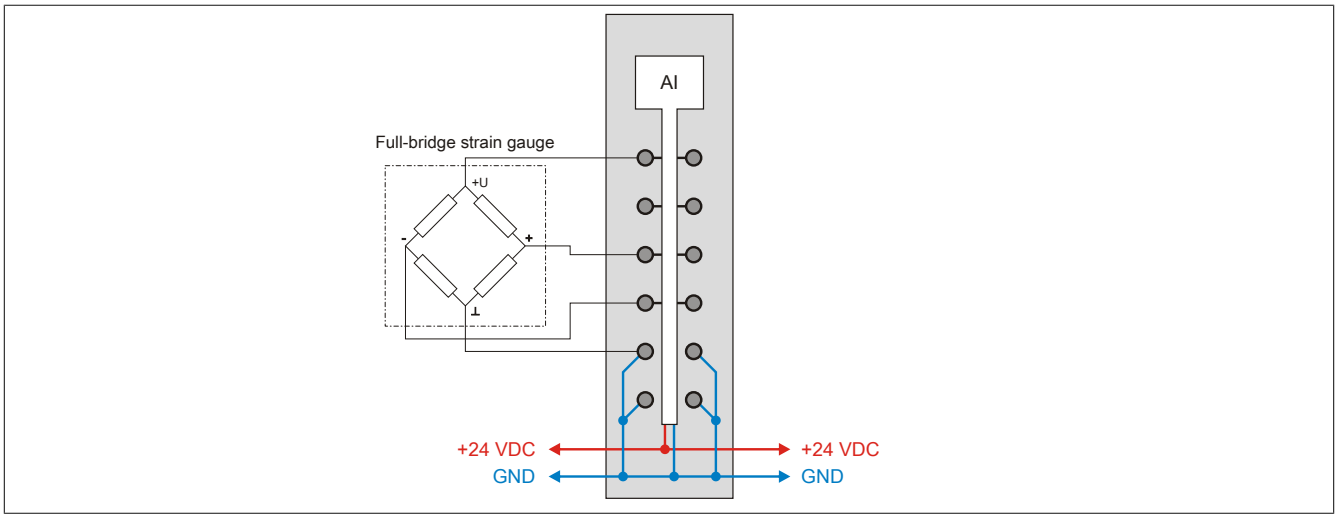
1) Depending on the configuration, a firmware update can take up to several minutes.

1.1.2.5 Pinout



1.1.2.6 Connection examples

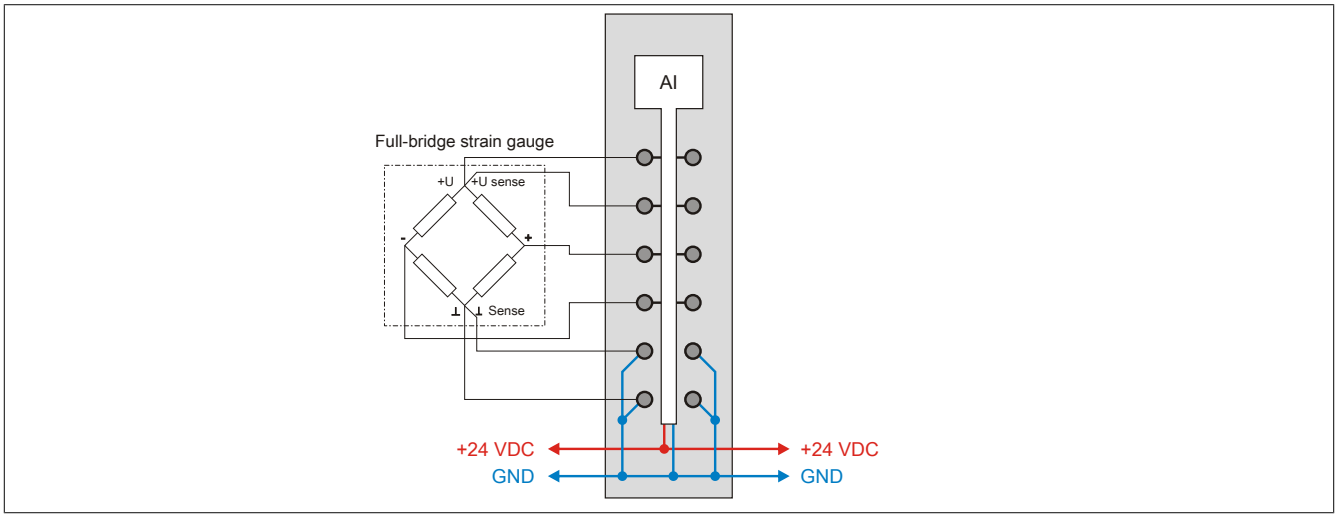
Full-bridge strain gauge with 4-wire connections



Full-bridge strain gauge with 6-wire connections

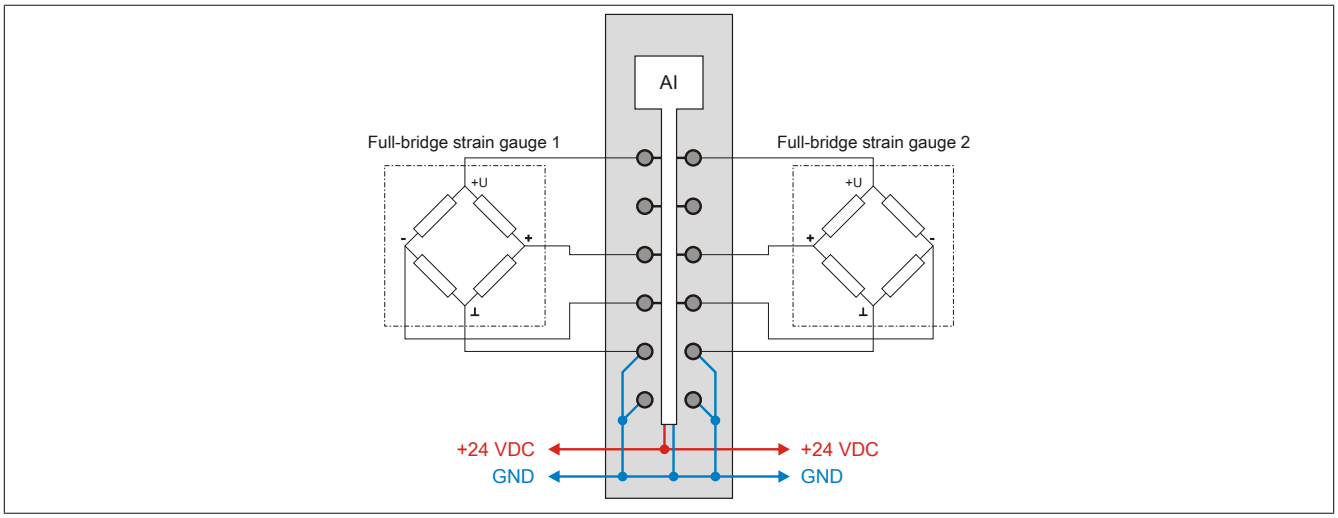
Full-bridge strain gauges can be connected to this module with 6-wire connections. Line compensation is not supported by the module, however. The sense lines are short circuited by the internally connected strain gauge VCC and GND connections (see "Input circuit diagram" on page 39). The measurement precision is therefore affected by changes in operating temperature. Longer cable lengths and smaller cable cross sections also increase the potential for errors in the measurement system.

In order to reduce cable resistance, the sense lines should be connected in parallel with the strain gauge supply lines. Optimal signal quality can be obtained by using a shielded twisted pair cable. The connections for the strain gauge supply lines, the sensor lines and the bridge differential voltage lines should each use one twisted pair cable.



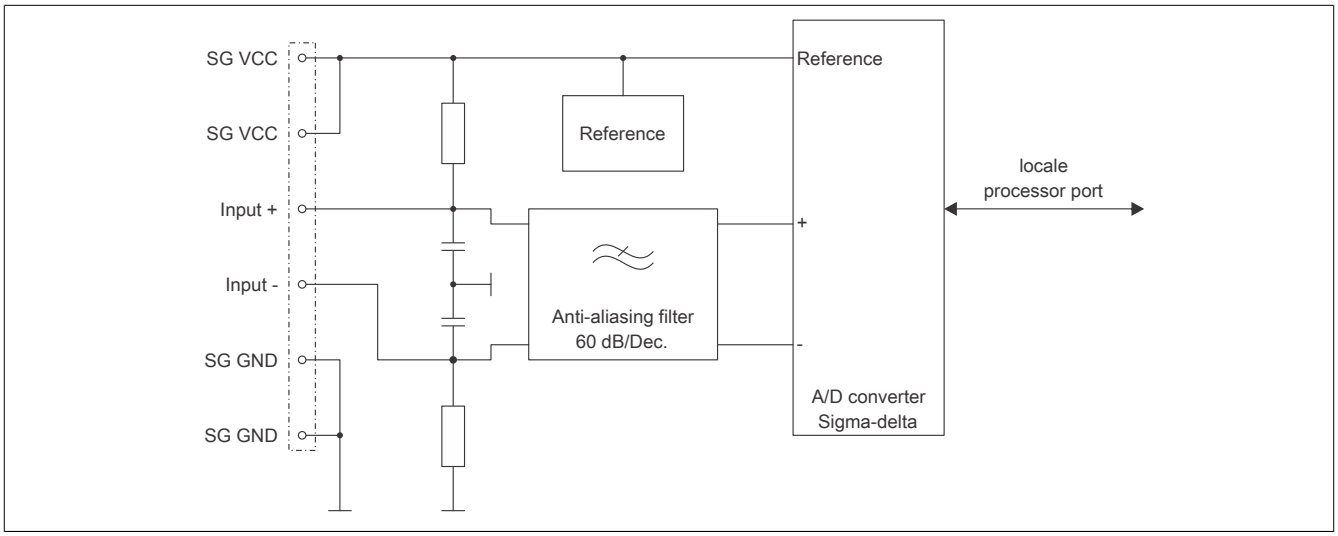
Parallel connection of 2 full-bridge strain gauges (4-wire connections)

If connecting the full-bridge strain gauges in parallel, the manufacturer's guidelines must be observed.

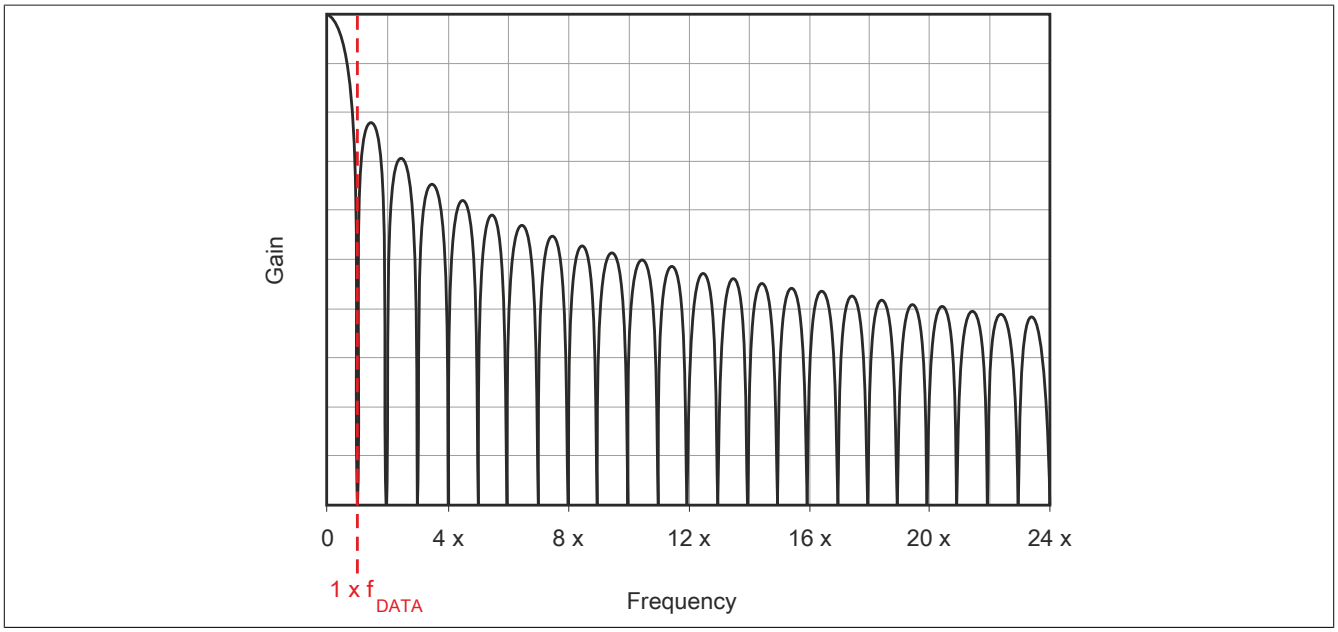


When connecting 3 or more full-bridge strain gauges in parallel, 2 lines must be connected together in an X20 terminal block.

1.1.2.7 Input circuit diagram



1.1.2.8 Filter characteristics of the sigma-delta A/D converter

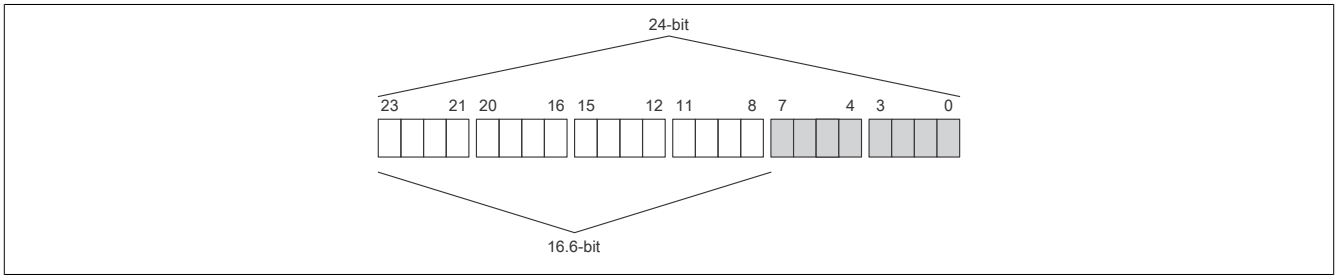


1.1.2.9 Effective resolution of the A/D converter

The A/D converter on the module provides a 24-bit measured value. The actual attainable noise-free resolution is always less than 24-bit, however. This "effective resolution" depends on the data rate and measurement range.

Example:

Based on the conversion method, a data rate of 2.5 Hz and a specified measurement range of 2 mV/V result in an effective resolution of 16.6 bits:



The low-order bits (grayed out) contain only noise instead of valid values and must therefore not be evaluated.

With "Function model 1 - Multisampling", only the highest 16 bits are made available.

1.1.2.10 Calculation example / Quantization

In a weighing application, the corresponding weight located on the connected load cell should be determined from the value derived from the module.

The characteristics of the strain gauge load cell are as follows:

- Rated load: 1000 kg
- Strain gauge factor: 4 mV/V

The bridge factor of the strain gauge load cell now yields (by multiplying with the bridge supply voltage from the module) the value for the positive full-scale deflection at the specified nominal load of 1000 kg:

4 mV/V × 5.5 V = 22 mV

With a simple Rule of Three calculation, the corresponding value can be calculated (as seen in the table) from weight to the converter value and vice versa. This simplified theoretical approach is only valid for an ideal measurement system. Calibration of the entire measurement system is recommended because not only the module, but particularly the strain gauge bridges exhibit tolerances (offset, gain). When taring, the gradient offset is recalculated and the gain of the linear equation is determined when normalized. In addition to the calculation displayed in the table, these calculations must also be carried out in the application.

24-bit value of the module		Quantization	Corresponding weight
0x007F FFFF	8,388,607	22.0 mV	1000 kg
0x0000 0001	1	2.62 nV	0.119 g
0x0000 20C3	8387	22.0 µV	1 kg
0x0001 0000	65536	171.9 µV	7.81 kg

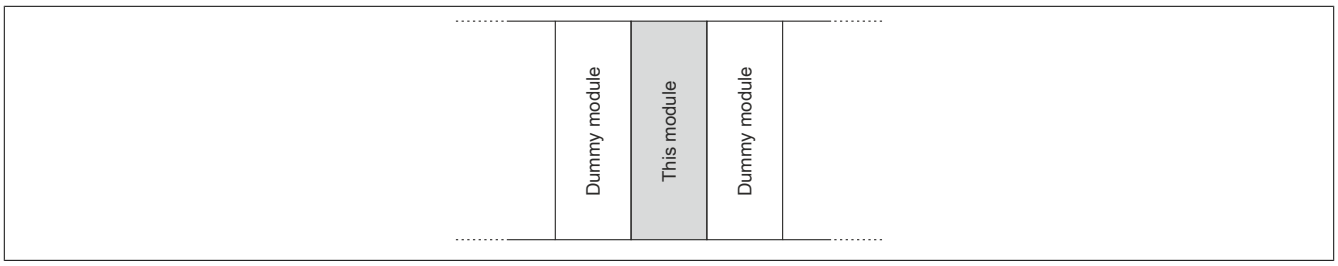
The values for one LSB are also included in the module's technical data under item "Quantization" (1 LSB each for 16 bits and 24 bits).

1.1.2.11 Hardware configuration

1.1.2.11.1 Hardware configuration for horizontal installation at 50°C ambient temperature

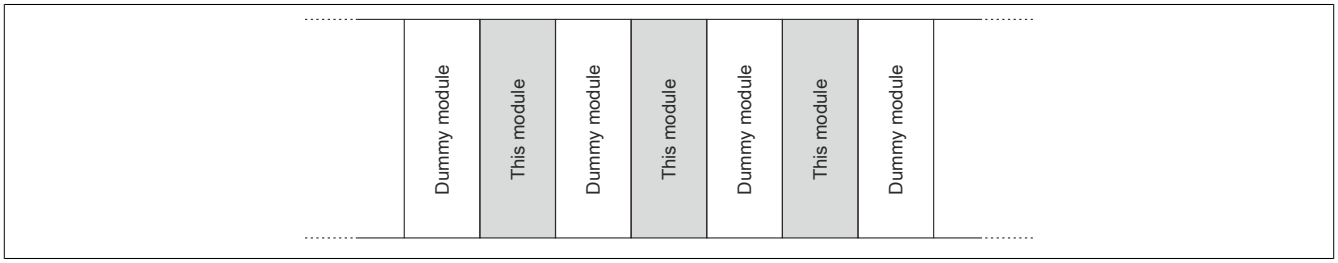
Operating a strain gauge module

Starting at an ambient temperature of 50°C, a dummy module must be connected to the left and right of the strain gauge module in a horizontal mounting orientation.



Operating multiple strain gauge modules side by side

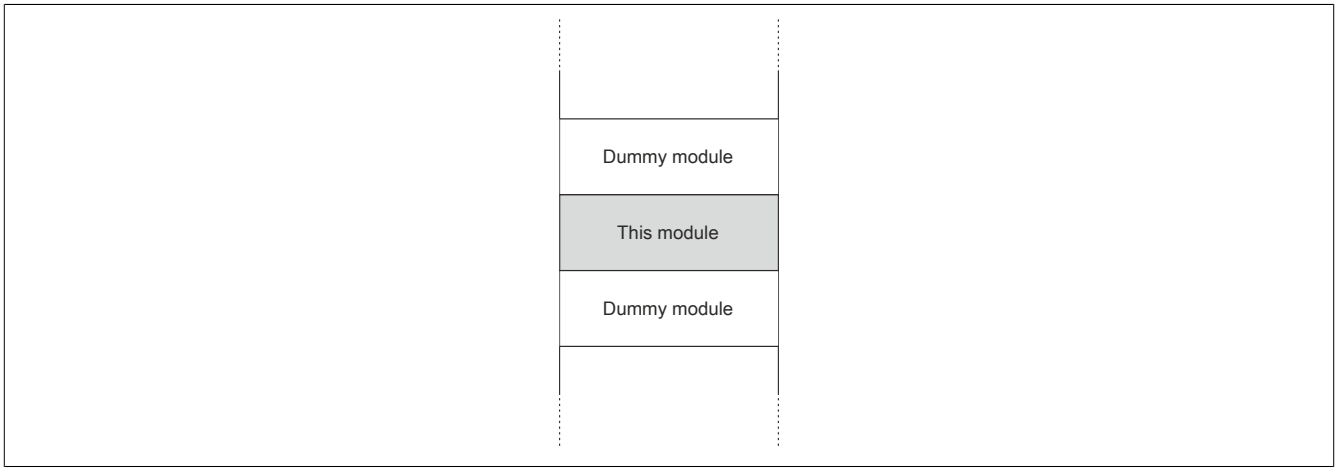
If 2 or more horizontal strain gauge modules are being operated in a cluster, the following arrangement of modules must be observed.



1.1.2.11.2 Hardware configuration for vertical installation at 40°C ambient temperature

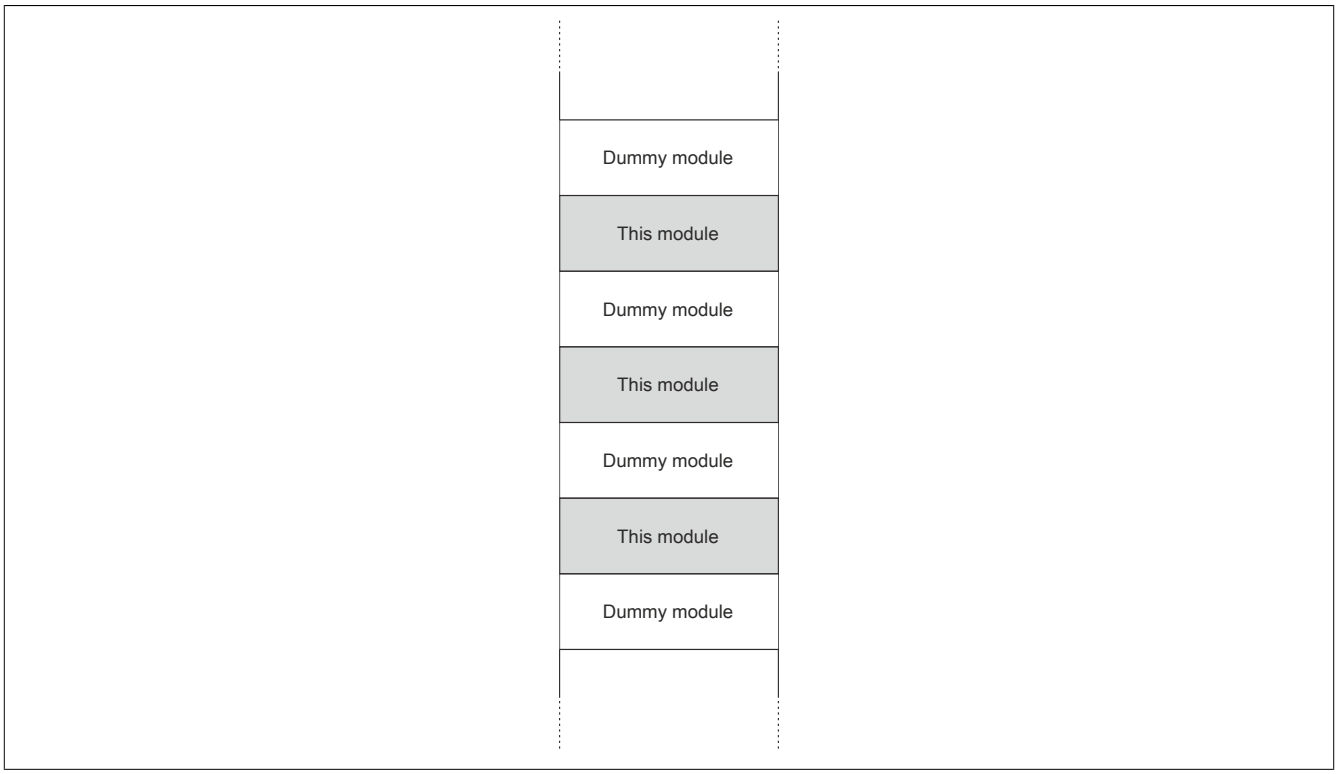
Operating a strain gauge module

Starting at an ambient temperature of 40°C, a dummy module must be connected to the left and right of the strain gauge module in a vertical mounting orientation.



Operating multiple strain gauge modules side by side

If 2 or more vertical strain gauge modules are being operated in a cluster, the following arrangement of modules must be observed.


Dummy module
This module
Dummy module
This module
Dummy module
This module
Dummy module

1.1.2.12 Register description

1.1.2.12.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 system user's manual.

1.1.2.12.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
2	StatusInput01	USINT	•			
4	AnalogInput01	DINT	•			
16	ConfigOutput01	USINT			•	
18	ConfigCycletime01	UINT				•
32	AdcClkFreqShift01[1)]	USINT				•

1) Firmware version 8 / Upgrade 1.3.0.0 or later

1.1.2.12.3 Function model 1 - Multisampling

In this function model, the A/D converter is operated synchronously to X2X Link with a predefined A/D converter cycle time. The value is configurable as 50 or 100 µs.

The module returns between 3 and 10 measured values per X2X cycle depending on the configuration. With an X2X cycle time of 400 µs and A/D converter cycle time of 50 µs, exactly 8 measurements are performed and the module can return 8 values (strain gauge value 01 to strain gauge value 08).

If a longer cycle time is used, the values returned correspond to the last measurements. If using an X2X cycle time that is not a whole number multiple of the A/D converter cycle time, then the conversion cannot be synchronized with X2X Link. In this case, the module outputs the invalid value 0x8000.

Example 1

If using an X2X cycle time of 800 µs, it is possible to perform 16 measurements per X2X cycle if the A/D converter cycle time equals 50 µs. The first 6 measured values are discarded; the last 10 measured values are provided by the module.

With a shorter X2X cycle time, the number of measured values should not exceed the number of measurements that can actually be made. All other measured values are invalid (0x8000). To minimize the load on the X2X Link network, it is possible to disable these unneeded registers (see "Number of measured values" on page 50).

Example 2

If using an X2X cycle time of 300 µs, it is possible to perform 6 measurements per X2X cycle if the A/D converter cycle time equals 50 µs. For this reason, only the first 6 registers are valid. The registers for the 7th through 10th measured value (AnalogInput07 to AnalogInput10) should be disabled by setting Number of measured values to "6 measured values" in the I/O configuration.

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration						
1601	ConfigGain01_MultiSample	USINT			•	
1603	ConfigCycletime01_MultiSample	USINT				•
Analog signal - Communication						
2	StatusInput01	USINT	•			
1534 + N * 4	AnalogInput0N (N = 1 to 10)	INT	•			

1.1.2.12.4 Function model 254 - Bus controller

In function model "254 - Bus controller", the module behaves as it does in "Function model 0 - Standard" with the exception that it is not synchronized to the X2X Link network even if synchronous mode is enabled in register "ConfigOutput01" on page 46. Instead, the module behaves as if the set A/D converter cycle time is not a factor or multiple of the X2X cycle time and attempts to maintain the set A/D converter cycle time as precisely as possible.

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
2	StatusInput01	USINT	•			
4	AnalogInput01	DINT	•			
16	ConfigOutput01	USINT			•	
18	ConfigCycletime01	UINT				•
32	AdcClkFreqShift01[1)]	USINT				•

1) Firmware version 8 / Upgrade 1.3.0.0 or later

1.1.2.12.5 Registers for function models "0 - Standard" and "254 - Bus controller"

1.1.2.12.5.1 Module status

Name:
StatusInput01

The current state of the module is indicated in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	A/D converter value	0	Valid A/D converter value
		1	Invalid A/D converter value (analog value = 0xFF800000). Possible causes: • Strain gauge supply error • I/O power supply error • A/D converter not (yet) configured
1	Line monitoring	0	Ok
		1	Open circuit
2	Only valid in synchronous mode	0	A/D converter runs synchronous to X2X Link
		1	A/D converter does not run synchronous to X2X Link
3 - 7	Reserved	-	

1.1.2.12.5.2 Strain gauge value

Name:
AnalogInput01

This register contains the raw value determined by the A/D converter for the full-bridge strain gauge with 24-bit resolution.

Data type	Values	Information
DINT	-8,388,608	Negative invalid value
	-8,388,607	Negative full-scale deflection / Underflow
	-8,388,606 to 8,388,606	Valid range
	8,388,607	Positive full-scale deflection / Overflow / Open circuit

Effective resolution

In principle, the effective resolution of the A/D converter is dependent on the data rate and measurement range (see "Effective resolution of the A/D converter" on page 40).

The following table shows how the effective resolution (in bits), or the RMS value range of the strain gauge value depend on the module configuration (data rate, measurement area).

	Measurement range							
	±16 mV/V		±8 mV/V		±4 mV/V		±2 mV/V	
Data rate f_{DATA} [Hz]	Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
2.5	21.3	±1,290,000	20.8	±912,000	19.7	±425,000	18.7	±212,000
5	20.7	±851,000	20.3	±645,000	19.3	±322,000	18.3	±161,000
10	20.4	±691,000	19.9	±490,000	18.9	±244,000	17.9	±122,000
15	20.1	±562,000	19.3	±320,000	18.7	±212,000	17.7	±106,000
25	19.7	±425,000	19.2	±301,000	18.5	±185,000	17.5	±92,000
30	19.6	±397,000	19.0	±262,000	18.1	±140,000	17.1	±72,000
50	19.4	±346,000	18.8	±230,000	17.9	±122,000	16.9	±61,000
60	19.3	±320,000	18.8	±230,000	17.8	±114,000	16.8	±57,000
100	19.1	±280,000	18.5	±185,000	17.4	±86,000	16.4	±43,000
500	18.0	±130,000	17.3	±80,000	16.3	±40,000	15.3	±20,000
1000	17.2	±75,000	16.5	±46,000	15.6	±25,000	14.6	±12,000
2000	16.6	±49,600	16.1	±35,000	15.3	±20,000	14.3	±10,000
3750	16.2	±37,600	15.7	±26,600	14.7	±13,000	13.7	±6,600
7500	15.8	±28,500	15.3	±20,200	14.4	±10,800	13.4	±5,400

Table 9: Effective resolution of the strain gauge value in bits for the measurement range 2 to 16 mV/V

	Measurement range							
	±256 mV/V		±128 mV/V		±64 mV/V		±32 mV/V	
Data rate f_{DATA} [Hz]	Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
2.5	23	±4,194,000	22.6	±3,179,000	22.1	±2,248,000	21.7	±1,703,000
5	22.3	±2,582,000	22.4	±2,767,000	21.9	±1,957,000	21.3	±1,291,000
10	22.3	±2,582,000	22	±2,097,000	21.6	±1,589,000	21	±1,049,000
15	22	±2,097,000	21.7	±1,703,000	21.3	±1,291,000	20.7	±852,000
25	21.7	±1,703,000	21.4	±1,384,000	21.1	±1,124,000	20.5	±741,000
30	21.8	±1,826,000	21.3	±1,291,000	20.8	±913,000	20.4	±692,000
50	21.3	±1,291,000	21.1	±1,124,000	20.4	±692,000	19.9	±489,000
60	21.3	±1,291,000	20.9	±978,000	20.5	±741,000	19.8	±456,000
100	20.9	±978,000	20.7	±852,000	20.2	±602,000	19.6	±397,000
500	20.1	±562,000	19.6	±397,000	19.1	±281,000	18.6	±199,000
1000	19	±262,000	18.6	±199,000	18.1	±140,000	17.5	±93,000
2000	18.5	±185,000	18.1	±140,000	17.8	±114,000	17	±66,000
3750	18.1	±140,000	17.8	±114,000	17.3	±81,000	16.6	±50,000
7500	17.7	±106,000	17.3	±81,000	16.9	±61,000	16.2	±38,000

Table 10: Effective resolution of the strain gauge value in bits for the measurement range 32 to 256 mV/V

1.1.2.12.5.3 A/D converter configuration

Name:
ConfigOutput01

The data rate and measurement range of the A/D converter can be configured in this register.

Data type	Values	Bus controller default setting
USINT	See bit structure.	13

Bit structure:

Bit	Description	Value	Information
0 - 3	Data rate f_{DATA} (samples per second):	0000	2.5
		0001	5
		0010	10
		0011	15
		0100	25
		0101	30
		0110	50
		0111	60
		1000	100
		1001	500
		1010	1000
		1011	2000
		1100	3750
		1101	7500 (bus controller default setting)
		1110	Synchronous mode[1)]
		1111	Reserved
4 - 6	Standard measurement range (bit 6 = 0)	000	16 mV/V (bus controller default setting)
		001	8 mV/V
		010	4 mV/V
		011	2 mV/V
	Extended measurement range (bit 6 = 1)[2)]	100	256 mV/V
		101	128 mV/V
		110	64 mV/V
		111	32 mV/V
7	Reserved	0	(must be 0)

1) The A/D converter is synchronized as much as possible with the X2X Link network. Starting with firmware version 2.
2) Firmware version 4 or later

Synchronous mode

With firmware version 2 and later, the module's analog/digital converter (A/D converter) can be operated and read synchronously to the X2X Link network. Synchronous mode is enabled by selecting the respective operating mode in register "ConfigOutput01" on page 46. A time between 200 and 2000 µs must be set in register "ConfigCycletime01" on page 47 for this. If this time is a whole number factor or multiple of the configured cycle time of X2X Link, then the A/D converter is read synchronously to X2X Link.

Information:

The A/D converter cycle time must be ≥1/4 of the X2X cycle time!

Bit 2 in *Module status* is set (i.e. A/D converter not running synchronously)...

- ... If the configured A/D converter cycle time cannot be synchronized with X2X Link.
- ... If the module is still in the settling phase.

Jitter, dead time and settling time:

Jitter A/D converter cycle times <1500 µs A/D converter cycle times >1500 µs	 Max. ±1 µs Max. ±4 µs
X2X link dead time	$50\ \mu s + \frac{\text{X2X cycle time}}{128}$
Settling time Firmware version ≤4 Firmware version ≥5	 Max. 150 x A/D converter cycle time 150 x X2X cycle time

The settling time corresponds to the time needed until the A/D converter can be operated after enabling synchronous mode or following conversion of the A/D converter cycle time.

1.1.2.12.5.4 A/D converter cycle time

Name:
ConfigCycletime01

This register is only used in Synchronous mode. If synchronous mode is enabled in the A/D converter configuration, then the module attempts to operate the A/D converter as synchronously as possible to X2X Link (based on the A/D converter cycle time set in this register). It is of course necessary for the X2X Link cycle time and the A/D converter cycle time to have a certain ratio. The following conditions must be observed:

1) A/D converter cycle time ≥ 1/4 X2X cycle time
2) A/D converter cycle time corresponds to a whole number factor or multiple of the X2X cycle time
3) A/D converter cycle time must be in the range 50 to 2000 µs

Data type	Value
UINT	50 to 2000

1.1.2.12.5.5 A/D converter clock frequency shift

Name:
AdcClkFreqShift01

In rare cases, strain gauge modules connected to neighboring slots can influence one another. This can result in temporary, minimal deviations in measured values. This can only occur if the sigma-delta A/D converters on the neighboring strain gauge modules are operated at exactly the same clock frequency.

In most cases, these clock frequencies vary slightly due to part variances. When they are the same however, this register on the strain gauge module provides a safe way for an application to prevent this type of mutual influence.

Data type	Value
SINT	-128 to 127

This register can be used to vary the clock frequency in increments of 200 ppm. Setting values from -50 to 50 cover a range of -10000 ppm to 10000 ppm. This corresponds with -1% to 1%.

Values beyond this range will cause activation of a default mode. The frequency shift is derived from the last 2 digits of the serial number by the module firmware. This saves time that would otherwise be needed for programming, provided that the last two digits of the serial numbers on the neighboring modules are not the same

Register value	Frequency shift in ppm	Example of a sampling rate[1)]
127	((SerialNo. modulo 100) - 50) * (-200) ppm	Based on the serial number
...	...	...
51	((SerialNo. modulo 100) - 50) * (-200) ppm	Based on the serial number
50	10000	505
49	9800	504.9
...	...	...
2	400	500.2
1	200	500.1
0	0	500
-1	-200	499.9
-2	-400	499.8
...	...	...
-50	-10000	495
-51	((SerialNo. modulo 100) - 50) * (-200) ppm	Based on the serial number
...	...	...
-128	((SerialNo. modulo 100) - 50) * (-200) ppm	Based on the serial number

1) Nominal sampling rate of 500 samples per second

Important:

As shown in the table above, shifting the A/D converter clock frequency will equally shift the A/D converter sampling rate. Shifting the A/D converter clock frequency too much can cause problems with disturbance suppression particularly when a very specific sampling rate has been defined to suppress existing disturbances (e.g. 50 Hz to suppress the 50 Hz hum). See also "Filter characteristics of the sigma-delta A/D converter" on page 39.
It's situations like this where the option to manually shift the frequency in the I/O configuration or ASIOACC library should be utilized rather than relying on the default frequency shift that is based on the serial number.

A frequency shift like the one shown below would be sufficient to prevent modules from influencing one another and would not cause any noticeable difference to the filter characteristics.

Slot	1	2	3	4	5	6	...
A/D converter clock frequency shift	0	2	-1	1	-2	0	...

Information:

- **This register has no effect in synchronous mode because the firmware regulates the A/D converter clock frequency in such a way that the A/D converter cycle is synchronous with the X2X cycle.**
- **When writing to this register using the ASIOACC library, only the lowest value byte of the written value is accepted. For example, the value 256 (=0x100) is identical to the value 0 (=0x00).**

1.1.2.12.6 Register for "Function model 1 - Multisampling"

1.1.2.12.6.1 Module status

Name:
StatusInput01

This register contains the current state of the module.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	A/D converter values	0	Valid A/D converter value
		1	Invalid A/D converter value
1	Line monitoring	0	OK
		1	Open circuit An open circuit was found during at least one measurement in this X2X cycle. This bit is reset if all measurements are OK after correcting this error, i.e. it does not have to be acknowledged.
2	Synchronous mode	0	A/D converter runs synchronous to X2X Link
		1	A/D converter does not run synchronous to X2X Link
3 - 7	Reserved	-	

1.1.2.12.6.2 Strain gauge value - Multiple

Name:
AnalogInput01 to AnalogInput10

This register contains the raw value determined by the A/D converter for the full-bridge strain gauge with 16-bit resolution. The module returns between 3 and 10 measured values per X2X cycle depending on the configuration.

Effective resolution

In principle, the effective resolution of the A/D converter is dependent on the data rate and measurement range (see "Effective resolution of the A/D converter" on page 40).

The following table shows how the effective resolution (in bits) or effective range of values of the strain gauge value depend on the module configuration (data rate, measurement range):

1.1.2.12.6.3 A/D converter configuration

Name:
ConfigGain01_MultiSample

The measurement range for the A/D converter can be configured in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Standard measurement range (bit 2 = 0)	000	16 mV/V
		001	8 mV/V
		010	4 mV/V
		011	2 mV/V
	Extended measurement range (bit 2 = 1)[1)]	100	256 mV/V
		101	128 mV/V
		110	64 mV/V
		111	32 mV/V
3 - 7	Reserved	0	(must be 0)

1) Firmware V4 and later. In the standard measurement range (2 to 16 mV/V), open-circuit detection works reliably at all adjustable data rates. In the extended measurement range (32 to 256 mV/V), open-circuit detection does not work reliably (because of the variable input impedance of the amplifier in relation to the set data rate).

1.1.2.12.6.4 A/D converter cycle time

Name:
ConfigCycletime01_MultiSample

The A/D converter cycle time can be configured in this register.

In order for multisampling to work, the X2X cycle time must be divisible by the A/D converter cycle time to produce a whole number.

Data type	Value	Information
USINT	0	50 µs (default)
	1	100 µs
	2 to 255	Reserved

1.1.2.12.6.5 Number of measured values

If the X2X cycle time is too short, then not all 10 measurements can be performed. To reduce the load on X2X Link, it makes sense to only transfer as many values as measurements that can be made. This is why it is possible to configure the number of measured values to be transferred (see "Function model 1 - Multisampling" on page 43).

Example: A/D converter cycle time = 50 µs

X2X cycle time	Number of measured values to be transferred
250 µs	5
300 µs	6
350 µs	7
400 µs	8
450 µs	9
≥500 µs	10

Example: A/D converter cycle time = 100 µs

X2X cycle time	Number of measured values to be transferred
300 µs	3
400 µs	4
500 µs	5
600 µs	6
700 µs	7
800 µs	8
900 µs	9
≥1 ms	10

1.1.2.12.7 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
250 µs

1.1.2.12.8 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

There is no limitation or basic dependency on the bus cycle time. In function model "0 - Standard", the I/O update time is defined using registers "ConfigOutput01" on page 46 and "ConfigCycletime01" on page 47.

Depending on the setting in register "ConfigCycletime01_MultiSample" on page 50, the I/O update time in function model "1 - Multiple sampling" is 50 or 100 µs.

1.2 X20(c)AI1744-3

This data sheet describes 2 module revisions. The module revision is laser-marked on the side of the module. Select the desired module revision from the following table to view its description.

Module	Revision	Page
X20AI1744-3	≥G0	52
X20cAI1744-3	All	
X20AI1744-3	<G0	82

1.2.1 X20(c)AI1744-3 with Rev. ≥G0

1.2.1.1 General information

This module works with both 4-wire and 6-wire strain gauge load cells. The concept applied by the module requires compensation in the measurement system. This compensation eliminates the absolute uncertainty in the measurement circuit, such as component tolerances, effective bridge voltage or zero point offset. The measurement precision refers to the absolute (compensated) value, which will only change as a result of changes in the operating temperature.

- 1 full-bridge strain gauge input
- Data output rate configurable from 0.1 Hz to 7.5 kHz
- Special operating modes (synchronous mode and multiple sampling)
- Configurable filter level

1.2.1.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, method 4, exposure 21 days

1.2.1.2.1 Starting temperature

The starting temperature describes the minimum permissible ambient temperature in a voltage-free state at the time the coated module is switched on. This is permitted to be as low as -40°C. During operation, the conditions as specified in the technical data continue to apply.

Information:

It is important to absolutely ensure that there is no forced cooling by air currents in the closed control cabinet, e.g. due to the use of a fan or ventilation slots.

1.2.1.3 Order data

Order number	Short description	Figure
	Analog inputs	
X20AI1744-3	X20 analog input module, 1 full-bridge strain gauge input, 24-bit converter resolution, 5 Hz input filter	
X20cAI1744-3	X20 analog input module, coated, 1 full-bridge strain gauge input, 24-bit converter resolution, 5 Hz input filter	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 11: X20AI1744-3, X20cAI1744-3 - Order data

1.2.1.4 Technical data

Order number	X20AI1744-3	X20cAI1744-3
Short description		
I/O module	1 full-bridge strain gauge input	
General information		
B&R ID code	0xA4EF	0xEB00
Status indicators	Channel status, operating status, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Open circuit	Yes, using status LED and software	
Input	Yes, using status LED and software	
Power consumption		
Bus	0.01 W	
Internal I/O	0.5 W	
Additional power dissipation caused by actuators (resistive) [W]	Max. +0.36 [1]	
Certifications		
CE	Yes	
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X	
UL	cULus E115267 Industrial control equipment	
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5	
EAC	Yes	
KC	Yes	-
Full-bridge strain gauge		
Strain gauge factor	2 to 256 mV/V, configurable using software	
Connection	4- or 6-wire connections [2]	
Input type	Differential, used to evaluate a full-bridge strain gauge	
Digital converter resolution	24-bit	
Conversion time	Depends on the configured data output rate	
Data output rate	0.1 - 7500 samples per second, configurable using software (f_{DATA})	
Input filter		
Cutoff frequency	5 Hz	
Order	3	
Slope	60 dB	
ADC filter characteristics	Sigma-delta, see section "Filter characteristics of the sigma-delta A/D converter"	
Operating range / Measurement sensor	85 to 5000 Ω	
Influence of cable length [3]	See section "Calculation example".	
Input protection	RC protection	
Common-mode range	0 to 3 VDC Permissible input voltage range (with regard to the potential strain gauge GND) on the inputs "Input +" and "Input -"	
Isolation voltage between input and bus	500 V_{Eff}	
Conversion procedure	Sigma-delta	

Table 12: X20AI1744-3, X20cAI1744-3 - Technical data

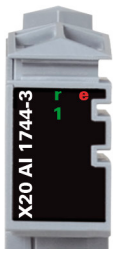
Order number	X20AI1744-3	X20cAI1744-3
Output of digital value		
Broken bridge supply line	Value approaches 0	
Broken sensor line	Value approaching ±end value (status bit "Line status monitoring" is set in register "Module status")	
Valid range of values	0xFF800001 to 0x007FFFFF (-8,388,607 to 8,388,607)	
Strain gauge supply		
Voltage	5.5 VDC / max. 65 mA	
Short-circuit and overload resistant	Yes	
Voltage drop for short-circuit protection	Max. 0.2 VDC at 65 mA and 25°C	
Quantization [4]		
LSB value (16-bit)		
2 mV/V	336 nV	
4 mV/V	671 nV	
8 mV/V	1.343 µV	
16 mV/V	2.686 µV	
32 mV/V	5.371 µV	
64 mV/V	10.74 µV	
128 mV/V	21.48 µV	
256 mV/V	42.97 µV	
LSB value (24-bit)		
2 mV/V	1.31 nV	
4 mV/V	2.62 nV	
8 mV/V	5.25 nV	
16 mV/V	10.49 nV	
32 mV/V	20.98 nV	
64 mV/V	41.96 nV	
128 mV/V	83.92 nV	
256 mV/V	167.85 nV	
Temperature coefficient		
Rev. ≥E0	10 ppm/°C	-
Rev. <E0	30 ppm/°C	-
Max. gain drift	12 ppm/°C [5]	
Max. offset drift	2 ppm/°C [6]	
Nonlinearity	<10 ppm [6]	
Electrical properties		
Electrical isolation	Bus isolated from analog input and strain gauge supply voltage Channel not isolated from I/O power supply	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation elevation above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
Degree of protection per EN 60529	IP20	
Ambient conditions		
Temperature		
Operation		
Horizontal mounting orientation	-25 to 60°C	
Vertical mounting orientation	-25 to 50°C	
Derating	See section "Hardware configuration"	
Starting temperature	-	Yes, -40°C
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical properties		
Note	Order 1x terminal block X20TB12 separately Order 1x bus module X20BM11 separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Pitch	$12.5^{+0.2}$ mm	

Table 12: X20AI1744-3, X20cAI1744-3 - Technical data

1) Depends on the full-bridge strain gauge being used.
2) With 6-wire connections, line compensation does not function (see section "Connection examples").
3) Sensor cable with twisted and shielded conductors, cable length as short as possible, cable routing separate from load circuits, without intermediate terminal to the sensor.
4) Quantization depends on the strain gauge factor.
5) Based on the current measured value.
6) Based on the entire measurement range.

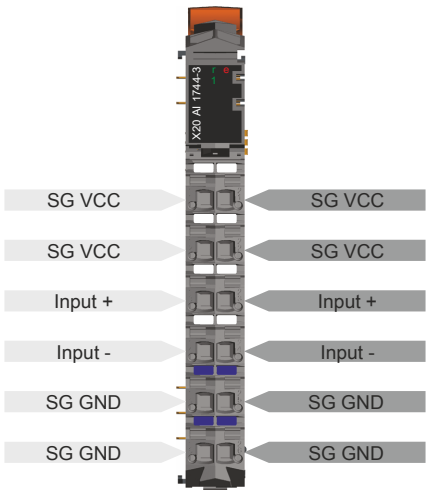
1.2.1.5 LED status indicators

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 system user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	1	Green	Off	Possible causes: • Open circuit • Sensor is disconnected • Converter is busy
			On	Analog/digital converter running, value OK

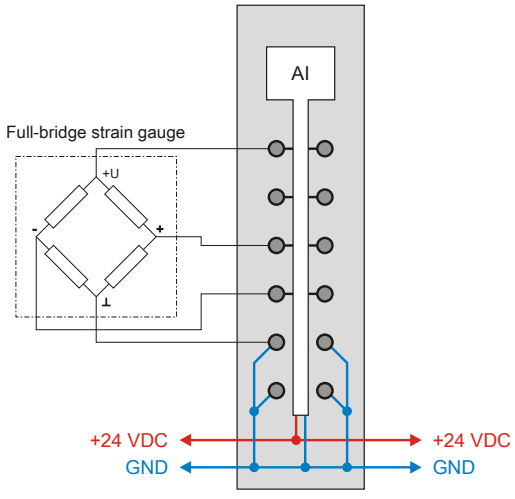
1) Depending on the configuration, a firmware update can take up to several minutes.

1.2.1.6 Pinout



1.2.1.7 Connection examples

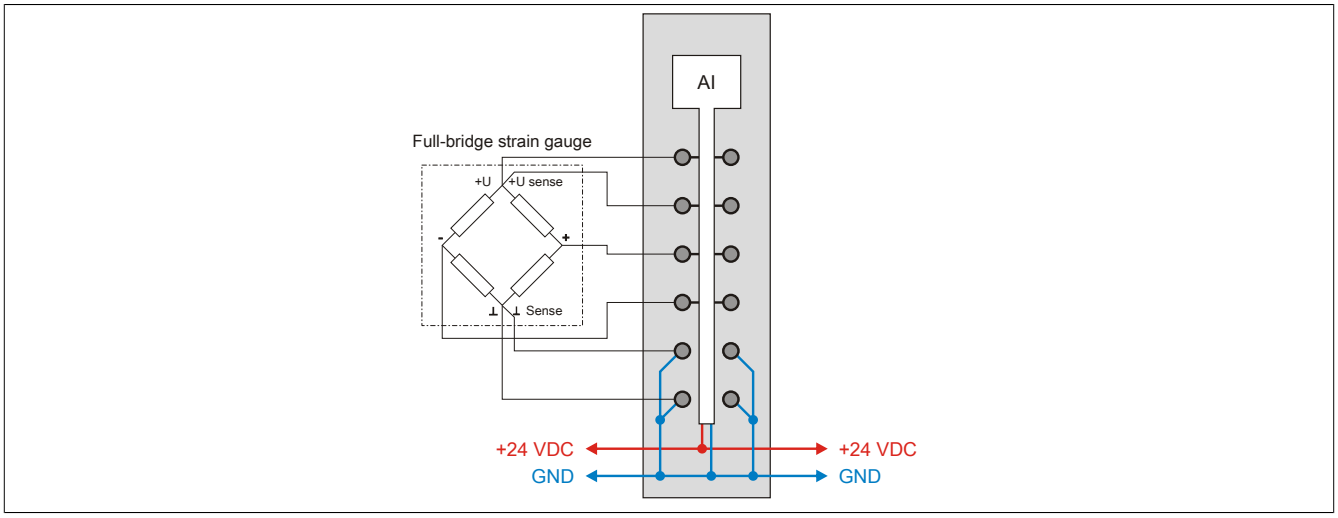
Full-bridge strain gauge with 4-wire connections



Full-bridge strain gauge with 6-wire connections

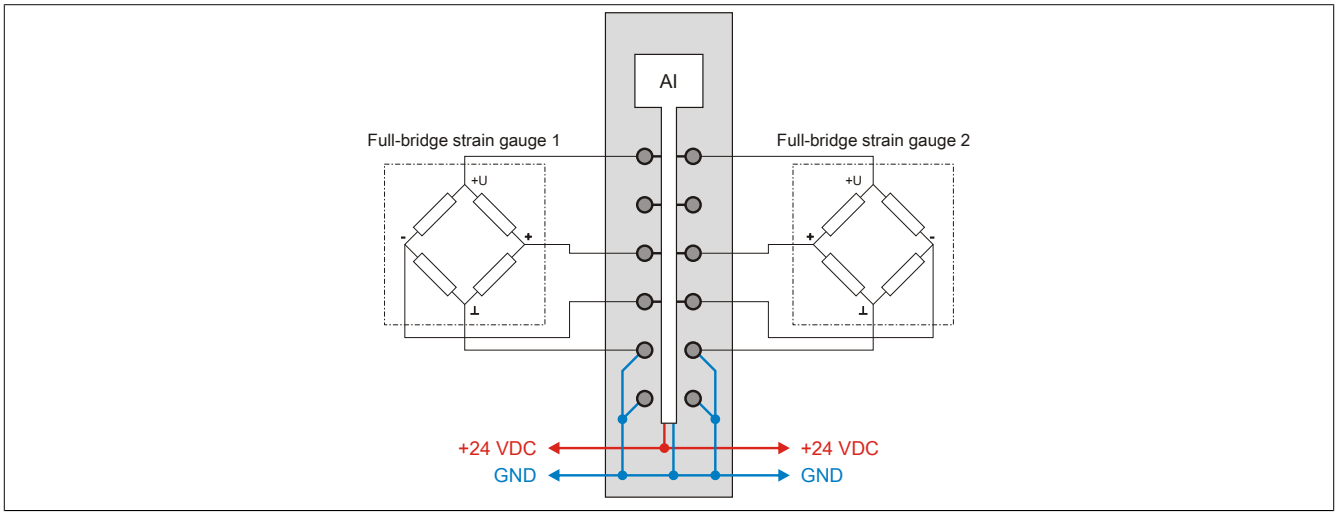
Full-bridge strain gauges can be connected to this module with 6-wire connections. Line compensation is not supported by the module, however. The sense lines are short circuited by the internally connected strain gauge VCC and GND connections (see "Input circuit diagram" on page 57). The measurement precision is therefore affected by changes in operating temperature. Longer cable lengths and smaller cable cross sections also increase the potential for errors in the measurement system.

In order to reduce cable resistance, the sense lines should be connected in parallel with the strain gauge supply lines. Optimal signal quality can be obtained by using a shielded twisted pair cable. The connections for the strain gauge supply lines, the sensor lines and the bridge differential voltage lines should each use one twisted pair cable.



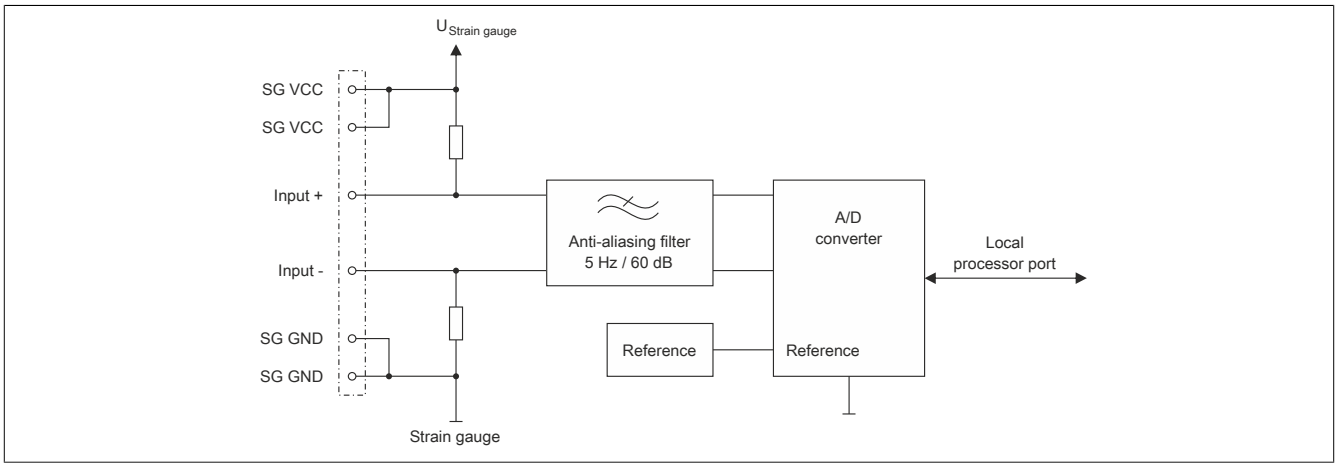
Parallel connection of 2 full-bridge strain gauges (4-wire connections)

If connecting the full-bridge strain gauges in parallel, the manufacturer's guidelines must be observed.



When connecting 3 or more full-bridge strain gauges in parallel, 2 lines must be connected together in an X20 terminal block.

1.2.1.8 Input circuit diagram

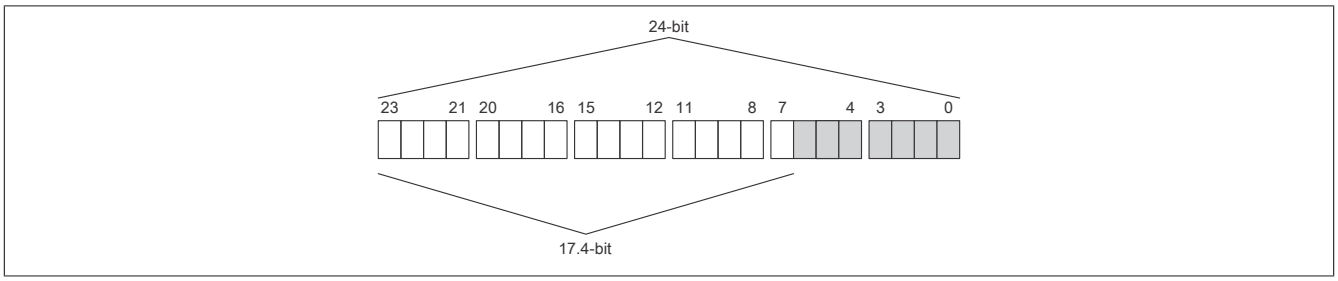


1.2.1.9 Effective resolution of the A/D converter

The A/D converter on the module provides a 24-bit measured value. The actual attainable noise-free resolution is always less than 24-bit, however. This "effective resolution" depends on the data rate and measurement range.

Example:

Based on the conversion method, a data rate of 2.5 Hz and a specified measurement range of 2 mV/V result in an effective resolution of17.4 bits:



The low-order bits (grayed out) contain only noise instead of valid values and are therefore not permitted to be evaluated.

With "Function model 1 - Multisampling", only the highest 16 bits are made available.

1.2.1.10 Calculation example

The following example shows the influence of the length of the measuring cable on the bridge voltage of the module and the quantization calculated with it.

1.2.1.10.1 Bridge voltage

Although the measuring bridge must be adjusted with the module, the cable length has an influence on the accuracy of the measurement. The reason for this is the voltage drop on the power supply lines of the measuring bridge. As a result, the strain gauge supply voltage at the measuring bridge no longer amounts to the full 5.5 V. The reduced bridge voltage also has an effect on the quantization.

Example

Characteristics of the measuring device used:

- Full-bridge strain gauge with 4-wire connections
- Material-dependent conductivity of the cable (copper: $12\frac{m}{\Omega \cdot mm^2}$)
- Cross section of the cable: 22 AWG = 0.34 mm²
- Length of the cable: 5 m
- Nominal current of the measuring bridge: 15 mA
- Bridge voltage of the module: 5.5 V

Actual bridge voltage taking the voltage drop on the measuring line into account:

$$5.5V - \frac{2 \cdot 5\,m}{12\frac{m}{\Omega \cdot mm^2} \cdot 0.34\,mm^2} \cdot 0.015A = 5.463\ V$$

The quantization must be calculated using the actual calculated bridge voltage (see "Quantization" on page 59).

1.2.1.10.2 Quantization

In a weighing application, the corresponding weight located on the connected load cell should be determined from the value derived from the module.

Example

The characteristics of the strain gauge load cell are as follows:

- Rated load: 1000 kg
- Strain gauge factor: 4 mV/V
- Actual bridge voltage: 5.463 V

Maximum quantization:
Multiplying the bridge factor of the strain gauge load cell with the bridge supply voltage from the module results in the value for the positive full-scale deflection at a specified rated load of 1000 kg:

4 mV/V · 5.5 V = 22 mV

Actual quantization:
Taking the voltage drop on the measuring line into account, the actual bridge voltage is 5.463 V (for the calculation, see section "Bridge voltage" on page 58). If this voltage is multiplied by the strain gauge factor of 4 mV/V, the following actual quantization results:

4 mV/V · 5.463 V = 21.85 mV

These 21.85 mVcorrespond to 99.3% of the maximum possible measurement range.

Information:

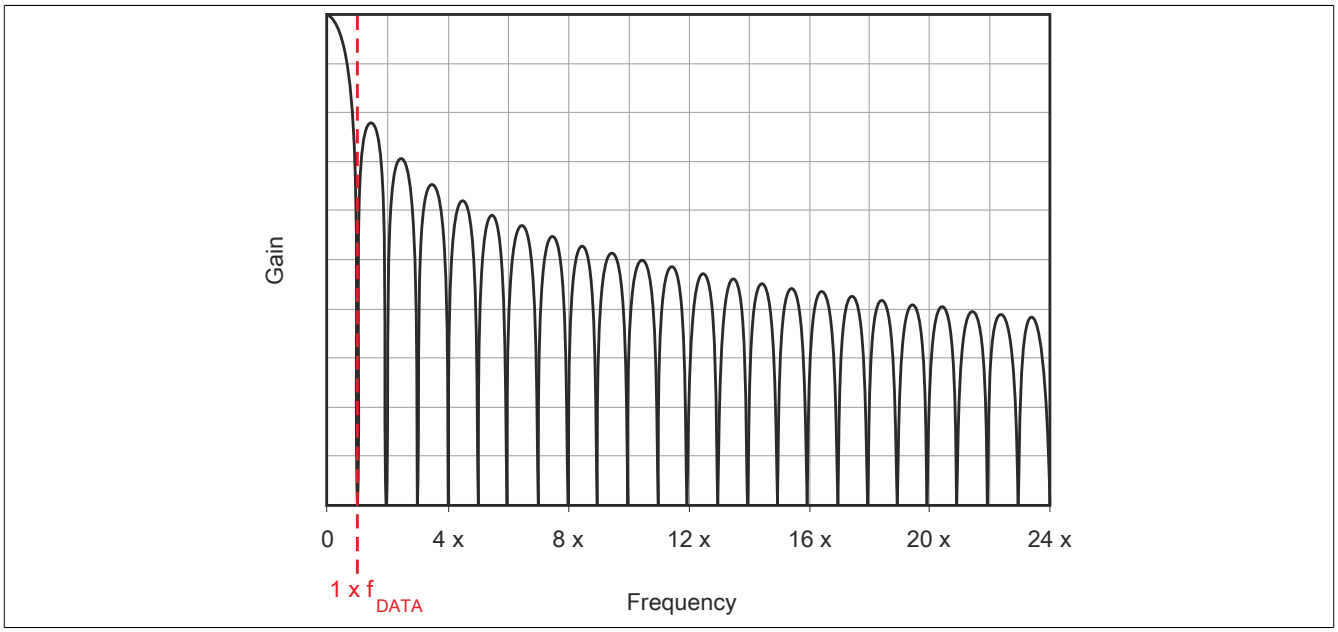
If the quantization decreases, the maximum possible effective resolution also decreases (see "Effective resolution of the A/D converter" on page 57).

With a simple Rule of Three calculation, the corresponding value can be calculated (as seen in the table) from weight to the converter value and vice versa. This simplified theoretical approach is only valid for an ideal measurement system. Calibration of the entire measurement system is recommended because not only the module, but particularly the strain gauge bridges exhibit tolerances (offset, gain). When taring, the gradient offset is recalculated and the gain of the linear equation is determined when normalized. In addition to the calculation displayed in the table, these calculations must also be carried out in the application.

24-bit value of the module		Quantization	Corresponding weight
0x007F FFFF	8,388,607	21.85 mV	1000 kg
0x0000 0001	1	2.61 nV	0.119 g
0x0000 20C3	8387	21.85 µV	1 kg
0x0001 0000	65536	170.7 µV	7.81 kg

The values for 1 LSB are also included in the module's technical data under item "Quantization" (1 LSB each for 16 bits and 24 bits).

1.2.1.11 Filter characteristics of the sigma-delta A/D converter

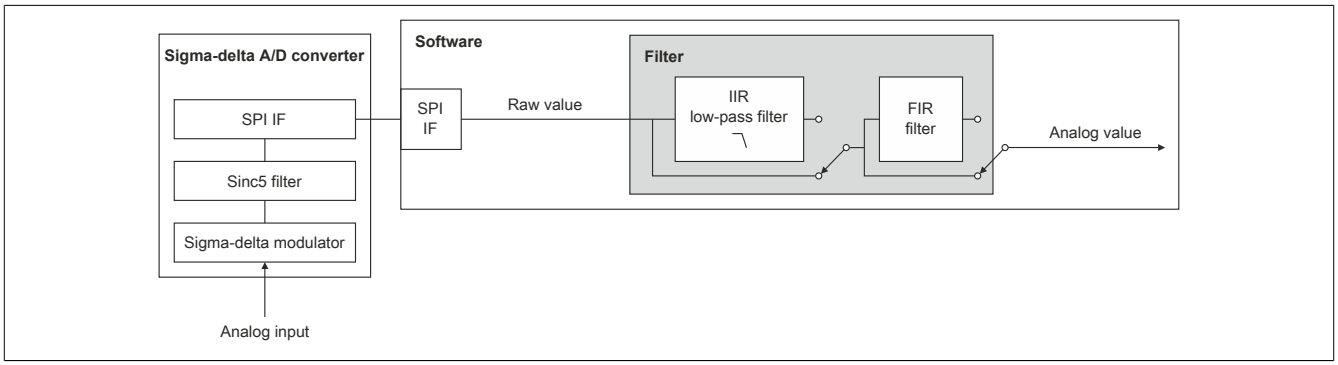


1.2.1.12 Software filters

2 filters are available for the analog input. They can be individually enabled and configured at runtime. By default, both filters are disabled when the device is switched on. The filters are controlled and configured using "Function model 2 - Extended filter".

In order to allow the filter behavior to be adapted to the measuring situation or machine cycle (high dynamics and low precision or low dynamics and high precision), the filter characteristics of both the IIR low-pass filter as well as the FIR filter can be changed synchronously at any time.

Filter diagram



1.2.1.12.1 IIR low-pass filter

1.2.1.12.1.1 General information

The IIR low-pass filter is used to generally smooth and increase the resolution of the analog value. The filter works according to the following formula:

$$y = y_{Old} + \frac{x - y_{Old}}{2^{Filter\ level}}$$

x ... Current filter input value
y_{Old} ... Old filter output value
y ... New filter output value

Parameter "Filter level" in the formula above is configured using register "ConfigCommonOutput01" on page 79. "Filter level" = 0 if the IIR low-pass filter is disabled.

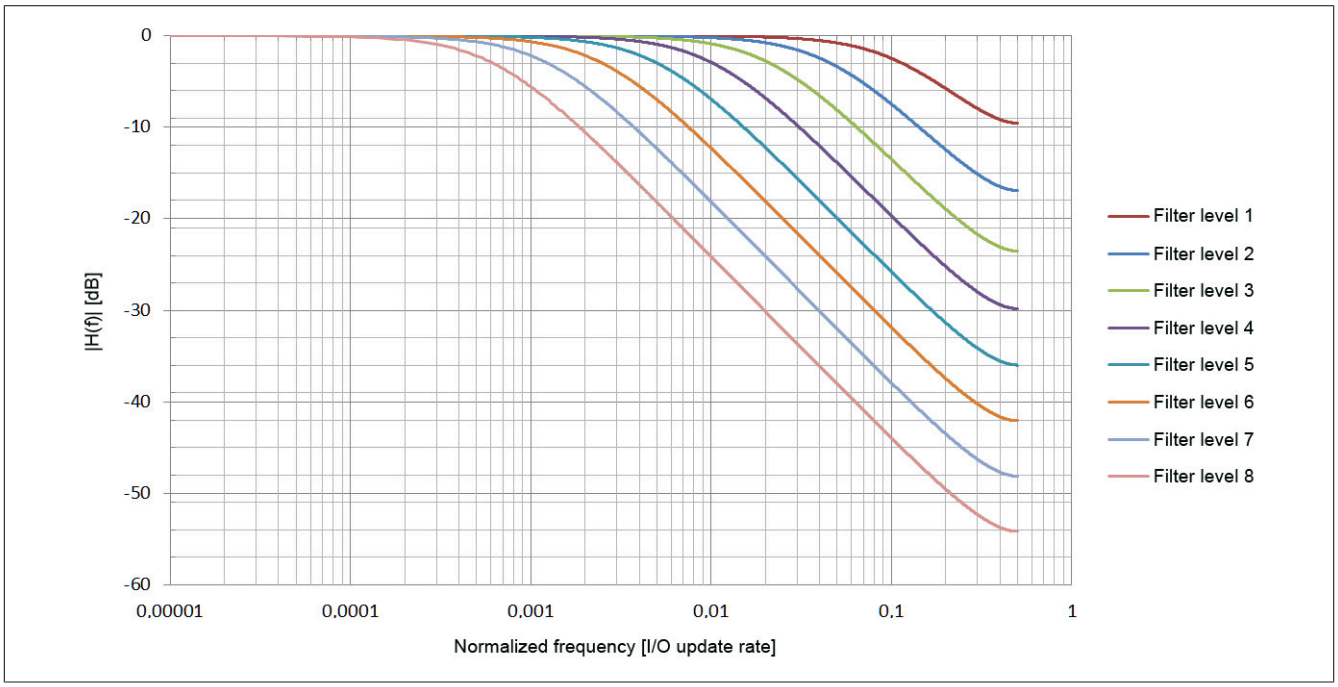
1.2.1.12.1.2 Filter characteristics of the first-order IIR low-pass filter

Limit frequency f_c

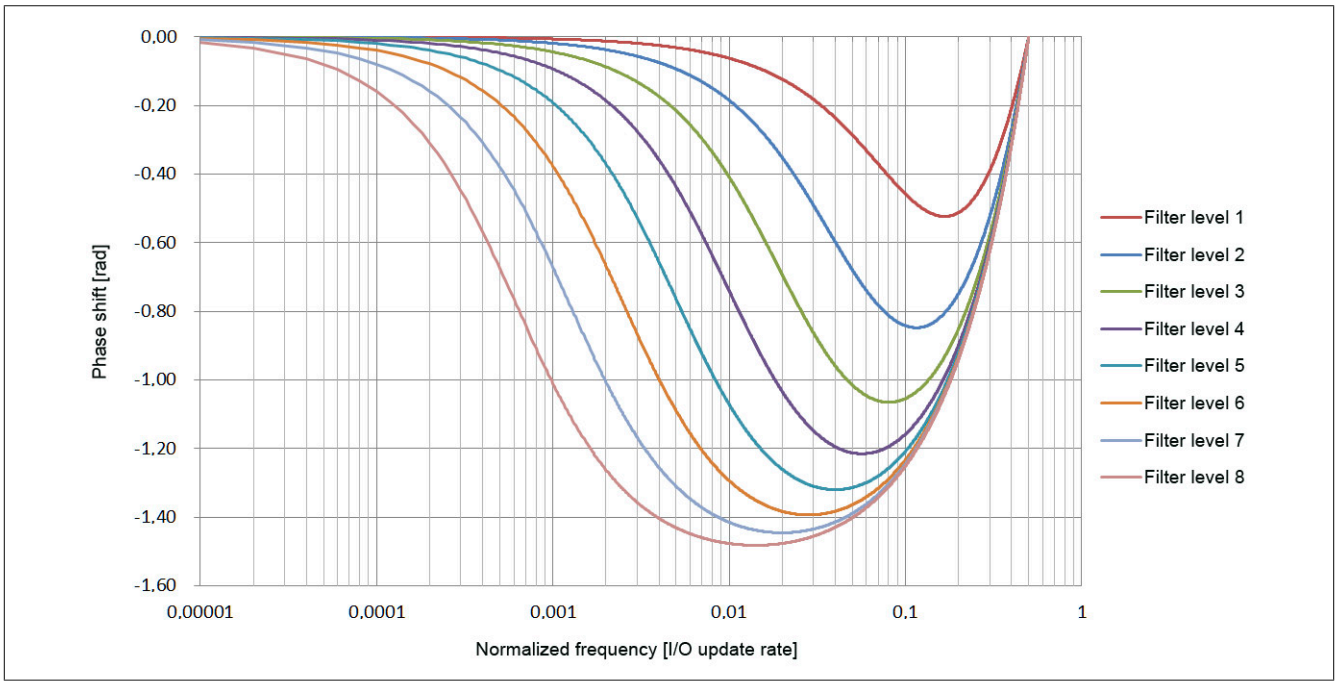
The following table provides an overview of the -3 dB limit frequency f_c depending on the configured filter level.

Filter level	Normalized f_c [I/O update rate]	f_c [Hz] I/O update rate = 15000/s	f_c [Hz] I/O update rate = 20000/s
1	0.11476	1721.4	2295.2
2	0.046	690	920
3	0.02124	318.6	424.8
4	0.01026	153.9	205.2
5	0.00504	75.6	100.8
6	0.0025	37.5	50
7	0.00124	18.6	24.8
8	0.00062	9.3	12.4

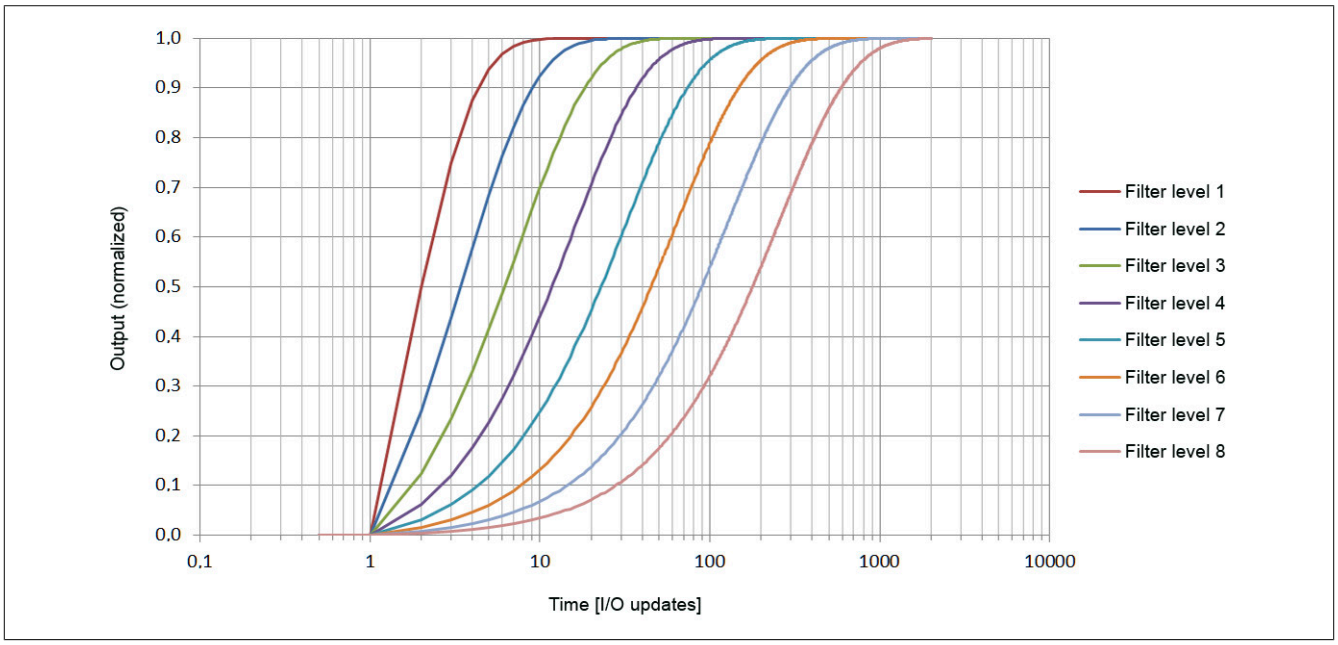
Gain of the IIR low-pass filter



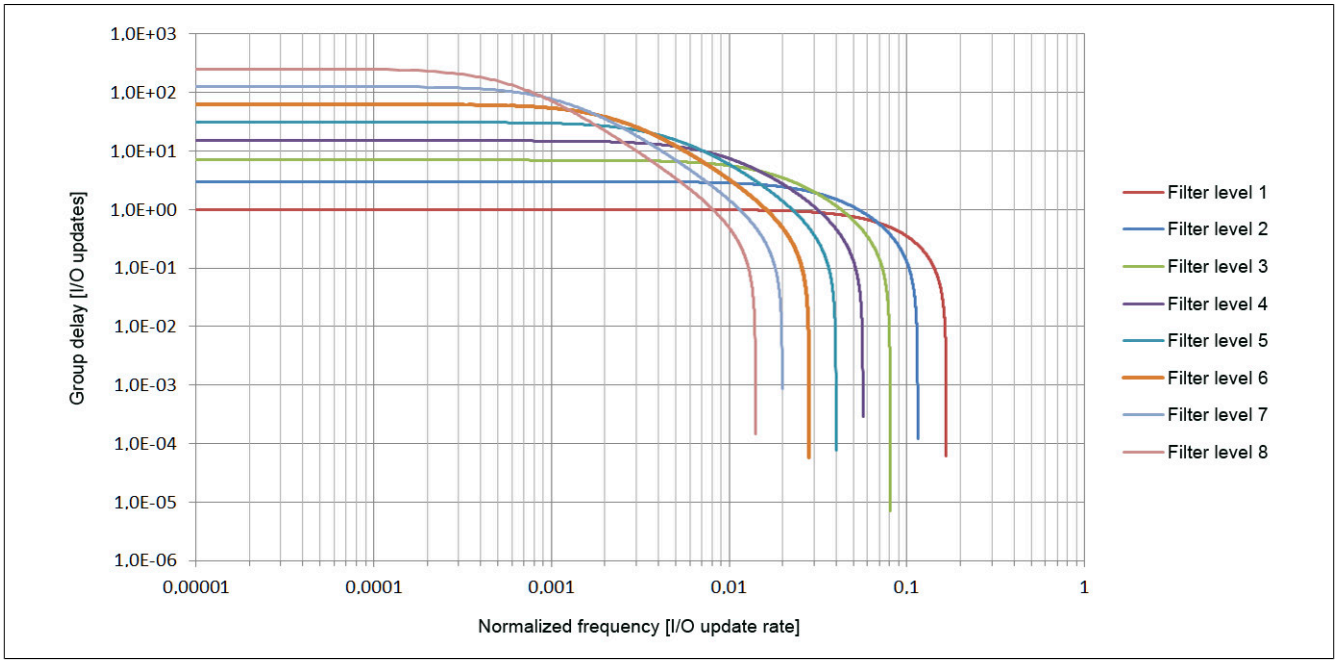
Phase shift of the IIR low-pass filter



Step response of the IIR low-pass filter



Group delay of the IIR low-pass filter



1.2.1.12.2 FIR filter

Like the IIR low-pass filter, the FIR filter can also be used to smooth out the signal and increase its resolution. In addition, configuring the filter length accordingly makes it possible to target and efficiently filter out individual interference frequencies. The source of these interference frequencies may be mechanical or electromagnetic. Multiples of these are also filtered out (as long as they are a whole-number factor of the data output rate).

Example:
Data output rate = 15000 samples/s, averaging over 15 values → "Notch" at 1 kHz (2 kHz, etc.)

When reconfiguring the filter, it takes 1/data rate (FIR filter in mode "Selectable data rate") or 1/filter frequency (FIR filter in mode"High-resolution data rate") until the filter is tuned. During tuning, bit 5 is set in register "StatusInput01" on page 81.

1.2.1.12.2.1 Characteristics of the FIR filter in mode "Selectable data rate"

The following table applies to "Function model 0 - Standard" and "Function model 254 - Bus controller" as well as for "Function model 2 - Extended filter" in mode "Selectable data rate".

			I/O update rate [Hz]		I/O update time [ms]	
Set value [1) 2)]	**Data rate (f_{Data}) [Hz]** [3) 4)]	**f_{Notch} [Hz]**	**Function models 0 and 254**	**Function model 2 (mode "Selectable data rate")**	**Function models 0 and 254**	**Function model 2 (mode "Selectable data rate")**
0000	2.5	2.5	2.5	15000	400	0.0667
0001	5	5	5	15000	200	0.0667
0010	10	10	10	15000	100	0.0667
0011	15	15	15	15000	66.6667	0.0667
0100	25	25	25	15000	40	0.0667
0101	30	30	30	15000	33.3333	0.0667
0110	50	50	50	15000	20	0.0667
0111	60	60	60	15000	16.6667	0.0667
1000	100	100	100	15000	10	0.0667
1001	500	500	500	15000	2	0.0667
1010	1000	1000	1000	15000	1	0.0667
1011	2000	2000	2000	20000	0.5	0.05
1100	3750	3750	3750	15000	0.2667	0.0667
1101	7500	7500	7500	15000	0.1333	0.0667
1110	Reserved					
1111	Reserved					

1) Function model 0 and 254: Bits 0 to 3 of register "ConfigOutput01" on page 72
2) Function model 2: Bits 0 to 3 of register "ConfigDatarateOutput01" on page 33
3) Function models 0 and 254: Data rate = 1/Filter length [s] (f_{Notch}) = I/O update rate
4) Function model 2: Data rate = 1/Filter length [s] (f_{Notch})

1.2.1.12.2.2 Characteristics of the FIR filter in mode "High-resolution data rate"

The following table applies to "Function model 2 - Extended filter".

Setpoint [0.1 Hz] 1)	Data rate (f_{Data}) [Hz]	f_{Notch} [Hz]	I/O update time [µs]
1 to 65535	Setpoint / 10	= Data rate	≈50 µs 2)

1) Setpoint from register "ConfigHighResolutionOutput01" on page 33
2) The value varies between 42 and 56 µs (see also the next section "I/O update time")

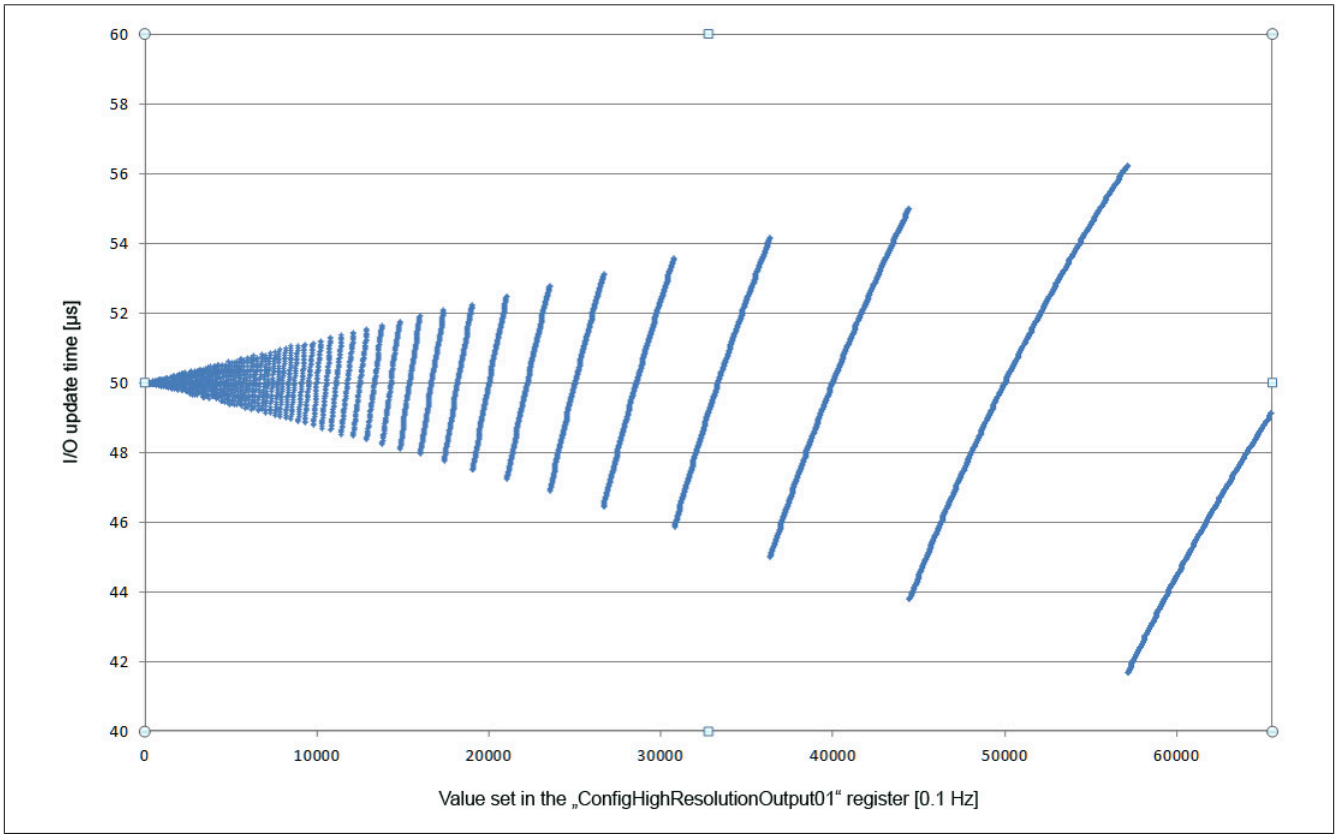
I/O update time

The value of the I/O update time depends on the setpoint and varies between 42 and 56 µs. The following formula can be used to precisely calculate the I/O update time:

I/O update time = 1e6 · (1e-4 - 10 / (Setpoint · [10 / (5e-5 · Setpoint)]))

Legend: The square brackets in the formula above mean that the calculated value must be rounded to a whole number.

The following image shows the I/O update time depending on the setpoint:

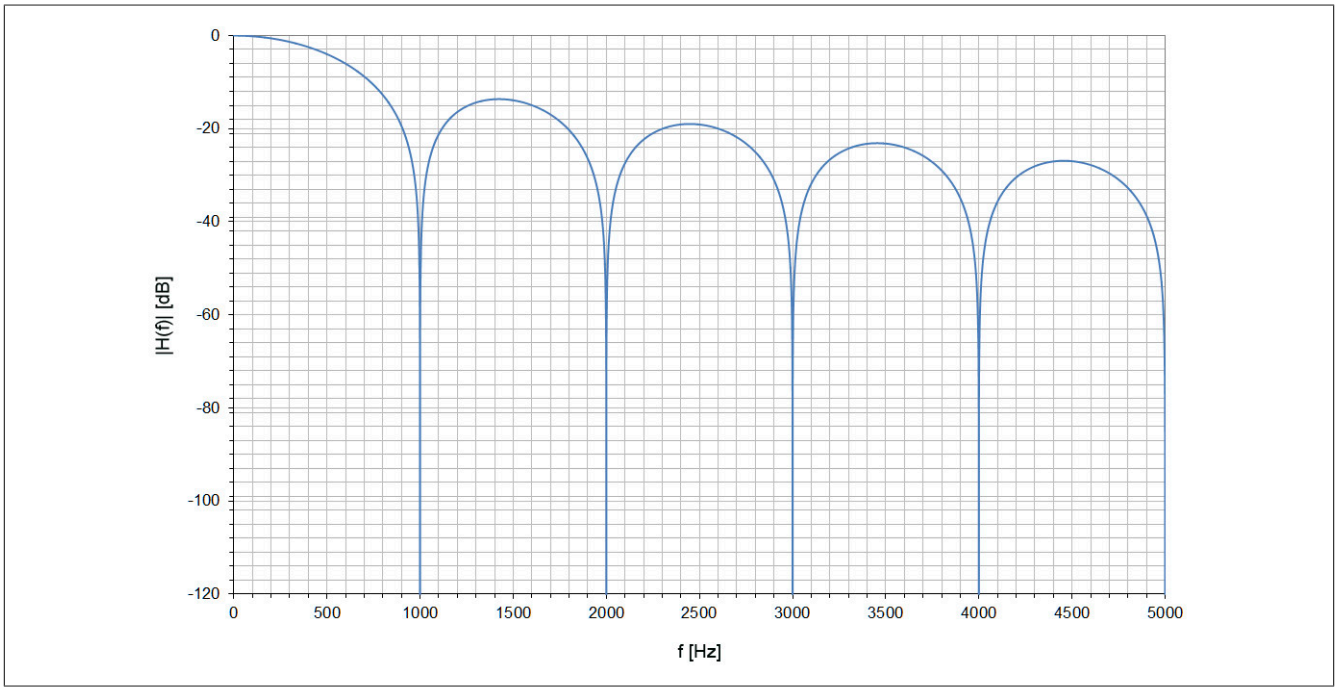


1.2.1.12.2.3 Examples for the gain of the FIR filter

Example 1

Filter setting = 10:

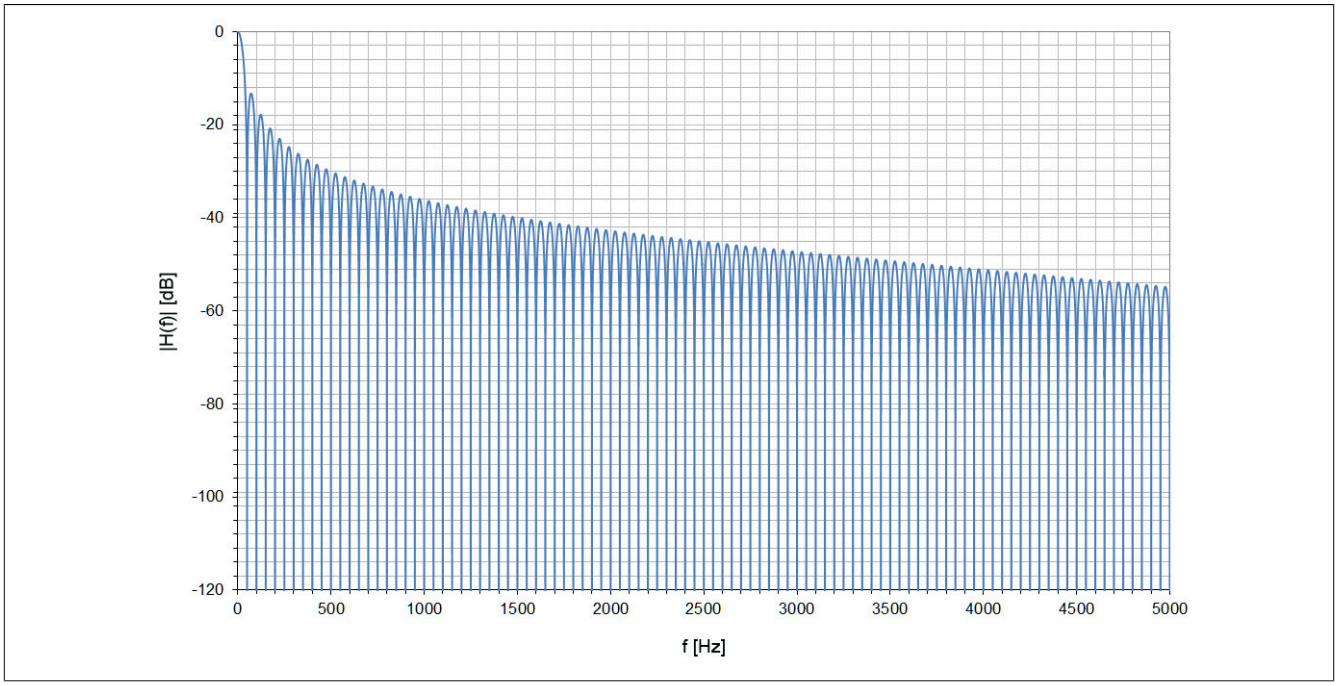
- f_{Notch} = 1000 Hz
- f_c = 439.3 Hz



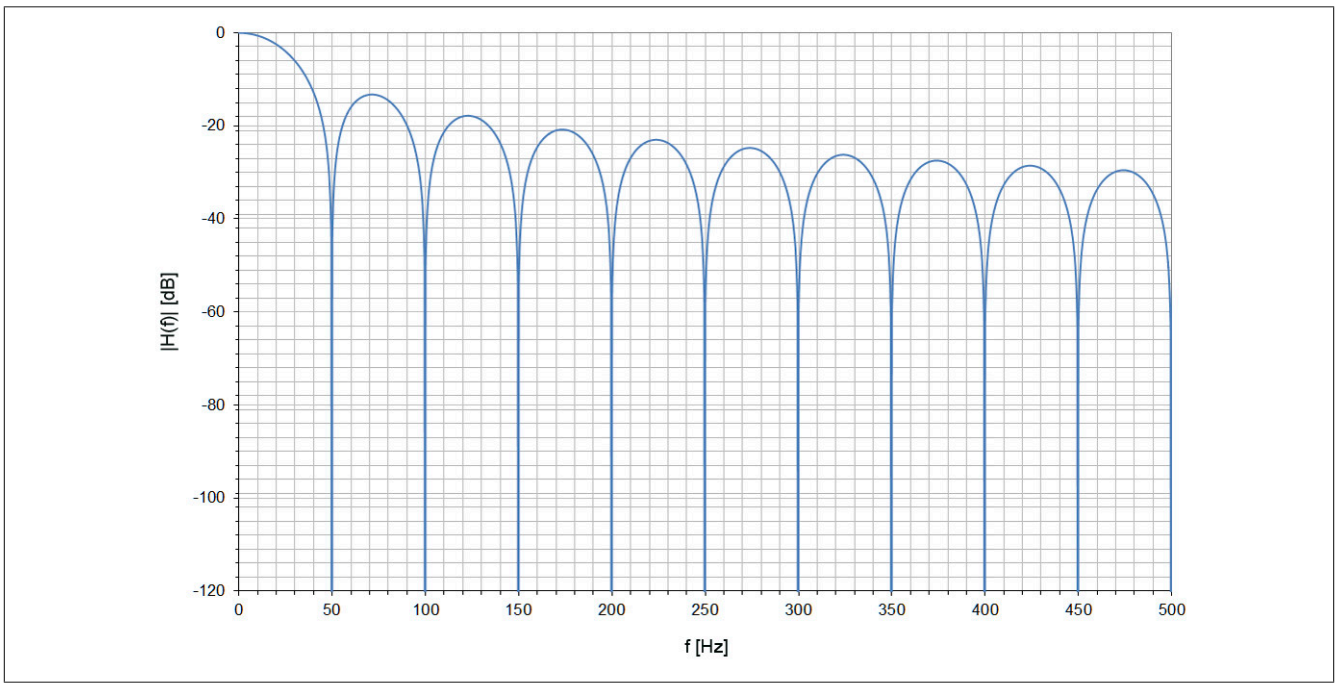
Example 2

Filter setting = 6:

- f_{Notch} = 50 Hz
- f_c = 21.8 Hz



Detailed excerpt from the filter curve shown above:

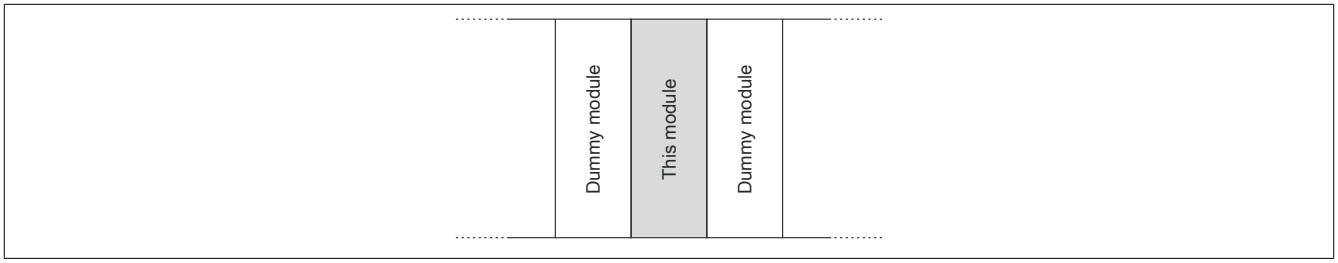


1.2.1.13 Hardware configuration

1.2.1.13.1 Hardware configuration for horizontal installation starting at 55°C ambient temperature

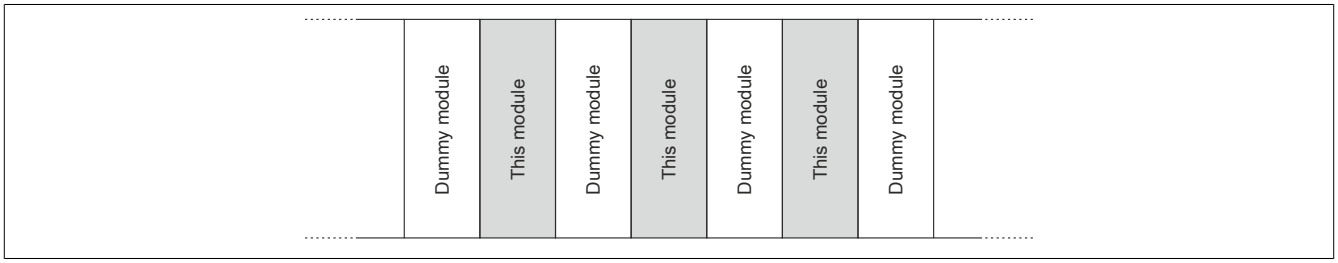
Operating a strain gauge module

Starting at an ambient temperature of 55°C, a dummy module must be connected to the left and right of the strain gauge module in a horizontal mounting orientation.



Operating multiple strain gauge modules side by side

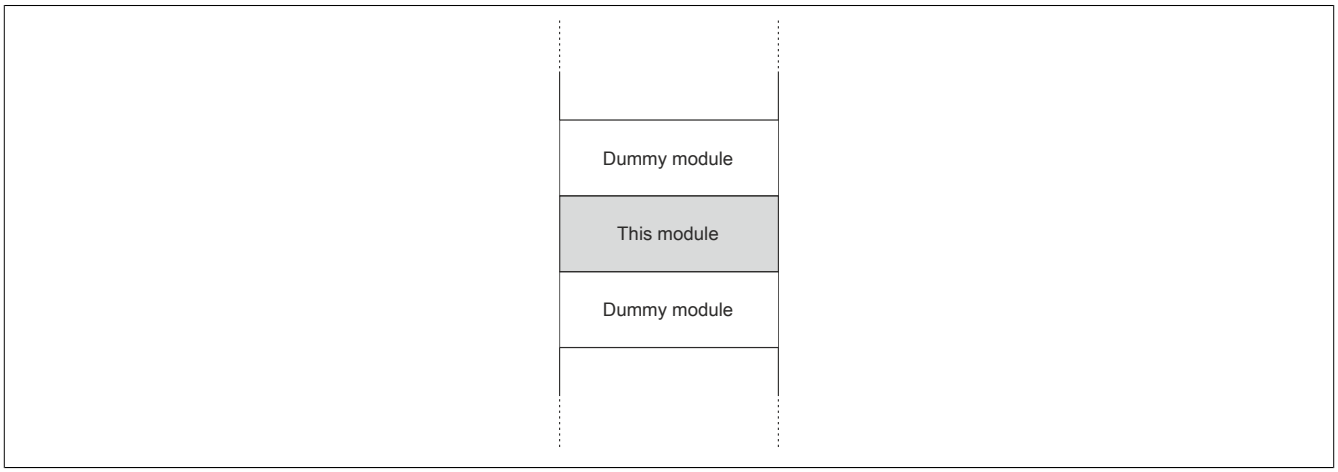
If 2 or more horizontal strain gauge modules are being operated in a cluster, the following arrangement of modules must be observed.



1.2.1.13.2 Hardware configuration for vertical installation starting at 45°C ambient temperature

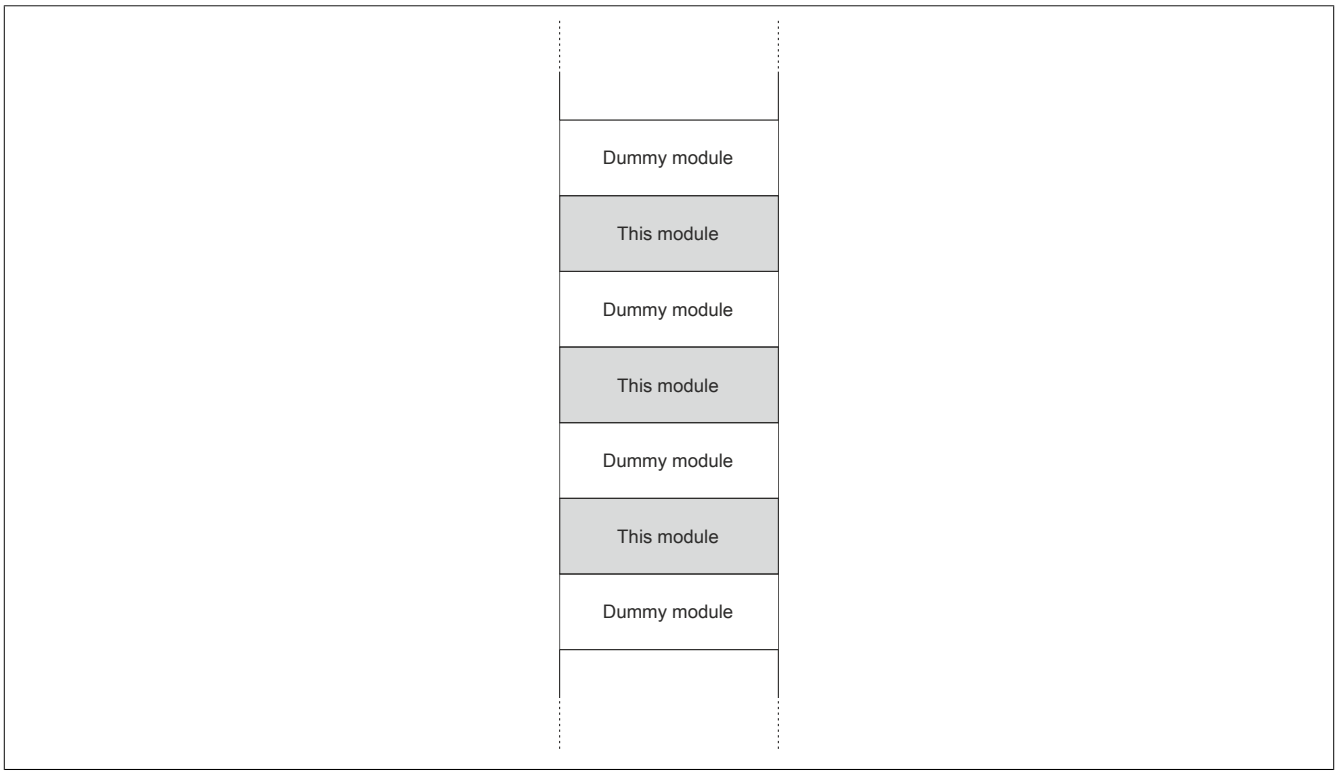
Operating a strain gauge module

Starting at an ambient temperature of 45°C, a dummy module must be connected to the left and right of the strain gauge module in a vertical mounting orientation.



Operating multiple strain gauge modules side by side

If 2 or more vertical strain gauge modules are being operated in a cluster, the following arrangement of modules must be observed.



1.2.1.14 Register description

1.2.1.14.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 system user's manual.

1.2.1.14.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration						
16	ConfigOutput01 (A/D converter configuration)	USINT			•	
18	ConfigCycletime01	UINT				•
32	AdcClkFreqShift01	USINT				•
Analog signal - Communication						
2	StatusInput01	USINT	•			
4	AnalogInput01	DINT	•			

1.2.1.14.3 Function model 1 - Multisampling

In this function model, the A/D converter is operated synchronously to X2X Link with a predefined A/D converter cycle time. The value is configurable as 50 or 100 µs.

The module returns between 3 and 10 measured values per X2X cycle depending on the configuration. With an X2X cycle time of 400 µs and A/D converter cycle time of 50 µs, exactly 8 measurements are performed and the module can return 8 values (strain gauge value 01 to strain gauge value 08).

If a longer cycle time is used, the values returned correspond to the last measurements. If using an X2X cycle time that is not a whole number multiple of the A/D converter cycle time, then the conversion cannot be synchronized with X2X Link. In this case, the module outputs the invalid value 0x8000.

Example 1

If using an X2X cycle time of 800 µs, it is possible to perform 16 measurements per X2X cycle if the A/D converter cycle time equals 50 µs. The first 6 measured values are discarded; the last 10 measured values are provided by the module.

With a shorter X2X cycle time, the number of measured values should not exceed the number of measurements that can actually be made. All other measured values are invalid (0x8000). To minimize the load on the X2X Link network, it is possible to disable these unneeded registers (see "Number of measured values" on page 77).

Example 2

If using an X2X cycle time of 300 µs, it is possible to perform 6 measurements per X2X cycle if the A/D converter cycle time equals 50 µs. For this reason, only the first 6 registers are valid. The registers for the 7th through 10th measured value (AnalogInput07 to AnalogInput10) should be disabled by setting Number of measured values to "6 measured values" in the I/O configuration.

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration						
1601	ConfigGain01_MultiSample	USINT			•	
1603	ConfigCycletime01_MultiSample	USINT				•
Analog signal - Communication						
2	StatusInput01	USINT	•			
1534 + N * 4	AnalogInput0N (N = 1 to 10)	INT	•			

1.2.1.14.4 Function model 2 - Extended filter

This function model allows the IIR low-pass filter and the FIR filter to be enabled.

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration						
272	ConfigCommonOutput01 (A/D converter and IIR filter configuration)	USINT			•	
288	ConfigFilterOutput01	UINT				•
273	ConfigDatarateOutput01	USINT			•	
274	ConfigHighResolutionOutput01	UINT			•	
Analog signal - Communication						
2	StatusInput01	USINT	•			
4	AnalogInput01	DINT	•			
256	AdcConvTimeStampInput01	DINT	•			

1.2.1.14.5 Function model 254 - Bus controller

In function model "254 - Bus controller", the module behaves as it does in "Function model 0 - Standard" with the exception that it is not synchronized to the X2X Link network even if synchronous mode is enabled in register "ConfigOutput01" on page 72. Instead, the module behaves as if the set A/D converter cycle time is not a factor or multiple of the X2X cycle time and attempts to maintain the set A/D converter cycle time as precisely as possible.

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration							
16	0	ConfigOutput01 (A/D converter configuration)	USINT			•	
18	18	ConfigCycletime01	UINT				•
32	32	AdcClkFreqShift01	USINT				•
Analog signal - Communication							
2	4	StatusInput01	USINT	•			
4	0	AnalogInput01	DINT	•			

1) The offset specifies the position of the register within the CAN object.

1.2.1.14.5.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

1.2.1.14.5.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

1.2.1.14.6 Registers for function models "0 - Standard" and "254 - Bus controller"

1.2.1.14.6.1 A/D converter configuration

Name:
ConfigOutput01

The data rate and measurement range of the A/D converter can be configured in this register.

Data type	Values	Bus controller default setting
USINT	See bit structure.	13

Bit structure:

Bit	Description	Value	Information
0 - 3	Data rate f_{DATA} (samples per second):	0000	2.5
		0001	5
		0010	10
		0011	15
		0100	25
		0101	30
		0110	50
		0111	60
		1000	100
		1001	500
		1010	1000
		1011	2000
		1100	3750
		1101	7500 (bus controller default setting)
		1110	Synchronous mode
		1111	Reserved
4 - 6	Standard measurement range (bit 6 = 0)	000	16 mV/V (bus controller default setting)
		001	8 mV/V
		010	4 mV/V
		011	2 mV/V
	Extended measurement range (bit 6 = 1)	100	256 mV/V
		101	128 mV/V
		110	64 mV/V
		111	32 mV/V
7	Reserved	0	(must be 0)

Synchronous mode

The module's analog/digital converter (A/D converter) can optionally be operated and read synchronously to the X2X Link network. Synchronous mode is enabled by selecting the respective operating mode in register "ConfigOutput01" on page 72. A time between 200 and 2000 µs must be set in register "ConfigCycletime01" on page 73 for this. If this time is a whole number factor or multiple of the configured cycle time of X2X Link, then the A/D converter is read synchronously to X2X Link.

Information:

The A/D converter cycle time must be ≥1/4 of the X2X cycle time!

Bit 2 in *Module status* is set (i.e. A/D converter not running synchronously)...

- ... If the configured A/D converter cycle time cannot be synchronized with X2X Link.
- ... If the module is still in the settling phase.

Jitter, dead time and settling time:

Jitter A/D converter cycle times <1500 µs A/D converter cycle times >1500 µs	 Max. ±1 µs Max. ±4 µs
X2X link dead time	$50\ \mu s + \frac{\text{X2X cycle time}}{128}$
Settling time	150 x X2X cycle time

The settling time corresponds to the time needed until the A/D converter can be operated after enabling synchronous mode or following conversion of the A/D converter cycle time.

1.2.1.14.6.2 A/D converter cycle time

Name:
ConfigCycletime01

This register is only used in Synchronous mode. If synchronous mode is enabled in the A/D converter configuration, then the module attempts to operate the A/D converter as synchronously as possible to the X2X Link network (based on the A/D converter cycle time set in this register). It is of course necessary for the X2X Link cycle time and the A/D converter cycle time to have a certain ratio. The following conditions must be observed:

1) A/D converter cycle time ≥ 1/4 X2X cycle time
2) A/D converter cycle time corresponds to a whole number factor or multiple of the X2X cycle time
3) A/D converter cycle time must be in the range 50 to 2000 µs

Data type	Values	Information
UINT	50 to 2000	Bus controller default setting: 400

1.2.1.14.6.3 A/D converter clock frequency shift

Name:
AdcClkFreqShift01

In rare cases, strain gauge modules connected to neighboring slots can influence one another. This can result in temporary, minimal deviations in measured values. This can only occur if the sigma-delta A/D converters on the neighboring strain gauge modules are operated at exactly the same clock frequency.

In most cases, these clock frequencies vary slightly due to part variances. When they are the same however, this register on the strain gauge module provides a safe way for an application to prevent this type of mutual influence.

Data type	Values	Information
SINT	-128 to 127	Bus controller default setting: 127

This register can be used to vary the clock frequency in increments of 200 ppm. Setting values from -50 to 50 cover a range of -10000 ppm to 10000 ppm. This corresponds with -1% to 1%.

Values beyond this range will cause activation of a default mode. The frequency shift is derived from the last 2 digits of the serial number by the module firmware. This saves time that would otherwise be needed for programming, provided that the last two digits of the serial numbers on the neighboring modules are not the same

Register value	Frequency shift in ppm	Example of a sampling rate[1)]
127	((SerialNo. modulo 100) - 50) * (-200) ppm	Based on the serial number
...	...	...
51	((SerialNo. modulo 100) - 50) * (-200) ppm	Based on the serial number
50	10000	505
49	9800	504.9
...	...	...
2	400	500.2
1	200	500.1
0	0	500
-1	-200	499.9
-2	-400	499.8
...	...	...
-50	-10000	495
-51	((SerialNo. modulo 100) - 50) * (-200) ppm	Based on the serial number
...	...	...
-128	((SerialNo. modulo 100) - 50) * (-200) ppm	Based on the serial number

1) Nominal sampling rate of 500 samples per second

Important:

As shown in the table above, shifting the A/D converter clock frequency will equally shift the A/D converter sampling rate. Shifting the A/D converter clock frequency too much can cause problems with disturbance suppression particularly when a very specific sampling rate has been defined to suppress existing disturbances (e.g. 50 Hz to suppress the 50 Hz hum). See also "Filter characteristics of the sigma-delta A/D converter" on page 60.
It is situations like this where the option to manually shift the frequency in the I/O configuration or ASIOACC library should be utilized rather than relying on the default frequency shift that is based on the serial number.

A frequency shift like the one shown below would be sufficient to prevent modules from influencing one another and would not cause any noticeable difference to the filter characteristics.

Slot	1	2	3	4	5	6	...
A/D converter clock frequency shift	0	2	-1	1	-2	0	...

Information:

- **This register has no effect in synchronous mode because the firmware regulates the A/D converter clock frequency in such a way that the A/D converter cycle is synchronous with the X2X cycle.**
- **When writing to this register using the ASIOACC library, only the lowest value byte of the written value is accepted. For example, the value 256 (=0x100) is identical to the value 0 (=0x00).**

1.2.1.14.6.4 Module status

Name:
StatusInput01

The current state of the module is indicated in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	A/D converter value	0	Valid A/D converter value
		1	Invalid A/D converter value (analog value = 0xFF800000). Possible causes: • Strain gauge supply error • I/O power supply error • A/D converter not (yet) configured
1	Line monitoring	0	Ok
		1	Open circuit
2	Only valid in synchronous mode	0	A/D converter runs synchronous to X2X Link
		1	A/D converter does not run synchronous to X2X Link
3 - 7	Reserved	-	

1.2.1.14.6.5 Strain gauge value

Name:
AnalogInput01

This register contains the raw value determined by the A/D converter for the full-bridge strain gauge with 24-bit resolution.

Data type	Values	Information
DINT	-8,388,608	Negative invalid value
	-8,388,607	Negative full-scale deflection / Underflow
	-8,388,606 to 8388606	Valid range
	8,388,607	Positive full-scale deflection / Overflow / Open circuit

Effective resolution

In principle, the effective resolution of the A/D converter is dependent on the data rate and the measurement range (see "Effective resolution of the A/D converter" on page 57).

The following table shows how the effective resolution (in bits) or effective range of values of the strain gauge value depend on the module configuration (data rate, measurement range):

	Measurement range							
	±16 mV/V		±8 mV/V		±4 mV/V		±2 mV/V	
Data rate f_{DATA} [Hz]	Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
2.5	19.9	±489,000	19.1	±281,000	18.0	±131,000	17.4	±86,500
5	19.4	±346,000	18.2	±151,000	17.5	±92,700	16.4	±43,200
10	18.5	±185,000	17.8	±114,000	16.8	±57,100	15.9	±30,600
15	18.2	±151,000	17.3	±80,700	16.4	±43,200	15.4	±21,600
25	17.8	±114,000	16.9	±61,100	16.0	±32,800	14.9	±15,300
30	17.8	±114,000	16.8	±57,100	15.9	±30,600	14.8	±14,300
50	17.4	±86,500	16.3	±40,300	15.4	±21,600	14.4	±10,800
60	17.4	±86,500	16.2	±37,600	15.3	±20,200	14.1	±8,780
100	16.9	±61,100	15.9	±30,600	14.8	±14,300	13.8	±7,130
500	15.5	±23,200	14.5	±11,600	13.5	±5,790	12.5	±2,900
1000	15.0	±16,400	14.1	±8,780	13.1	±4,390	11.9	±1,910
2000	14.5	±11,600	13.4	±5,400	12.6	±3,100	11.4	±1,350
3750	14.1	±8,780	13.1	±4,390	12.1	±2,190	11.1	±1,100
7500	13.8	±7,130	12.7	±3,330	11.8	±1,780	10.6	±776

Table 13: Effective resolution of the strain gauge value in bits for the measurement range 2 to 16 mV/V

	Measurement range							
	±256 mV/V		±128 mV/V		±64 mV/V		±32 mV/V	
Data rate f_{DATA} [Hz]	Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
2.5	22.0	±2,100,000	22.0	±2,100,000	21.2	±1,200,000	20.5	±741,000
5	21.7	±1,700,000	21.4	±1,380,000	20.8	±913,000	20.3	±645,000
10	20.8	±913,000	20.8	±913,000	20.2	±602,000	19.4	±346,000
15	20.7	±852,000	20.5	±741,000	19.9	±489,000	19.3	±323,000
25	20.1	±562,000	19.9	±489,000	19.7	±426,000	18.9	±245,000
30	19.9	±489,000	19.9	±489,000	19.4	±346,000	18.8	±228,000
50	19.8	±456,000	19.2	±301,000	19.2	±301,000	18.2	±151,000
60	19.5	±371,000	19.2	±301,000	19.0	±262,000	18.2	±151,000
100	19.0	±262,000	18.8	±228,000	18.5	±185,000	17.6	±99,300
500	17.8	±114,000	17.5	±92,700	17.1	±70,200	16.4	±43,200
1000	17.2	±75,300	17.1	±70,200	16.7	±53,200	15.8	±28,500
2000	16.7	±53,200	16.5	±46,300	16.1	±35,100	15.2	±18,800
3750	16.2	±37,600	16.1	±35,100	15.8	±28,500	14.9	±15,300
7500	15.9	±30,600	15.8	±28,500	15.3	±20,200	14.6	±12,400

Table 14: Effective resolution of the strain gauge value in bits for the measurement range 32 to 256 mV/V

1.2.1.14.7 Register for "Function model 1 - Multisampling"

1.2.1.14.7.1 A/D converter configuration

Name:
ConfigGain01_MultiSample

The measurement range for the A/D converter can be configured in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Standard measurement range (bit 2 = 0)	000	16 mV/V
		001	8 mV/V
		010	4 mV/V
		011	2 mV/V
	Extended measurement range (bit 2 = 1)	100	256 mV/V
		101	128 mV/V
		110	64 mV/V
		111	32 mV/V
3 - 7	Reserved	0	(must be 0)

1.2.1.14.7.2 A/D converter cycle time

Name:
ConfigCycletime01_MultiSample

The A/D converter cycle time can be configured in this register.

In order for multisampling to work, the X2X cycle time must be divisible by the A/D converter cycle time to produce a whole number.

Data type	Value	Information
USINT	0	50 µs (default)
	1	100 µs
	2 to 255	Reserved

1.2.1.14.7.3 Number of measured values

If the X2X cycle time is too short, then not all 10 measurements can be performed. To reduce the load on X2X Link, it makes sense to only transfer as many values as measurements that can be made. This is why it is possible to configure the number of measured values to be transferred (see "Function model 1 - Multisampling" on page 70).

Example: A/D converter cycle time = 50 µs

X2X cycle time	Number of measured values to be transferred
250 µs	5
300 µs	6
350 µs	7
400 µs	8
450 µs	9
≥500 µs	10

Example: A/D converter cycle time = 100 µs

X2X cycle time	Number of measured values to be transferred
300 µs	3
400 µs	4
500 µs	5
600 µs	6
700 µs	7
800 µs	8
900 µs	9
≥1 ms	10

1.2.1.14.7.4 Module status

Name:
StatusInput01

This register contains the current state of the module.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	A/D converter values	0	Valid A/D converter value
		1	Invalid A/D converter value
1	Line monitoring	0	OK
		1	Open circuit An open circuit was found during at least one measurement in this X2X cycle. This bit is reset if all measurements are OK after correcting this error, i.e. it does not have to be acknowledged.
2	Synchronous mode	0	A/D converter runs synchronous to X2X Link
		1	A/D converter does not run synchronous to X2X Link
3 - 7	Reserved	-	

1.2.1.14.7.5 Strain gauge value - Multiple

Name:
AnalogInput01 to AnalogInput10

This register contains the raw value determined by the A/D converter for the full-bridge strain gauge with 16-bit resolution. The module returns between 3 and 10 measured values per X2X cycle depending on the configuration.

Effective resolution

In principle, the effective resolution of the A/D converter is dependent on the data rate and measurement range (see "Effective resolution of the A/D converter" on page 57).

The following table shows how the effective resolution (in bits) or effective range of values of the strain gauge value depend on the module configuration (data rate, measurement range).

Measurement range							
±16 mV/V		±8 mV/V		±4 mV/V		±2 mV/V	
Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
13.4	±5,240	12.3	±2,510	11.3	±1,300	10.3	±630

Table 15: Effective resolution of the strain gauge value in bits for the measurement range 2 to 16 mV/V

Measurement range							
±256 mV/V		±128 mV/V		±64 mV/V		±32 mV/V	
Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
15.5	±23,200	15.0	±16,400	15.0	±16,400	14.1	±8,490

Table 16: Effective resolution of the strain gauge value in bits for the measurement range 32 to 256 mV/V

1.2.1.14.8 Register for "Function model 2 - Extended filter"

1.2.1.14.8.1 A/D converter and IIR filter configuration

Name:
ConfigCommonOutput01

The IIR low-pass filter and measurement range of the A/D converter can be configured in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
			Filter level
0 - 3	IIR low-pass filter	0000	0: IIR low-pass filter switched off
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001 - 1111	The analog input value indicates an invalid range.
4 - 6	Default measurement range	000	16 mV/V
		001	8 mV/V
		010	4 mV/V
		011	2 mV/V
	Extended measurement range	100	256 mV/V
		101	128 mV/V
		110	64 mV/V
		111	32 mV/V
7	Reserved	0	(must be 0)

1.2.1.14.8.2 Data rate configuration

Name:
ConfigFilterOutput01

Whether a selectable data rate or a high-resolution data rate is being used for the FIR filter is configured in this register.

Data type	Values	Information
UINT	0	Mode "Selectable data rate": A selectable data rate is used for the FIR filter (default). Configuration takes place in register "ConfigDatarateOutput01" on page 33.
	1	Mode "High-resolution data rate": A high-resolution data rate is used for the FIR filter. Configuration takes place in register "ConfigHighResolutionOutput01" on page 33.

Name:
ConfigDatarateOutput01

The data rate of the FIR filter in mode "Selectable data rate" is configured in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Data rate f_{DATA} (samples per second):	0000	2.5
		0001	5
		0010	10
		0011	15
		0100	25
		0101	30
		0110	50
		0111	60
		1000	100
		1001	500
		1010	1000
		1011	2000
		1100	3750
		1101	7500
		1110 - 1111	The analog input value indicates an invalid range.
4 - 7	Reserved	0	(must be 0)

Name:
ConfigHighResolutionOutput01

The data rate of the FIR filter in 0.1 Hz steps is configured in this register (0.1 to 6553.5 Hz).

Data type	Values	Information
UINT	0	Disables the FIR filter
	1 to 65,535	0.1 to 6553.5 Hz

1.2.1.14.8.3 Module status

Name:
StatusInput01

This register contains the current state of the module. If there is a fault in the module power supply or strain gauge supply, the analog input value indicates an invalid range and the buffer of the enabled filter is reset.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	A/D converter values	0	Valid A/D converter value
		1	Invalid A/D converter value
1	Line monitoring	0	OK
		1	Open circuit
2	Reserved	-	
3	Module power supply	0	OK
		1	Error in module power supply
4	Strain gauge supply	0	OK
		1	Error in strain gauge supply
5	FIR filter ready	0	OK
		1	FIR filter not yet ready
6 - 7	Reserved	-	

1.2.1.14.8.4 A/D converter conversion timestamp

Name:
AdcConvTimeStampInput01

This register holds the timestamp of the last analog conversion. This is always the point in time in [µs] at which the conversion of the latest A/D converter raw value is completed.

Data type	Values	Explanation
DINT	-2,147,483,648 to 2,147,483,647	Timestamp [µs] of the last analog conversion

1.2.1.14.9 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
250 µs

1.2.1.14.10 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

For the I/O update times for function models "0 - Standard", "2 - Extended filter" and "254 - Bus controller", see section "Characteristics of the FIR filter in mode "Selectable data rate"" on page 64.

Depending on the setting in register "ConfigCycletime01_MultiSample" on page 77, the I/O update time in "Function model 1 - Multisampling" is 50 or 100 µs.

1.2.2 X20AI1744-3 with Rev. <G0

1.2.2.1 General information

This module works with both 4-wire and 6-wire strain gauge load cells. The concept applied by the module requires compensation in the measurement system. This compensation eliminates the absolute uncertainty in the measurement circuit, such as component tolerances, effective bridge voltage or zero point offset. The measurement precision refers to the absolute (compensated) value, which will only change as a result of changes in the operating temperature.

- 1 full-bridge strain gauge input
- Data output rate configurable from 2.5 Hz to 7.5 kHz
- Special operating modes (synchronous mode and multiple sampling)

1.2.2.2 Order data

Model number	Short description	Figure
	Analog inputs	
X20AI1744-3	X20 analog input module,1 full-bridge strain gauge input,24-bit converter resolution,5 Hz input filter	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply continuous	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 17: X20AI1744-3 - Order data

1.2.2.3 Technical data

Product ID	X20AI1744-3
Short description	
I/O module	1 full-bridge strain gauge input
General information	
B&R ID code	0xA4EF
Status indicators	Channel status, operating status, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Open circuit	Yes, using status LED and software
Input	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1.25 W
Additional power dissipation caused by actuators (resistive) [W]	Max. +0.36 [1)]
Certifications	
CE	Yes
KC	Yes
EAC	Yes
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
Full-bridge strain gauge	
Strain gauge factor	2 to 256 mV/V, configurable using software
Connection	4- or 6-wire connections [2)]
Input type	Differential, used to evaluate a full-bridge strain gauge
Digital converter resolution	24-bit
Conversion time	Depends on the configured data output rate

Table 18: X20AI1744-3 - Technical data

Product ID	X20AI1744-3
Data output rate	2.5 - 7500 samples per second, configurable using software (f_{DATA})
Input filter	
Cutoff frequency	5 Hz
Order	3
Slope	60 dB
ADC filter characteristics	Sigma-delta, see section "Filter characteristics of the sigma-delta A/D converter"
Operating range / Measurement sensor	85 to 5000 Ω
Influence of cable length	The shielded twisted pair cable should be as short as possible and run separately to the sensor (isolated from load circuit) without intermediate terminals
Input protection	RC protection
Common-mode range	0 to 3 VDC Permissible input voltage range (with regard to the potential strain gauge GND) on the inputs "Input +" and "Input -"
Isolation voltage between input and bus	500 V_{Eff}
Conversion procedure	Sigma-delta
Output of digital value	
Broken bridge supply line	Value approaches 0
Broken sensor line	Value approaches ±end value ("open circuit" status bit is set in the *Module status* register)
Valid range of values	0xFF800001 to 0x007FFFFF (-8,388,607 to 8,388,607)
Strain gauge supply	
Voltage	5.5 VDC / max. 65 mA [3]
Short-circuit and overload resistant	Yes
Voltage drop for short-circuit protection	Max. 0.2 VDC at 65 mA
Quantization [4]	
LSB value (16-bit)	
2 mV/V	336 nV
4 mV/V	671 nV
8 mV/V	1.343 µV
16 mV/V	2.686 µV
32 mV/V	5.371 µV
64 mV/V	10.74 µV
128 mV/V	21.48 µV
256 mV/V	42.97 µV
LSB value (24-bit)	
2 mV/V	1.31 nV
4 mV/V	2.62 nV
8 mV/V	5.25 nV
16 mV/V	10.49 nV
32 mV/V	20.98 nV
64 mV/V	41.96 nV
128 mV/V	83.92 nV
256 mV/V	167.85 nV
Temperature coefficient	
Rev. ≥E0	10 ppm/°C
Rev. <E0	30 ppm/°C
Electrical isolation	Bus isolated from analog input and strain gauge supply voltage Channel not isolated from I/O power supply
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	0 to 55°C
Vertical mounting orientation	0 to 50°C
Derating	See section "Hardware configuration"
Storage	-25 to 70°C
Transport	-25 to 70°C

Table 18: X20AI1744-3 - Technical data

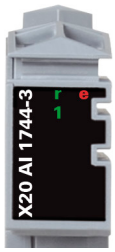
Product ID	X20AI1744-3
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x terminal block X20TB12 separately Order 1x bus module X20BM11 separately
Spacing	12.5$^{+0.2}$ mm

Table 18: X20AI1744-3 - Technical data

1) Depends on the full-bridge strain gauge being used.
2) With 6-wire connections, line compensation does not function (see section "Connection examples").
3) The maximum current of 90 mA is permitted up to an operating temperature of 45°C.
4) Quantization depends on the strain gauge factor.

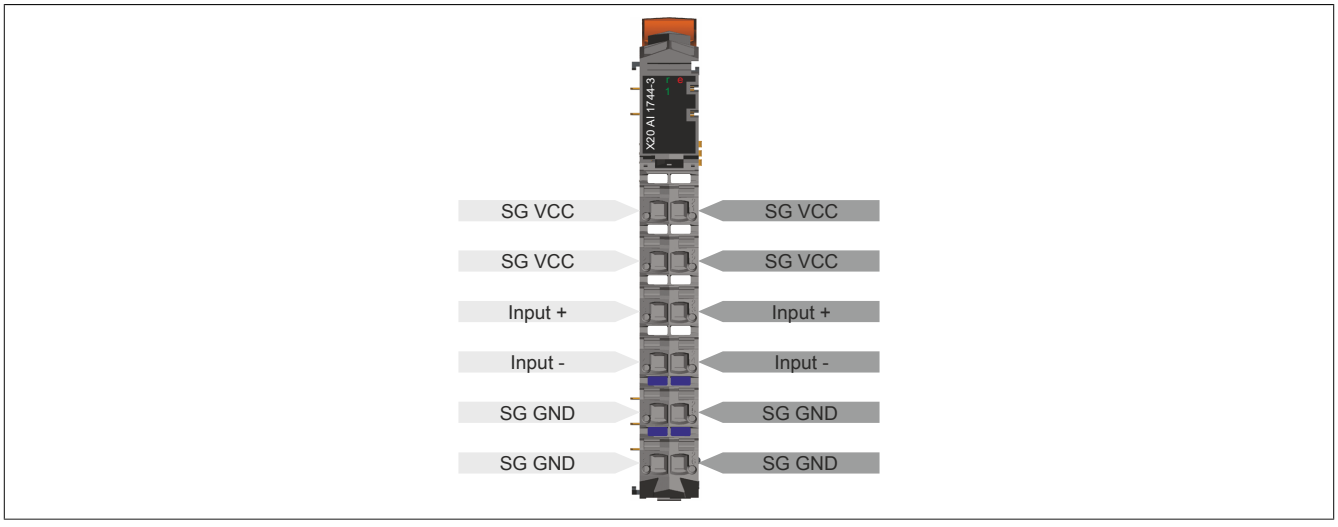
1.2.2.4 LED status indicators

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 system user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	1	Green	Off	Possible causes: • Open circuit • Sensor is disconnected • Converter is busy
			On	Analog/digital converter running, value OK

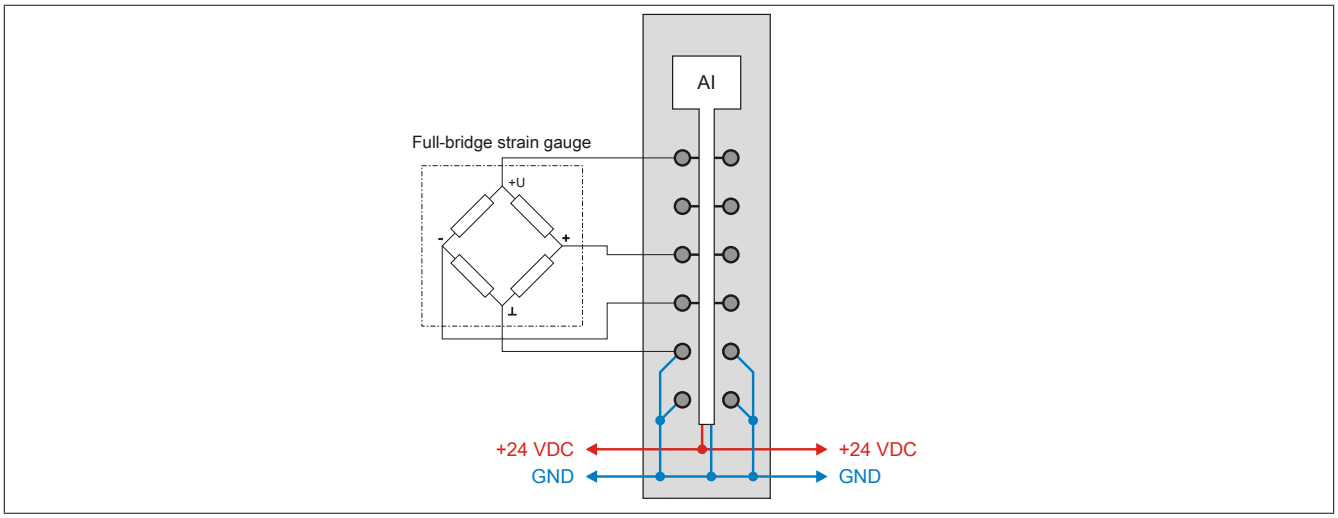
1) Depending on the configuration, a firmware update can take up to several minutes.

1.2.2.5 Pinout



1.2.2.6 Connection examples

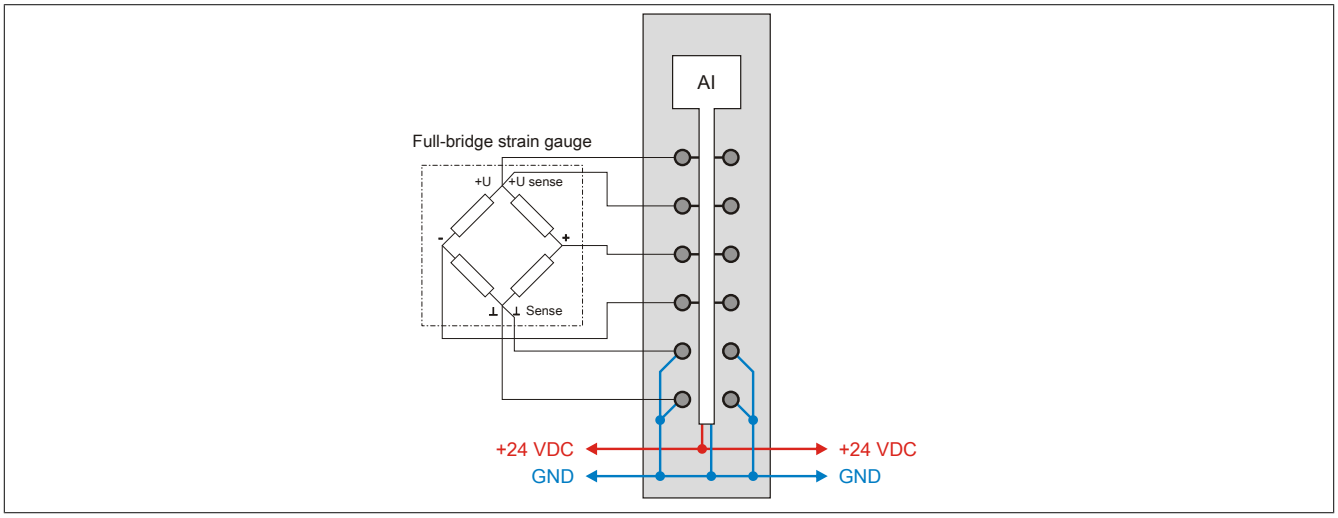
Full-bridge strain gauge with 4-wire connections



Full-bridge strain gauge with 6-wire connections

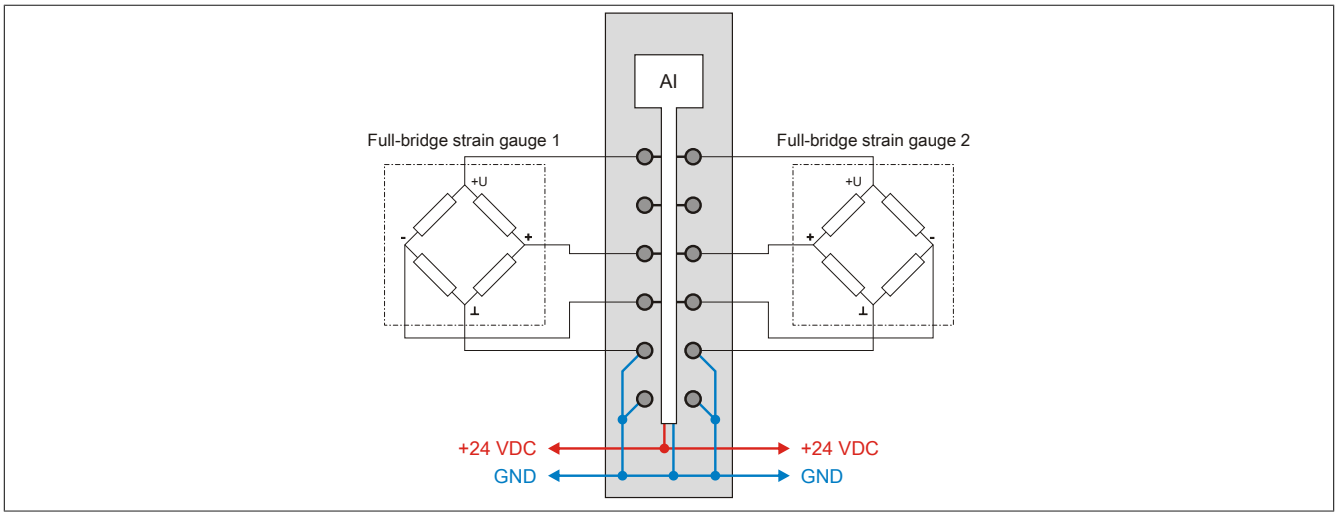
Full-bridge strain gauges can be connected to this module with 6-wire connections. Line compensation is not supported by the module, however. The sense lines are short circuited by the internally connected strain gauge VCC and GND connections (see "Input circuit diagram" on page 86). The measurement precision is therefore affected by changes in operating temperature. Longer cable lengths and smaller cable cross sections also increase the potential for errors in the measurement system.

In order to reduce cable resistance, the sense lines should be connected in parallel with the strain gauge supply lines. Optimal signal quality can be obtained by using a shielded twisted pair cable. The connections for the strain gauge supply lines, the sensor lines, and the bridge differential voltage lines should each use one twisted pair cable.



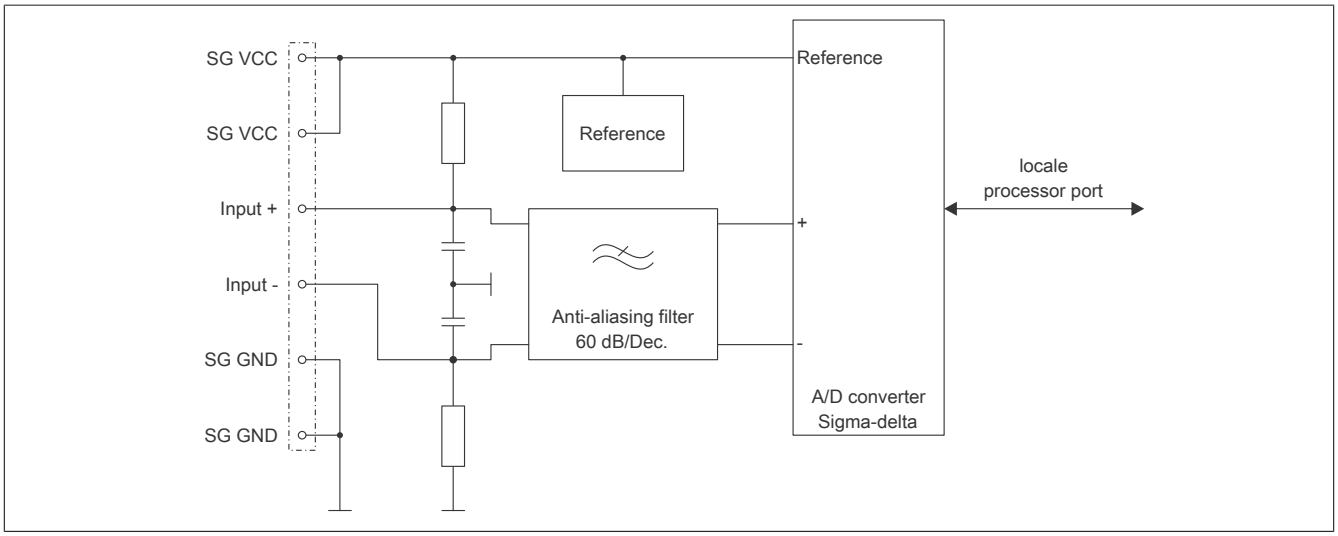
Parallel connection of 2 full-bridge strain gauges (4-wire connections)

If connecting the full-bridge strain gauges in parallel, the manufacturer's guidelines must be observed.

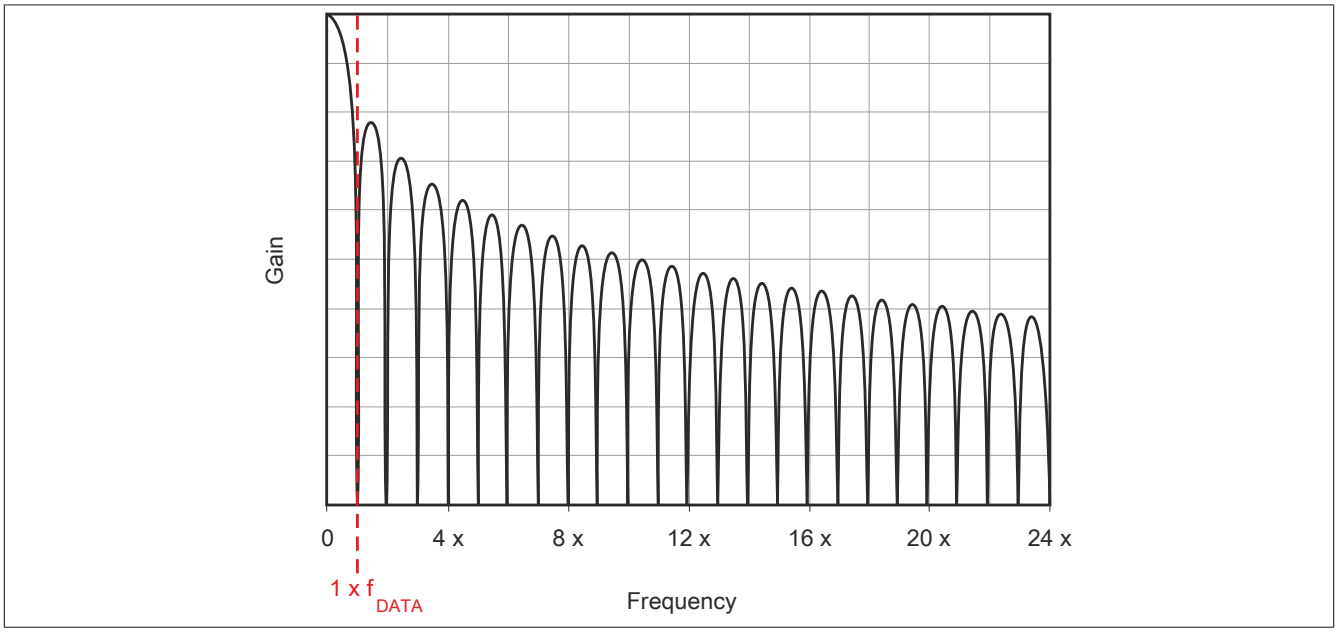


When connecting 3 or more full-bridge strain gauges in parallel, 2 lines must be connected together in an X20 terminal block.

1.2.2.7 Input circuit diagram



1.2.2.8 Filter characteristics of the sigma-delta A/D converter

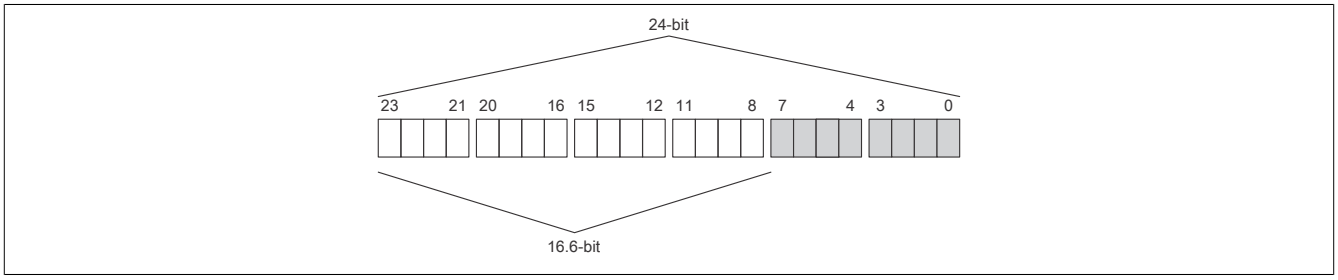


1.2.2.9 Effective resolution of the A/D converter

The A/D converter on the module provides a 24-bit measured value. The actual attainable noise-free resolution is always less than 24-bit, however. This "effective resolution" depends on the data rate and measurement range.

Example:

Based on the conversion method, a data rate of 2.5 Hz and a specified measurement range of 2 mV/V result in an effective resolution of 16.6 bits:



The low-order bits (grayed out) contain only noise instead of valid values and must therefore not be evaluated.

With "Function model 1 - Multisampling", only the highest 16 bits are made available.

1.2.2.10 Calculation example / Quantization

In a weighing application, the corresponding weight located on the connected load cell should be determined from the value derived from the module.

The characteristics of the strain gauge load cell are as follows:

- Rated load: 1000 kg
- Strain gauge factor: 4 mV/V

The bridge factor of the strain gauge load cell now yields (by multiplying with the bridge supply voltage from the module) the value for the positive full-scale deflection at the specified nominal load of 1000 kg:

4 mV/V × 5.5 V = 22 mV

With a simple Rule of Three calculation, the corresponding value can be calculated (as seen in the table) from weight to the converter value and vice versa. This simplified theoretical approach is only valid for an ideal measurement system. Calibration of the entire measurement system is recommended because not only the module, but particularly the strain gauge bridges exhibit tolerances (offset, gain). When taring, the gradient offset is recalculated and the gain of the linear equation is determined when normalized. In addition to the calculation displayed in the table, these calculations must also be carried out in the application.

24-bit value of the module		Quantization	Corresponding weight
0x007F FFFF	8,388,607	22.0 mV	1000 kg
0x0000 0001	1	2.62 nV	0.119 g
0x0000 20C3	8387	22.0 µV	1 kg
0x0001 0000	65536	171.9 µV	7.81 kg

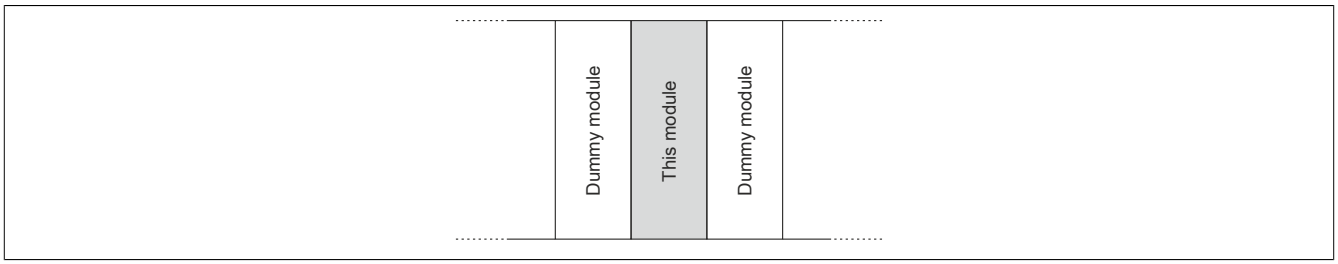
The values for one LSB are also included in the module's technical data under item "Quantization" (1 LSB each for 16 bits and 24 bits).

1.2.2.11 Hardware configuration

1.2.2.11.1 Hardware configuration for horizontal installation at 50°C ambient temperature

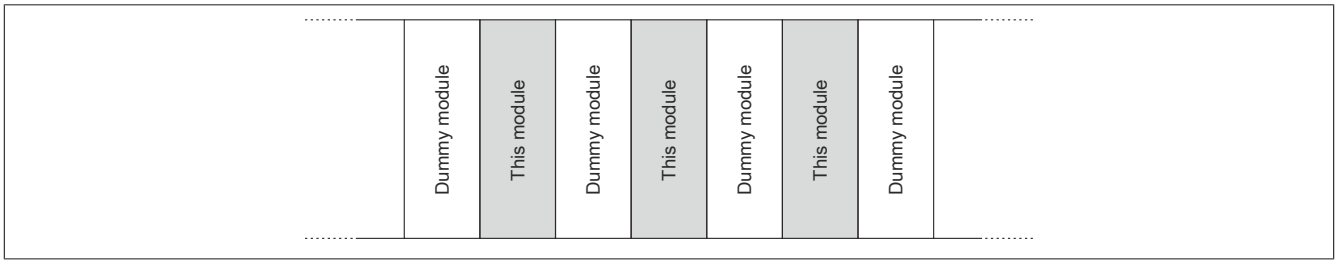
Operating a strain gauge module

Starting at an ambient temperature of 50°C, a dummy module must be connected to the left and right of the strain gauge module in a horizontal mounting orientation.



Operating multiple strain gauge modules side by side

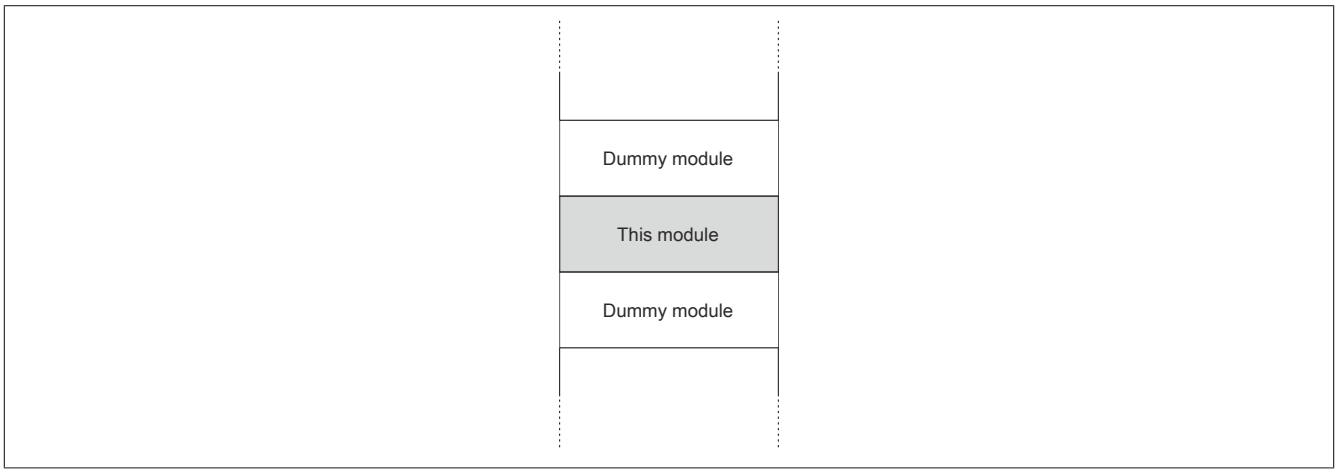
If 2 or more horizontal strain gauge modules are being operated in a cluster, the following arrangement of modules must be observed.



1.2.2.11.2 Hardware configuration for vertical installation at 40°C ambient temperature

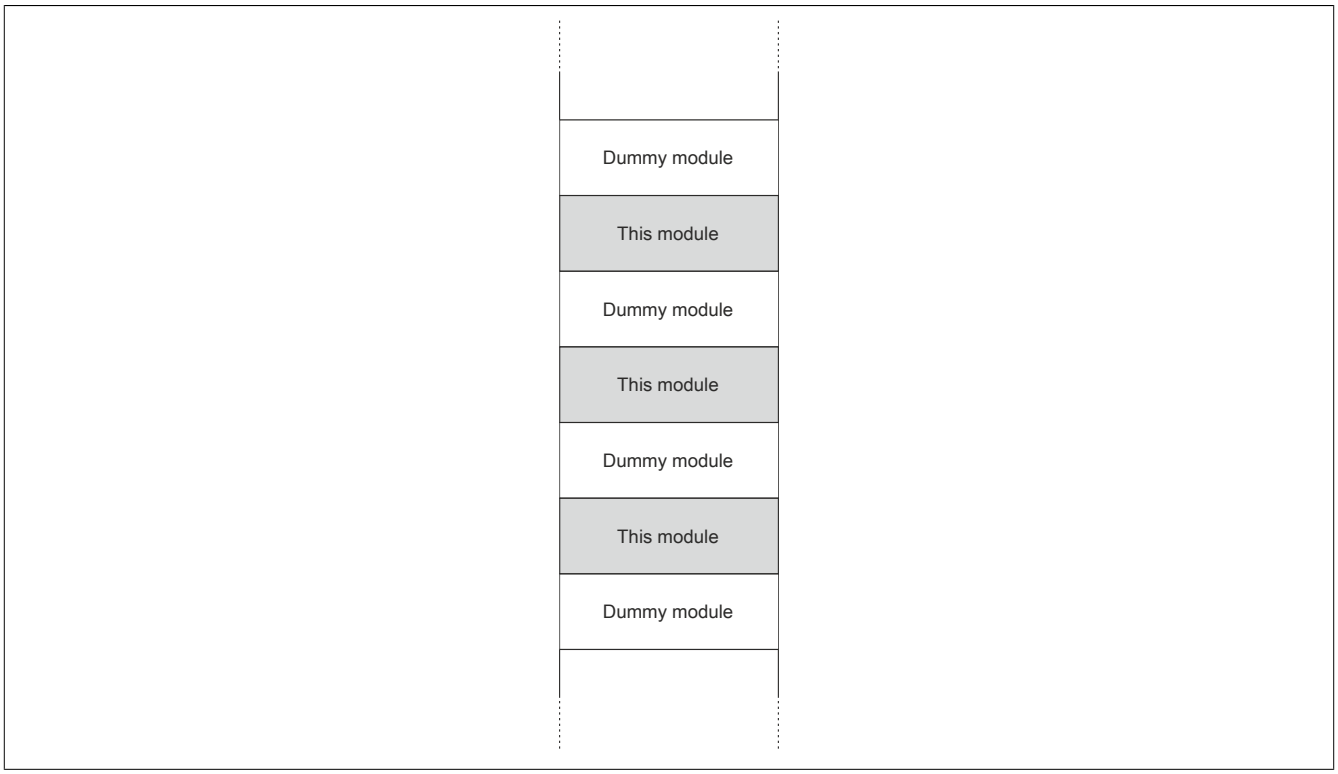
Operating a strain gauge module

Starting at an ambient temperature of 40°C, a dummy module must be connected to the left and right of the strain gauge module in a vertical mounting orientation.



Operating multiple strain gauge modules side by side

If 2 or more vertical strain gauge modules are being operated in a cluster, the following arrangement of modules must be observed.


Dummy module
This module
Dummy module
This module
Dummy module
This module
Dummy module

1.2.2.12 Register description

1.2.2.12.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 system user's manual.

1.2.2.12.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
2	StatusInput01	USINT	•			
4	AnalogInput01	DINT	•			
16	ConfigOutput01	USINT			•	
18	ConfigCycletime01	UINT				•
32	AdcClkFreqShift01[1)]	USINT				•

1) Firmware version 8 / Upgrade 1.2.0.0 or higher

1.2.2.12.3 Function model 1 - Multisampling

In this function model, the A/D converter is operated synchronously to X2X Link with a predefined A/D converter cycle time. The value is configurable as 50 or 100 µs.

The module returns between 3 and 10 measured values per X2X cycle depending on the configuration. With an X2X cycle time of 400 µs and A/D converter cycle time of 50 µs, exactly 8 measurements are performed and the module can return 8 values (strain gauge value 01 to strain gauge value 08).

If a longer cycle time is used, the values returned correspond to the last measurements. If using an X2X cycle time that is not a whole number multiple of the A/D converter cycle time, then the conversion cannot be synchronized with X2X Link. In this case, the module outputs the invalid value 0x8000.

Example 1

If using an X2X cycle time of 800 µs, it is possible to perform 16 measurements per X2X cycle if the A/D converter cycle time equals 50 µs. The first 6 measured values are discarded; the last 10 measured values are provided by the module.

With a shorter X2X cycle time, the number of measured values should not exceed the number of measurements that can actually be made. All other measured values are invalid (0x8000). To minimize the load on the X2X Link network, it is possible to disable these unneeded registers (see "Number of measured values" on page 97).

Example 2

If using an X2X cycle time of 300 µs, it is possible to perform 6 measurements per X2X cycle if the A/D converter cycle time equals 50 µs. For this reason, only the first 6 registers are valid. The registers for the 7th through 10th measured value (AnalogInput07 to AnalogInput10) should be disabled by setting Number of measured values to "6 measured values" in the I/O configuration.

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration						
1601	ConfigGain01_MultiSample	USINT			•	
1603	ConfigCycletime01_MultiSample	USINT				•
Analog signal - Communication						
2	StatusInput01	USINT	•			
1534 + N * 4	AnalogInput0N (N = 1 to 10)	INT	•			

1.2.2.12.4 Function model 254 - Bus controller

In function model "254 - Bus controller", the module behaves as it does in "Function model 0 - Standard" with the exception that it is not synchronized to the X2X Link network even if synchronous mode is enabled in register "ConfigOutput01" on page 93. Instead, the module behaves as if the set A/D converter cycle time is not a factor or multiple of the X2X cycle time and attempts to maintain the set A/D converter cycle time as precisely as possible.

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
2	StatusInput01	USINT	•			
4	AnalogInput01	DINT	•			
16	ConfigOutput01	USINT			•	
18	ConfigCycletime01	UINT				•
32	AdcClkFreqShift01[1)]	USINT				•

1) Firmware version 8 / Upgrade 1.2.0.0 or later

1.2.2.12.5 Registers for function models "0 - Standard" and "254 - Bus controller"

1.2.2.12.5.1 Module status

Name:
StatusInput01

The current state of the module is indicated in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	A/D converter value	0	Valid A/D converter value
		1	Invalid A/D converter value (analog value = 0xFF800000). Possible causes: • Strain gauge supply error • I/O power supply error • A/D converter not (yet) configured
1	Line monitoring	0	Ok
		1	Open circuit
2	Only valid in synchronous mode	0	A/D converter runs synchronous to X2X Link
		1	A/D converter does not run synchronous to X2X Link
3 - 7	Reserved	-	

1.2.2.12.5.2 Strain gauge value

Name:
AnalogInput01

This register contains the raw value determined by the A/D converter for the full-bridge strain gauge with 24-bit resolution.

Data type	Values	Information
DINT	-8,388,608	Negative invalid value
	-8,388,607	Negative full-scale deflection / Underflow
	-8,388,606 to 8,388,606	Valid range
	8,388,607	Positive full-scale deflection / Overflow / Open circuit

Effective resolution

In principle, the effective resolution of the A/D converter is dependent on the data rate and measurement range (see "Effective resolution of the A/D converter" on page 87).

The following table shows how the effective resolution (in bits), or the RMS value range of the strain gauge value depend on the module configuration (data rate, measurement area).

	Measurement range							
	±16 mV/V		±8 mV/V		±4 mV/V		±2 mV/V	
Data rate f_{DATA} [Hz]	Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
2.5	21.3	±1,290,000	20.8	±912,000	19.7	±425,000	18.7	±212,000
5	20.7	±851,000	20.3	±645,000	19.3	±322,000	18.3	±161,000
10	20.4	±691,000	19.9	±490,000	18.9	±244,000	17.9	±122,000
15	20.1	±562,000	19.3	±320,000	18.7	±212,000	17.7	±106,000
25	19.7	±425,000	19.2	±301,000	18.5	±185,000	17.5	±92,000
30	19.6	±397,000	19.0	±262,000	18.1	±140,000	17.1	±72,000
50	19.4	±346,000	18.8	±230,000	17.9	±122,000	16.9	±61,000
60	19.3	±320,000	18.8	±230,000	17.8	±114,000	16.8	±57,000
100	19.1	±280,000	18.5	±185,000	17.4	±86,000	16.4	±43,000
500	18.0	±130,000	17.3	±80,000	16.3	±40,000	15.3	±20,000
1000	17.2	±75,000	16.5	±46,000	15.6	±25,000	14.6	±12,000
2000	16.6	±49,600	16.1	±35,000	15.3	±20,000	14.3	±10,000
3750	16.2	±37,600	15.7	±26,600	14.7	±13,000	13.7	±6,600
7500	15.8	±28,500	15.3	±20,200	14.4	±10,800	13.4	±5,400

Table 19: Effective resolution of the strain gauge value in bits for the measurement range 2 to 16 mV/V

	Measurement range							
	±256 mV/V		±128 mV/V		±64 mV/V		±32 mV/V	
Data rate f_{DATA} [Hz]	Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
2.5	23	±4,194,000	22.6	±3,179,000	22.1	±2,248,000	21.7	±1,703,000
5	22.3	±2,582,000	22.4	±2,767,000	21.9	±1,957,000	21.3	±1,291,000
10	22.3	±2,582,000	22	±2,097,000	21.6	±1,589,000	21	±1,049,000
15	22	±2,097,000	21.7	±1,703,000	21.3	±1,291,000	20.7	±852,000
25	21.7	±1,703,000	21.4	±1,384,000	21.1	±1,124,000	20.5	±741,000
30	21.8	±1,826,000	21.3	±1,291,000	20.8	±913,000	20.4	±692,000
50	21.3	±1,291,000	21.1	±1,124,000	20.4	±692,000	19.9	±489,000
60	21.3	±1,291,000	20.9	±978,000	20.5	±741,000	19.8	±456,000
100	20.9	±978,000	20.7	±852,000	20.2	±602,000	19.6	±397,000
500	20.1	±562,000	19.6	±397,000	19.1	±281,000	18.6	±199,000
1000	19	±262,000	18.6	±199,000	18.1	±140,000	17.5	±93,000
2000	18.5	±185,000	18.1	±140,000	17.8	±114,000	17	±66,000
3750	18.1	±140,000	17.8	±114,000	17.3	±81,000	16.6	±50,000
7500	17.7	±106,000	17.3	±81,000	16.9	±61,000	16.2	±38,000

Table 20: Effective resolution of the strain gauge value in bits for the measurement range 32 to 256 mV/V

1.2.2.12.5.3 A/D converter configuration

Name:
ConfigOutput01

The data rate and measurement range of the A/D converter can be configured in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Data rate f_{DATA} (samples per second):	0000	2.5
		0001	5
		0010	10
		0011	15
		0100	25
		0101	30
		0110	50
		0111	60
		1000	100
		1001	500
		1010	1000
		1011	2000
		1100	3750
		1101	7500
		1110	Synchronous mode[1)]
		1111	Reserved
4 - 6	Standard measurement range (bit 6 = 0)	000	16 mV/V
		001	8 mV/V
		010	4 mV/V
		011	2 mV/V
	Extended measurement range (bit 6 = 1)[2)]	100	256 mV/V
		101	128 mV/V
		110	64 mV/V
		111	32 mV/V
7	Reserved	0	(must be 0)

1) A/D converter is operated synchronously with X2X Link if possible - firmware version 2 or higher.
2) Firmware version 4 or higher

Synchronous mode

Beginning with firmware version 2, the analog/digital converter (A/D converter) of the module can be operated and read synchronously to X2X Link. Synchronous mode is enabled by selecting the respective operating mode in register "ConfigOutput01" on page 93. A time between 200 and 2000 µs must also be set in register "Config-Cycletime01" on page 94. If this time is a whole number factor or multiple of the configured cycle time of X2X Link, then the A/D converter is read synchronously to X2X Link.

Information:

The A/D converter cycle time must be ≥1/4 of the X2X cycle time!

Bit 2 in *Module status* is set (i.e. A/D converter not running synchronously)...

- ... If the configured A/D converter cycle time cannot be synchronized with X2X Link.
- ... If the module is still in the settling phase.

Jitter, dead time and settling time:

Jitter A/D converter cycle times <1500 µs A/D converter cycle times >1500 µs	 Max. ±1 µs Max. ±4 µs
X2X link dead time	$50\ \mu s + \frac{\text{X2X cycle time}}{128}$
Settling time Firmware version ≤4 Firmware version ≥5	 Max. 150 x A/D converter cycle time 150 x X2X cycle time

The settling time corresponds to the time needed until the A/D converter can be operated after enabling synchronous mode or following conversion of the A/D converter cycle time.

1.2.2.12.5.4 A/D converter cycle time

Name:
ConfigCycletime01

This register is only used in Synchronous mode. If synchronous mode is enabled in the A/D converter configuration, then the module attempts to operate the A/D converter as synchronously as possible to X2X Link (based on the A/D converter cycle time set in this register). It is of course necessary for the X2X Link cycle time and the A/D converter cycle time to have a certain ratio. The following conditions must be observed:

1) A/D converter cycle time ≥ 1/4 X2X cycle time
2) A/D converter cycle time corresponds to a whole number factor or multiple of the X2X cycle time
3) A/D converter cycle time must be in the range 50 to 2000 µs

Data type	Value
UINT	50 to 2000

1.2.2.12.5.5 A/D converter clock frequency shift

Name:
AdcClkFreqShift01

In rare cases, strain gauge modules connected to neighboring slots can influence one another. This can result in temporary, minimal deviations in measured values. This can only occur if the sigma-delta A/D converters on the neighboring strain gauge modules are operated at exactly the same clock frequency.

In most cases, these clock frequencies vary slightly due to part variances. When they are the same however, this register on the strain gauge module provides a safe way for an application to prevent this type of mutual influence.

Data type	Value
SINT	-128 to 127

This register can be used to vary the clock frequency in increments of 200 ppm. Setting values from -50 to 50 cover a range of -10000 ppm to 10000 ppm. This corresponds with -1% to 1%.

Values beyond this range will cause activation of a default mode. The frequency shift is derived from the last 2 digits of the serial number by the module firmware. This saves time that would otherwise be needed for programming, provided that the last two digits of the serial numbers on the neighboring modules are not the same

Register value	Frequency shift in ppm	Example of a sampling rate[1)]
127	((SerialNo. modulo 100) - 50) * (-200) ppm	Based on the serial number
...	...	...
51	((SerialNo. modulo 100) - 50) * (-200) ppm	Based on the serial number
50	10000	505
49	9800	504.9
...	...	...
2	400	500.2
1	200	500.1
0	0	500
-1	-200	499.9
-2	-400	499.8
...	...	...
-50	-10000	495
-51	((SerialNo. modulo 100) - 50) * (-200) ppm	Based on the serial number
...	...	...
-128	((SerialNo. modulo 100) - 50) * (-200) ppm	Based on the serial number

1) Nominal sampling rate of 500 samples per second

Important:

As shown in the table above, shifting the A/D converter clock frequency will equally shift the A/D converter sampling rate. Shifting the A/D converter clock frequency too much can cause problems with disturbance suppression particularly when a very specific sampling rate has been defined to suppress existing disturbances (e.g. 50 Hz to suppress the 50 Hz hum). See also "Filter characteristics of the sigma-delta A/D converter" on page 86.
It's situations like this where the option to manually shift the frequency in the I/O configuration or ASIOACC library should be utilized rather than relying on the default frequency shift that is based on the serial number.

A frequency shift like the one shown below would be sufficient to prevent modules from influencing one another and would not cause any noticeable difference to the filter characteristics.

Slot	1	2	3	4	5	6	...
A/D converter clock frequency shift	0	2	-1	1	-2	0	...

Information:

- **This register has no effect in synchronous mode because the firmware regulates the A/D converter clock frequency in such a way that the A/D converter cycle is synchronous with the X2X cycle.**
- **When writing to this register using the ASIOACC library, only the lowest value byte of the written value is accepted. For example, the value 256 (=0x100) is identical to the value 0 (=0x00).**

1.2.2.12.6 Register for "Function model 1 - Multisampling"

1.2.2.12.6.1 Module status

Name:
StatusInput01

This register contains the current state of the module.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	A/D converter values	0	Valid A/D converter value
		1	Invalid A/D converter value
1	Line monitoring	0	OK
		1	Open circuit An open circuit was found during at least one measurement in this X2X cycle. This bit is reset if all measurements are OK after correcting this error, i.e. it does not have to be acknowledged.
2	Synchronous mode	0	A/D converter runs synchronous to X2X Link
		1	A/D converter does not run synchronous to X2X Link
3 - 7	Reserved	-	

1.2.2.12.6.2 Strain gauge value - Multiple

Name:
AnalogInput01 to AnalogInput10

This register contains the raw value determined by the A/D converter for the full-bridge strain gauge with 16-bit resolution. The module returns between 3 and 10 measured values per X2X cycle depending on the configuration.

Effective resolution

In principle, the effective resolution of the A/D converter is dependent on the data rate and measurement range (see).

The following table shows how the effective resolution (in bits), or the RMS value range of the strain gauge value depend on the module configuration (data rate, measurement area).

Measurement range							
±16 mV/V		±8 mV/V		±4 mV/V		±2 mV/V	
Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
15.4	22,000	14.6	12,000	13.8	7,000	12.8	4,000

Table 21: Effective resolution of the strain gauge value in bits for the measurement range 2 to 16 mV/V

Measurement range							
±256 mV/V		±128 mV/V		±64 mV/V		±32 mV/V	
Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
17.1	70,000	16.7	53,000	16.4	43,000	15.9	31,000

Table 22: Effective resolution of the strain gauge value in bits for the measurement range 32 to 256 mV/V

1.2.2.12.6.3 A/D converter configuration

Name:
ConfigGain01_MultiSample

The measurement range for the A/D converter can be configured in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Standard measurement range (bit 2 = 0)	000	16 mV/V
		001	8 mV/V
		010	4 mV/V
		011	2 mV/V
	Extended measurement range (bit 2 = 1)[1)]	100	256 mV/V
		101	128 mV/V
		110	64 mV/V
		111	32 mV/V
3 - 7	Reserved	0	(must be 0)

1) Firmware V4 and later. In the standard measurement range (2 to 16 mV/V), open-circuit detection works reliably at all adjustable data rates. In the extended measurement range (32 to 256 mV/V), open circuit detection does not work reliably (because of the variable input impedance of the amplifier in relation to the set data rate).

1.2.2.12.6.4 A/D converter cycle time

Name:
ConfigCycletime01_MultiSample

The A/D converter cycle time can be configured in this register.

In order for multiple sampling to work, the X2X cycle time must be divisible by the A/D converter cycle time (i.e. result in a whole number).

Data type	Value	Information
USINT	0	50 µs (default)
	1	100 µs
	2 to 255	Reserved

1.2.2.12.6.5 Number of measured values

If the X2X cycle time is too short, then not all 10 measurements can be performed. To reduce the load on X2X Link, it makes sense to only transfer as many values as measurements that can be made. This is why it is possible to configure the number of measured values to be transferred (see "Function model 1 - Multisampling" on page 90).

Example: A/D converter cycle time = 50 µs

X2X cycle time	Number of measured values to be transferred
250 µs	5
300 µs	6
350 µs	7
400 µs	8
450 µs	9
≥500 µs	10

Example: A/D converter cycle time = 100 µs

X2X cycle time	Number of measured values to be transferred
300 µs	3
400 µs	4
500 µs	5
600 µs	6
700 µs	7
800 µs	8
900 µs	9
≥1 ms	10

1.2.2.12.7 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
250 µs

1.2.2.12.8 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

There is no limitation or basic dependency on the bus cycle time. In function model "0 - Standard", the I/O update time is defined using registers "ConfigOutput01" on page 93 and "ConfigCycletime01" on page 94.

Depending on the setting in register "ConfigCycletime01_MultiSample" on page 97, the I/O update time in function model "1 - Multiple sampling" is 50 or 100 µs.

1.3 X20AI1744-10

1.3.1 General information

This module works with both 4-wire and 6-wire strain gauge load cells. The concept applied by the module requires compensation in the measurement system. This compensation eliminates the absolute uncertainty in the measurement circuit, such as component tolerances, effective bridge voltage or zero point offset. The measurement precision refers to the absolute (compensated) value, which will only change as a result of changes in the operating temperature.

- 1 full-bridge strain gauge input
- Bridge voltage 10 VDC
- Data output rate configurable from 0.1 Hz to 7.5 kHz
- Special operating modes (synchronous mode and multisampling)
- Configurable filter level

1.3.2 Order data

Order number	Short description	Figure
	Analog inputs	
X20AI1744-10	X20 analog input module, 1 full-bridge strain input 10 V, 24-bit converter resolution, 5 kHz input filter	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 23: X20AI1744-10 - Order data

1.3.3 Technical data

Order number	X20AI1744-10
Short description	
I/O module	1 full-bridge strain gauge input
General information	
B&R ID code	0xF1A7
Status indicators	Channel status, operating state, module status
Diagnostics	
Module run/error	Yes, using LED status indicator and software
Open circuit	Yes, using LED status indicator and software
Input	Yes, using LED status indicator and software
Power consumption	
Bus	0.01 W
Internal I/O	0.65 W
Additional power dissipation caused by actuators (resistive) [W]	Max. +0.68 [1)]
Certifications	
CE	Yes
EAC	Yes
UL	cULus E115267 Industrial control equipment
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
Full-bridge strain gauge	
Strain gauge factor	2 to 256 mV/V, configurable using software
Connection	4- or 6-wire connections [2)]
Input type	Differential, used to evaluate a full-bridge strain gauge
Digital converter resolution	24-bit
Conversion time	Depends on the configured data output rate
Data output rate	0.1 - 7500 samples per second, configurable using software (f_{DATA})

Table 24: X20AI1744-10 - Technical data

Order number	X20AI1744-10
Input filter	
Cutoff frequency	5 kHz
Order	3
Slope	60 dB
ADC filter characteristics	Sigma-delta, see section "Filter characteristics of the sigma-delta A/D converter"
Operating range / Measurement sensor	162 to 5000 Ω
Influence of cable length [3]	See section "Calculation example".
Input protection	RC protection
Common-mode range	0 to 3 VDC Permissible input voltage range (with regard to the potential strain gauge GND) on inputs "Input +" and "Input -"
Insulation voltage between input and bus	500 V_{eff}
Conversion procedure	Sigma-delta
Output of digital value	
Broken bridge supply line	Value approaching 0
Broken sensor line	Value approaching ±end value (status bit "Line status monitoring" is set in register "Module status")
Valid range of values	0xFF800001 to 0x007FFFFF (-8,388,607 to 8,388,607)
Strain gauge supply	
Voltage	10.5 VDC / Max. 65 mA [4]
Short-circuit and overload resistant	Yes
Voltage drop for short-circuit protection	Max. 0.2 VDC at 65 mA and 25°C
Quantization [5]	
LSB value (16-bit)	
2 mV/V	641 nV
4 mV/V	1.28 µV
8 mV/V	2.56 µV
16 mV/V	5.13 µV
32 mV/V	10.25 µV
64 mV/V	20.51 µV
128 mV/V	41.02 µV
256 mV/V	82.03 µV
LSB value (24-bit)	
2 mV/V	2.50 nV
4 mV/V	5.01 nV
8 mV/V	10.01 nV
16 mV/V	20.03 nV
32 mV/V	40.05 nV
64 mV/V	80.11 nV
128 mV/V	160.22 nV
256 mV/V	320.43 nV
Temperature coefficient	
Rev. ≥E0	10 ppm/°C
Rev. <E0	30 ppm/°C
Electrical properties	
Electrical isolation	Bus isolated from analog input and strain gauge supply voltage Channel not isolated from I/O power supply
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	See section "Hardware configuration"
Storage	-40 to 85°C
Transport	-40 to 85°C

Table 24: X20AI1744-10 - Technical data

Order number	X20AI1744-10
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x terminal block X20TB12 separately. Order 1x bus module X20BM11 separately.
Pitch	12.5 $^{+0.2}$ mm

Table 24: X20AI1744-10 - Technical data

1) Depends on the full-bridge strain gauge being used.
2) With 6-wire connections, line compensation does not function (see section "Connection examples").
3) Sensor cable with twisted and shielded conductors, cable length as short as possible, cable routing separate from load circuits, without intermediate terminal to the sensor.
4) The maximum current of 90 mA is permitted up to an operating temperature of 45°C.
5) Quantization depends on the strain gauge factor.

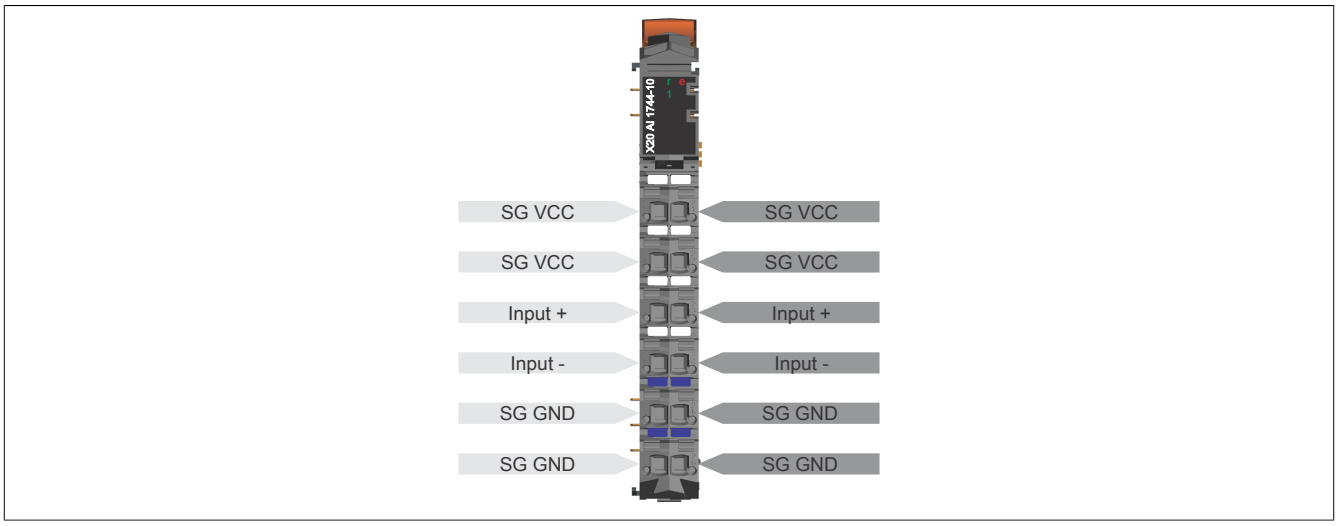
1.3.4 LED status indicators

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 system user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	Mode RESET
			Double flash	Mode BOOT (during firmware update)[1]
			Blinking	Mode PREOPERATIONAL
			On	Mode RUN
	e	Red	Off	No power to module or everything OK
			On	Error or reset state
	1	Green	Off	Possible causes: • Open circuit • Sensor is disconnected • Converter is busy
			On	Analog/digital converter running, value OK

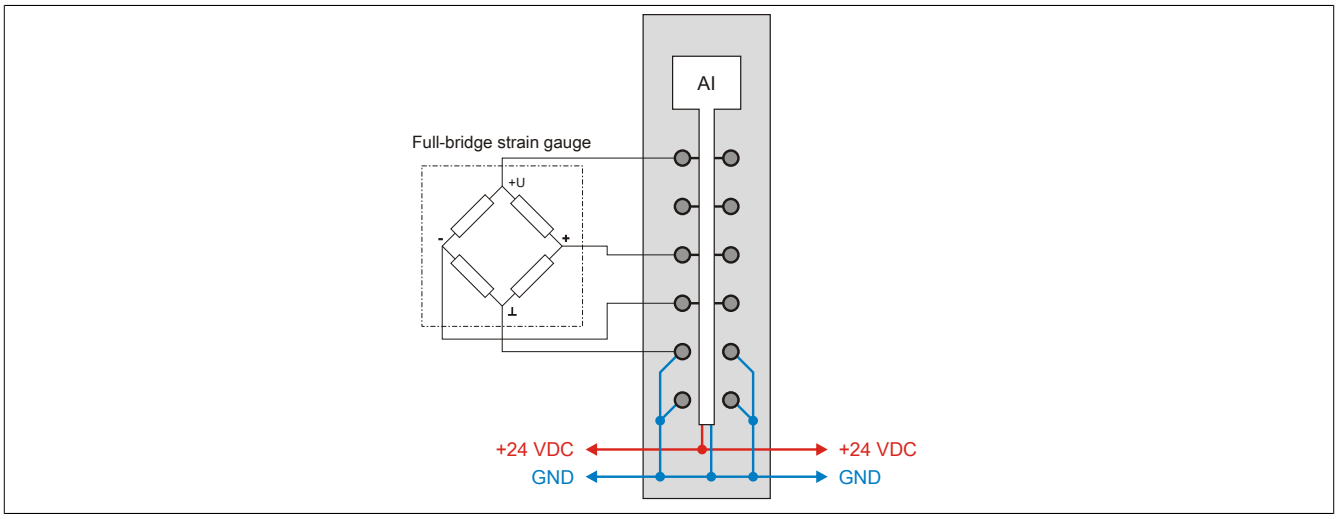
1) Depending on the configuration, a firmware update can take up to several minutes.

1.3.5 Pinout



1.3.6 Connection examples

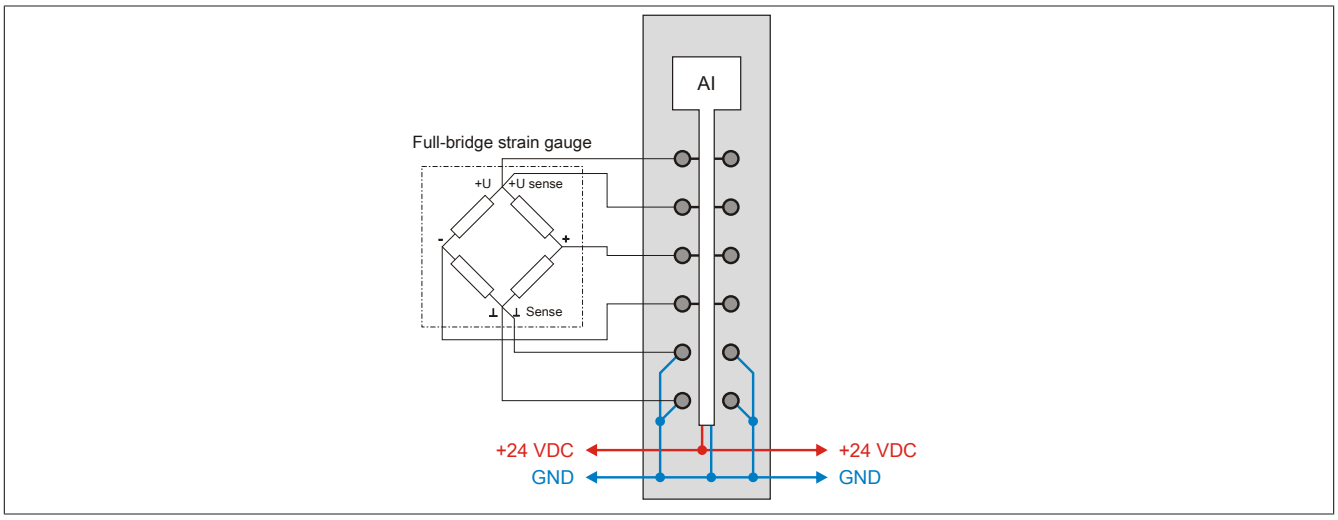
Full-bridge strain gauge with 4-wire connections



Full-bridge strain gauge with 6-wire connections

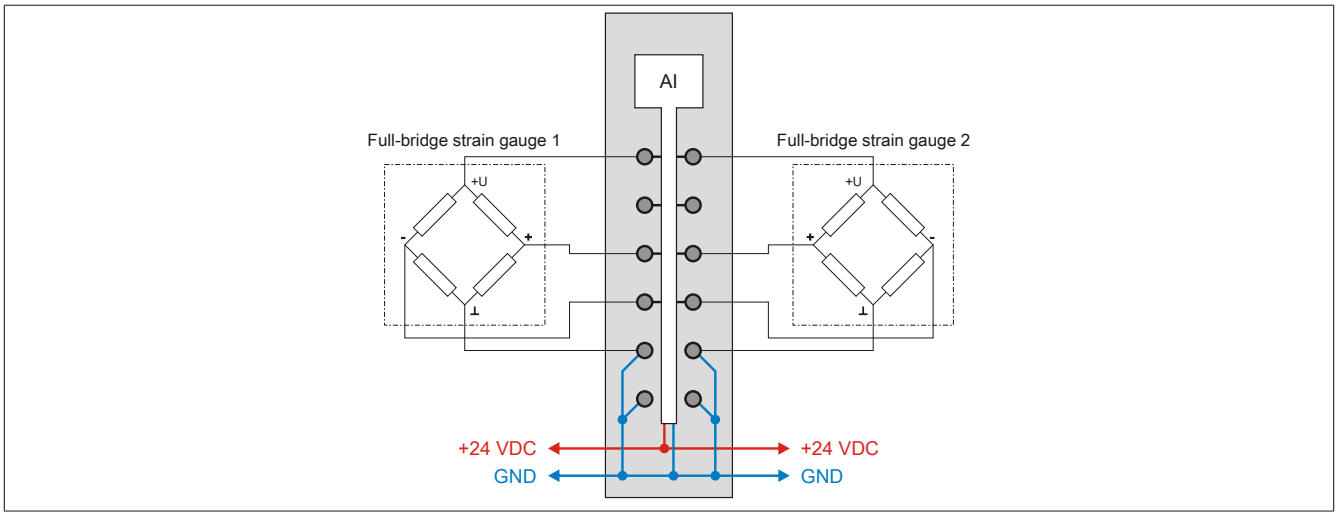
Full-bridge strain gauges can be connected to this module with 6-wire connections. Line compensation is not supported by the module, however. The sense lines are short circuited by the internally connected strain gauge VCC and GND connections (see "Input circuit diagram" on page 103). The measurement precision is therefore affected by changes in operating temperature. Longer cable lengths and smaller cable cross sections also increase the potential for errors in the measurement system.

In order to reduce cable resistance, the sense lines should be connected in parallel with the strain gauge supply lines. Optimal signal quality can be obtained by using a shielded twisted pair cable. The connections for the strain gauge supply lines, the sensor lines and the bridge differential voltage lines should each use one twisted pair cable.



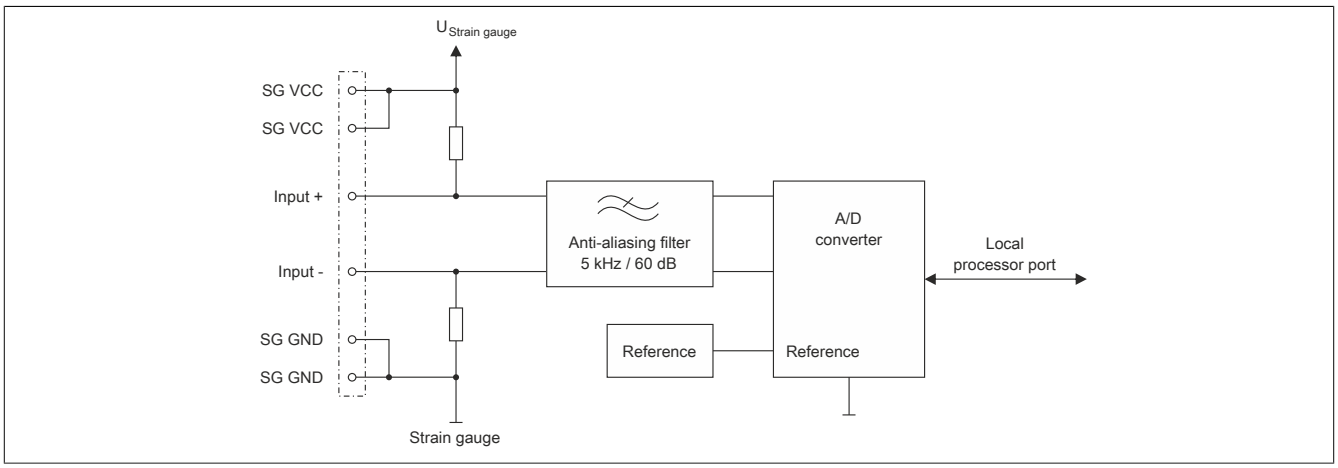
Parallel connection of 2 full-bridge strain gauges (4-wire connections)

If connecting the full-bridge strain gauges in parallel, the manufacturer's guidelines must be observed.



When connecting 3 or more full-bridge strain gauges in parallel, 2 lines must be connected together in an X20 terminal block.

1.3.7 Input circuit diagram

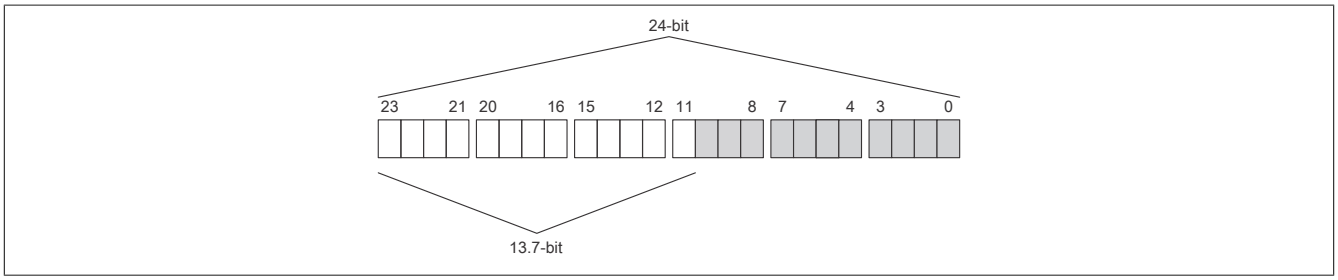


1.3.8 Effective resolution of the A/D converter

The A/D converter on the module provides a 24-bit measured value. The actual attainable noise-free resolution is always less than 24-bit, however. This "effective resolution" depends on the data rate and measurement range.

Example:

Based on the conversion method, a data rate of 2.5 Hz and a specified measurement range of 2 mV/V result in an effective resolution of13.7 bits:



The low-order bits (grayed out) contain only noise instead of valid values and are therefore not permitted to be evaluated.

With "Function model 1 - Multisampling", only the highest 16 bits are made available.

1.3.9 Calculation example

The following example shows the influence of the length of the measuring cable on the bridge voltage of the module and the quantization calculated with it.

1.3.9.1 Bridge voltage

Although the measuring bridge must be adjusted with the module, the cable length has an influence on the accuracy of the measurement. The reason for this is the voltage drop on the power supply lines of the measuring bridge. As a result, the strain gauge supply voltage at the measuring bridge no longer amounts to the full 10.5 V. The reduced bridge voltage also has an effect on the quantization.

Example

Characteristics of the measuring device used:

- Full-bridge strain gauge with 4-wire connections
- Material-dependent conductivity of the cable (copper: $12\frac{m}{\Omega \cdot mm^2}$)
- Cross section of the cable: 22 AWG = 0.34 mm²
- Length of the cable: 5 m
- Nominal current of the measuring bridge: 15 mA
- Bridge voltage of the module: 10.5 V

Actual bridge voltage taking the voltage drop on the measuring line into account:

$$10.5\ V - \frac{2 \cdot 5\,m}{12\frac{m}{\Omega \cdot mm^2} \cdot 0.34\,mm^2} \cdot 0.015A = 10.463\ V$$

The quantization must be calculated using the actual calculated bridge voltage (see "Quantization" on page 105).

1.3.9.2 Quantization

In a weighing application, the corresponding weight located on the connected load cell should be determined from the value derived from the module.

Example

The characteristics of the strain gauge load cell are as follows:

- Rated load: 1000 kg
- Strain gauge factor: 4 mV/V
- Actual bridge voltage: 10.463 V

Maximum quantization:
Multiplying the bridge factor of the strain gauge load cell with the bridge supply voltage from the module results in the value for the positive full-scale deflection at a specified rated load of 1000 kg:

4 mV/V · 10.5 V = 42 mV

Actual quantization:
Taking the voltage drop on the measuring line into account, the actual bridge voltage is 10.463 V (for the calculation, see section "Bridge voltage" on page 104). If this voltage is multiplied by the strain gauge factor of 4 mV/V, the following actual quantization results:

4 mV/V · 10.463 V = 41.85 mV

These 41.85 mVcorrespond to 99.6% of the maximum possible measurement range.

Information:

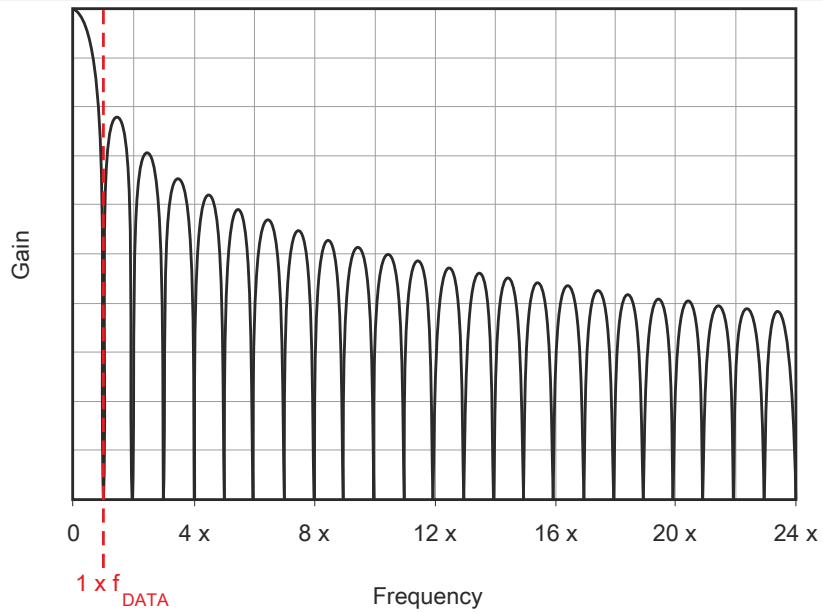
If the quantization decreases, the maximum possible effective resolution also decreases (see "Effective resolution of the A/D converter" on page 103).

With a simple Rule of Three calculation, the corresponding value can be calculated (as seen in the table) from weight to the converter value and vice versa. This simplified theoretical approach is only valid for an ideal measurement system. Calibration of the entire measurement system is recommended because not only the module, but particularly the strain gauge bridges exhibit tolerances (offset, gain). When taring, the gradient offset is recalculated and the gain of the linear equation is determined when normalized. In addition to the calculation displayed in the table, these calculations must also be carried out in the application.

24-bit value of the module		Quantization	Corresponding weight
0x007F FFFF	8,388,607	41.85 mV	1000 kg
0x0000 0001	1	4.99 nV	0.119 g
0x0000 20C3	8387	41.84 µV	1 kg
0x0001 0000	65536	327.0 µV	7.81 kg

The values for 1 LSB are also included in the module's technical data under item "Quantization" (1 LSB each for 16 bits and 24 bits).

1.3.10 Filter characteristics of the sigma-delta A/D converter

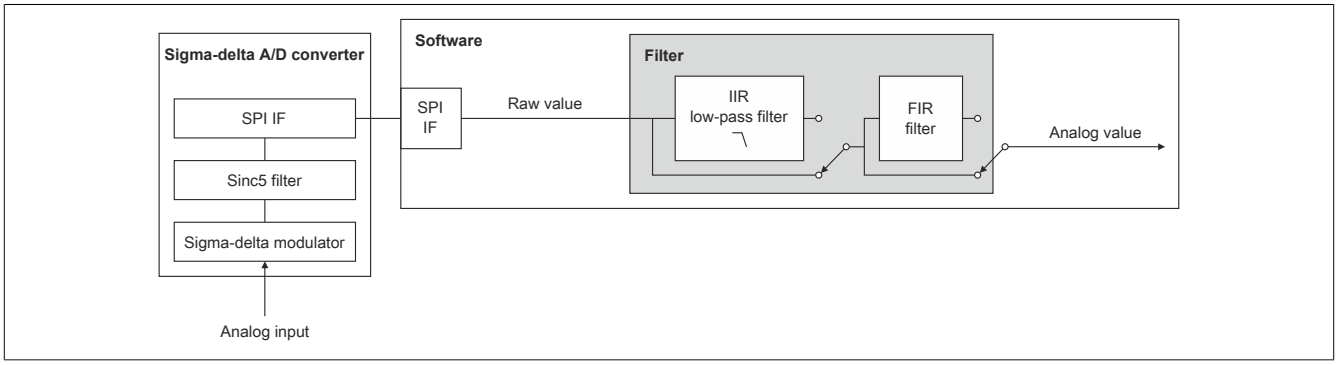


1.3.11 Software filters

2 filters are available for the analog input. They can be individually enabled and configured at runtime. By default, both filters are disabled when the device is switched on. The filters are controlled and configured using "Function model 2 - Extended filter".

In order to allow the filter behavior to be adapted to the measuring situation or machine cycle (high dynamics and low precision or low dynamics and high precision), the filter characteristics of both the IIR low-pass filter as well as the FIR filter can be changed synchronously at any time.

Filter diagram



1.3.11.1 IIR low-pass filter

1.3.11.1.1 General information

The IIR low-pass filter is used to generally smooth and increase the resolution of the analog value. The filter works according to the following formula:

$$y = y_{Old} + \frac{x - y_{Old}}{2^{Filter\ level}}$$

- x ... Current filter input value
- y_{Old} ... Old filter output value
- y ... New filter output value

Parameter "Filter level" in the formula above is configured using register "ConfigCommonOutput01" on page 125. "Filter level" = 0 if the IIR low-pass filter is disabled.

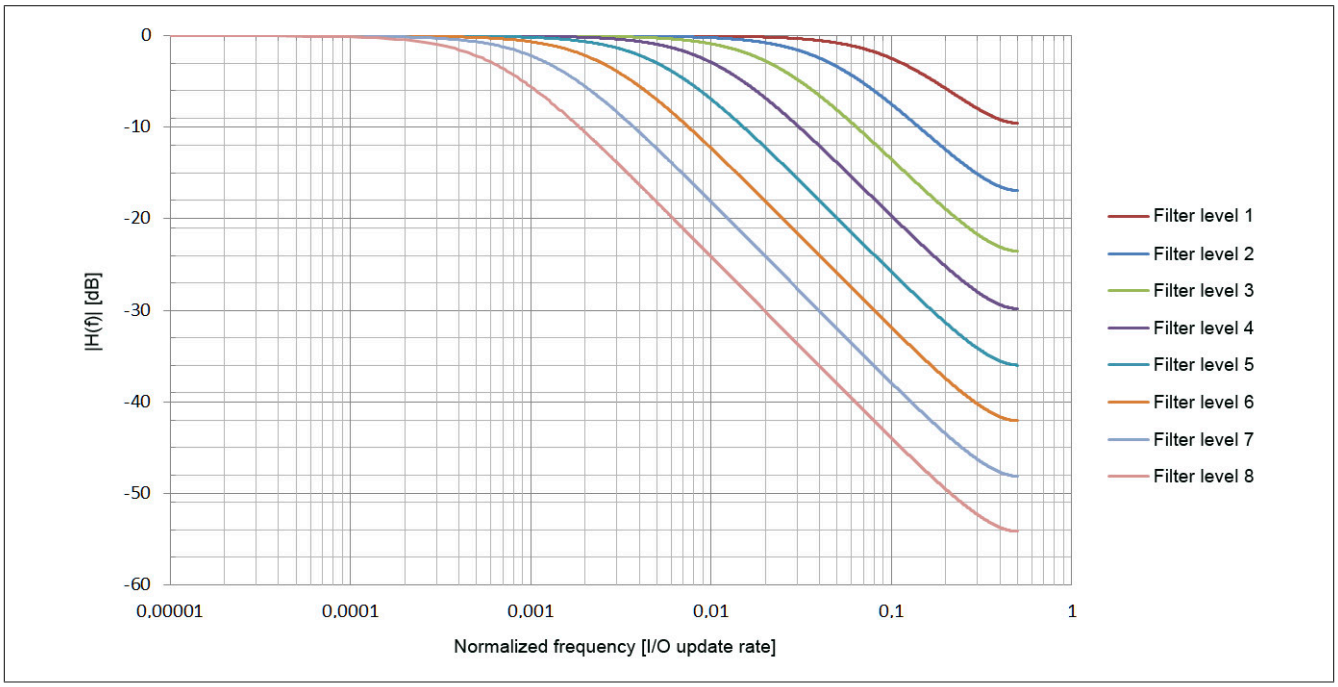
1.3.11.1.2 Filter characteristics of the first-order IIR low-pass filter

Limit frequency f_c

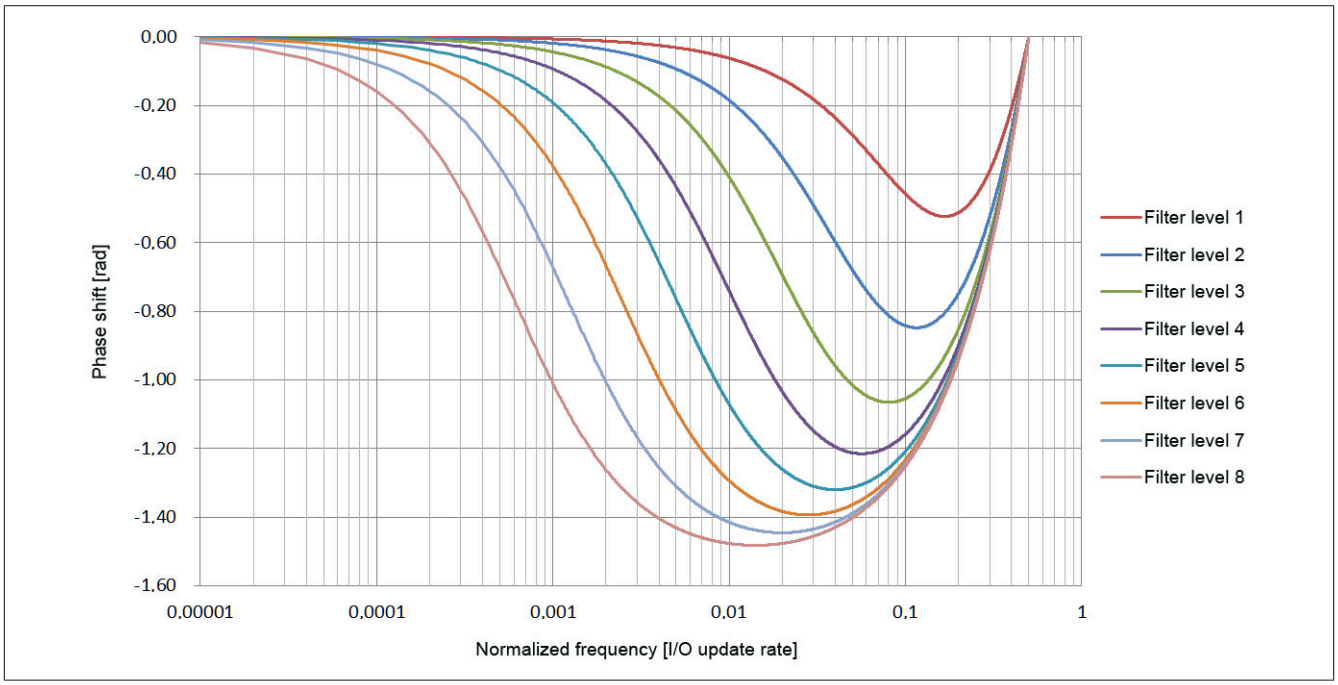
The following table provides an overview of the -3 dB limit frequency f_c depending on the configured filter level.

Filter level	Normalized f_c [I/O update rate]	f_c [Hz] I/O update rate = 15000/s	f_c [Hz] I/O update rate = 20000/s
1	0.11476	1721.4	2295.2
2	0.046	690	920
3	0.02124	318.6	424.8
4	0.01026	153.9	205.2
5	0.00504	75.6	100.8
6	0.0025	37.5	50
7	0.00124	18.6	24.8
8	0.00062	9.3	12.4

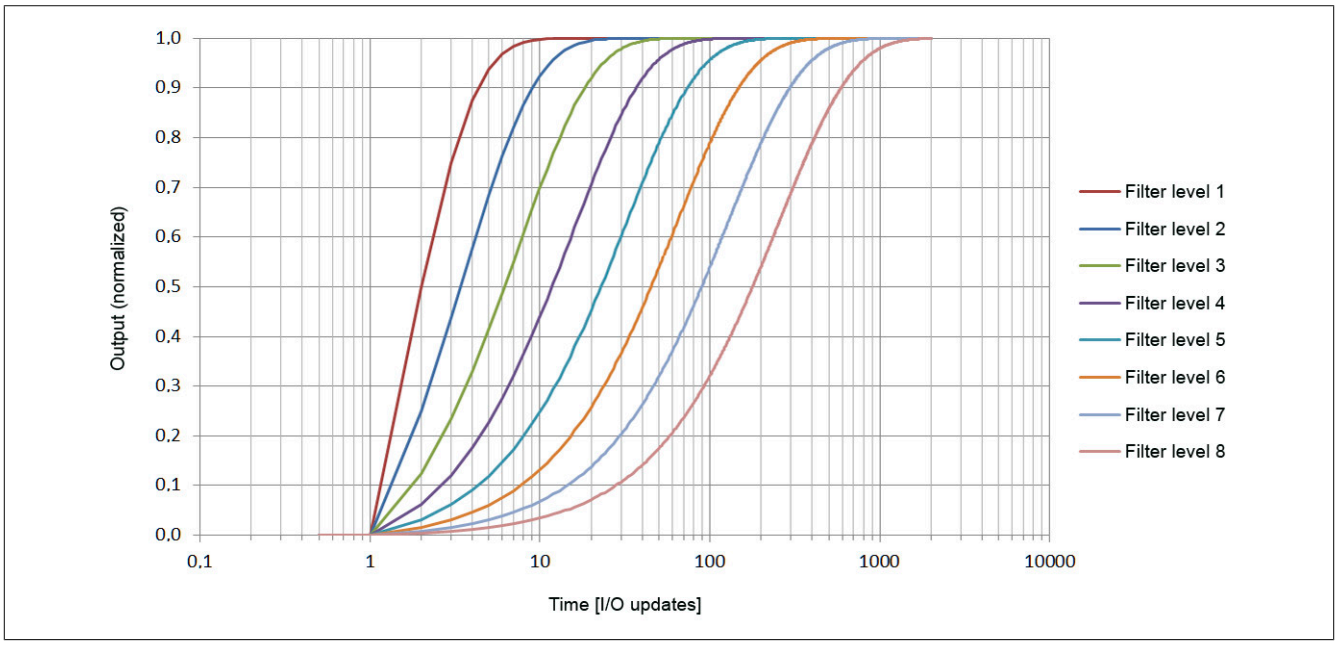
Gain of the IIR low-pass filter



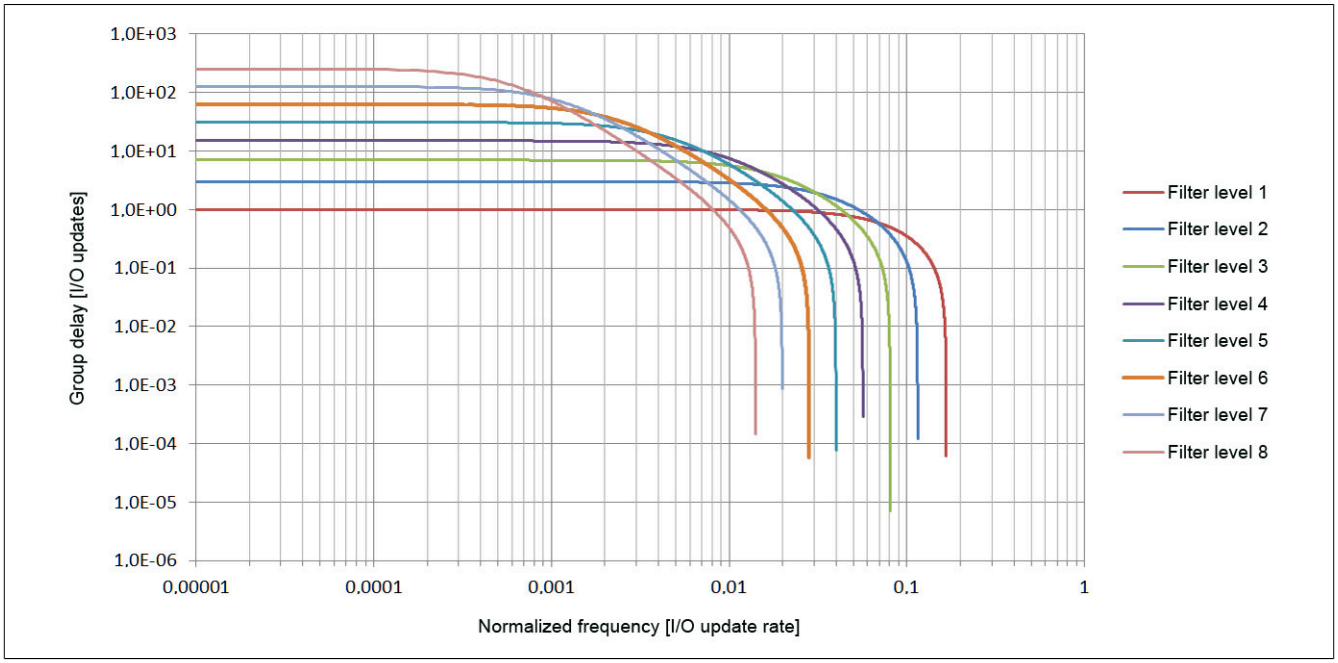
Phase shift of the IIR low-pass filter



Step response of the IIR low-pass filter



Group delay of the IIR low-pass filter



1.3.11.2 FIR filter

Like the IIR low-pass filter, the FIR filter can also be used to smooth out the signal and increase its resolution. In addition, configuring the filter length accordingly makes it possible to target and efficiently filter out individual interference frequencies. The source of these interference frequencies may be mechanical or electromagnetic. Multiples of these are also filtered out (as long as they are a whole-number factor of the data output rate).

Example:
Data output rate = 15000 samples/s, averaging over 15 values → "Notch" at 1 kHz (2 kHz, etc.)

When reconfiguring the filter, it takes 1/data rate (FIR filter in mode "Selectable data rate") or 1/filter frequency (FIR filter in mode"High-resolution data rate") until the filter is tuned. During tuning, bit 5 is set in register "StatusInput01" on page 127.

1.3.11.2.1 Characteristics of the FIR filter in mode "Selectable data rate"

The following table applies to "Function model 0 - Standard" and "Function model 254 - Bus controller" as well as for "Function model 2 - Extended filter" in mode "Selectable data rate".

			I/O update rate [Hz]		I/O update time [ms]	
Set value [1) 2)]	**Data rate (f_{Data}) [Hz]** [3) 4)]	**f_{Notch} [Hz]**	**Function models 0 and 254**	**Function model 2 (mode "Selectable data rate")**	**Function models 0 and 254**	**Function model 2 (mode "Selectable data rate")**
0000	2.5	2.5	2.5	15000	400	0.0667
0001	5	5	5	15000	200	0.0667
0010	10	10	10	15000	100	0.0667
0011	15	15	15	15000	66.6667	0.0667
0100	25	25	25	15000	40	0.0667
0101	30	30	30	15000	33.3333	0.0667
0110	50	50	50	15000	20	0.0667
0111	60	60	60	15000	16.6667	0.0667
1000	100	100	100	15000	10	0.0667
1001	500	500	500	15000	2	0.0667
1010	1000	1000	1000	15000	1	0.0667
1011	2000	2000	2000	20000	0.5	0.05
1100	3750	3750	3750	15000	0.2667	0.0667
1101	7500	7500	7500	15000	0.1333	0.0667
1110	Reserved					
1111	Reserved					

1) Function model 0 and 254: Bits 0 to 3 of register "ConfigOutput01" on page 118
2) Function model 2: Bits 0 to 3 of register "ConfigDatarateOutput01" on page 33
3) Function models 0 and 254: Data rate = 1/Filter length [s] (f_{Notch}) = I/O update rate
4) Function model 2: Data rate = 1/Filter length [s] (f_{Notch})

1.3.11.2.2 Characteristics of the FIR filter in mode "High-resolution data rate"

The following table applies to "Function model 2 - Extended filter".

Setpoint [0.1 Hz] 1)	Data rate (f_{Data}) [Hz]	f_{Notch} [Hz]	I/O update time [µs]
1 to 65535	Setpoint / 10	= Data rate	≈50 µs 2)

1) Setpoint from register "ConfigHighResolutionOutput01" on page 33
2) The value varies between 42 and 56 µs (see also the next section "I/O update time")

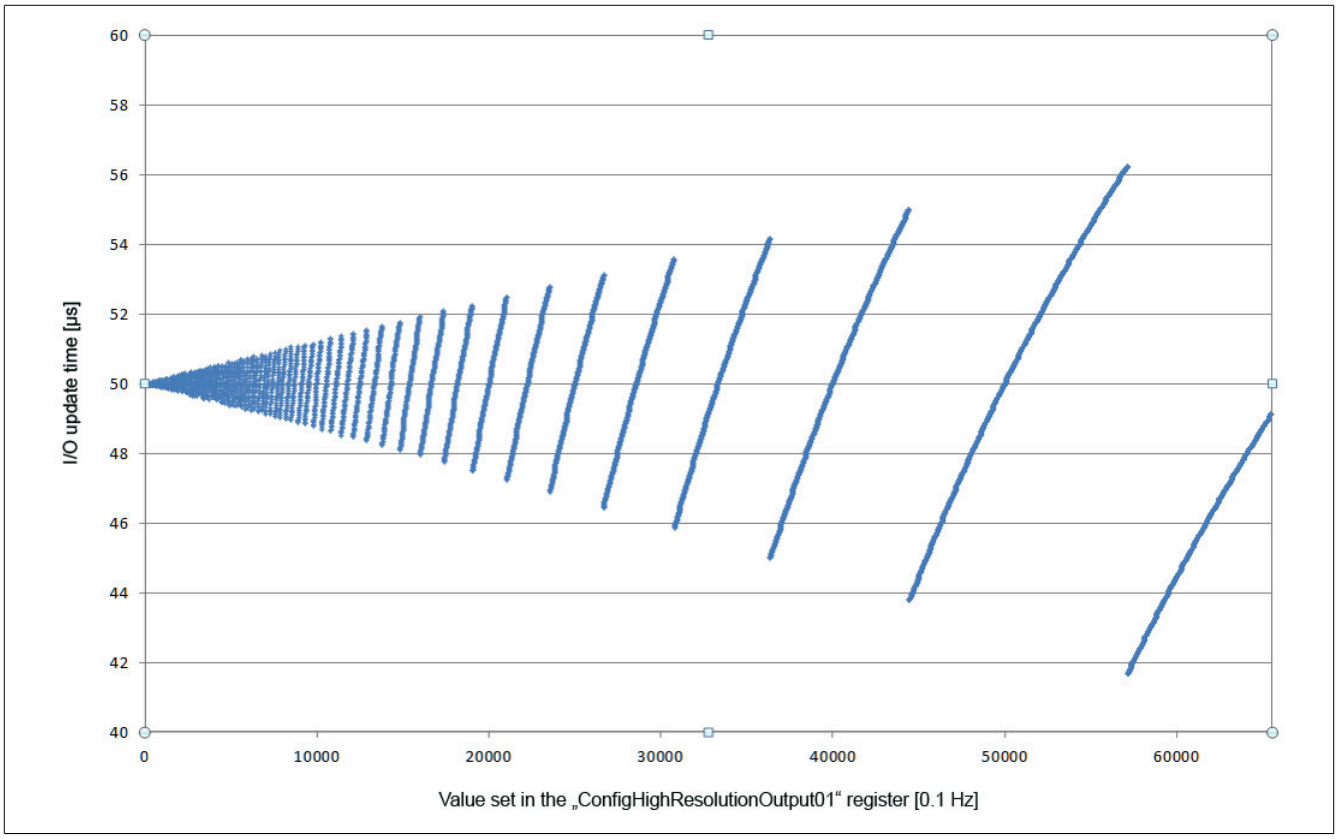
I/O update time

The value of the I/O update time depends on the setpoint and varies between 42 and 56 µs. The following formula can be used to precisely calculate the I/O update time:

I/O update time = 1e6 · (1e-4 - 10 / (Setpoint · [10 / (5e-5 · Setpoint)]))

Legend: The square brackets in the formula above mean that the calculated value must be rounded to a whole number.

The following image shows the I/O update time depending on the setpoint:

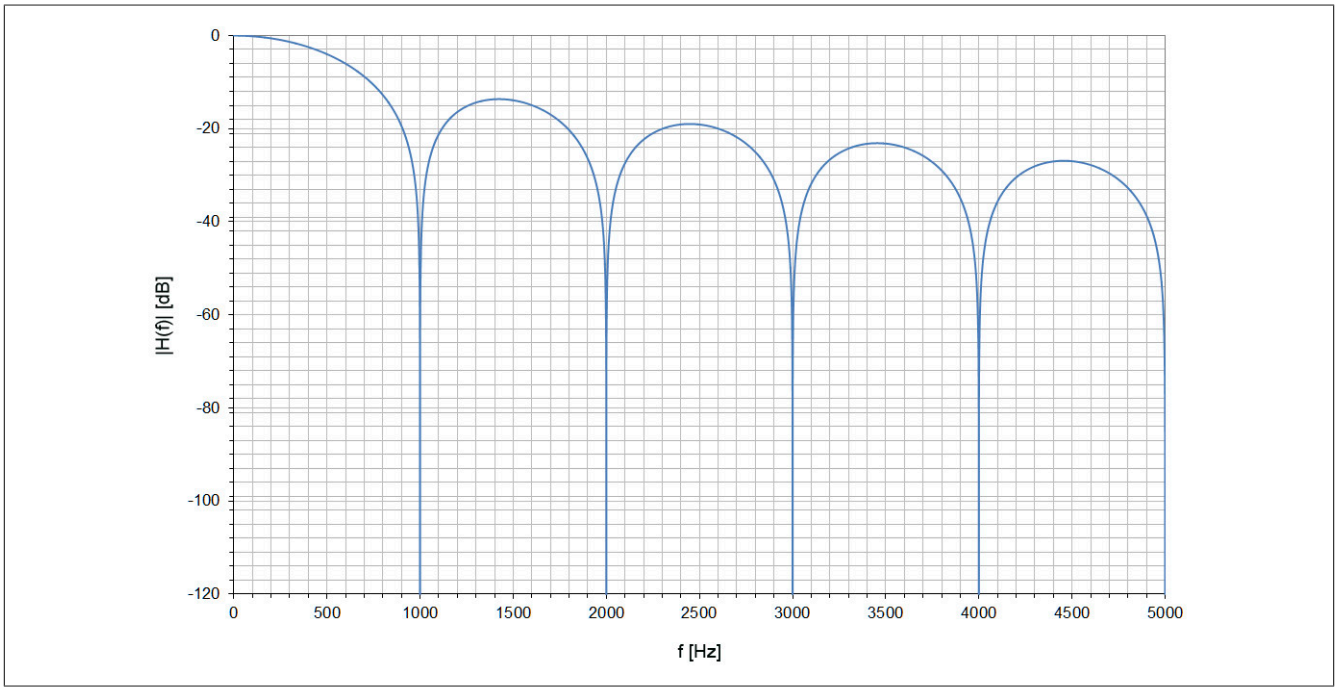


1.3.11.2.3 Examples for the gain of the FIR filter

Example 1

Filter setting = 10:

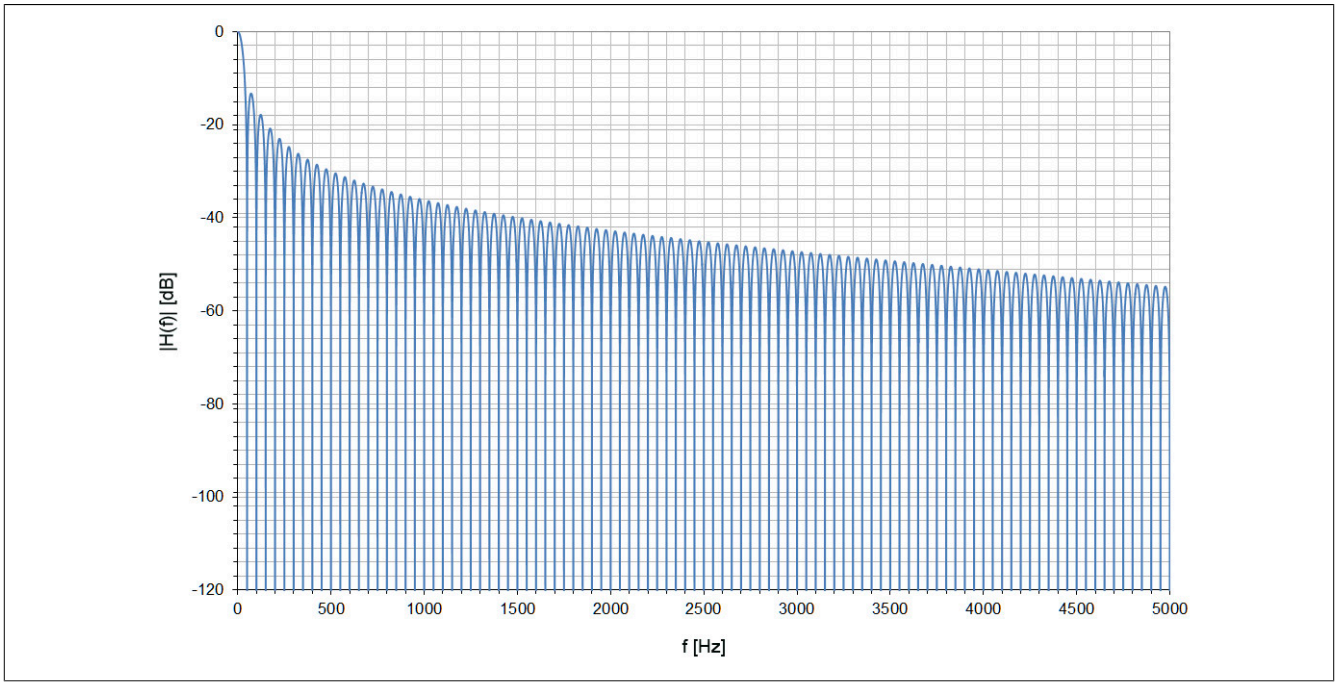
- f_{Notch} = 1000 Hz
- f_c = 439.3 Hz



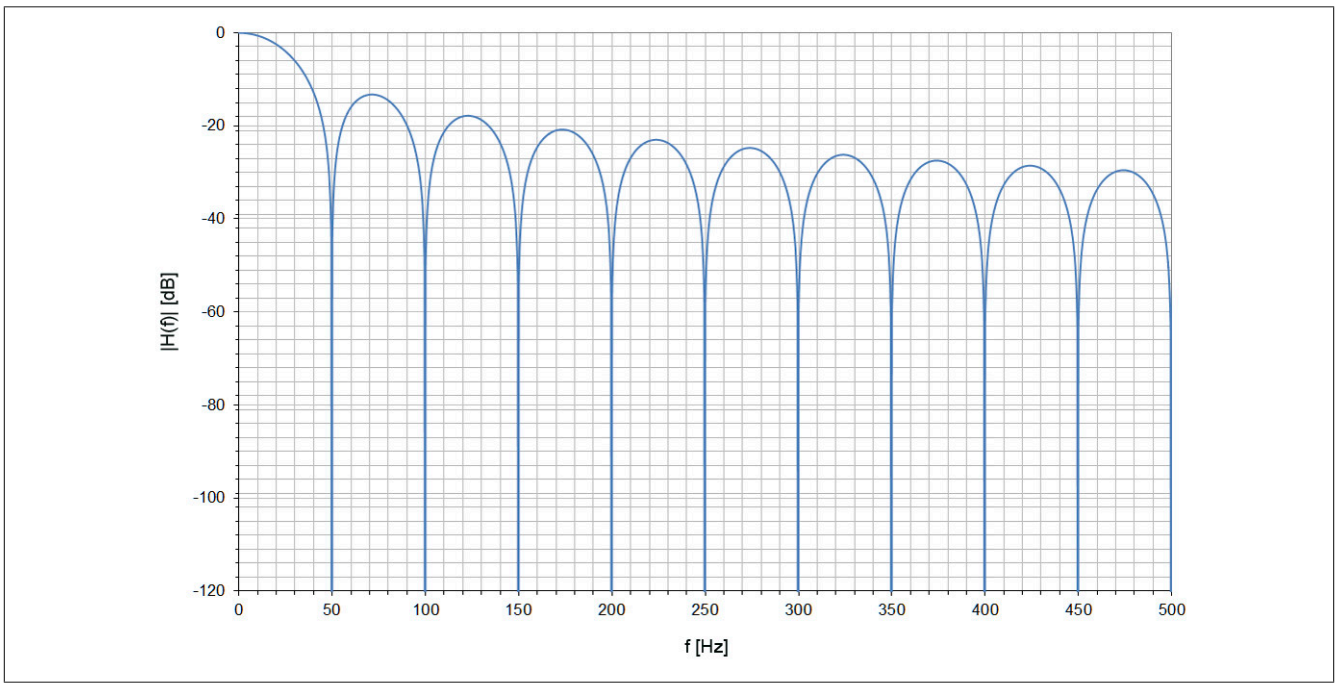
Example 2

Filter setting = 6:

- f_{Notch} = 50 Hz
- f_c = 21.8 Hz



Detailed excerpt from the filter curve shown above:

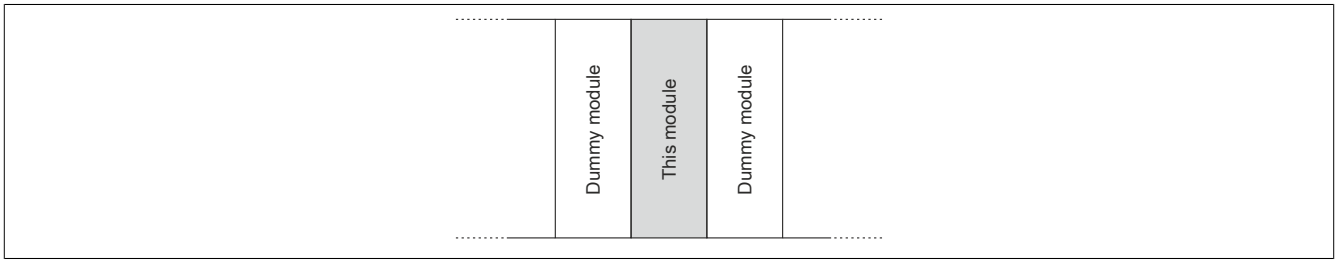


1.3.12 Hardware configuration

1.3.12.1 Hardware configuration for horizontal installation starting at 55°C ambient temperature

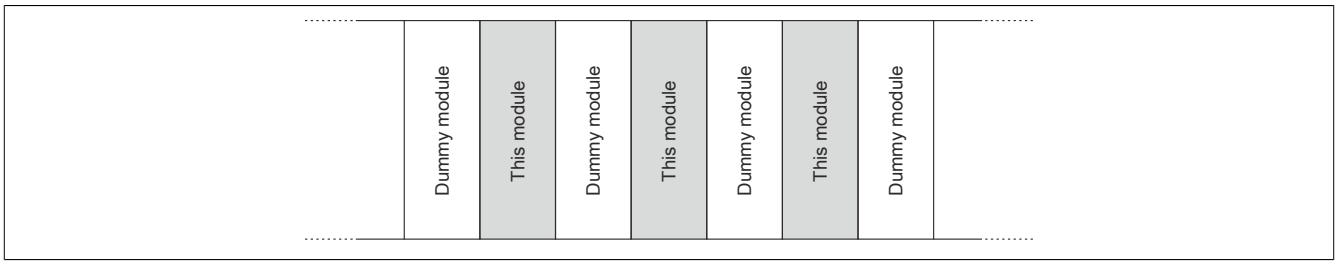
Operating a strain gauge module

Starting at an ambient temperature of 55°C, a dummy module must be connected to the left and right of the strain gauge module in a horizontal mounting orientation.



Operating multiple strain gauge modules side by side

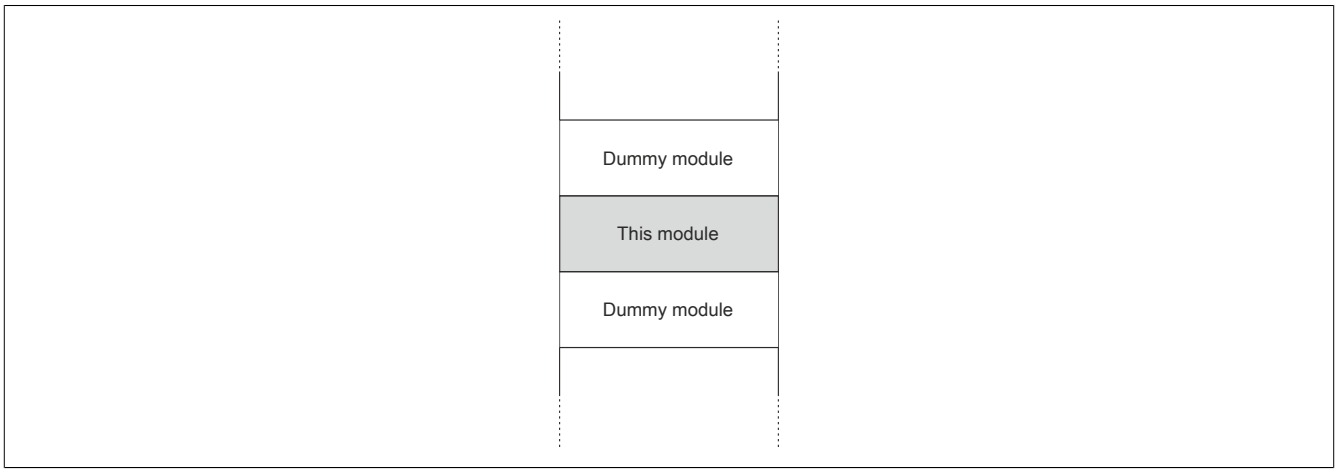
If 2 or more horizontal strain gauge modules are being operated in a cluster, the following arrangement of modules must be observed.



1.3.12.2 Hardware configuration for vertical installation starting at 45°C ambient temperature

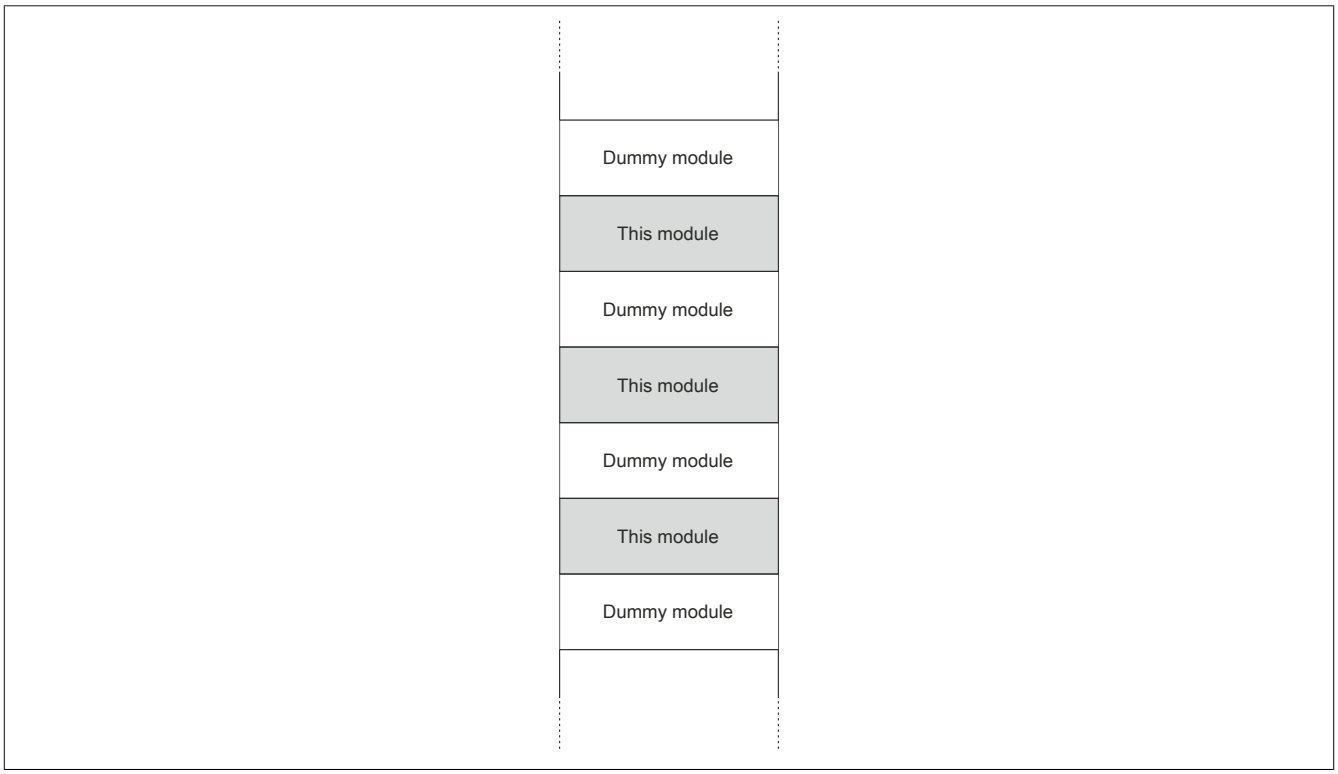
Operating a strain gauge module

Starting at an ambient temperature of 45°C, a dummy module must be connected to the left and right of the strain gauge module in a vertical mounting orientation.



Operating multiple strain gauge modules side by side

If 2 or more vertical strain gauge modules are being operated in a cluster, the following arrangement of modules must be observed.



1.3.13 Register description

1.3.13.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 system user's manual.

1.3.13.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration						
16	ConfigOutput01 (A/D converter configuration)	USINT			•	
18	ConfigCycletime01	UINT				•
32	AdcClkFreqShift01	USINT				•
Analog signal - Communication						
2	StatusInput01	USINT	•			
4	AnalogInput01	DINT	•			

1.3.13.3 Function model 1 - Multisampling

In this function model, the A/D converter is operated synchronously to X2X Link with a predefined A/D converter cycle time. The value is configurable as 50 or 100 µs.

The module returns between 3 and 10 measured values per X2X cycle depending on the configuration. With an X2X cycle time of 400 µs and A/D converter cycle time of 50 µs, exactly 8 measurements are performed and the module can return 8 values (strain gauge value 01 to strain gauge value 08).

If a longer cycle time is used, the values returned correspond to the last measurements. If using an X2X cycle time that is not a whole number multiple of the A/D converter cycle time, then the conversion cannot be synchronized with X2X Link. In this case, the module outputs the invalid value 0x8000.

Example 1

If using an X2X cycle time of 800 µs, it is possible to perform 16 measurements per X2X cycle if the A/D converter cycle time equals 50 µs. The first 6 measured values are discarded; the last 10 measured values are provided by the module.

With a shorter X2X cycle time, the number of measured values should not exceed the number of measurements that can actually be made. All other measured values are invalid (0x8000). To minimize the load on the X2X Link network, it is possible to disable these unneeded registers (see "Number of measured values" on page 123).

Example 2

If using an X2X cycle time of 300 µs, it is possible to perform 6 measurements per X2X cycle if the A/D converter cycle time equals 50 µs. For this reason, only the first 6 registers are valid. The registers for the 7th through 10th measured value (AnalogInput07 to AnalogInput10) should be disabled by setting Number of measured values to "6 measured values" in the I/O configuration.

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration						
1601	ConfigGain01_MultiSample	USINT			•	
1603	ConfigCycletime01_MultiSample	USINT				•
Analog signal - Communication						
2	StatusInput01	USINT	•			
1534 + N * 4	AnalogInput0N (N = 1 to 10)	INT	•			

1.3.13.4 Function model 2 - Extended filter

This function model allows the IIR low-pass filter and the FIR filter to be enabled.

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration						
272	ConfigCommonOutput01 (A/D converter and IIR filter configuration)	USINT			•	
288	ConfigFilterOutput01	UINT				•
273	ConfigDatarateOutput01	USINT			•	
274	ConfigHighResolutionOutput01	UINT			•	
Analog signal - Communication						
2	StatusInput01	USINT	•			
4	AnalogInput01	DINT	•			
256	AdcConvTimeStampInput01	DINT	•			

1.3.13.5 Function model 254 - Bus controller

In function model "254 - Bus controller", the module behaves as it does in "Function model 0 - Standard" with the exception that it is not synchronized to the X2X Link network even if synchronous mode is enabled in register "ConfigOutput01" on page 118. Instead, the module behaves as if the set A/D converter cycle time is not a factor or multiple of the X2X cycle time and attempts to maintain the set A/D converter cycle time as precisely as possible.

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration							
16	0	ConfigOutput01 (A/D converter configuration)	USINT			•	
18	18	ConfigCycletime01	UINT				•
32	32	AdcClkFreqShift01	USINT				•
Analog signal - Communication							
2	4	StatusInput01	USINT	•			
4	0	AnalogInput01	DINT	•			

1) The offset specifies the position of the register within the CAN object.

1.3.13.5.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

1.3.13.5.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

1.3.13.6 Registers for function models "0 - Standard" and "254 - Bus controller"

1.3.13.6.1 A/D converter configuration

Name:
ConfigOutput01

The data rate and measurement range of the A/D converter can be configured in this register.

Data type	Values	Bus controller default setting
USINT	See bit structure.	13

Bit structure:

Bit	Description	Value	Information
0 - 3	Data rate f_{DATA} (samples per second):	0000	2.5
		0001	5
		0010	10
		0011	15
		0100	25
		0101	30
		0110	50
		0111	60
		1000	100
		1001	500
		1010	1000
		1011	2000
		1100	3750
		1101	7500 (bus controller default setting)
		1110	Synchronous mode
		1111	Reserved
4 - 6	Standard measurement range (bit 6 = 0)	000	16 mV/V (bus controller default setting)
		001	8 mV/V
		010	4 mV/V
		011	2 mV/V
	Extended measurement range (bit 6 = 1)	100	256 mV/V
		101	128 mV/V
		110	64 mV/V
		111	32 mV/V
7	Reserved	0	(must be 0)

1.3.13.6.1.1 Synchronous mode

The module's analog/digital converter (A/D converter) can optionally be operated and read synchronously to the X2X Link network. Synchronous mode is enabled by selecting the respective operating mode in register "ConfigOutput01" on page 118. A time between 200 and 2000 µs must be set in register "ConfigCycletime01" on page 119 for this. If this time is a whole number factor or multiple of the configured cycle time of X2X Link, then the A/D converter is read synchronously to X2X Link.

Information:

The A/D converter cycle time must be ≥1/4 of the X2X cycle time!

Bit 2 in *Module status* is set (i.e. A/D converter not running synchronously)...

- ... If the configured A/D converter cycle time cannot be synchronized with X2X Link.
- ... If the module is still in the settling phase.

Jitter, dead time and settling time:

Jitter A/D converter cycle times <1500 µs A/D converter cycle times >1500 µs	 Max. ±1 µs Max. ±4 µs
X2X link dead time	$50\ \mu s + \frac{\text{X2X cycle time}}{128}$
Settling time	150 x X2X cycle time

The settling time corresponds to the time needed until the A/D converter can be operated after enabling synchronous mode or following conversion of the A/D converter cycle time.

1.3.13.6.2 A/D converter cycle time

Name:
ConfigCycletime01

This register is only used in Synchronous mode. If synchronous mode is enabled in the A/D converter configuration, then the module attempts to operate the A/D converter as synchronously as possible to the X2X Link network (based on the A/D converter cycle time set in this register). It is of course necessary for the X2X Link cycle time and the A/D converter cycle time to have a certain ratio. The following conditions must be observed:

1) A/D converter cycle time ≥ 1/4 X2X cycle time
2) A/D converter cycle time corresponds to a whole number factor or multiple of the X2X cycle time
3) A/D converter cycle time must be in the range 50 to 2000 µs

Data type	Values	Information
UINT	50 to 2000	Bus controller default setting: 400

1.3.13.6.3 A/D converter clock frequency shift

Name:
AdcClkFreqShift01

In rare cases, strain gauge modules connected to neighboring slots can influence one another. This can result in temporary, minimal deviations in measured values. This can only occur if the sigma-delta A/D converters on the neighboring strain gauge modules are operated at exactly the same clock frequency.

In most cases, these clock frequencies vary slightly due to part variances. When they are the same however, this register on the strain gauge module provides a safe way for an application to prevent this type of mutual influence.

Data type	Values	Information
SINT	-128 to 127	Bus controller default setting: 127

This register can be used to vary the clock frequency in increments of 200 ppm. Setting values from -50 to 50 cover a range of -10000 ppm to 10000 ppm. This corresponds with -1% to 1%.

Values beyond this range will cause activation of a default mode. The frequency shift is derived from the last 2 digits of the serial number by the module firmware. This saves time that would otherwise be needed for programming, provided that the last two digits of the serial numbers on the neighboring modules are not the same

Register value	Frequency shift in ppm	Example of a sampling rate[1)]
127	((SerialNo. modulo 100) - 50) * (-200) ppm	Based on the serial number
...	...	...
51	((SerialNo. modulo 100) - 50) * (-200) ppm	Based on the serial number
50	10000	505
49	9800	504.9
...	...	...
2	400	500.2
1	200	500.1
0	0	500
-1	-200	499.9
-2	-400	499.8
...	...	...
-50	-10000	495
-51	((SerialNo. modulo 100) - 50) * (-200) ppm	Based on the serial number
...	...	...
-128	((SerialNo. modulo 100) - 50) * (-200) ppm	Based on the serial number

1) Nominal sampling rate of 500 samples per second

Important:

As shown in the table above, shifting the A/D converter clock frequency will equally shift the A/D converter sampling rate. Shifting the A/D converter clock frequency too much can cause problems with disturbance suppression particularly when a very specific sampling rate has been defined to suppress existing disturbances (e.g. 50 Hz to suppress the 50 Hz hum). See also "Filter characteristics of the sigma-delta A/D converter" on page 106.
It is situations like this where the option to manually shift the frequency in the I/O configuration or ASIOACC library should be utilized rather than relying on the default frequency shift that is based on the serial number.

A frequency shift like the one shown below would be sufficient to prevent modules from influencing one another and would not cause any noticeable difference to the filter characteristics.

Slot	1	2	3	4	5	6	...
A/D converter clock frequency shift	0	2	-1	1	-2	0	...

Information:

- **This register has no effect in synchronous mode because the firmware regulates the A/D converter clock frequency in such a way that the A/D converter cycle is synchronous with the X2X cycle.**
- **When writing to this register using the ASIOACC library, only the lowest value byte of the written value is accepted. For example, the value 256 (=0x100) is identical to the value 0 (=0x00).**

1.3.13.6.4 Module status

Name:
StatusInput01

The current state of the module is indicated in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	A/D converter value	0	Valid A/D converter value
		1	Invalid A/D converter value (analog value = 0xFF800000). Possible causes: • Strain gauge supply error • I/O power supply error • A/D converter not (yet) configured
1	Line monitoring	0	Ok
		1	Open circuit
2	Only valid in synchronous mode	0	A/D converter runs synchronous to X2X Link
		1	A/D converter does not run synchronous to X2X Link
3 - 7	Reserved	-	

1.3.13.6.5 Strain gauge value

Name:
AnalogInput01

This register contains the raw value determined by the A/D converter for the full-bridge strain gauge with 24-bit resolution.

Data type	Values	Information
DINT	-8,388,608	Negative invalid value
	-8,388,607	Negative full-scale deflection / Underflow
	-8,388,606 to 8388606	Valid range
	8,388,607	Positive full-scale deflection / Overflow / Open circuit

Effective resolution

In principle, the effective resolution of the A/D converter is dependent on the data rate and the measurement range (see "Effective resolution of the A/D converter" on page 103).

The following table shows how the effective resolution (in bits) or effective range of values of the strain gauge value depend on the module configuration (data rate, measurement range):

	Measurement range							
	±16 mV/V		±8 mV/V		±4 mV/V		±2 mV/V	
Data rate f_{DATA} [Hz]	Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
2.5	16.9	±61,100	15.4	±21,600	14.5	±11,600	13.7	±6,650
5	16.6	±49,700	15.2	±18,800	14.2	±9,410	13.6	±6,210
10	16.0	±32,800	15.2	±18,800	14.2	±9,410	13.1	±4,390
15	16.0	±32,800	15.2	±18,800	14.1	±8,780	13.1	±4,390
25	15.9	±30,600	14.7	±13,300	13.9	±7,640	12.7	±3,330
30	15.7	±26,600	14.6	±12,400	13.6	±6,210	12.7	±3,330
50	15.4	±21,600	14.5	±11,600	13.3	±5,040	12.2	±2,350
60	15.2	±18,800	14.3	±10,100	13.1	±4,390	12.2	±2,350
100	14.9	±15,300	13.8	±7,130	13.0	±4,100	12.0	±2,050
500	13.8	±7,130	12.8	±3,570	11.7	±1,660	10.7	±832
1000	13.3	±5,040	12.3	±2,520	11.3	±1,260	10.3	±630
2000	12.7	±3,330	11.9	±1,910	10.8	±891	9.7	±416
3750	12.4	±2,700	11.4	±1,350	10.4	±676	9.2	±294
7500	12.0	±2,050	11.0	±1,020	10.1	±549	8.9	±239

Table 25: Effective resolution of the strain gauge value in bits for the measurement range 2 to 16 mV/V

	Measurement range							
	±256 mV/V		±128 mV/V		±64 mV/V		±32 mV/V	
Data rate f_{DATA} [Hz]	Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
2.5	20.8	±913,000	20.0	±524,000	18.8	±228,000	17.6	±99,300
5	20.2	±602,000	19.5	±371,000	18.3	±161,000	17.4	±86,500
10	20.1	±562,000	19.4	±346,000	18.3	±161,000	17.0	±65,500
15	19.8	±456,000	19.0	±262,000	17.9	±122,000	17.0	±65,500
25	19.7	±426,000	18.8	±228,000	17.9	±122,000	16.7	±53,200
30	19.7	±426,000	18.5	±185,000	17.5	±92,700	16.7	±53,200
50	19.2	±301,000	18.3	±161,000	17.5	±92,700	16.3	±40,300
60	19.2	±301,000	18.2	±151,000	17.2	±75,300	16.2	±37,600
100	18.9	±245,000	17.9	±122,000	16.8	±57,100	15.9	±30,600
500	17.6	±99,300	16.8	±57,100	15.8	±28,500	14.8	±14,300
1000	17.2	±75,300	16.2	±37,600	15.2	±18,800	14.3	±10,100
2000	16.5	±46,300	15.8	±28,500	14.7	±13,300	13.8	±7,130
3750	16.1	±35,100	15.4	±21,600	14.3	±10,100	13.3	±5,040
7500	15.9	±30,600	15.0	±16,400	14.0	±8,190	13.0	±4,100

Table 26: Effective resolution of the strain gauge value in bits for the measurement range 32 to 256 mV/V

1.3.13.7 Register for "Function model 1 - Multisampling"

1.3.13.7.1 A/D converter configuration

Name:
ConfigGain01_MultiSample

The measurement range for the A/D converter can be configured in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Standard measurement range (bit 2 = 0)	000	16 mV/V
		001	8 mV/V
		010	4 mV/V
		011	2 mV/V
	Extended measurement range (bit 2 = 1)	100	256 mV/V
		101	128 mV/V
		110	64 mV/V
		111	32 mV/V
3 - 7	Reserved	0	(must be 0)

1.3.13.7.2 A/D converter cycle time

Name:
ConfigCycletime01_MultiSample

The A/D converter cycle time can be configured in this register.

In order for multisampling to work, the X2X cycle time must be divisible by the A/D converter cycle time to produce a whole number.

Data type	Value	Information
USINT	0	50 µs (default)
	1	100 µs
	2 to 255	Reserved

1.3.13.7.3 Number of measured values

If the X2X cycle time is too short, then not all 10 measurements can be performed. To reduce the load on X2X Link, it makes sense to only transfer as many values as measurements that can be made. This is why it is possible to configure the number of measured values to be transferred (see "Function model 1 - Multisampling" on page 116).

Example: A/D converter cycle time = 50 µs

X2X cycle time	Number of measured values to be transferred
250 µs	5
300 µs	6
350 µs	7
400 µs	8
450 µs	9
≥500 µs	10

Example: A/D converter cycle time = 100 µs

X2X cycle time	Number of measured values to be transferred
300 µs	3
400 µs	4
500 µs	5
600 µs	6
700 µs	7
800 µs	8
900 µs	9
≥1 ms	10

1.3.13.7.4 Module status

Name:
StatusInput01

This register contains the current state of the module.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	A/D converter values	0	Valid A/D converter value
		1	Invalid A/D converter value
1	Line monitoring	0	OK
		1	Open circuit An open circuit was found during at least one measurement in this X2X cycle. This bit is reset if all measurements are OK after correcting this error, i.e. it does not have to be acknowledged.
2	Synchronous mode	0	A/D converter runs synchronous to X2X Link
		1	A/D converter does not run synchronous to X2X Link
3 - 7	Reserved	-	

1.3.13.7.5 Strain gauge value - Multiple

Name:
AnalogInput01 to AnalogInput10

This register contains the raw value determined by the A/D converter for the full-bridge strain gauge with 16-bit resolution. The module returns between 3 and 10 measured values per X2X cycle depending on the configuration.

Effective resolution

In principle, the effective resolution of the A/D converter is dependent on the data rate and measurement range (see "Effective resolution of the A/D converter" on page 103).

The following table shows how the effective resolution (in bits) or effective range of values of the strain gauge value depend on the module configuration (data rate, measurement range).

Measurement range							
±16 mV/V		±8 mV/V		±4 mV/V		±2 mV/V	
Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
11.7	±1,700	10.7	±840	9.8	±430	8.8	±220

Table 27: Effective resolution of the strain gauge value in bits for the measurement range 2 to 16 mV/V

Measurement range							
±256 mV/V		±128 mV/V		±64 mV/V		±32 mV/V	
Bits	Range of values	Bits	Range of values	Bits	Range of values	Bits	Range of values
15.8	±27,600	15.0	±16,400	13.7	±6,520	12.8	±3,570

Table 28: Effective resolution of the strain gauge value in bits for the measurement range 32 to 256 mV/V

1.3.13.8 Register for "Function model 2 - Extended filter"

1.3.13.8.1 A/D converter and IIR filter configuration

Name:
ConfigCommonOutput01

The IIR low-pass filter and measurement range of the A/D converter can be configured in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
			Filter level
0 - 3	IIR low-pass filter	0000	0: IIR low-pass filter switched off
		0001	1
		0010	2
		0011	3
		0100	4
		0101	5
		0110	6
		0111	7
		1000	8
		1001 - 1111	The analog input value indicates an invalid range.
4 - 6	Default measurement range	000	16 mV/V
		001	8 mV/V
		010	4 mV/V
		011	2 mV/V
	Extended measurement range	100	256 mV/V
		101	128 mV/V
		110	64 mV/V
		111	32 mV/V
7	Reserved	0	(must be 0)

1.3.13.8.2 Data rate configuration

Name:
ConfigFilterOutput01

Whether a selectable data rate or a high-resolution data rate is being used for the FIR filter is configured in this register.

Data type	Values	Information
UINT	0	Mode "Selectable data rate": A selectable data rate is used for the FIR filter (default). Configuration takes place in register "ConfigDatarateOutput01" on page 33.
	1	Mode "High-resolution data rate": A high-resolution data rate is used for the FIR filter. Configuration takes place in register "ConfigHighResolutionOutput01" on page 33.

Name:
ConfigDatarateOutput01

The data rate of the FIR filter in mode "Selectable data rate" is configured in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Data rate f_{DATA} (samples per second):	0000	2.5
		0001	5
		0010	10
		0011	15
		0100	25
		0101	30
		0110	50
		0111	60
		1000	100
		1001	500
		1010	1000
		1011	2000
		1100	3750
		1101	7500
		1110 - 1111	The analog input value indicates an invalid range.
4 - 7	Reserved	0	(must be 0)

Name:
ConfigHighResolutionOutput01

The data rate of the FIR filter in 0.1 Hz steps is configured in this register (0.1 to 6553.5 Hz).

Data type	Values	Information
UINT	0	Disables the FIR filter
	1 to 65,535	0.1 to 6553.5 Hz

1.3.13.8.3 Module status

Name:
StatusInput01

This register contains the current state of the module. If there is a fault in the module power supply or strain gauge supply, the analog input value indicates an invalid range and the buffer of the enabled filter is reset.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	A/D converter values	0	Valid A/D converter value
		1	Invalid A/D converter value
1	Line monitoring	0	OK
		1	Open circuit
2	Reserved	-	
3	Module power supply	0	OK
		1	Error in module power supply
4	Strain gauge supply	0	OK
		1	Error in strain gauge supply
5	FIR filter ready	0	OK
		1	FIR filter not yet ready
6 - 7	Reserved	-	

1.3.13.8.4 A/D converter conversion timestamp

Name:
AdcConvTimeStampInput01

This register holds the timestamp of the last analog conversion. This is always the point in time in [µs] at which the conversion of the latest A/D converter raw value is completed.

Data type	Values	Explanation
DINT	-2,147,483,648 to 2,147,483,647	Timestamp [µs] of the last analog conversion

1.3.13.9 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
250 µs

1.3.13.10 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

For the I/O update times for function models "0 - Standard", "2 - Extended filter" and "254 - Bus controller", see section "Characteristics of the FIR filter in mode "Selectable data rate"" on page 110.

Depending on the setting in register "ConfigCycletime01_MultiSample" on page 123, the I/O update time in "Function model 1 - Multisampling" is 50 or 100 µs.

1.4 X20AI2222

1.4.1 General information

The module is equipped with 2 inputs with 13-bit (including sign) digital converter resolution. It can be used to capture voltage signals in the range from ±10 V.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

- 2 analog inputs ±10 V
- 13-bit digital converter resolution

1.4.2 Order data

Order number	Short description	Figure
	Analog inputs	
X20AI2222	X20 analog input module, 2 inputs, ±10 V, 13-bit converter resolution, configurable input filter	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 29: X20AI2222 - Order data

1.4.3 Technical data

Order number	X20AI2222
Short description	
I/O module	2 analog inputs ±10 V
General information	
B&R ID code	0xCAB0
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	0.8 W [1]
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
EAC	Yes
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
DNV GL	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
LR	ENV1
KR	Yes
Analog inputs	
Input	±10 V
Input type	Differential input
Digital converter resolution	±12-bit
Conversion time	300 µs for all inputs
Output format	
Data type	INT
Voltage	0x8001 - 0x7FFF / 1 LSB = 0x0008 = 2.441 mV
Input impedance in signal range	20 MΩ
Input protection	Protection against wiring with supply voltage
Permissible input signal	Max. ±30 V
Output of digital value during overload	Configurable
Conversion procedure	SAR
Input filter	3rd-order low pass / cut-off frequency 1 kHz
Max. error at 25°C	
Gain	0.08% [2]
Offset	0.015% [3]
Max. gain drift	0.006 %/°C [2]
Max. offset drift	0.002 %/°C [3]
Common-mode rejection	
DC	70 dB
50 Hz	70 dB
Common-mode range	±12 V
Crosstalk between channels	-70 dB
Nonlinearity	<0.025% [3]
Isolation voltage between channel and bus	500 V_{eff}
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20

Table 30: X20AI2222 - Technical data

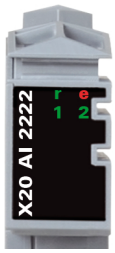
Order number	X20AI2222
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5 $^{+0.2}$ mm

Table 30: X20AI2222 - Technical data

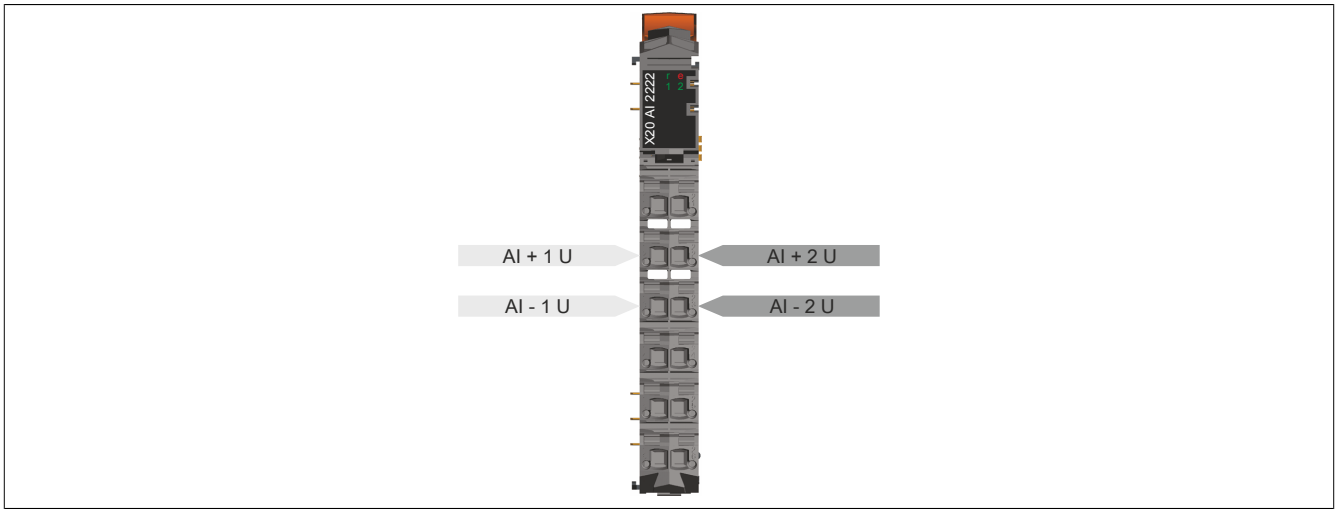
1) To reduce power dissipation, B&R recommends bridging unused inputs on the terminals.
2) Based on the current measured value.
3) Based on the 20 V measurement range.

1.4.4 LED status indicators

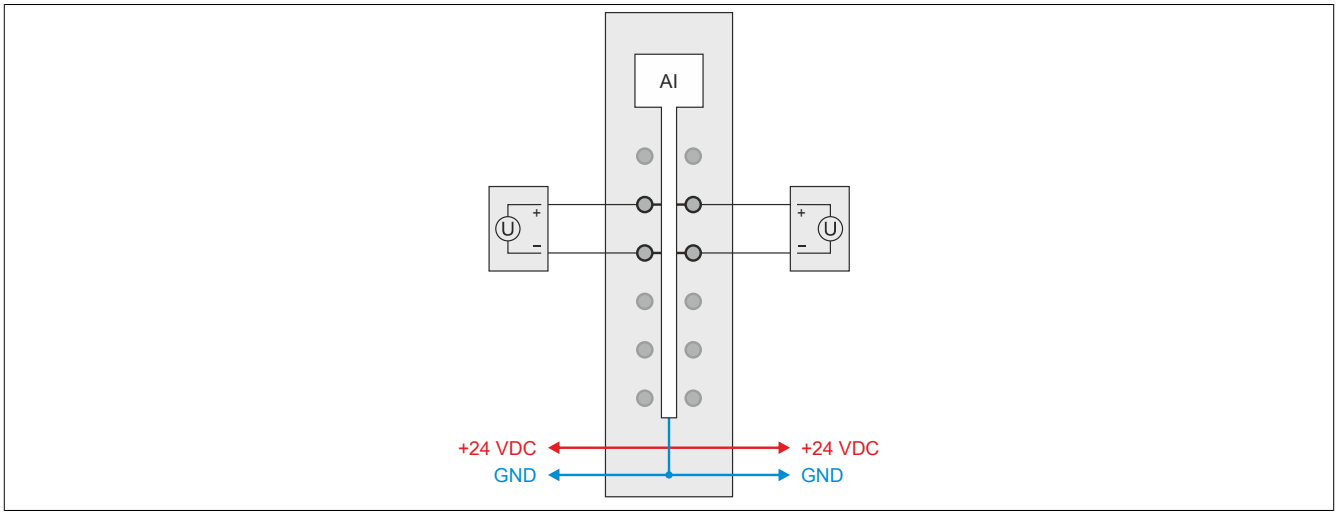
For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 system user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 2	Green	Off	Open line or sensor is disconnected
			Blinking	Input signal overflow or underflow
			On	Analog/digital converter running, value OK

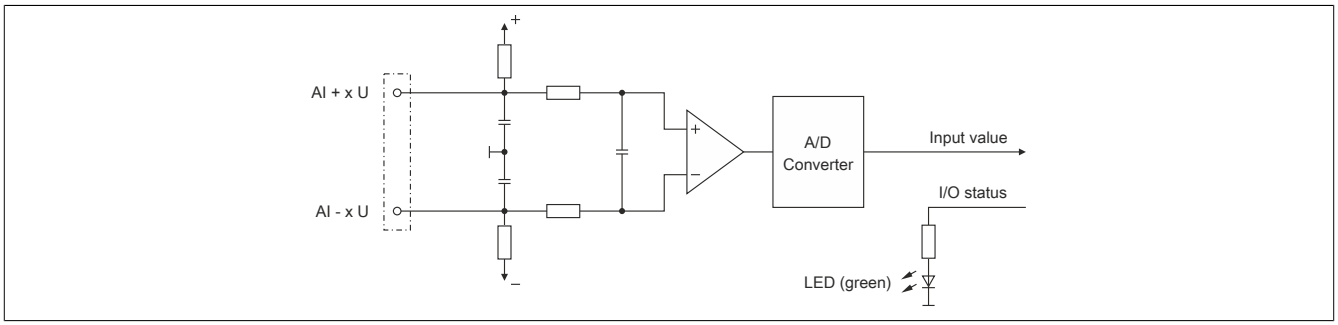
1.4.5 Pinout



1.4.6 Connection example



1.4.7 Input circuit diagram



1.4.8 Register description

1.4.8.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 system user's manual.

1.4.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration						
16	ConfigOutput01 (Input filter)	USINT				•
20	ConfigOutput03 (Lower limit value)	INT				•
22	ConfigOutput04 (Upper limit value)	INT				•
Analog signal - Communication						
0	AnalogInput01	INT	•			
2	AnalogInput02	INT	•			
30	StatusInput01	USINT	•			

1.4.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration							
16	-	ConfigOutput01 (Input filter)	USINT				•
20	-	ConfigOutput03 (Lower limit value)	INT				•
22	-	ConfigOutput04 (Upper limit value)	INT				•
Analog signal - Communication							
0	0	AnalogInput01	INT	•			
2	2	AnalogInput02	INT	•			
30	-	StatusInput01	USINT		•		

1) The offset specifies the position of the register within the CAN object.

1.4.8.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

1.4.8.3.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

1.4.8.4 Analog inputs

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

1.4.8.5 Input values of analog inputs

Name:
AnalogInput01 to AnalogInput02

This register contains the analog input value.

Data type	Values	Input signal:
INT	-32768 to 32767	Voltage signal -10 to 10 VDC

1.4.8.6 Input filter

This module is equipped with a configurable input filter. The minimum cycle time must be >500 µs. Filtering is disabled for shorter cycle times.

If the input filter is active, then the scan rate for the channels is measured in ms. The time offset between the channels is 200 µs. The conversion takes place asynchronously to the network cycle.

1.4.8.6.1 Input ramp limiting

Input ramp limiting can only be performed in conjunction with filtering. Input ramp limiting is performed before filtering.

The difference of the input value change is checked for exceeding the specified limit. In the event of overshoot, the tracked input value is equal to the old value ± the limit value.

Configurable limit values:

Value	Limit value
0	The input value is used without limitation.
1	0x3FFF = 16383
2	0x1FFF = 8191
3	0x0FFF = 4095
4	0x07FF = 2047
5	0x03FF = 1023
6	0x01FF = 511
7	0x00FF = 255

Input ramp limiting is well suited for suppressing disturbances (spikes). The following examples show the functionality of input ramp limiting based on an input step and a disturbance.

Example 1

The input value jumps from 8000 to 17000. The diagram shows the tracked input value with the following settings:

Input ramp limiting = 4 = 0x07FF = 2047

Filter level = 2

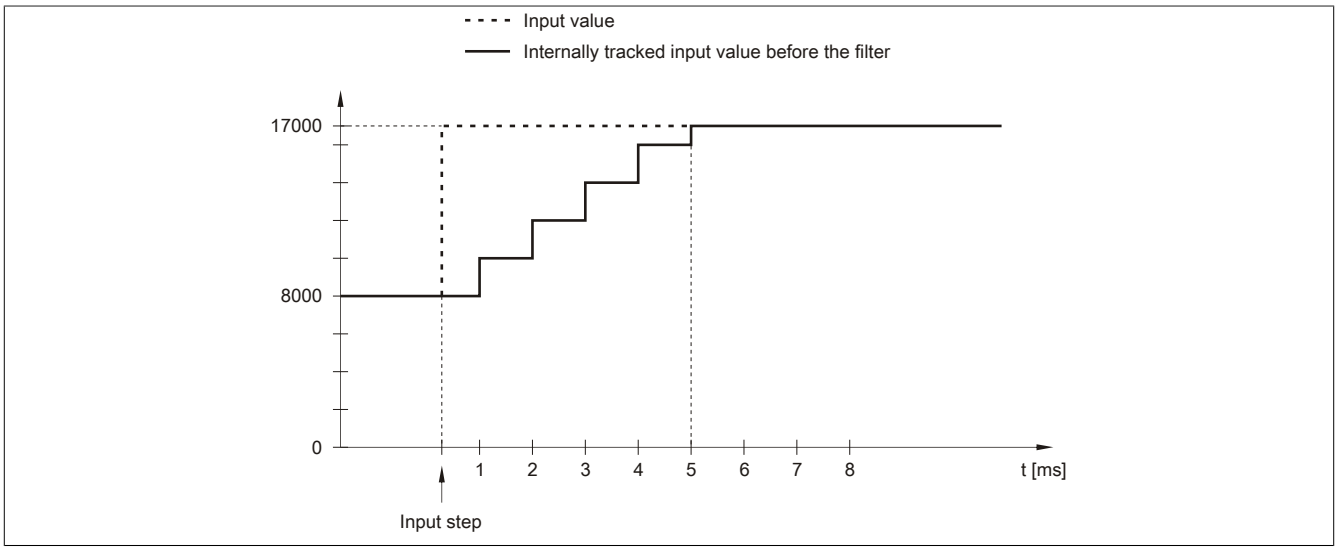


Figure 1: Tracked input value for input step

Example 2

A disturbance interferes with the input value. The diagram shows the tracked input value with the following settings:

Input ramp limiting = 4 = 0x07FF = 2047

Filter level = 2

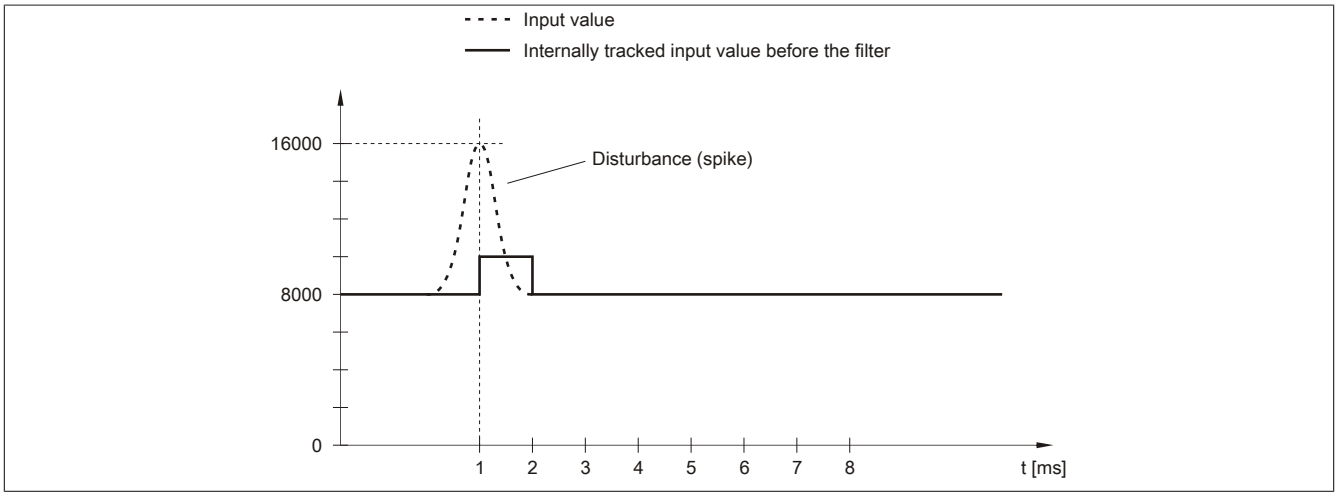


Figure 2: Tracked input value for disturbance

1.4.8.6.2 Filter level

A filter can be defined to prevent large input steps. This filter is used to bring the input value closer to the actual analog value over a period of several bus cycles.
Filtering takes place after any input ramp limiting has been carried out.

Formula for calculating the input value:

$$\text{Value}_{\text{New}} = \text{Value}_{\text{Old}} - \frac{\text{Value}_{\text{Old}}}{\text{Filter level}} + \frac{\text{Input value}}{\text{Filter level}}$$

Adjustable filter levels:

Value	Filter level
0	Filter switched off
1	Filter level 2
2	Filter level 4
3	Filter level 8
4	Filter level 16
5	Filter level 32
6	Filter level 64
7	Filter level 128

The following examples show the functionality of the filter based on an input step and a disturbance.

Example 1

The input value jumps from 8000 to 16000. The diagram shows the calculated value with the following settings:

Input ramp limiting = 0

Filter level = 2 or 4

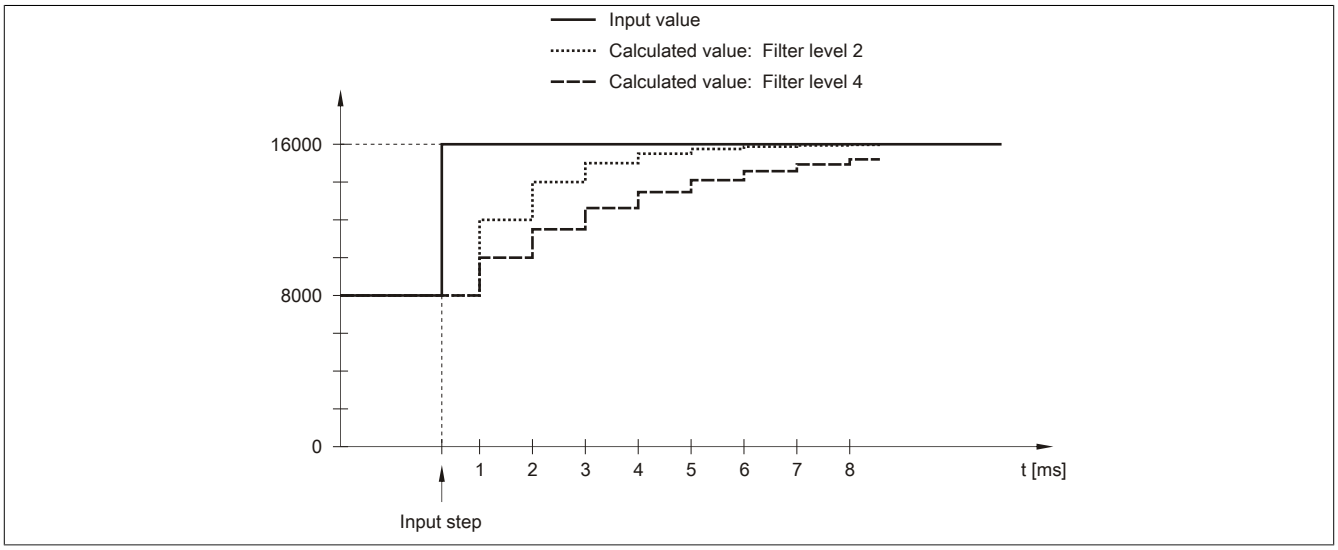


Figure 3: Calculated value during input step

Example 2

A disturbance interferes with the input value. The diagram shows the calculated value with the following settings:

Input ramp limiting = 0

Filter level = 2 or 4

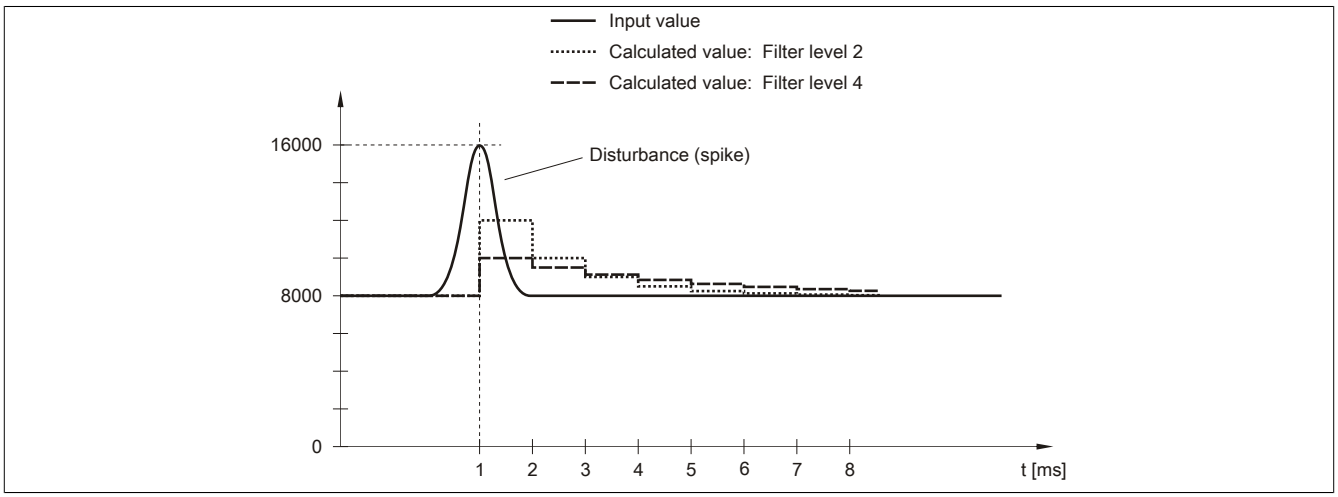


Figure 4: Calculated value during disturbance

1.4.8.7 Configuring the input filter

Name:
ConfigOutput01

The filter level and input ramp limiting of the input filter are set in this register.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter disabled (bus controller default setting)
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines input ramp limiting	000	The input value is applied without limitation (bus controller default setting)
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

1.4.8.8 Lower limit value

Name:
ConfigOutput03

The lower limit value for analog values can be set in this register. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Values	Information
INT	-32767 to 32767	Bus controller default setting: -32767

Information:

The default value of -32767 corresponds to the minimum default value of -10 VDC.

It is important to note that this setting applies to all channels!

1.4.8.9 Upper limit value

Name:
ConfigOutput04

The upper limit value for analog values can be set in this register. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Values	Information
INT	-32767 to 32767	Bus controller default setting: 32767

Information:

Default value 32767 corresponds to the maximum default value at +10 VDC.

It is important to note that this setting applies to all channels!

1.4.8.10 Input status

Name:
StatusInput01

This register is used to monitor the module inputs. A change in the monitoring status generates an error message.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
2 - 3	Channel 2	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
4 - 7	Reserved	0	

Limiting the analog value

In addition to the status information, the analog value is fixed to the values listed below by default in an error state. The analog value is limited to the new values if the limit values were changed.

Error state	Digital value on error (default values)
Open circuit	+32767 (0x7FFF)
Upper limit value overshot	+32767 (0x7FFF)
Lower limit value undershot	-32767 (0x8001)
Invalid value	-32768 (0x8000)

1.4.8.11 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
Inputs without filtering	100 µs
Inputs with filtering	500 µs

1.4.8.12 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

	Minimum I/O update time
Inputs without filtering	300 µs for all inputs
Inputs with filtering	1 ms

1.5 X20AI2237

1.5.1 General information

The module is equipped with 2 voltage measurement inputs with 16-bit digital converter resolution.

Each voltage input has its own sensor supply. The two channels with their respective sensor supplies are electrically isolated from each other.

- 2 analog voltage inputs
- Electrically isolated analog channels
- Electrically isolated sensor supplies
- 16-bit digital converter resolution
- Very high sampling rate
- NetTime timestamp: Moment of measurement

NetTime timestamp of the measurement

For many applications, not only the measured value is important, but also the exact time of the measurement. The module is equipped with a NetTime timestamp function for this that supplies a timestamp for the recorded position and trigger time with microsecond accuracy.

The timestamp function is based on synchronized timers. If a timestamp event occurs, the module immediately saves the current NetTime. After the respective data is transferred to the CPU, including this precise moment, the CPU can then evaluate the data using its own NetTime (or system time), if necessary.

1.5.2 Order data

Order number	Short description	Figure
	Analog inputs	
X20AI2237	X20 analog input module, 2 inputs, ±10 V, 16-bit converter resolution, single-channel isolation with separate sensor power supply, NetTime function	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 31: X20AI2237 - Order data

1.5.3 Technical data

Order number	X20AI2237
Short description	
I/O module	2 analog inputs ±10 V
General information	
B&R ID code	0xC9C4
Status indicators	I/O function per channel, operating state, module status, sensor power supply per channel
Diagnostics	
Module run/error	Yes, using LED status indicator and software
Inputs	Yes, using LED status indicator and software
Sensor power supply	Yes, using LED status indicator and software
Power consumption	
Bus	0.05 W
Internal I/O	1.05 W (Rev. ≥ D0), 1.15 W (Rev. < D0) [1]
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
EAC	Yes
Analog inputs	
Input	±10 V
Input type	Differential input
Digital converter resolution	±15-bit
Data output rate	10000 samples per second
Output format	
Data type	INT
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0001 = 305.176 µV
Input impedance in signal range	20 MΩ
Input protection	Up to 30 VDC, reverse polarity protection
Open-circuit detection	Yes, using software
Permissible input signal	Max. ±30 V
Output of digital value during overload	Configurable
Conversion procedure	SAR
Input filter	Fourth-order low-pass filter / Cutoff frequency 10 kHz
Max. error	
Gain	0.013% [2]
Offset	0.0035% [3]
Max. gain drift	<0.0008%/°C [2]
Max. offset drift	<0.0025%/°C [3]
Common-mode rejection	
DC	84 dB
Up to 60 Hz	84 dB
Up to 10 kHz	82 dB
Common-mode range	±14 V
Nonlinearity	<0.003% [3]
Test voltage	
Channel - Channel	1000 VAC
Channel - Bus	1000 VAC
Channel - Ground	1000 VAC
Bus - Ground	800 VAC
Sensor power supply	
Power consumption	0.75 W per channel
Nominal voltage	25 V ±2%
Nominal output current	Max. 30 mA
Short-circuit proof	Yes, continuous
Max. voltage ripple	
Up to 100 kHz	≤2.2 mV
Up to 1 MHz	≤22 mV
Higher	≤100 mV
Short-circuit current	
Typical	<50 mA
Maximum	60 mA
Behavior on short circuit	Current limiting

Table 32: X20AI2237 - Technical data

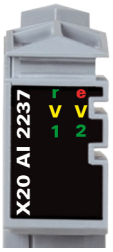
Order number	X20AI2237
Electrical properties	
Electrical isolation	Channel isolated from channel and bus Sensor power supply isolated from sensor power supply Sensor power supply not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x terminal block X20TB12 separately. Order 1x bus module X20BM11 separately.
Pitch	$12.5^{+0.2}$ mm

Table 32: X20AI2237 - Technical data

1) To reduce power dissipation, B&R recommends bridging unused inputs.
2) Based on the current measured value.
3) Based on the 20 V measurement range.

1.5.4 LED status indicators

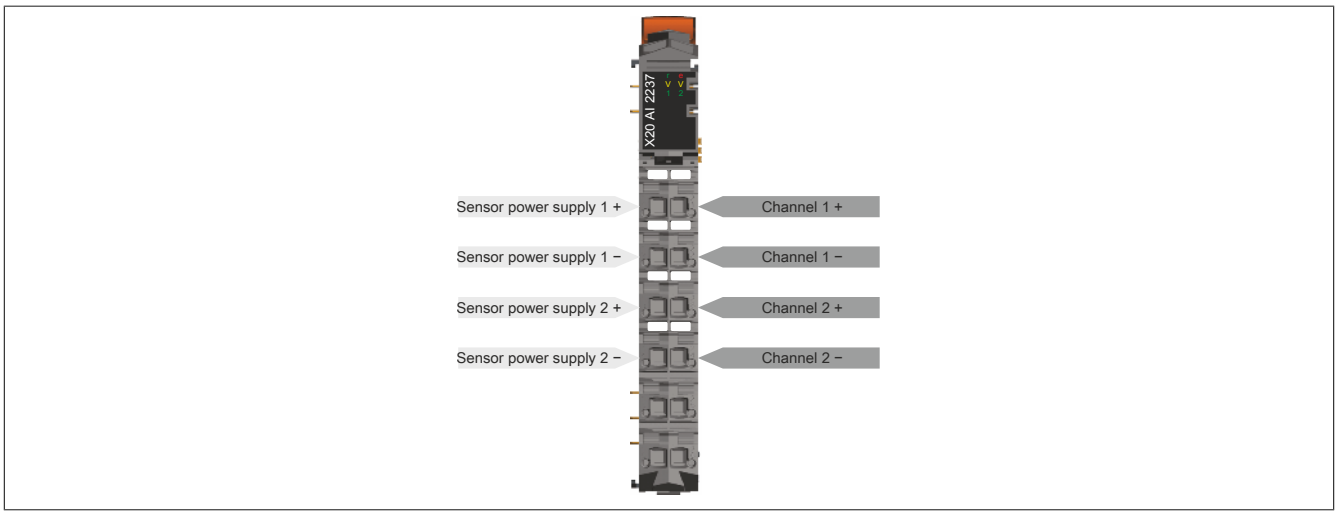
For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 system user's manual.

Figure	LED	Color	Status	Description
	**Operating state**			
	r	Green	Off	No power to module
			Single flash	UNLINK mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking quickly	SYNC mode
			Blinking slowly	PREOPERATIONAL mode
			On	RUN mode
	Module status			
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	Sensor supply			
	V	Yellow	Off	Module supply not connected or overload
			On	Sensor supply in its normal operating range
	Analog input			
	1 - 2	Green	Off	Indicates one of the following cases: • No power to module • Channel disabled • Open line
			Single flash	Input signal overflow or underflow
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.

1.5.5 Pinout

Shielded twisted pair cables should be used to minimize coupling disturbances. Use either one cable for each channel or a multiple twisted pair cable for both channels.

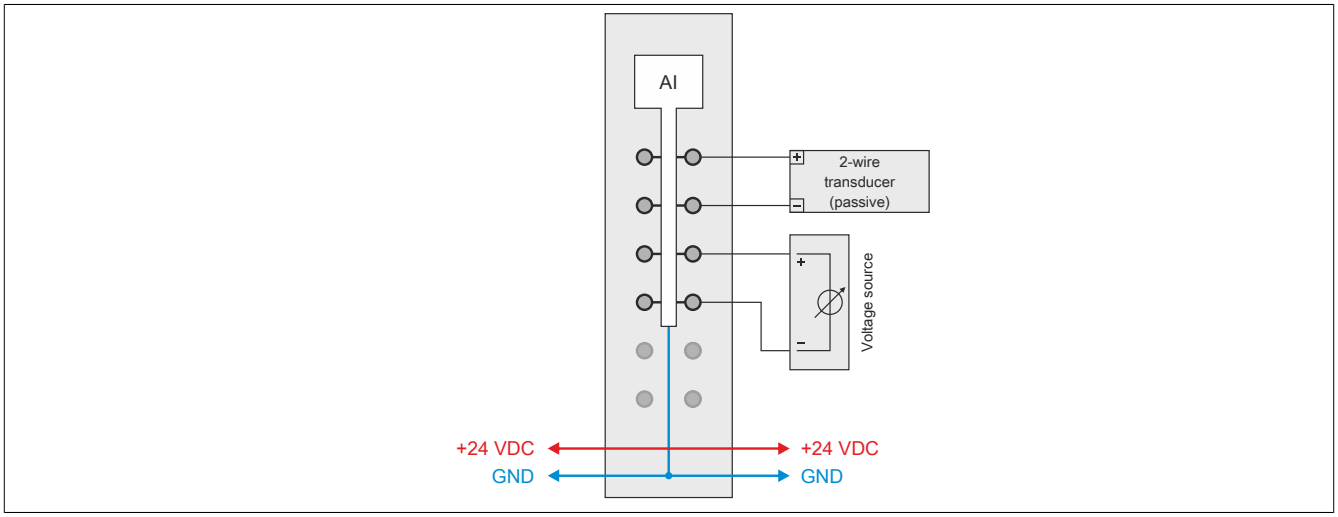


1.5.6 Connection examples

2-wire connections

A 2-wire connection can be implemented as follows:

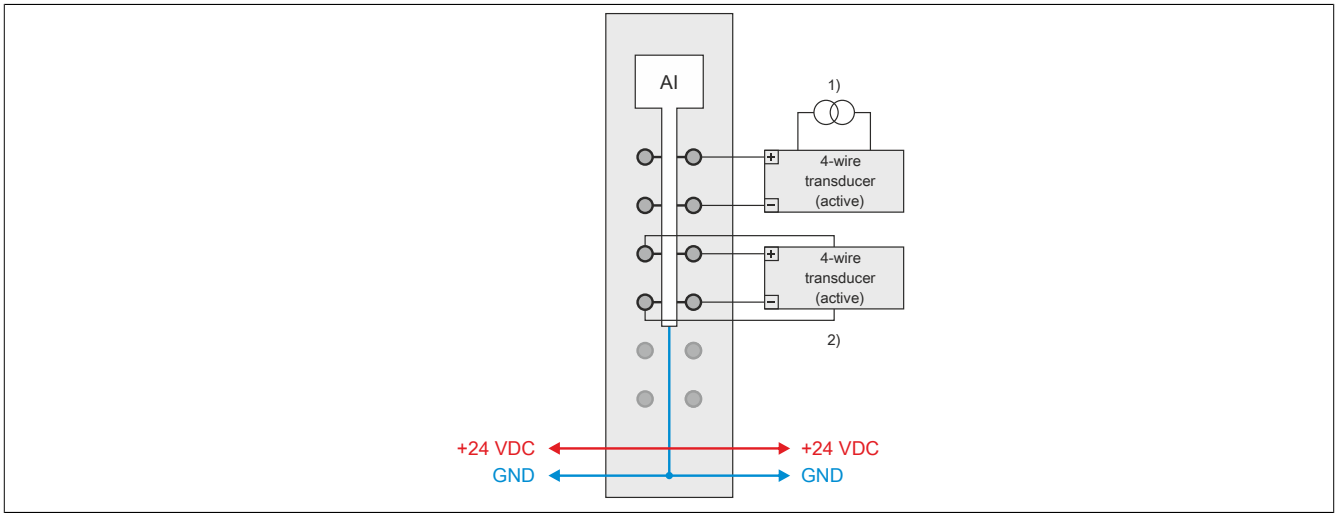
- 2-wire transducer
- Active voltage source



4-wire connections

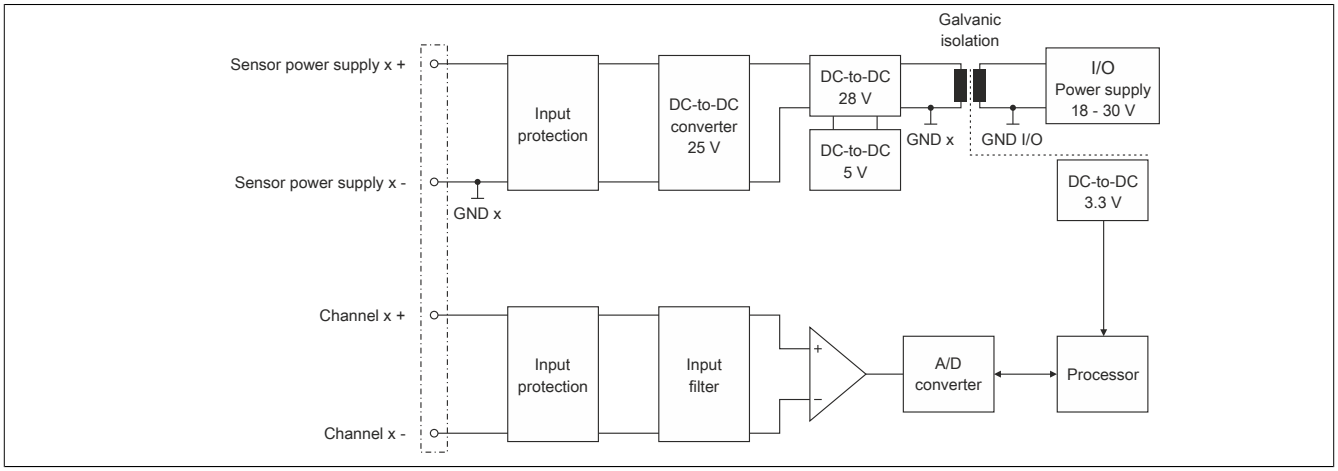
A 4-wire connection can be implemented as follows:

- 4-wire transducer with external supply
- 4-wire transducer supplied by the module



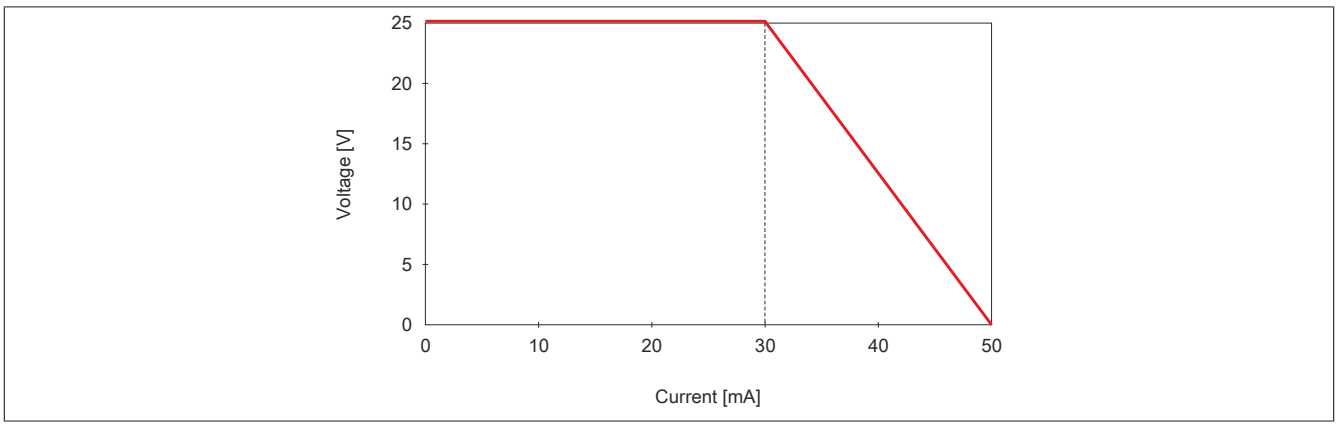
1) With external power supply.
2) With internal power supply. The internal power supply is only permitted to be loaded with max. 30 mA.

1.5.7 Input circuit diagram



1.5.8 Behavior in the event of short circuit

In the event of a short circuit, the output current for the sensor supply is limited according to the following diagram.



1.5.9 Register description

1.5.9.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 system user's manual.

1.5.9.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Analog input - Configuration						
390 434	AnalogFilter01 AnalogFilter02	UINT				•
386 430	AnalogMode01 AnalogMode02	UINT				•
402 446	UpperLimit01 UpperLimit02	INT				•
398 442	LowerLimit01 LowerLimit02	INT				•
406 450	Hysteres01 Hysteres02	INT				•
414 458	ReplacementUpper01 ReplacementUpper02	INT				•
410 454	ReplacementLower01 ReplacementLower02	INT				•
426 470	PreparationInterval01 PreparationInterval02	UINT				•
418 462	ErrorDelay01 ErrorDelay02	UINT				•
422 466	SumErrorDelay01 SumErrorDelay02	UINT				•
Analog input - Communication						
0 2	AnalogInput01 (limited) AnalogInput02 (limited)	INT	•			
258 262	AnalogInput01 (original value) AnalogInput02 (original value)	INT	•			
284 292	AnalogSampletime01 (32-bit) AnalogSampletime02 (32-bit)	DINT	•			
282 290	AnalogSampletime01 (16-bit) AnalogSampletime02 (16-bit)	INT	•			
273 275	AnalogStatus01 AnalogStatus02	USINT	•			
	UnderflowAnalogInput01 or 02	Bit 0				
	OverflowAnalogInput01 or 02	Bit 1				
	OpenLineAnalogInput01 or 02	Bit 2				
	SumErrorAnalogInput01 or 02	Bit 4				
	SensorErrorAnalogInput01 or 02	Bit 6				
	IoSuppErrorAnalogInput01 or 02	Bit 7				

1.5.9.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Analog input - Configuration							
390 434	- -	AnalogFilter01 AnalogFilter02	UINT				•
386 430	- -	AnalogMode01 AnalogMode02	UINT				•
402 446	- -	UpperLimit01 UpperLimit02	INT				•
398 442	- -	LowerLimit01 LowerLimit02	INT				•
406 450	- -	Hysteres01 Hysteres02	INT				•
414 458	- -	ReplacementUpper01 ReplacementUpper02	INT				•
410 454	- -	ReplacementLower01 ReplacementLower02	INT				•
426 470	- -	PreparationInterval01 PreparationInterval02	UINT				•
418 462	- -	ErrorDelay01 ErrorDelay02	UINT				•
422 466	- -	SumErrorDelay01 SumErrorDelay02	UINT				•
Analog input - Communication							
0 2	0 2	AnalogInput01 AnalogInput02	INT	•			
273 275	- -	AnalogStatus01 AnalogStatus02	USINT		•		
		UnderflowAnalogInput01 or 02	Bit 0				
		OverflowAnalogInput01 or 02	Bit 1				
		OpenLineAnalogInput01 or 02	Bit 2				
		SumErrorAnalogInput01 or 02	Bit 4				
		SensorErrorAnalogInput01 or 02	Bit 6				
		IoSuppErrorAnalogInput01 or 02	Bit 7				

1) The offset specifies the position of the register within the CAN object.

1.5.9.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

1.5.9.3.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

1.5.9.4 General information

The module provides 2 electrically isolated channels. Each channel can read an electrical voltage signal in the ±10 V range and supply the signal encoder with 24 VDC.

1.5.9.5 Analog input - Configuration

Each channel is configured and enabled separately. First, the user must set the scaling of the input value and select a replacement value strategy. Depending on the requirements of the application, the user can also set user-defined limit values and define an input filter.

Scaling

The module's A/D converter works with a resolution of 16 bits (±15 bits). This allows the input value of ±10 V to be mapped using ±32767 steps. To simplify implementation, the user can configure scaling to ±10000 steps. The conversion value corresponds to the voltage in mV, and with a resolution of more than 14 bits (±13 bits) is still precise enough for the many different application that use this technology.

Replacement value strategy

The detected voltage is evaluated in order to ensure the quality of the read value. For example, if a logically impermissible voltage value or an open line is detected, the limit monitor triggers an appropriate response.

The response is determined by the replacement value strategy selected by the user. With the option "Replace with static value", the user defines two values that replace the converted value when the upper and lower limits are exceeded. The alternative "Retain last valid value" keeps the last validated value. However, the evaluation for this option takes more time. Depending on the "preparation interval", the value currently being read may be delayed.

Limit Value Monitoring

In addition to the qualitative evaluation of the input, the module also provides the option of adapting the range of permitted values to the requirements of the application. The registers "UpperLimit" on page 151 and "LowerLimit" on page 151 can be used to place additional restrictions on the permitted upper and lower limit. When this feature is used, the selected replacement value strategy is implemented according to the new limits.

1.5.9.5.1 Input filter

Analog input signals can experience brief disturbances caused by external factors (EMC). The A/D converters high sampling rate allows you to filter out these types of signal peaks without hindering the application processes.

2 configuration points are available for interpolating the input signal:

- "Input ramp limiting" on page 147
- "Filter level" on page 148

1.5.9.5.1.1 Input ramp limiting

Input ramp limiting can only be performed in conjunction with filtering. Input ramp limiting is performed before filtering.

The difference of the input value change is checked for exceeding the specified limit. In the event of overshoot, the tracked input value is equal to the old value ± the limit value.

Configurable limit values:

Value	Limit value
0	The input value is used without limitation.
1	0x3FFF = 16383
2	0x1FFF = 8191
3	0x0FFF = 4095
4	0x07FF = 2047
5	0x03FF = 1023
6	0x01FF = 511
7	0x00FF = 255

Input ramp limiting is well suited for suppressing disturbances (spikes). The following examples show the functionality of input ramp limiting based on an input step and a disturbance.

Example 1

The input value jumps from 8000 to 17000. The diagram shows the tracked input value with the following settings:

Input ramp limiting = 4 = 0x07FF = 2047

Filter level = 2

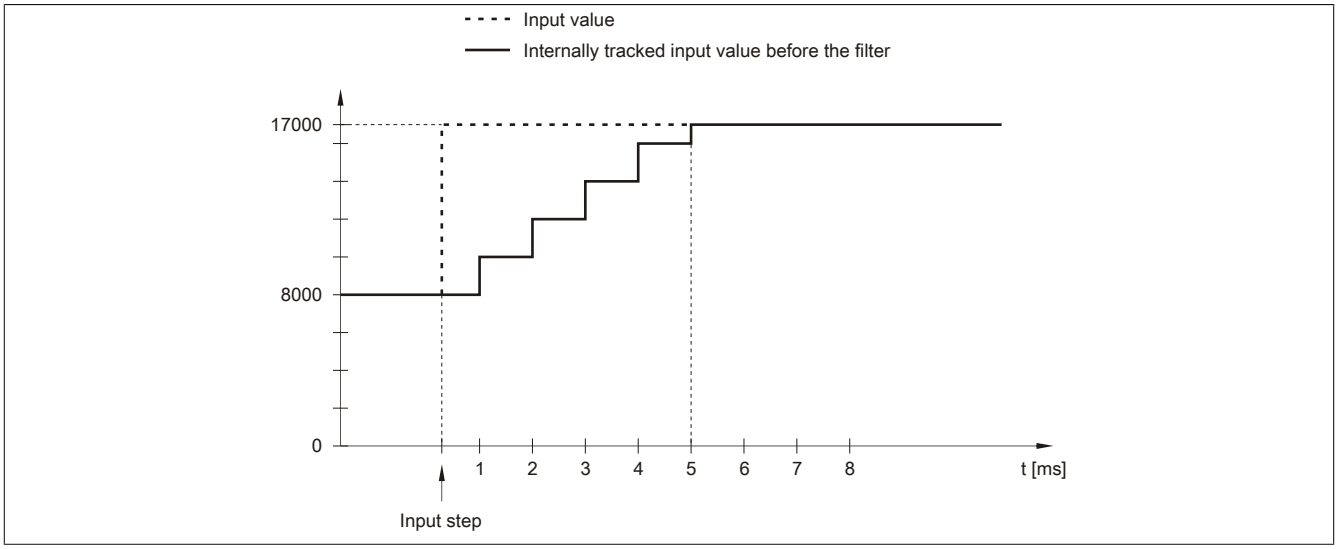


Figure 5: Tracked input value for input step

Example 2

A disturbance interferes with the input value. The diagram shows the tracked input value with the following settings:

Input ramp limiting = 4 = 0x07FF = 2047

Filter level = 2

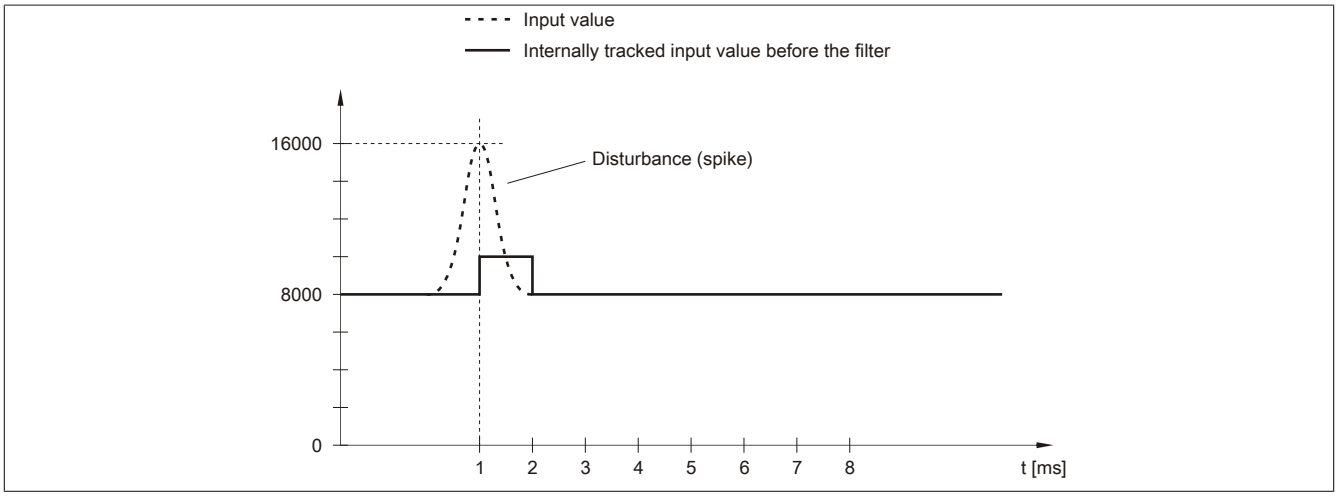


Figure 6: Tracked input value for disturbance

1.5.9.5.1.2 Filter level

A filter can be defined to prevent large input steps. This filter is used to bring the input value closer to the actual analog value over a period of several bus cycles.
Filtering takes place after any input ramp limiting has been carried out.

Formula for calculating the input value:

$$\text{Value}_{\text{New}} = \text{Value}_{\text{Old}} - \frac{\text{Value}_{\text{Old}}}{\text{Filter level}} + \frac{\text{Input value}}{\text{Filter level}}$$

Adjustable filter levels:

Value	Filter level
0	Filter switched off
1	Filter level 2
2	Filter level 4
3	Filter level 8
4	Filter level 16
5	Filter level 32
6	Filter level 64
7	Filter level 128

The following examples show the functionality of the filter based on an input step and a disturbance.

Example 1

The input value jumps from 8000 to 16000. The diagram shows the calculated value with the following settings:

Input ramp limiting = 0

Filter level = 2 or 4

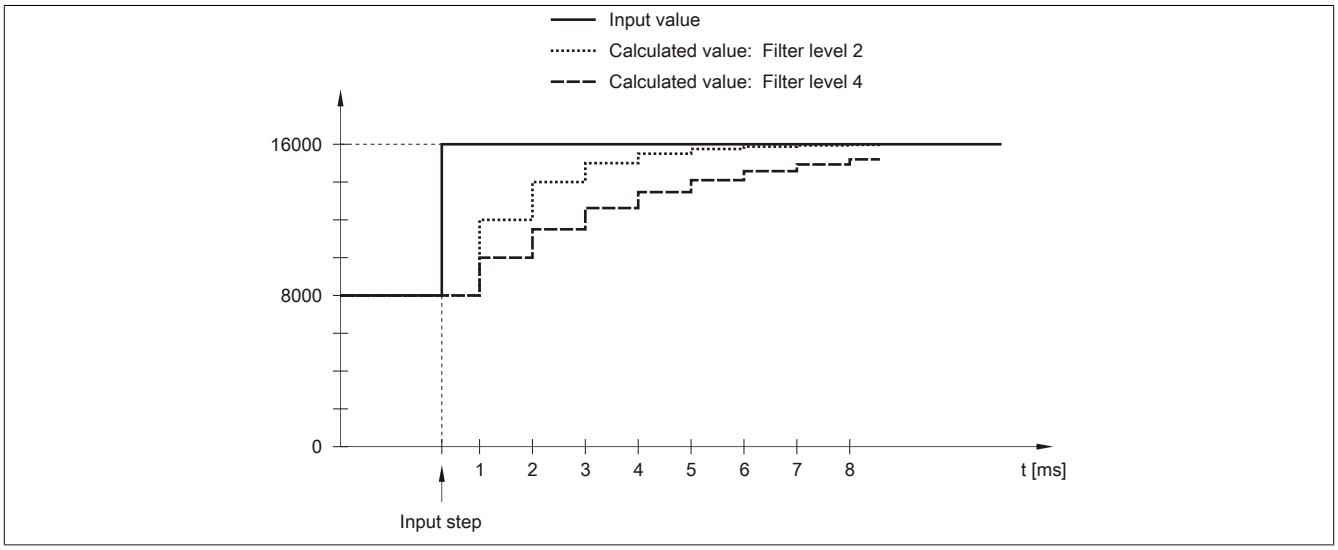


Figure 7: Calculated value during input step

Example 2

A disturbance interferes with the input value. The diagram shows the calculated value with the following settings:

Input ramp limiting = 0

Filter level = 2 or 4

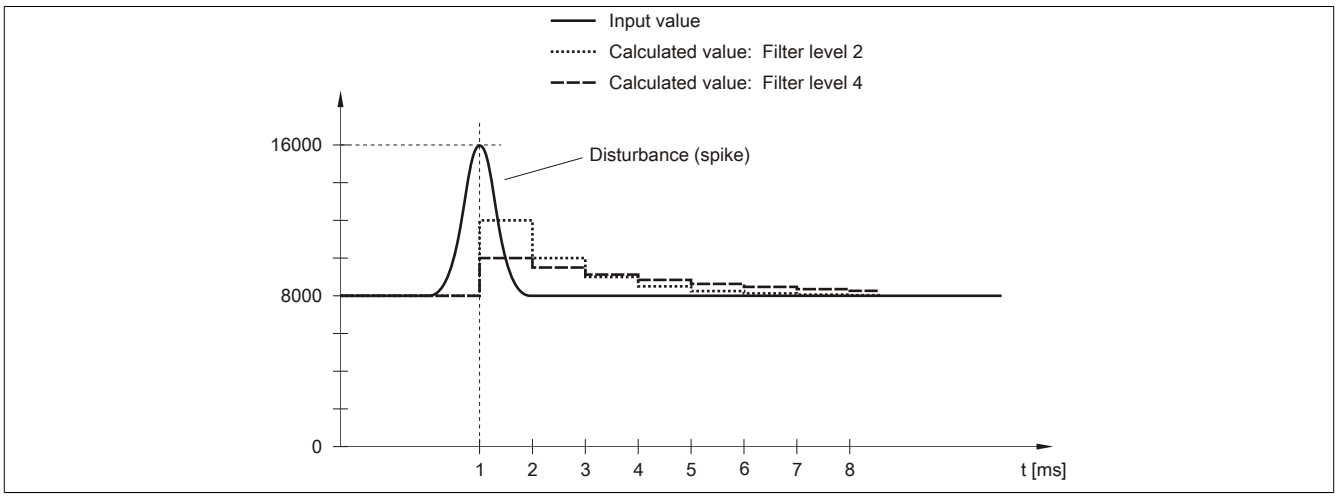


Figure 8: Calculated value during disturbance

1.5.9.5.1.3 Configuring filters

Name:
AnalogFilter01 to AnalogFilter02

This register is used to define the filter level and input ramp limitation of the input filter.

Data type	Value	Bus controller default setting
UINT	See bit structure.	0

Bit structure:

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter disabled (bus controller default setting)
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines input ramp limiting	000	The input value is applied without limitation (bus controller default setting)
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

1.5.9.5.2 Channel parameters

Name:
AnalogMode01 to AnalogMode02

These registers are used to predefine the operating parameters that the module will be using for the respective channel. Each channel must be enabled individually and can be configured and operated independently.

Information:

Different limit values must be configured for any display normalizing that needs to take place.

Data type	Value	Bus controller default setting
UINT	See bit structure.	15

Bit structure:

Bit	Name	Value	Information
0	Channel (on/off)	0	Disabled
		1	Enabled (bus controller default setting)
1	Limit exceeded	0	Disabled
		1	Enabled (bus controller default setting)
2	Lower limit violation	0	Disabled
		1	Enabled (bus controller default setting)
3	Reserved	0	
4	Replacement value strategy	0	Replace with static value
		1	Retain last valid value
5	Measured value scaling	0	±32767 (resolution: 16-bit)
		1	±10000 (resolution: >14-bit)
6 - 15	Reserved	0	

1.5.9.5.3 Upper limit value

Name:
UpperLimit01 to UpperLimit02

If the value range needs to be restricted further, this register can be used to enter new user-specific upper limit values.

Data type	Value	Information
INT	-32767 to 32767.	Bus controller default setting: 32767
	-10000 to 10000	

Information:

The defined limit values must take the configured scaling into consideration.

1.5.9.5.4 Lower limit value

Name:
LowerLimit01 to LowerLimit02

If the value range needs to be restricted further, this register can be used to enter new user-specific lower limit values.

Data type	Value	Information
INT	-32767 to 32767.	Bus controller default setting: -32767
	-10000 to 10000	

Information:

The defined limit values must take the configured scaling into consideration.

1.5.9.5.5 Hysteresis

Name:
Hysteres01 to Hysteres02

If the user-specific limit values are being used, then a hysteresis range should also be defined. These registers configure how far a limit value can be exceeded before a response is triggered.
The error status is cleared when the scaled input value once again passes the limit by at least the hysteresis value in the permitted direction.

Data type	Value	Information
INT	-32767 to 32767.	Bus controller default setting: 100
	-10000 to 10000	

Information:

The hysteresis value must take the scaling into consideration.

1.5.9.5.6 Upper replacement value

Name:
ReplacementUpper01 to ReplacementUpper02

This register is used to define the static values to be displayed instead of the current measured value when the limit is violated.

Data type	Value	Information
INT	-32767 to 32767.	Bus controller default setting: 32767

1.5.9.5.7 Lower replacement value

Name:
ReplacementLower01 to ReplacementLower02

This register is used to define the lower static values to be displayed instead of the current measured value when the limit is violated.

Data type	Value	Information
INT	-32767 to 32767	Bus controller default setting: -32767

1.5.9.5.8 Preparation time for the measured values

Name:
PreparationInterval01 to PreparationInterval02

If the last valid measured value should be kept when violating the limit value, then PreparationInterval must be defined. The measured values continue to be acquired and converted according to the configured I/O update time. They are then checked and discarded if they do not meet the specifications. When an error does not occur, therefore, the measured value acquired 2 preparation intervals ago is constantly output.

Data type	Value	Information
UINT	0 to 65535	In 0.1 ms. Bus controller default setting: 0

Functionality:
Measured values are continuously converted and stored to measured value memory depending on the configured input filter. The current contents of the measured value memory are checked within the configured interval. If a permissible value is present, then the contents of the buffer memory are passed to output memory and the contents of the measured value memory are passed to the buffer.
If the check turns up an impermissible value, then the contents of the measured value memory are discarded. The copy direction between output and buffer memory reverses and the last valid value continues to be output.

Information:

If configured to keep the last valid value, the delay time from measuring to outputting the value will be at least twice the preparation interval. In the worst case scenario, this can also take twice the interval time plus the configured conversion rate of the A/D converter.

"Application" Value being measured (analog)	
↓	Condition: - Conversion interval (A/D converter) elapsed
"Measured value memory" Measured value (digital)	
↓	Condition: - PreparationInterval elapsed - Measured value permissible
"Buffer" Last valid value	
↓	Condition: - PreparationInterval elapsed - Measured value permissible
"Output memory" Next-to-last valid/ displayed value	

1.5.9.5.9 Delaying error messages

Name:
ErrorDelay01 to ErrorDelay02

This register specifies the number of consecutive conversion procedures where an error is pending until the corresponding individual error status bit is set. The delay applies to underflow, overflow and open circuit errors. This delay can be used to hide temporary measured value deviations, for example.

Data type	Value	Information
UINT	0 to 65535	Bus controller default setting: 2

1.5.9.5.10 Time for composite error bit

Name:
SumErrorDelay01 to SumErrorDelay02

This register can be used to set the time that an error must remain pending before the composite error bit is set.

Data type	Value	Information
UINT	0 to 65535	Bus controller default setting: 4000

1.5.9.6 Analog input - Communication

The measured voltage data can be obtained via 2 different registers: The unevaluated measured value contains the scaled converter value. The evaluated measured value also takes the limit values and the configured replacement value strategy into consideration.

1.5.9.6.1 Analog input values - Original values

Name:
AnalogInput01 to AnalogInput02

These registers are used to indicate the actual input values after standardization.

Data type	Value
INT	-32767 to 32767
	-10000 to 10000

1.5.9.6.2 Analog input values - Limited

Name:
AnalogInput01 to AnalogInput02

These registers are used to indicate the actual input values after standardization. In addition, the settings for limit value monitoring and replacement value strategy are applied to this register.

Data type	Value
INT	-32767 to 32767
	-10000 to 10000

1.5.9.6.3 Sample time

Name:
Sampletime01 to Sampletime02

These registers return the timestamp for when the module reads the current channel mapping. The values are provided as signed 2-byte or 4-byte values.

For additional information about NetTime and timestamps, see "NetTime Technology" on page 155.

Data type	Values [µs]	Information
INT	-32,768 to 32767	NetTime timestamp of the current input value
DINT	-2,147,483,648 to 2,147,483,647	NetTime timestamp of the current input value

1.5.9.6.4 Status of the inputs

Name:
AnalogStatus01 to AnalogStatus02
UnderflowAnalogInput01 to UnderflowAnalogInput02
OverflowAnalogInput01 to OverflowAnalogInput02
OpenLineAnalogInput01 to OpenLineAnalogInput02
SumErrorAnalogInput01 to SumErrorAnalogInput02
SensorErrorAnalogInput01 to SensorErrorAnalogInput02
IoSuppErrorAnalogInput01 to IoSuppErrorAnalogInput02

The current error status of the module channels is displayed in this register, regardless of the configured replacement value strategy. Some error information may be delayed according to the previously configured condition.

Setting "Format of status information" in Automation Studio allows you to specify whether the status information is transferred as USINT or bitwise.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	UnderflowAnalogInput01 or 02	0	No error
		1	Below lower limit value
1	OverflowAnalogInput01 or 02	0	No error
		1	Above upper limit value
2	OpenLineAnalogInput01 or 02	0	No error
		1	Open line detected
3	Reserved	0	
4	SumErrorAnalogInput01 or 02	0	No error
		1	Composite error detected
5	Reserved	0	
6	SensorErrorAnalogInput01 or 02	0	Sensor voltage OK
		1	Sensor load too high
7	IoSuppErrorAnalogInput01 or 02	0	I/O power supply OK
		1	I/O power supply error detected

UnderflowAnalogInput

The signal underflow error status is indicated here according to the configuration. This error information is enabled as a multiple of the conversion cycle only after the configurable delay time has passed (see "ErrorDelay" on page 152 register).

OverflowAnalogInput

The signal overflow error status is indicated here according to the configuration. This error information is enabled as a multiple of the conversion cycle only after the configurable delay time has passed (see "ErrorDelay" on page 152 register).

SumErrorAnalogInput

This error information derives from the status of individual errors and is only activated after the configurable delay time has passed [ms] (see "SumErrorDelay" on page 152 register). Linking this error information to an application makes it possible to hide temporary temperature value overflows and underflows, for example.

SensorErrorAnalogInput

In addition to the analog input, the module also provides the option of supplying the connected encoder with 24 VDC. If the input impedance for the sensor is too high, however, the integrated voltage supply will fail.

IoSuppErrorAnalogInput

This error is activated immediately as soon as the module detects that the necessary supply voltage is no longer being provided (<20 VDC).

1.5.9.7 NetTime Technology

NetTime refers to the ability to precisely synchronize and transfer system times between individual components of the controller or network (CPU, I/O modules, X2X Link, POWERLINK, etc.).

This allows the moment that events occur to be determined system-wide with microsecond precision. Upcoming events can also be executed precisely at a specified moment.

1.5.9.7.1 Time information

Various time information is available in the controller or on the network:

- System time (on the PLC, Automation PC, etc.)
- X2X Link time (for each X2X Link network)
- POWERLINK time (for each POWERLINK network)
- Time data points of I/O modules

The NetTime is based on 32-bit counters, which are increased with microsecond resolution. The sign of the time information changes after 35 min, 47 s, 483 ms and 648 µs; an overflow occurs after 71 min, 34 s, 967 ms and 296 µs.

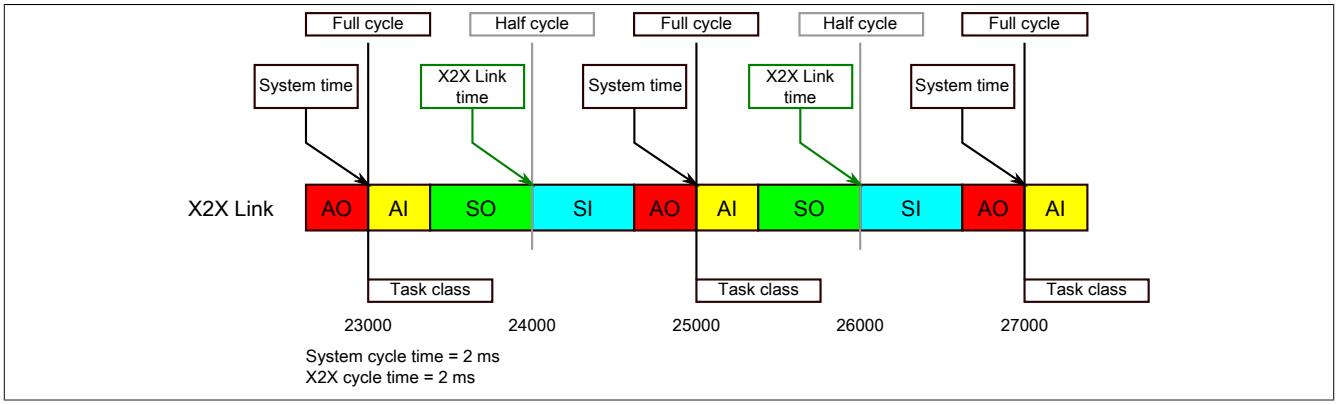
The initialization of the times is based on the system time during the startup of the X2X Link, the I/O modules or the POWERLINK interface.

Current time information in the application can also be determined via library AsIOTime.

1.5.9.7.1.1 PLC/Controller data points

The NetTime I/O data points of the PLC or the controller are latched to each system clock and made available.

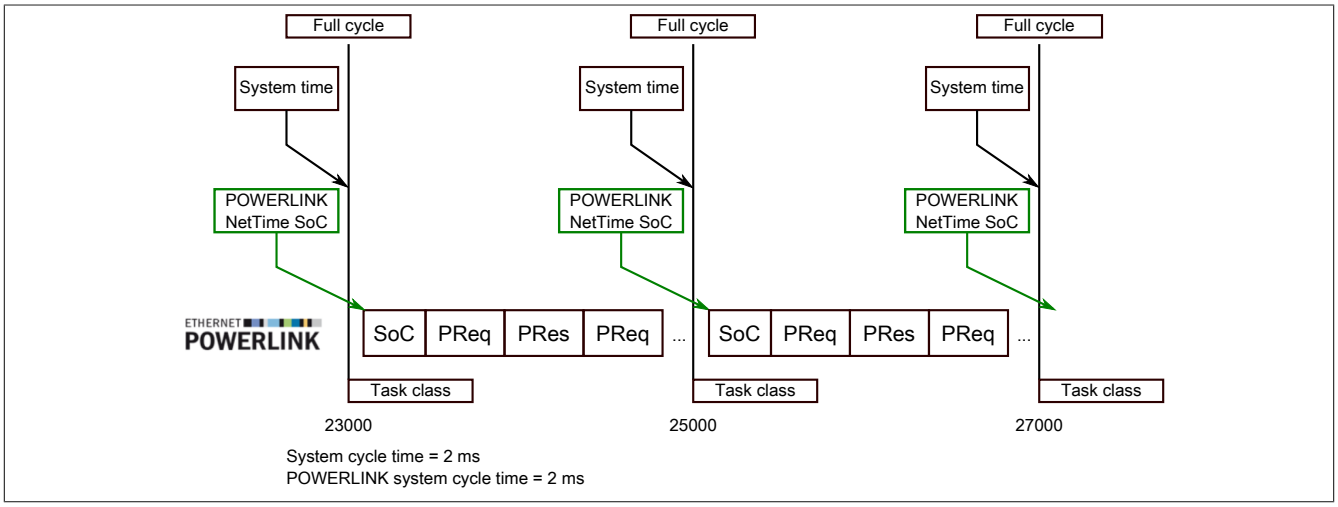
1.5.9.7.1.2 X2X Link reference moment



The reference moment on the X2X Link network is always calculated at the half cycle of the X2X Link cycle. This results in a difference between the system time and the X2X Link reference moment when the reference time is read out.

In the example above, this results in a difference of 1 ms, i.e. if the system time and X2X Link reference moment are compared at time 25000 in the task, then the system time returns the value 25000 and the X2X Link reference moment returns the value 24000.

1.5.9.7.1.3 POWERLINK - Reference time point

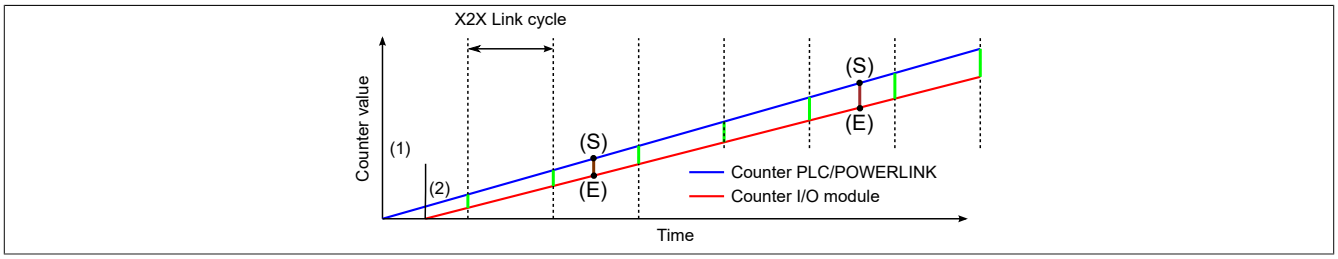


The reference time point on the POWERLINK network is always calculated at the start of cycle (SoC) of the POWERLINK network. The SoC starts 20 µs after the system clock due to the system. This results in the following difference between the system time and the POWERLINK reference time:

POWERLINK reference time = System time - POWERLINK cycle time + 20 µs.

In the example above, this means a difference of 1980 µs, i.e. if the system time and POWERLINK reference time are compared at time 25000 in the task, then the system time returns the value 25000 and the POWERLINK reference time returns the value 23020.

1.5.9.7.1.4 Synchronization of system time/POWERLINK time and I/O module



At startup, the internal counters for the PLC/POWERLINK (1) and the I/O module (2) start at different times and increase the values with microsecond resolution.

At the beginning of each X2X Link cycle, the PLC or the POWERLINK network sends time information to the I/O module. The I/O module compares this time information with the module's internal time and forms a difference (green line) between the two times and stores it.

When a NetTime event (E) occurs, the internal module time is read out and corrected with the stored difference value (brown line). This means that the exact system moment (S) of an event can always be determined, even if the counters are not absolutely synchronous.

Note

The deviation from the clock signal is strongly exaggerated in the picture as a red line.

1.5.9.7.2 Timestamp functions

NetTime-capable modules provide various timestamp functions depending on the scope of functions. If a timestamp event occurs, the module immediately saves the current NetTime. After the respective data is transferred to the CPU, including this precise moment, the CPU can then evaluate the data using its own NetTime (or system time), if necessary.

1.5.9.7.2.1 Time-based inputs

NetTime Technology can be used to determine the exact moment of a rising edge at an input. The rising and falling edges can also be detected and the duration between 2 events can be determined.

Information:

The determined moment always lies in the past.

1.5.9.7.2.2 Time-based outputs

NetTime Technology can be used to specify the exact moment of a rising edge on an output. The rising and falling edges can also be specified and a pulse pattern generated from them.

Information:

The specified time must always be in the future, and the set X2X Link cycle time must be taken into account for the definition of the moment.

1.5.9.7.2.3 Time-based measurements

NetTime Technology can be used to determine the exact moment of a measurement that has taken place. Both the starting and end moment of the measurement can be transmitted.

1.5.9.8 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

1.5.9.9 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time
1 ms

1.6 X20AI2322

1.6.1 General information

The module is equipped with 2 inputs with 12-bit digital converter resolution. It is possible to select between the two current ranges 0 to 20 mA and 4 to 20 mA.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

- 2 analog inputs, 0 to 20 mA or 4 to 20 mA
- 12-bit digital converter resolution

1.6.2 Order data

Order number	Short description	Figure
	Analog inputs	
X20AI2322	X20 analog input module, 2 inputs, 0-20 mA / 4-20 mA, 12-bit converter resolution, configurable input filter	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 33: X20AI2322 - Order data

1.6.3 Technical data

Order number	X20AI2322
Short description	
I/O module	2 analog inputs 0 to 20 mA / 4 to 20 mA
General information	
B&R ID code	0xCAB2
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	0.8 W
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
EAC	Yes
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
DNV GL	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
LR	ENV1
Analog inputs	
Input	0 to 20 mA/4 to 20 mA
Input type	Differential input
Digital converter resolution	12-bit
Conversion time	300 µs for all inputs
Output format	
Data type	INT
Current	0x0000 - 0x7FFF / 1 LSB = 0x0008 = 4.883 µA
Load	<400 Ω
Input protection	Protection against wiring with supply voltage
Permissible input signal	Max. ±50 mA
Output of digital value during overload	Configurable
Conversion procedure	SAR
Input filter	3rd-order low pass / cutoff frequency 1 kHz
Max. error at 25°C	
Gain	
0 to 20 mA	0.08% [1]
4 to 20 mA	0.1% [1]
Offset	
0 to 20 mA	0.03% [2]
4 to 20 mA	0.16% [2]
Max. gain drift	
0 to 20 mA	0.009 %/°C [1]
4 to 20 mA	0.0113 %/°C [1]
Max. offset drift	
0 to 20 mA	0.004 %/°C [2]
4 to 20 mA	0.005 %/°C [2]
Common-mode rejection	
DC	70 dB
50 Hz	70 dB
Common-mode range	±12 V
Crosstalk between channels	-70 dB
Nonlinearity	<0.05% [2]
Insulation voltage between channel and bus	500 V_{eff}
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes

Table 34: X20AI2322 - Technical data

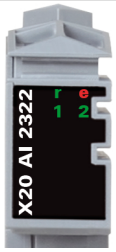
Order number	X20AI2322
Installation elevation above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Pitch	$12.5^{+0.2}$ mm

Table 34: X20AI2322 - Technical data

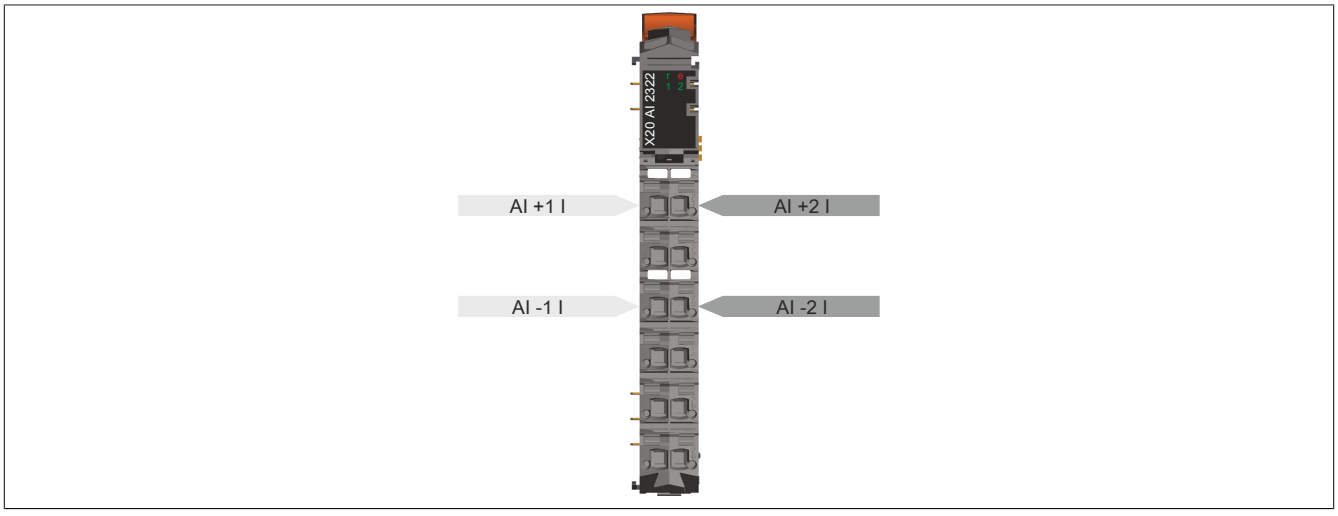
1) Based on the current measured value.
2) Based on the 20 mA measurement range.

1.6.4 LED status indicators

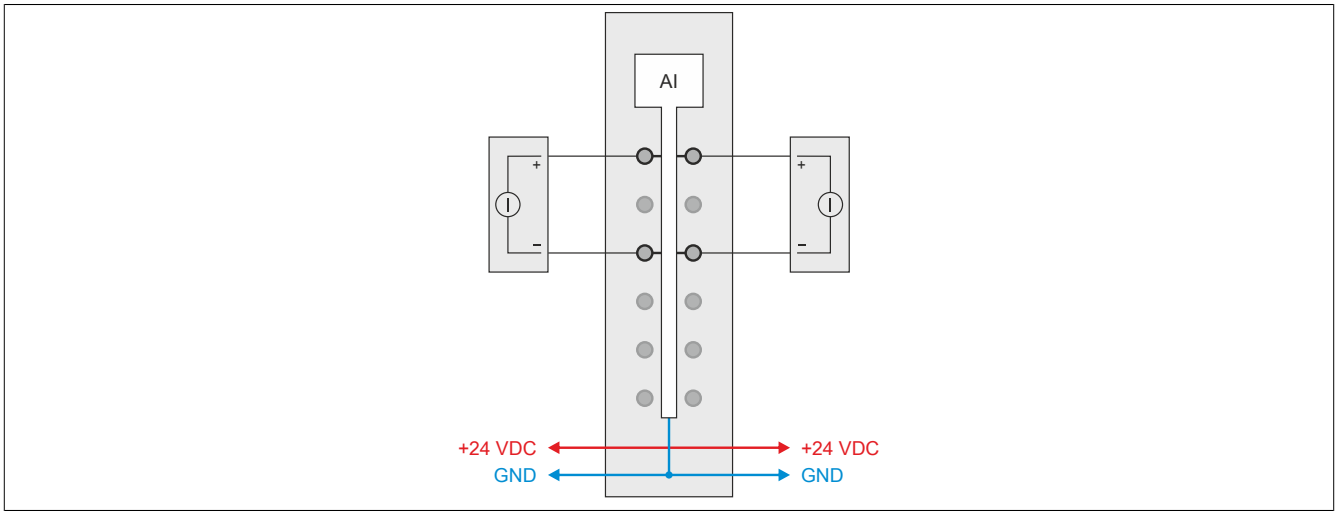
For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 system user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 2	Green	Blinking	Input signal overflow or underflow
			On	Analog/digital converter running, value OK

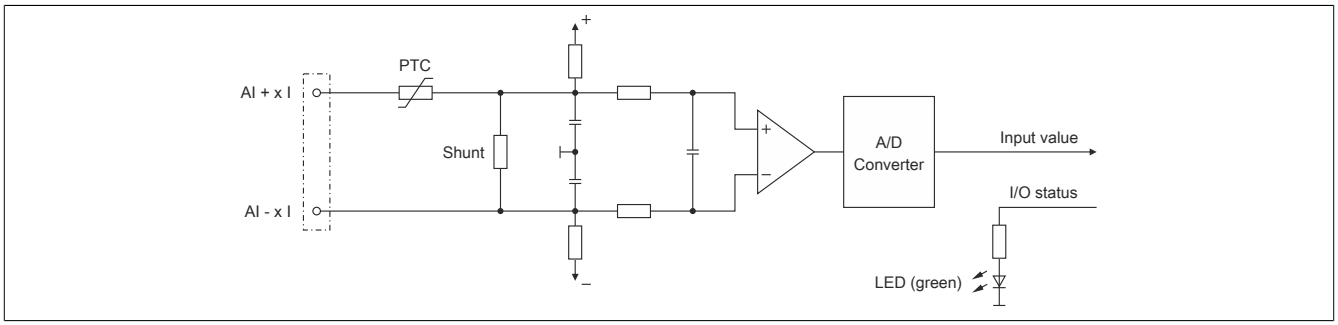
1.6.5 Pinout



1.6.6 Connection example



1.6.7 Input circuit diagram



1.6.8 Register description

1.6.8.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 system user's manual.

1.6.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration						
16	ConfigOutput01 (Input filter)	USINT				•
18	ConfigOutput02 (Channel type)	USINT				•
20	ConfigOutput03 (Lower limit value)	INT				•
22	ConfigOutput04 (Upper limit value)	INT				•
Analog signal - Communication						
0	AnalogInput01	INT	•			
2	AnalogInput02	INT	•			
30	StatusInput01	USINT	•			

1.6.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration							
16	-	ConfigOutput01 (Input filter)	USINT				•
18	-	ConfigOutput02 (Channel type)	USINT				•
20	-	ConfigOutput03 (Lower limit value)	INT				•
22	-	ConfigOutput04 (Upper limit value)	INT				•
Analog signal - Communication							
0	0	AnalogInput01	INT	•			
2	2	AnalogInput02	INT	•			
30	-	StatusInput01	USINT		•		

1) The offset specifies the position of the register within the CAN object.

1.6.8.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

1.6.8.3.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

1.6.8.4 Analog inputs

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

1.6.8.5 Analog input values

Name:
AnalogInput01 to AnalogInput02

The analog input values are mapped to this register.

Data type	Value	Input signal:
INT	0 to 32767	Current signal 0 to 20 mA
	-8192 to 32767	Current signal 4 to 20 mA (value 0 corresponds to 4 mA)

1.6.8.6 Input filter

This module is equipped with a configurable input filter. The minimum cycle time must be >500 µs. Filtering is disabled for shorter cycle times.

If the input filter is active, then the scan rate for the channels is measured in ms. The time offset between the channels is 200 µs. The conversion takes place asynchronously to the network cycle.

1.6.8.6.1 Input ramp limiting

Input ramp limiting can only be performed in conjunction with filtering. Input ramp limiting is performed before filtering.

The difference of the input value change is checked for exceeding the specified limit. In the event of overshoot, the tracked input value is equal to the old value ± the limit value.

Configurable limit values:

Value	Limit value
0	The input value is used without limitation.
1	0x3FFF = 16383
2	0x1FFF = 8191
3	0x0FFF = 4095
4	0x07FF = 2047
5	0x03FF = 1023
6	0x01FF = 511
7	0x00FF = 255

Input ramp limiting is well suited for suppressing disturbances (spikes). The following examples show the functionality of input ramp limiting based on an input step and a disturbance.

Example 1

The input value jumps from 8000 to 17000. The diagram shows the tracked input value with the following settings:

Input ramp limiting = 4 = 0x07FF = 2047

Filter level = 2

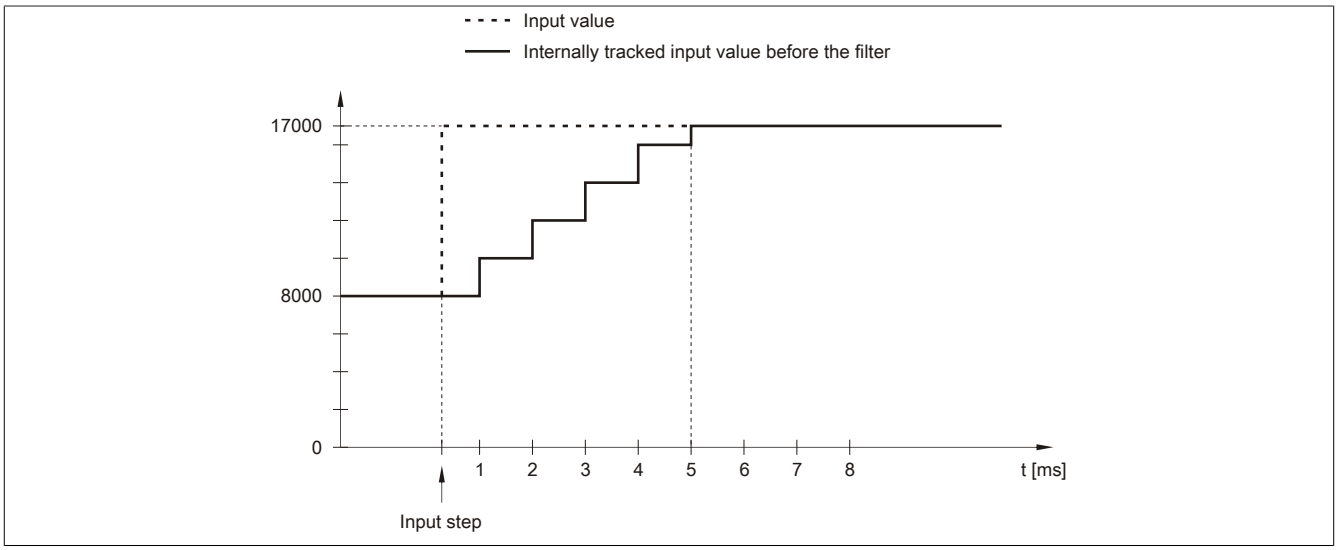


Figure 9: Tracked input value for input step

Example 2

A disturbance interferes with the input value. The diagram shows the tracked input value with the following settings:

Input ramp limiting = 4 = 0x07FF = 2047

Filter level = 2

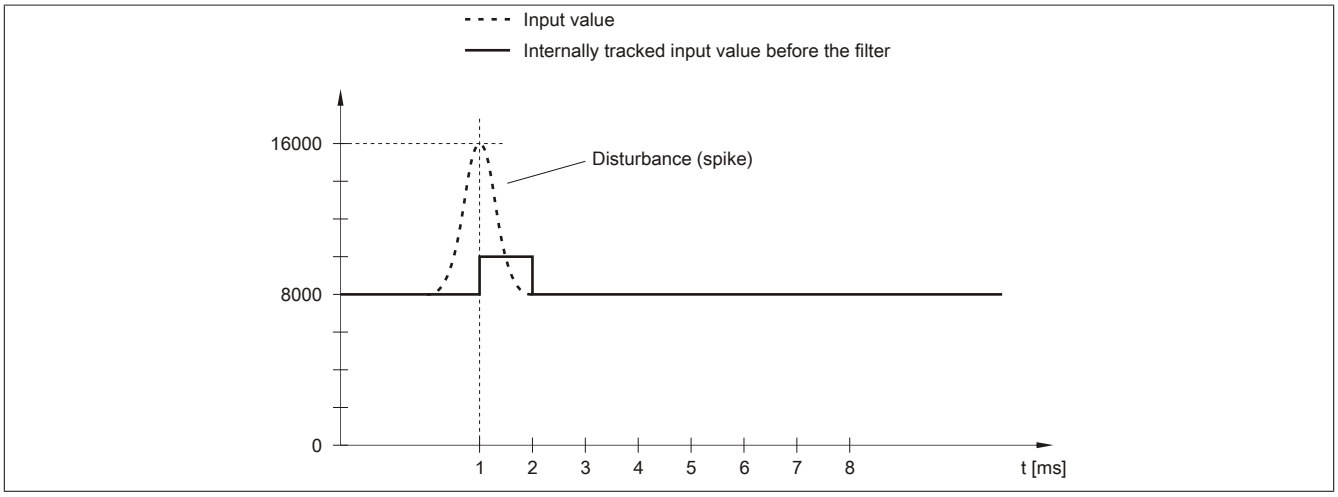


Figure 10: Tracked input value for disturbance

1.6.8.6.2 Filter level

A filter can be defined to prevent large input steps. This filter is used to bring the input value closer to the actual analog value over a period of several bus cycles.
Filtering takes place after any input ramp limiting has been carried out.

Formula for calculating the input value:

$$\text{Value}_{\text{New}} = \text{Value}_{\text{Old}} - \frac{\text{Value}_{\text{Old}}}{\text{Filter level}} + \frac{\text{Input value}}{\text{Filter level}}$$

Adjustable filter levels:

Value	Filter level
0	Filter switched off
1	Filter level 2
2	Filter level 4
3	Filter level 8
4	Filter level 16
5	Filter level 32
6	Filter level 64
7	Filter level 128

The following examples show the functionality of the filter based on an input step and a disturbance.

Example 1

The input value jumps from 8000 to 16000. The diagram shows the calculated value with the following settings:

Input ramp limiting = 0

Filter level = 2 or 4

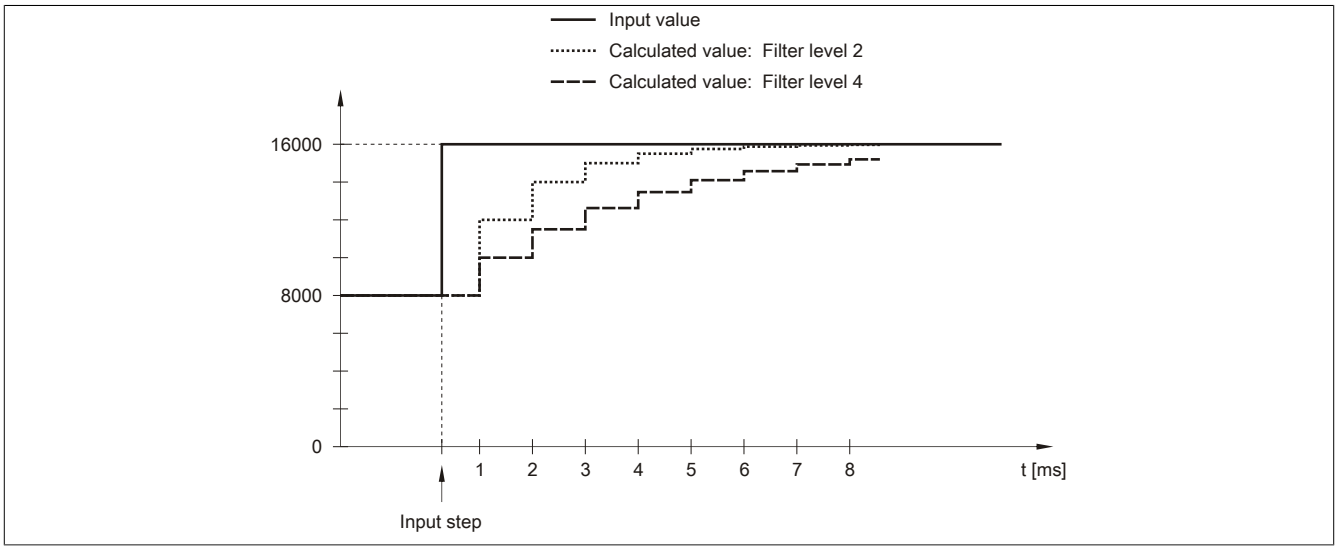


Figure 11: Calculated value during input step

Example 2

A disturbance interferes with the input value. The diagram shows the calculated value with the following settings:

Input ramp limiting = 0

Filter level = 2 or 4

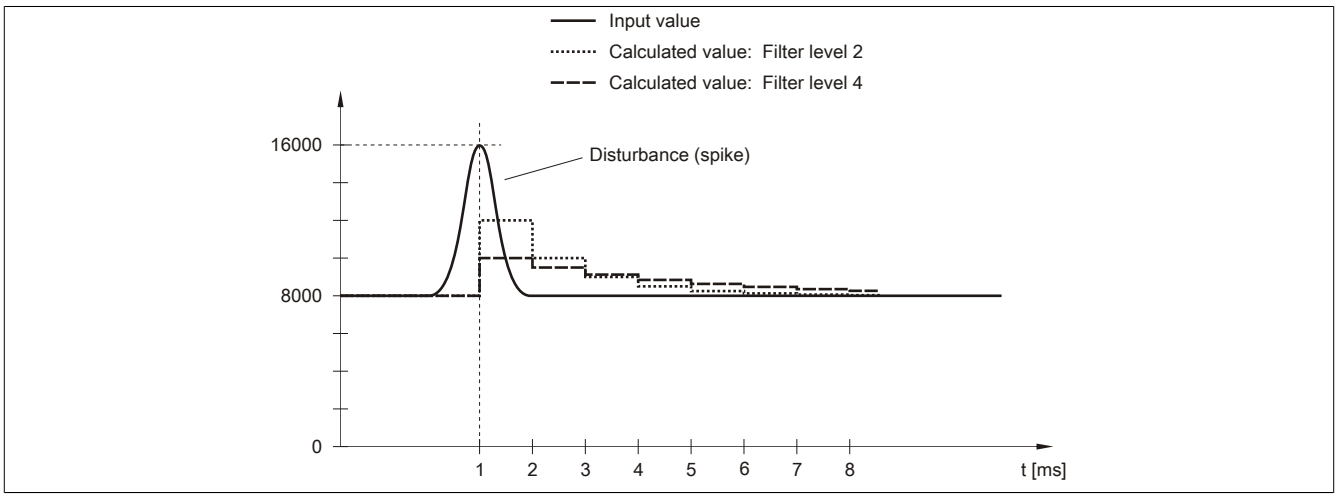


Figure 12: Calculated value during disturbance

1.6.8.7 Configuring the input filter

Name:
ConfigOutput01

The filter level and input ramp limiting of the input filter are set in this register.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter disabled (bus controller default setting)
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines input ramp limiting	000	The input value is applied without limitation (bus controller default setting)
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

1.6.8.8 Channel type

Name:
ConfigOutput02

This register can be used to set the range of the current signal. This is determined by how they are configured. The following input signals can be set:

- 0 to 20 mA current signal
- 4 to 20 mA current signal

Data type	Values	Bus controller default setting
USINT	See the bit structure.	3

Bit structure:

Bit	Description	Value	Information
0 - 1	Reserved	1	
2 - 3	Reserved	0	
4	Channel 1: Current measurement range	0	0 to 20 mA current signal (bus controller default setting)
		1	4 to 20 mA current signal
5	Channel 2: Current measurement range	0	0 to 20 mA current signal (bus controller default setting)
		1	4 to 20 mA current signal
6 - 7	Reserved	0	

1.6.8.9 Lower limit value

Name:
ConfigOutput03

This register can be used to configure the lower limit for analog values. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Values	Information
INT	-32768 to 32767	Bus controller default setting: -32767

Information:

- **When configured as 0 to 20 mA, this value should be set to 0.**
- **When configured as 4 to 20 mA, this value can be set to -8192 (corresponds to 0 mA) in order to display values <4 mA.**

Keep in mind that this setting applies to all channels!

1.6.8.10 Upper limit value

Name:
ConfigOutput04

This register can be used to configure the upper limit for analog values. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Values	Information
INT	-32768 to 32767	Bus controller default setting: 32767

Information:

The default value of 32767 corresponds to the maximum default value at 20 mA.

Keep in mind that this setting applies to all channels!

1.6.8.11 Input status

Name:
StatusInput01

This register is used to monitor the module inputs. A change in the monitoring status generates an error message.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
2 - 3	Channel 2	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
4 - 7	Reserved	0	

Limiting the analog value

In addition to the status information, the analog value is set to the values listed below by default when an error occurs. The analog value is limited to the new values if the limit values were changed.

Error status	Digital value for error (default values)	
	0 to 20 mA	4 to 20 mA
Upper limit value exceeded	+32767 (0x7FFF)	
Lower limit value exceeded	0	-8191 (0xE001)

1.6.8.12 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Inputs without filtering	100 µs
Inputs with filtering	500 µs

1.6.8.13 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time	
Inputs without filtering	300 µs for all inputs
Inputs with filtering	1 ms

1.7 X20AI2437

1.7.1 General information

The module is equipped with 2 current measurement inputs with 16-bit digital converter resolution.

Each current measurement input has its own sensor supply. The two channels with their respective sensor supplies are electrically isolated from each other. The user can select between the two measurement ranges 4 to 20 mA and 0 to 25 mA.

- 2 analog current measurement inputs
- Electrically isolated analog channels
- Electrically isolated sensor supplies
- 16-bit digital converter resolution
- NetTime timestamp: Moment of measurement

NetTime timestamp of the measurement

For many applications, not only the measured value is important, but also the exact time of the measurement. The module is equipped with a NetTime timestamp function for this that supplies a timestamp for the recorded position and trigger time with microsecond accuracy.

The timestamp function is based on synchronized timers. If a timestamp event occurs, the module immediately saves the current NetTime. After the respective data is transferred to the CPU, including this precise moment, the CPU can then evaluate the data using its own NetTime (or system time), if necessary.

1.7.2 Order data

Order number	Short description	Figure
	Analog inputs	
X20AI2437	X20 analog input module, 2 inputs, 4 to 20 mA, 16-bit converter resolution, single-channel isolation with separate sensor power supply, NetTime function	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 35: X20AI2437 - Order data

1.7.3 Technical data

Order number	X20AI2437
Short description	
I/O module	2 analog inputs 4 to 20 mA or 0 to 25 mA
General information	
B&R ID code	0xB784
Status indicators	I/O function per channel, operating state, module status, sensor power supply per channel
Diagnostics	
Module run/error	Yes, using LED status indicator and software
Inputs	Yes, using LED status indicator and software
Sensor power supply	Yes, using LED status indicator and software
Power consumption	
Bus	0.05 W
Internal I/O	1.15 W [1)]
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
DNV GL	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
LR	ENV1
KR	Yes
ABS	Yes
EAC	Yes
KC	Yes
Analog inputs	
Input	4 to 20 mA or 0 to 25 mA configurable using software
Input type	Differential input
Digital converter resolution	15-bit
Data output rate	4.7 to 960 samples per second, configurable using software
Output format	INT
Output format	
4 to 20 mA	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 488.281 nA
0 to 25 mA	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 762.939 nA
0 to 25000 µA	INT 0x0000 - 0x61A8 / 1 LSB = 0x0001 = 1000 nA
Load	I_IN ≥ 0.1 mA: R < 8000 Ω I_IN ≥ 1 mA: R < 1100 Ω I_IN ≥ 4 mA: R < 510 Ω
Input protection	Up to 30 VDC, reverse polarity protection (max. 0.1 A)
Open-circuit detection	Yes, using software
Permissible input signal	0 to 25 mA
Output of digital value during overload	Configurable
Conversion procedure	Sigma-delta
Max. error	
Gain	
0 to 25 mA	<0.046% [2)]
4 to 20 mA	<0.046% [2)]
Offset	
0 to 25 mA	<0.004% [3)]
4 to 20 mA	<0.013% [3)]
Common-mode rejection	
DC	80 dB
50 Hz	Depends on the sampling rate: e.g. >130 dB for 50 samples per second
Common-mode range	0 to 7 V
Nonlinearity	<0.003% [3)]
Input filter	
Hardware	First-order low-pass filter / cutoff frequency 2.5 kHz
Software	Sinc^4 filter
Max. gain drift	
0 to 25 mA	0.003 %/°C [2)]
4 to 20 mA	0.003 %/°C [2)]

Table 36: X20AI2437 - Technical data

Order number	X20AI2437
Max. offset drift	
0 to 25 mA	0.0002 %/°C 3)
4 to 20 mA	0.0007 %/°C 3)
Test voltage	
Channel - Channel	1000 VAC
Channel - Bus	1000 VAC
Channel - Ground	1000 VAC
Sensor power supply	
Power consumption	0.75 W per channel
Nominal voltage	25 V ±2%
Nominal output current	Max. 30 mA
Short-circuit proof	Yes, continuous
Max. voltage ripple	
Up to 100 kHz	≤2.2 mV
Up to 1 MHz	≤22 mV
Higher	≤100 mV
Short-circuit current	
Typical	<50 mA
Maximum	60 mA
Behavior on short circuit	Current limiting
Electrical properties	
Electrical isolation	Channel isolated from channel and bus Sensor power supply isolated from sensor power supply Sensor power supply not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x terminal block X20TB12 separately. Order 1x bus module X20BM11 separately.
Pitch	$12.5^{+0.2}$ mm

Table 36: X20AI2437 - Technical data

1) To reduce power dissipation, B&R recommends leaving unused inputs open.
2) Based on the current measured value.
3) Based on the 25 mA measurement range.

1.7.4 LED status indicators

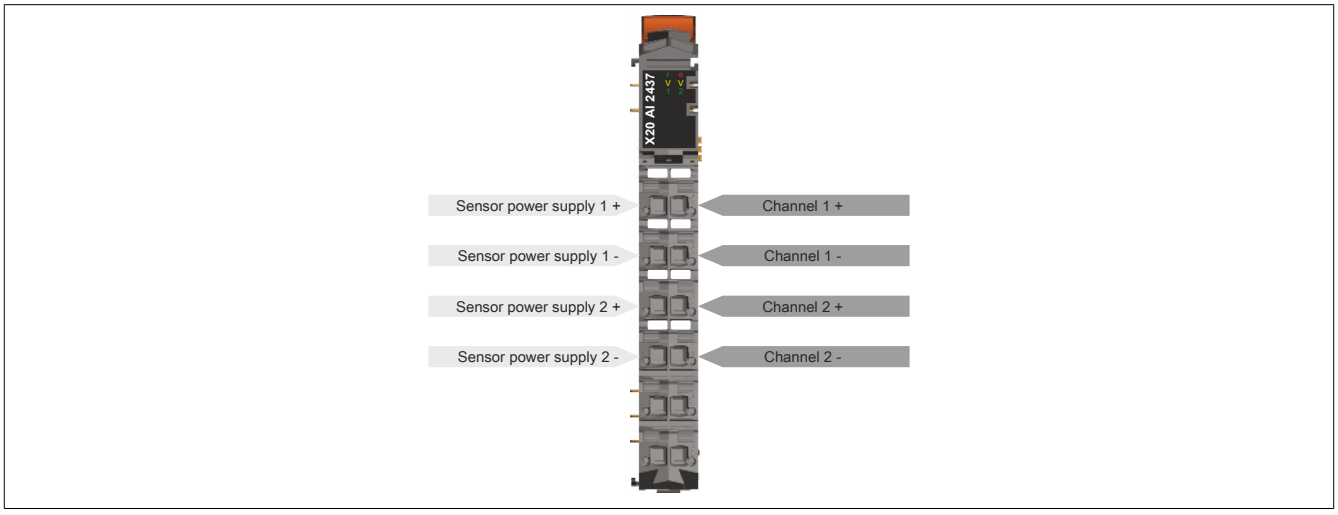
For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 system user's manual.

Figure	LED	Color	Status	Description
	**Operating state**			
	r	Green	Off	No power to module
			Single flash	UNLINK mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking quickly	SYNC mode
			Blinking slowly	PREOPERATIONAL mode
			On	RUN mode
	Module status			
	e	Red	Off	No power to module or everything OK
			Single flash	A conversion error has occurred. This status is output along with a double flash on the channel LED of the analog input where the error occurs.
			On	Error or reset status
	Sensor supply			
	V	Yellow	Off	Overload
			On	Sensor supply in its normal operating range
	Analog input			
	1 - 2	Green	Off	Indicates one of the following cases: • No power to module • Channel disabled • Open line
			Single flash	Input signal overflow or underflow
			Double flash	A conversion error has occurred. A single flash is output on the red "e" module status LED.
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.

1.7.5 Pinout

Shielded twisted pair cables should be used to minimize coupling disturbances. Use either one cable for each channel or a multiple twisted pair cable for both channels.

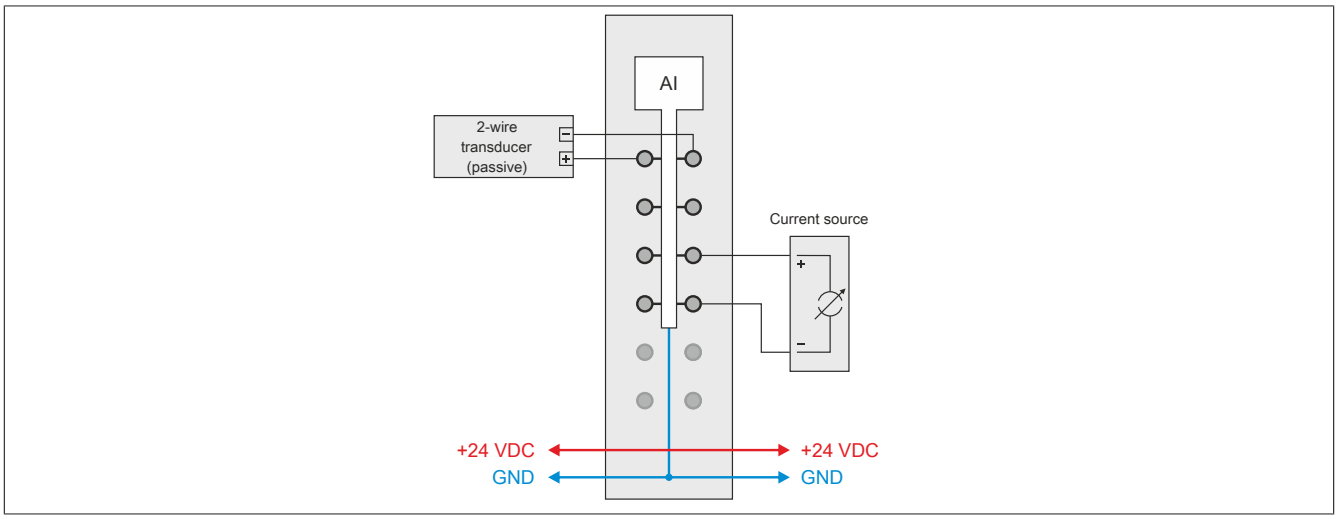


1.7.6 Connection examples

2-wire connections

A 2-wire connection can be implemented as follows:

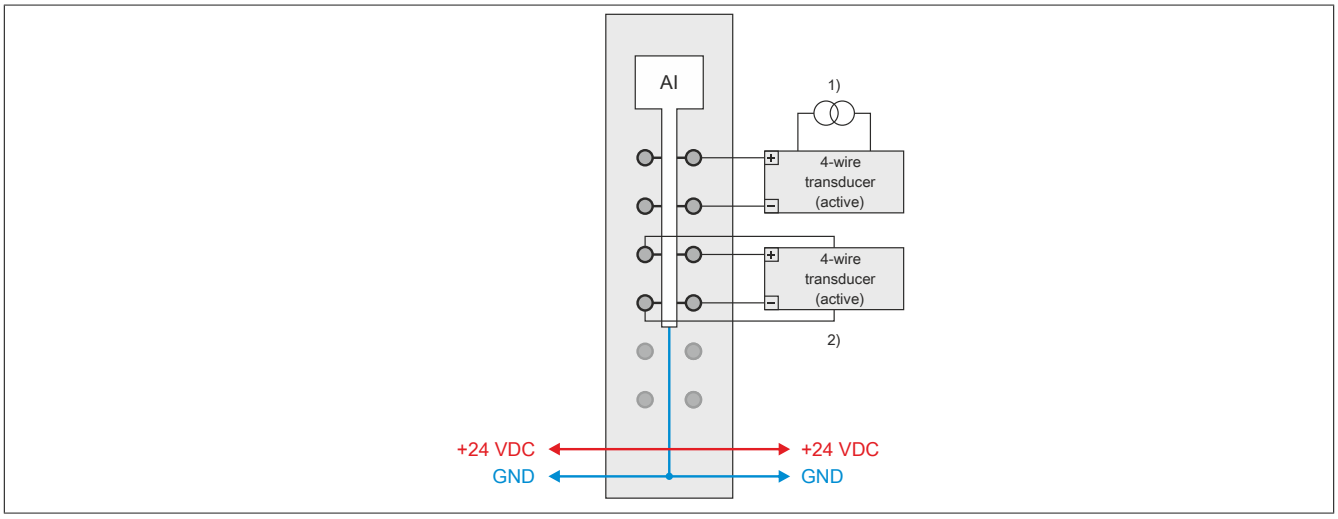
- 2-wire transducer
- Active current source



4-wire connections

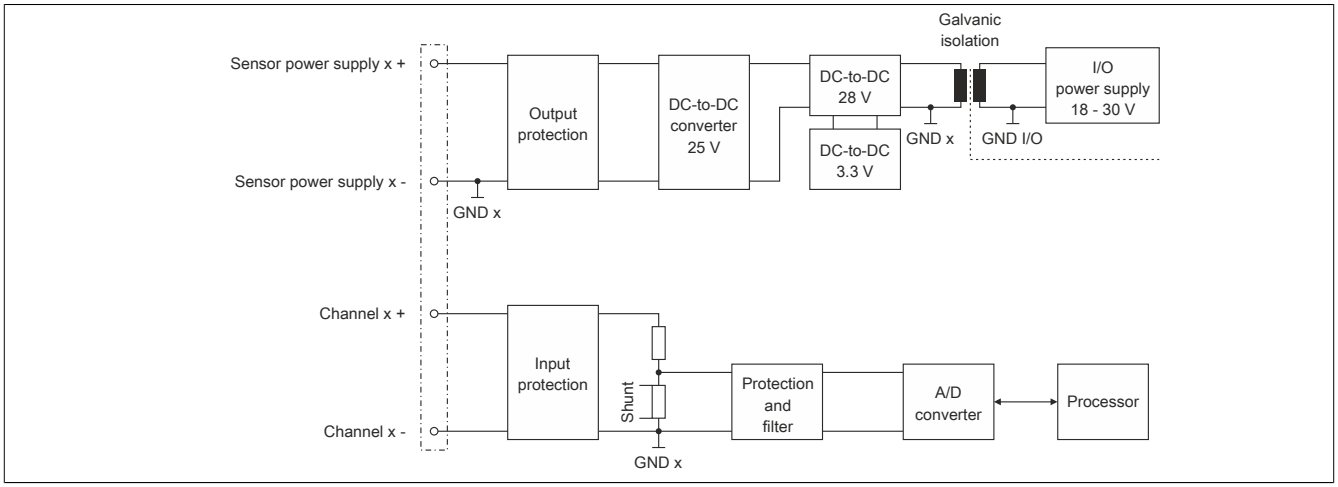
A 4-wire connection can be implemented as follows:

- 4-wire transducer with external supply
- 4-wire transducer supplied by the module



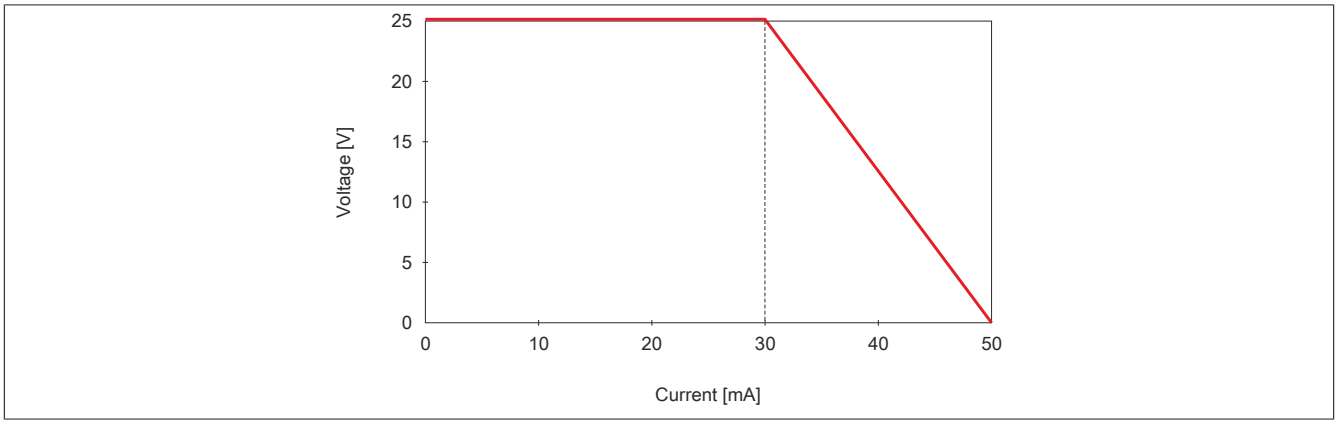
1) With external power supply.
2) With internal power supply. The internal power supply is only permitted to be loaded with max. 30 mA.

1.7.7 Input circuit diagram



1.7.8 Behavior in the event of short circuit

In the event of a short circuit, the output current for the sensor supply is limited according to the following diagram.



1.7.9 Register description

1.7.9.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 system user's manual.

1.7.9.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration						
386 426	AnMode_1 AnMode_2	UINT				•
390 430	Samplerate_1 Samplerate_2	UINT				•
394 434	OpenLoopLimit_1 OpenLoopLimit_2	(U)INT				•
398 438	LowerLimit_1 LowerLimit_2	(U)INT				•
402 442	UpperLimit_1 UpperLimit_2	(U)INT				•
406 446	Hysteres_1 Hysteres_2	(U)INT				•
410 450	ReplacementLower_1 ReplacementLower_2	(U)INT				•
414 454	ReplacementUpper_1 ReplacementUpper_2	INT				•
418 458	ErrorDelay_1 ErrorDelay_2	UINT				•
422 462	SumErrorDelay_1 SumErrorDelay_2	UINT				•
466 482	PreparationInterval_1 PreparationInterval_2	UINT				•
Analog signal - Communication						
266 270	AnalogInput01 (if replacement value strategy on) AnalogInput02 (if replacement value strategy on)	(U)INT	•			
258 262	AnalogInput01 (if replacement value strategy off) AnalogInput02 (if replacement value strategy off)	(U)INT	•			
282 290	AnalogSampletime01 (16-bit) AnalogSampletime02 (16-bit)	INT	•			
284 292	AnalogSampletime01 (32-bit) AnalogSampletime02 (32-bit)	DINT	•			
30 31	AnalogStatus01 AnalogStatus02	USINT	•			
	UnderflowAnalogInput01 or 02	Bit 0				
	OverflowAnalogInput01 or 02	Bit 1				
	OpenLineAnalogInput01 or 02	Bit 2				
	ConversionErrorAnalogInput01 or 02	Bit 3				
	SumErrorAnalogInput01 or 02	Bit 4				
	SensorErrorAnalogInput01 or 02	Bit 6				
	IoSuppErrorAnalogInput01 or 02	Bit 7				

1.7.9.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration							
386 426	- -	AnMode_1 AnMode_2	UINT				•
390 430	- -	Samplerate_1 Samplerate_2	UINT				•
394 434	- -	OpenLoopLimit_1 OpenLoopLimit_2	INT				•
398 438	- -	LowerLimit_1 LowerLimit_2	(U)INT				•
402 442	- -	UpperLimit_1 UpperLimit_2	(U)INT				•
406 446	- -	Hysteres_1 Hysteres_2	(U)INT				•
410 450	- -	ReplacementLower_1 ReplacementLower_2	(U)INT				•
414 454	- -	ReplacementUpper_1 ReplacementUpper_2	(U)INT				•
418 458	- -	ErrorDelay_1 ErrorDelay_2	UINT				•
422 462	- -	SumErrorDelay_1 SumErrorDelay_2	UINT				•
466 482	- -	PreparationInterval_1 PreparationInterval_2	UINT				•
Analog signal - Communication							
266 270	0 2	AnalogInput01 (if replacement value strategy on) AnalogInput02 (if replacement value strategy on)	(U)INT	•			
258 262	- -	AnalogInput01 (if replacement value strategy off) AnalogInput02 (if replacement value strategy off)	(U)INT		•		
30 31	- -	AnalogStatus01 AnalogStatus02	USINT		•		
		UnderflowAnalogInput01 or 02	Bit 0				
		OverflowAnalogInput01 or 02	Bit 1				
		OpenLineAnalogInput01 or 02	Bit 2				
		ConversionErrorAnalogInput01 or 02	Bit 3				
		SumErrorAnalogInput01 or 02	Bit 4				
		SensorErrorAnalogInput01 or 02	Bit 6				
		IoSuppErrorAnalogInput01 or 02	Bit 7				

1) The offset specifies the position of the register within the CAN object.

1.7.9.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

1.7.9.3.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

1.7.9.4 General information

The module is equipped with 2 independent electrically isolated channels. Both channels can be used to read in an analog signal. All registers necessary for this have a dual design so that the channels can be configured and operated independently of one another.
The current input signals (0 to 25 mA) can be displayed in different formats.

Specific features:

- Channels electrically isolated
- Internal supply with short circuit protection <30 mA per channel
- Configurable filter (default 50 Hz)
- Selective line monitoring can be enabled for: open line (<2 mA), underflow (<3.6 mA) or overflow (>21 mA) of a configurable threshold
- Selectable error strategy: Replacement value for the respective threshold (default) or use the last valid value

1.7.9.5 Analog signal - Configuration

How the analog signal is displayed can be adapted to the requirements of the application. Separate configuration registers per channel are available to aid in this.

1.7.9.5.1 Channel parameters

Name:
AnMode_1 to AnMode_2

These registers are used to predefine the operating parameters that the module will be using for the respective channel. Each channel must be enabled individually and can be configured and operated independently.

Information:

Different limit values must be configured for any display normalizing that needs to take place.

Data type	Values	Bus controller default setting
UINT	See bit structure.	29

Bit structure:

Bit	Name	Value	Information
0	Channel	0	Channel 0x turned off
		1	Channel 0x enabled (bus controller default setting)
1	Open line detection	0	Open line monitoring turned off
		1	Open circuit monitoring enabled (bus controller default setting)
2	Underflow detection	0	Underflow detection turned off
		1	Underflow detection enabled (bus controller default setting)
3	Replacement value strategy	0	Use replacement values in the event of error (bus controller default setting)
		1	Keep the last valid converted value
4 - 5	Normalization	00	Displays 0 to 25 mA as 0 to 32767
		01	Display 0 to 25 mA as 0 to 25000 [µA] (bus controller default setting)
		10	Displays 4 to 20 mA as 0 to 32767
		11	Displays 0 to 25 mA as 0 to 65535
6 - 15	Reserved	-	

1.7.9.5.2 Sample rate

Name:
Samplerate_1 to Samplerate_2

A sample rate can be configured for both analog inputs independently of one another. The following formula for this parameter is derived using the desired sampling frequency:

Sampling rate for A/D converter = (4920000 / 1024) / Sampling frequency

Data type	Value	Information
UINT	4 to 1023	Sample rate **Examples of configurable values** **Value** / **Time** / **Frequency** 960 ... 200 ms ... 5 Hz 480 ... 100 ms ... 10 Hz 320 ... 66.7 ms ... 15 Hz 192 ... 40 ms ... 25 Hz 160 ... 33.3 ms ... 30 Hz 96 ... 20 ms ... 50 Hz (bus controller default setting) 80 ... 16.7 ms ... 60 Hz 48 ... 10 ms ... 100 Hz 9 ... 2 ms ... 500 Hz 4 ... 1 ms ... 1000 Hz

Setting to 1000 Hz will result in jitter when acquiring measured values. Jitter-free operation is possible up to 960 Hz (sample rate setting = 5).

1.7.9.5.3 Limit value for open line detection

Name:
OpenLoopLimit_1 to OpenLoopLimit_2

The limit value for the respective analog input must be set when open circuit monitoring is enabled and if required by the configured normalization.

Data type	Value	Information
INT	-32767 to 32767	Open circuit limit value. Bus controller default setting: 2621
UINT	0 to 65535	Open circuit limit value

If limit value monitoring is active, the corresponding error status is output after a configured delay when falling below this value. Using a default value of 2000 µA, the following values and formulas result for this parameter:

- Displays 0 to 25 mA as 0 to 25000: 2000
- Displays 0 to 25 mA as 0 to 32767: 2621, limit value = ([µA] * 32767) / 25000
- Displays 4 to 20 mA as 0 to 32767: -4096, limit value = (([µA] * 1.31068) - 5242.72) * 1.5625
- Displays 0 to 25 mA as 0 to 65535: 5243, limit value = ([µA] * 65535) / 25000

1.7.9.5.4 Lower limit value

Name:
LowerLimit_1 to LowerLimit_2

If the value range needs to be restricted further, this register can be used to enter new user-specific lower limit values.

Data type	Value	Information
INT	-32767 to 32767	Bus controller default setting: 4718
UINT	0 to 65535	

The limit value must be set for the respective analog input depending on the configured normalization. After the configured delay time has passed, the corresponding error status is given if the respective value is overrun or underrun. When this error state occurs, the "AnalogInput0x" on page 181 channel is evaluated according to the replacement value strategy. Using a default value of 3600 µA, the following values and formulas result for this parameter:

- Displays 0 to 25 mA as 0 to 25000: 3600
- Displays 0 to 25 mA as 0 to 32767: 4718, limit value = ([µA] * 32767) / 25000
- Displays 4 to 20 mA as 0 to 32767: -819, limit value = (([µA] * 1.31068) - 5242.72) * 1.5625
- Displays 0 to 25 mA as 0 to 65535: 9437, limit value = ([µA] * 65535) / 25000

1.7.9.5.5 Upper limit value

Name:
UpperLimit_1 to UpperLimit_2

If the value range needs to be restricted further, this register can be used to enter new user-specific upper limit values.

Data type	Value	Information
INT	-32767 to 32767	Bus controller default setting: 27524
UINT	0 to 65535	

The limit value must be set for the respective analog input depending on the configured normalization. After the configured delay time has passed, the corresponding error status is given if the respective value is overrun or underrun. When this error state occurs, the "AnalogInput0x" on page 181 channel is evaluated according to the replacement value strategy. Using a default value of 21000 µA, the following values and formulas result for this parameter:

- Displays 0 to 25 mA as 0 to 25000: 21000
- Displays 0 to 25 mA as 0 to 32767: 27524, limit value = ([µA] * 32767) / 25000
- Displays 4 to 20 mA as 0 to 32767: 32767, limit value = (([µA] * 1.31068) - 5242.72) * 1.5625
- Displays 0 to 25 mA as 0 to 65535: 55049, limit value = ([µA] * 65535) / 25000

1.7.9.5.6 Hysteresis

Name:
Hysteres_1 to Hysteres_2

If the user-specific limit values are being used, then a hysteresis range should also be defined. These registers configure how far a limit value can be exceeded before a response is triggered.

Data type	Value	Information
INT	-32767 to 32767	Bus controller default setting: 131
UINT	0 to 65535	

The hysteresis value must be set for the respective analog input depending on the configured normalization. The error status is cleared if the actual analog value changes by at least this hysteresis value from the limit value in the allowed direction. Using a default value of 100 µA, the following values and formulas result for this parameter:

- Displays 0 to 25 mA as 0 to 25000: 100
- Displays 0 to 25 mA as 0 to 32767: 131, limit value = ([µA] * 32767) / 25000
- Displays 4 to 20 mA as 0 to 32767: 156, limit value = [µA] * 1.5625
- Displays 0 to 25 mA as 0 to 65535: 262, limit value = ([µA] * 65535) / 25000

1.7.9.5.7 Lower replacement value

Name:
ReplacementLower_1 to ReplacementLower_2

This register is used to define the lower static values to be displayed instead of the current measured value when the lower limit is violated.

Data type	Value	Information
INT	-32767 to 32767	Bus controller default setting: 4718
UINT	0 to 65535	

If the replacement strategy "Use replacement values when an error occurs" is enabled, the replacement value must be set for the respective analog input taking the configured normalization into account as well. When an overflow or underflow error status occurs, the "AnalogInput0x" on page 181 channel is replaced with the corresponding value. Using a default value of 3600 µA, the following values and formulas result for this parameter:

- Displays 0 to 25 mA as 0 to 25000: 3600
- Displays 0 to 25 mA as 0 to 32767: 4718, limit value = ([µA] * 32767) / 25000
- Displays 4 to 20 mA as 0 to 32767: -819, limit value = (([µA] * 1.31068) - 5242.72) * 1.5625
- Displays 0 to 25 mA as 0 to 65535: 9437, limit value = ([µA] * 65535) / 25000

1.7.9.5.8 Upper replacement value

Name:
ReplacementUpper_1 to ReplacementUpper_2

This register is used to define the static values to be displayed instead of the current measured value when the upper limit is violated.

Data type	Value	Information
INT	-32767 to 32767	Bus controller default setting: 27524
UINT	0 to 65535	

If the replacement strategy "Use replacement values when an error occurs" is activated, the replacement value must be set for the respective analog input taking the configured normalization into account as well. When an overflow or underflow error status occurs, the "AnalogInput0x" on page 181 channel is replaced with the corresponding value. Using a default value of 21000 µA, the following values and formulas result for this parameter:

- Displays 0 to 25 mA as 0 to 25000: 21000
- Displays 0 to 25 mA as 0 to 32767: 27524, limit value = ([µA] * 32767) / 25000
- Displays 4 to 20 mA as 0 to 32767: 32767, limit value = (([µA] * 1.31068) - 5242.72) * 1.5625
- Displays 0 to 25 mA as 0 to 65535: 55049, limit value = ([µA] * 65535) / 25000

1.7.9.5.9 Delaying error messages

Name:
ErrorDelay_1 to ErrorDelay_2

This register specifies the number of consecutive conversion procedures where an error is pending until the corresponding individual error status bit is set. The delay applies to underflow, overflow and open circuit errors. This delay can be used to hide temporary measured value deviations, for example.

Data type	Value	Information
UINT	0 to 10	Error formation delay in conversion cycles. Bus controller default setting: 2

1.7.9.5.10 Time for composite error bit

Name:
SumErrorDelay_1 to SumErrorDelay_2

This register specifies the time in milliseconds that one of the individual error bits must be pending until the composite error status bit is set.

Data type	Value	Information
UINT	0 to 65535	Composite error bit delay in ms. Bus controller default setting: 4000

1.7.9.5.11 Preparation time for the measured values

Name:
PreparationInterval01 to PreparationInterval02

If the last valid measured value should be kept when violating the limit value, then PreparationInterval must be defined. The measured values continue to be acquired and converted according to the configured I/O update time. They are then checked and discarded if they do not meet the specifications. When an error does not occur, therefore, the measured value acquired 2 preparation intervals ago is constantly output.

Data type	Value	Information
UINT	0 to 65535	In 0.1 ms. Bus controller default setting: 0

Functionality:
Measured values are continuously converted and stored to measured value memory. The current contents of the measured value memory are checked within the configured interval. If a permissible value is present, then the contents of the buffer memory are passed to output memory and the contents of the measured value memory are passed to the buffer.
If the check turns up an impermissible value, then the contents of the measured value memory are discarded. The copy direction between output and buffer memory reverses and the last valid value continues to be output.

Information:

If configured to keep the last valid value, the delay time from measuring to outputting the value will be at least twice the preparation interval. In the worst case scenario, this can also take twice the interval time plus the configured conversion rate of the A/D converter.

"Application" Value being measured (analog)	
↓	Condition: - Conversion interval (A/D converter) elapsed
"Measured value memory" Measured value (digital)	
↓	Condition: - PreparationInterval elapsed - Measured value permissible
"Buffer" Last valid value	
↓	Condition: - PreparationInterval elapsed - Measured value permissible
"Output memory" Next-to-last valid/ displayed value	

1.7.9.6 Analog signal - Communication

1.7.9.6.1 Analog input values

Name:
AnalogInput01 to AnalogInput02

The analog input value is mapped in this register.

Data type	Value	Information
INT	0 to 25000	Normalizing option 0 to 25 mA
	0 to 32,767	Normalizing option 0 to 25 mA
	-8192 to 32767	Normalizing option 4 to 20 mA (value 0 corresponds to 4 mA)
UINT	0 to 65535	Normalizing option 0 to 25 mA

Predefining values and timing
If a replacement value strategy was configured, value "0" (zero) is output from the beginning until a valid measured value has been calculated.

The timing for acquiring measured values is determined by the converter hardware and the set sampling rate. The two channels are converted independently of each other and are not synchronized with the X2X Link.

Conversion time
Channel 0x sampling rate

1.7.9.6.2 Sample time

Name:
AnalogSampletime01 to AnalogSampletime02

These registers return the timestamp for when the module reads the current channel mapping. The values are provided as signed 2-byte or 4-byte values.

For additional information about NetTime and timestamps, see "NetTime Technology" on page 184.

Data type	Values	Information
INT	-32,768 to 32767	NetTime timestamp of the current input value in µs
DINT	-2147483648 to 2147483647	NetTime timestamp of the current input value in µs

1.7.9.6.3 Status of the inputs

Name:
AnalogStatus01 to AnalogStatus02
UnderflowAnalogInput01 to UnderflowAnalogInput02
OverflowAnalogInput01 to OverflowAnalogInput02
OpenLineAnalogInput01 to OpenLineAnalogInput02
ConversionErrorAnalogInput01 to ConversionErrorAnalogInput02
SumErrorAnalogInput01 to SumErrorAnalogInput02
SensorErrorAnalogInput01 to SensorErrorAnalogInput02
IoSuppErrorAnalogInput01 to IoSuppErrorAnalogInput02

The current error state of the module channels is indicated in this register regardless of the configured replacement value strategy. Some error information is delayed according to the previously configured condition.

Setting "Format of status information" in Automation Studio makes it possible to define whether the status information is transferred as USINT or bit values.

Data type	Values
USINT	See bit structure.

Bit structure:

Bit	Name	Values	Information
0	UnderflowAnalogInput01 or 02	0	No error
		1	Lower limit value undershot
1	OverflowAnalogInput01 or 02	0	No error
		1	Upper limit value overshot
2	OpenLineAnalogInput01 or 02	0	No error
		1	Open circuit determined
3	ConversionErrorAnalogInput01 or 02	0	No error
		1	Conversion error determined
4	SumErrorAnalogInput01 or 02	0	No error
		1	Composite error determined
5	Reserved	-	
6	SensorErrorAnalogInput01 or 02	0	Sensor voltage OK
		1	Sensor load too high
7	IoSuppErrorAnalogInput01 or 02	0	I/O power supply OK
		1	Error in I/O power supply determined

UnderflowAnalogInput

The signal underflow error state is represented here based on the configuration. This error information is enabled as a multiple of the conversion cycles only after the configurable delay time has passed (see register "ErrorDelay" on page 180).

OverflowAnalogInput

The signal overflow error status state is represented here based on the configuration. This error information is enabled as a multiple of the conversion cycles only after the configurable delay time has passed (see register "ErrorDelay" on page 180).

OpenLineAnalogInput

Based on the configuration, the measurement information is checked for values <2 mA (register "OpenLoopLimit" on page 178) to detect a failure signal. Open circuit detection is performed using a configurable hysteresis value (default: 100 µA, register "Hysteresis" on page 179). It is possible to disable open circuit detection (register "AnalogMode" on page 177) to suppress the generation of alarms when hardware is missing. This error information is enabled as a multiple of the conversion cycles only after the configurable delay time has passed (register "ErrorDelay" on page 180).

ConversionErrorAnalogInput

This error state is triggered when the hardware overshoots the conversion time.

SumErrorAnalogInput

This error information is derived from the state of individual errors and enabled only after the configurable delay time has passed [ms] (see register "SumErrorDelay" on page 180). Linking this error information in an application makes it possible to hide temporary overshoots or undershoots of the temperature value, for example.

SensorErrorAnalogInput

This error is enabled immediately after a fault is detected in the internal sensor power supply.

IoSuppErrorAnalogInput

This error is enabled immediately after a supply voltage undershoot is detected (<20 VDC).

1.7.9.7 NetTime Technology

NetTime refers to the ability to precisely synchronize and transfer system times between individual components of the controller or network (CPU, I/O modules, X2X Link, POWERLINK, etc.).

This allows the moment that events occur to be determined system-wide with microsecond precision. Upcoming events can also be executed precisely at a specified moment.

1.7.9.7.1 Time information

Various time information is available in the controller or on the network:

- System time (on the PLC, Automation PC, etc.)
- X2X Link time (for each X2X Link network)
- POWERLINK time (for each POWERLINK network)
- Time data points of I/O modules

The NetTime is based on 32-bit counters, which are increased with microsecond resolution. The sign of the time information changes after 35 min, 47 s, 483 ms and 648 µs; an overflow occurs after 71 min, 34 s, 967 ms and 296 µs.

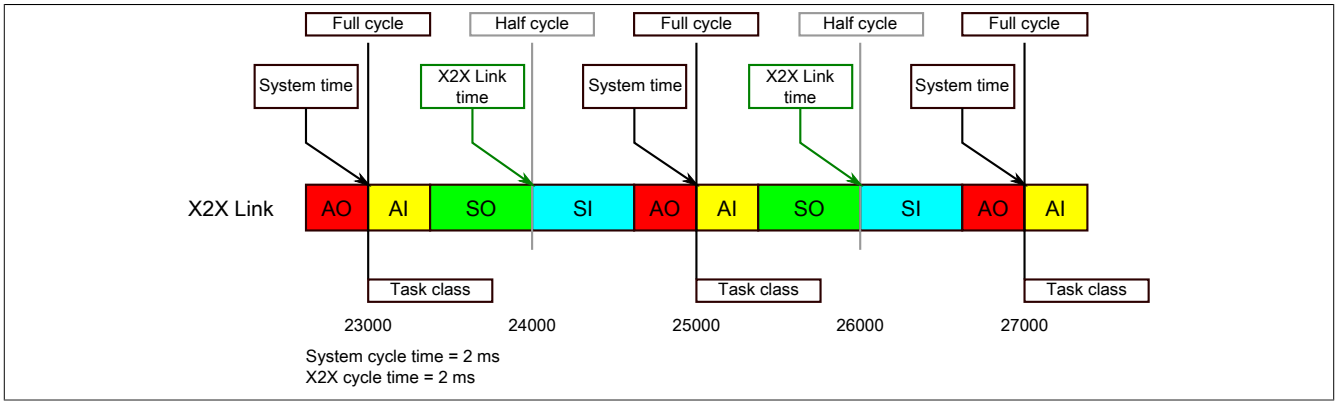
The initialization of the times is based on the system time during the startup of the X2X Link, the I/O modules or the POWERLINK interface.

Current time information in the application can also be determined via library AsIOTime.

1.7.9.7.1.1 PLC/Controller data points

The NetTime I/O data points of the PLC or the controller are latched to each system clock and made available.

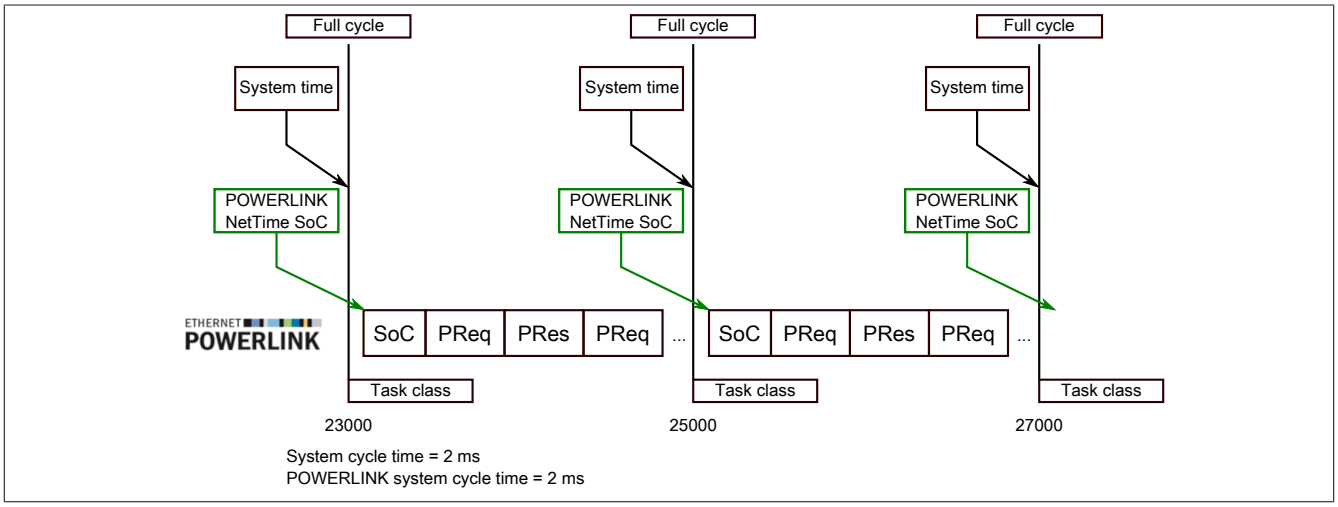
1.7.9.7.1.2 X2X Link reference moment



The reference moment on the X2X Link network is always calculated at the half cycle of the X2X Link cycle. This results in a difference between the system time and the X2X Link reference moment when the reference time is read out.

In the example above, this results in a difference of 1 ms, i.e. if the system time and X2X Link reference moment are compared at time 25000 in the task, then the system time returns the value 25000 and the X2X Link reference moment returns the value 24000.

1.7.9.7.1.3 POWERLINK - Reference time point

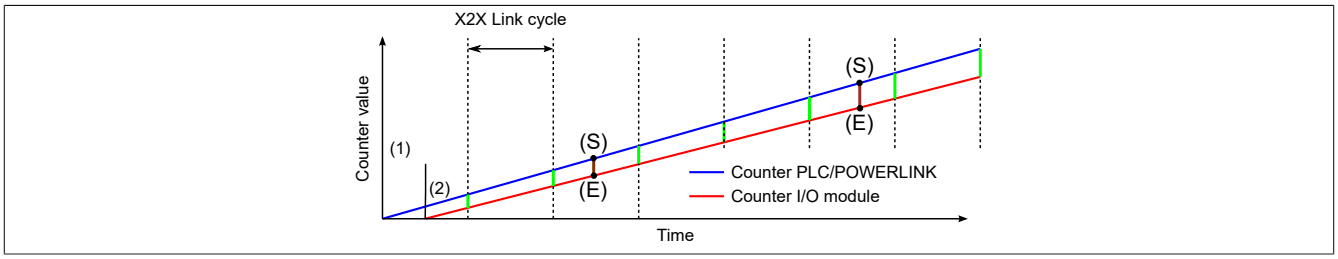


The reference time point on the POWERLINK network is always calculated at the start of cycle (SoC) of the POWERLINK network. The SoC starts 20 µs after the system clock due to the system. This results in the following difference between the system time and the POWERLINK reference time:

POWERLINK reference time = System time - POWERLINK cycle time + 20 µs.

In the example above, this means a difference of 1980 µs, i.e. if the system time and POWERLINK reference time are compared at time 25000 in the task, then the system time returns the value 25000 and the POWERLINK reference time returns the value 23020.

1.7.9.7.1.4 Synchronization of system time/POWERLINK time and I/O module



At startup, the internal counters for the PLC/POWERLINK (1) and the I/O module (2) start at different times and increase the values with microsecond resolution.

At the beginning of each X2X Link cycle, the PLC or the POWERLINK network sends time information to the I/O module. The I/O module compares this time information with the module's internal time and forms a difference (green line) between the two times and stores it.

When a NetTime event (E) occurs, the internal module time is read out and corrected with the stored difference value (brown line). This means that the exact system moment (S) of an event can always be determined, even if the counters are not absolutely synchronous.

Note

The deviation from the clock signal is strongly exaggerated in the picture as a red line.

1.7.9.7.2 Timestamp functions

NetTime-capable modules provide various timestamp functions depending on the scope of functions. If a timestamp event occurs, the module immediately saves the current NetTime. After the respective data is transferred to the CPU, including this precise moment, the CPU can then evaluate the data using its own NetTime (or system time), if necessary.

1.7.9.7.2.1 Time-based inputs

NetTime Technology can be used to determine the exact moment of a rising edge at an input. The rising and falling edges can also be detected and the duration between 2 events can be determined.

Information:

The determined moment always lies in the past.

1.7.9.7.2.2 Time-based outputs

NetTime Technology can be used to specify the exact moment of a rising edge on an output. The rising and falling edges can also be specified and a pulse pattern generated from them.

Information:

The specified time must always be in the future, and the set X2X Link cycle time must be taken into account for the definition of the moment.

1.7.9.7.2.3 Time-based measurements

NetTime Technology can be used to determine the exact moment of a measurement that has taken place. Both the starting and end moment of the measurement can be transmitted.

1.7.9.8 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

1.7.9.9 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time
1 ms

1.8 X20(c)AI2438

1.8.1 General information

The module is equipped with 2 current measurement inputs with 16-bit digital converter resolution. It supports the HART communication standard for data transfer, parameter configuration and diagnostics.

Each current measurement input has its own sensor supply. The two channels with their respective sensor supplies are electrically isolated from each other. The user can select between the two measurement ranges 4 to 20 mA and 0 to 25 mA.

- 2 analog current measurement inputs
- Integrated HART protocol
- Supports HART variables
- Electrically isolated analog channels
- Electrically isolated sensor supplies
- 16-bit digital converter resolution
- NetTime timestamp: Moment of measurement, HART image

NetTime timestamp of the measurement

For many applications, not only the measured value is important, but also the exact time of the measurement. The module is equipped with a NetTime timestamp function for this that supplies a timestamp for the recorded position and trigger time with microsecond accuracy.

The timestamp function is based on synchronized timers. If a timestamp event occurs, the module immediately saves the current NetTime. After the respective data is transferred to the controller, including this precise moment, the controller can then evaluate the data using its own NetTime (or system time), if necessary.

1.8.1.1 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, method 4, exposure 21 days

1.8.1.1.1 Starting temperature

The starting temperature describes the minimum permissible ambient temperature in a voltage-free state at the time the coated module is switched on. This is permitted to be as low as -40°C. During operation, the conditions as specified in the technical data continue to apply.

Information:

It is important to absolutely ensure that there is no forced cooling by air currents in the closed control cabinet, e.g. due to the use of a fan or ventilation slots.

1.8.1.2 Other applicable documents

For additional and supplementary information, see the following documents.

Other applicable documents

Document name	Title
MAX20	X20 System user's manual
MAEMV	Installation / EMC guide

1.8.2 Order data

Order number	Short description	Figure
	Analog inputs	
X20AI2438	X20 analog input module, 2 inputs, 4 to 20 mA, 16-bit converter resolution, single-channel galvanically isolated and with own sensor power supply, supports HART protocol, NetTime function	
X20cAI2438	X20 analog input module, coated, 2 inputs, 4 to 20 mA, 16-bit converter resolution, single-channel galvanically isolated and with own sensor power supply, supports HART protocol, NetTime function	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 37: X20AI2438, X20cAI2438 - Order data

1.8.3 Technical description

1.8.3.1 Technical data

Order number	X20AI2438	X20cAI2438
Short description		
I/O module	2 analog inputs 4 to 20 mA or 0 to 25 mA	
General information		
B&R ID code	0xB3A9	0xE1EE
Status indicators	I/O function per channel, operating state, module status, sensor power supply per channel, HART	
Diagnostics		
Module run/error	Yes, using LED status indicator and software	
Inputs	Yes, using LED status indicator and software	
Sensor power supply	Yes, using LED status indicator and software	
HART link	Yes, using LED status indicator and software	
HART error	Yes, using LED status indicator and software	
Power consumption		
Bus	0.05 W	
Internal I/O	1.15 W [1)]	
Additional power dissipation caused by actuators (resistive) [W]	-	

Table 38: X20AI2438, X20cAI2438 - Technical data

Order number	X20AI2438	X20cAI2438
Certifications		
CE	Yes	
UKCA	Yes	
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X	
UL	cULus E115267 Industrial control equipment	
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5	
DNV	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)	
LR	ENV1	
KR	Yes	
ABS	Yes	
EAC	Yes	
KC	Yes	-
Analog inputs		
Input	4 to 20 mA or 0 to 25 mA configurable using software	
Input type	Differential input	
Digital converter resolution	16-bit	
Data output rate		
With HART	4.7 to 10 samples per second, configurable using software	
Analog	4.7 to 100 samples per second, configurable using software	
Output format	INT	
Output format		
4 to 20 mA	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 488.281 nA	
0 to 25 mA	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 762.939 nA	
0 to 25000 µA	INT 0x0000 - 0x61A8 / 1 LSB = 0x0001 = 1000 nA	
Load	I_IN ≥ 0.1 mA: R < 8000 Ω I_IN ≥ 1 mA: R < 1100 Ω I_IN ≥ 4 mA: R < 510 Ω	
Input protection	Up to 30 VDC, reverse polarity protection (max. 0.1 A)	
Open-circuit detection	Yes, using software	
Permissible input signal	0 to 25 mA	
Output of digital value during overload	Configurable	
Conversion procedure	Sigma-delta	
Max. error		
Gain		
0 to 25 mA	<0.046% [2)]	
4 to 20 mA	<0.046% [2)]	
Offset		
0 to 25 mA	<0.004% [3)]	
4 to 20 mA	<0.013% [3)]	
Common-mode rejection		
DC	80 dB	
50 Hz	Depends on the sampling rate: e.g. >130 dB for 50 samples per second	
Common-mode range	0 to 7 V	
Nonlinearity	<0.003% [3)]	
Input filter		
Hardware	First-order low-pass filter / cutoff frequency 100 Hz	
Software	Sinc⁴ filter	
Max. gain drift		
0 to 25 mA	0.003 %/°C [2)]	
4 to 20 mA	0.003 %/°C [2)]	
Max. offset drift		
0 to 25 mA	0.0002 %/°C [3)]	
4 to 20 mA	0.0007 %/°C [3)]	
Test voltage		
Channel - Channel	1000 VAC	
Channel - Bus	1000 VAC	
Channel - Ground	1000 VAC	
Sensor power supply		
Power consumption	0.75 W per channel	
Nominal voltage	25 V ±2%	
Nominal output current	Max. 30 mA	
Short-circuit proof	Yes, continuous	

Table 38: X20AI2438, X20cAI2438 - Technical data

Order number	X20AI2438	X20cAI2438
Max. voltage ripple		
Up to 100 kHz	≤2.2 mV	
Up to 1 MHz	≤22 mV	
Higher	≤100 mV	
Short-circuit current		
Typical	<50 mA	
Maximum	60 mA	
Behavior on short circuit	Current limiting	
HART		
Transfer rate	1200 bit/s	
Operating frequencies	1200 Hz / 2200 Hz	
Multi-drop operation		
Possible	Yes	
Stations	5 nodes (when using HART slaves with a nominal current of 4 mA) Up to 15 (taking into account the maximum permissible input signal of 25 mA)	
Burst operation possible	Yes	
Transmission amplitude		
Minimum	400 mV_{pp}	
Typical	500 mV_{pp}	
Maximum	600 mV_{pp}	
Receiving amplitude		
Minimum	120 mV_{pp}	
Maximum	800 mV_{pp}	
Electrical properties		
Electrical isolation	Channel isolated from channel and bus Sensor power supply isolated from sensor power supply Sensor power supply not isolated from channel	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation elevation above sea level		
0 to 2000 m	No limitation	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
Degree of protection per EN 60529	IP20	
Ambient conditions		
Temperature		
Operation		
Horizontal mounting orientation	-25 to 60°C	
Vertical mounting orientation	-25 to 50°C	
Derating	-	
Starting temperature	-	Yes, -40°C
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical properties		
Note	Order 1x terminal block X20TB12 separately. Order 1x bus module X20BM11 separately.	Order 1x terminal block X20TB12 separately. Order 1x bus module X20cBM11 separately.
Pitch	$12.5^{+0.2}$ mm	

Table 38: X20AI2438, X20cAI2438 - Technical data

1) To reduce power dissipation, B&R recommends leaving unused inputs open.
2) Based on the current measured value.
3) Based on the 25 mA measurement range.

1.8.3.2 LED status indicators

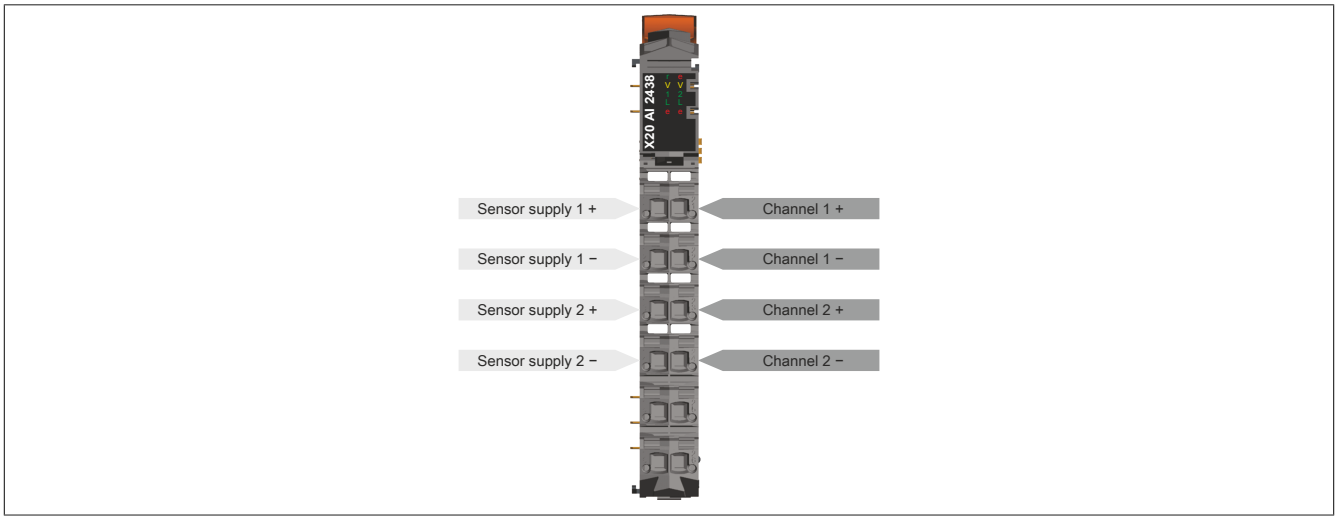
For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 System user's manual.

Figure	LED	Color	Status	Description
	**Operating state**			
	r	Green	Off	No power to module
			Single flash	UNLINK mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking quickly	SYNC mode
			Blinking slowly	Mode PREOPERATIONAL
			On	RUN mode
	Module status			
	e	Red	Off	No power to module or everything OK
			Single flash	A conversion error has occurred. This status is output along with a double flash on the channel LED of the analog input where the error occurs.
			On	Error or reset status
	Sensor supply			
	V	Yellow	Off	Module supply not connected or overload
			On	Sensor supply in its normal operating range
	Analog input			
	1 - 2	Green	Off	Indicates one of the following cases: • No power to module • Channel disabled • Open line
			Single flash	Input signal overflow or underflow
			Double flash	A conversion error has occurred. A single flash is output on the red "e" module status LED.
			On	Analog/digital converter running, value OK
	HART link			
	L	Green	Off	Indicates one of the following cases: • No power to module • HART disabled for the respective channel
			Flickering	Carrier signal active (DCD or RTS)
	HART error			
	e	Red	Off	Indicates one of the following cases: • Communication taking place without errors • No power to module • HART disabled for the respective channel
			On	Communication error

1) Depending on the configuration, a firmware update can take up to several minutes.

1.8.3.3 Pinout

Shielded twisted pair cables should be used to minimize coupling disturbances. Use either one cable for each channel or a multiple twisted pair cable for both channels.

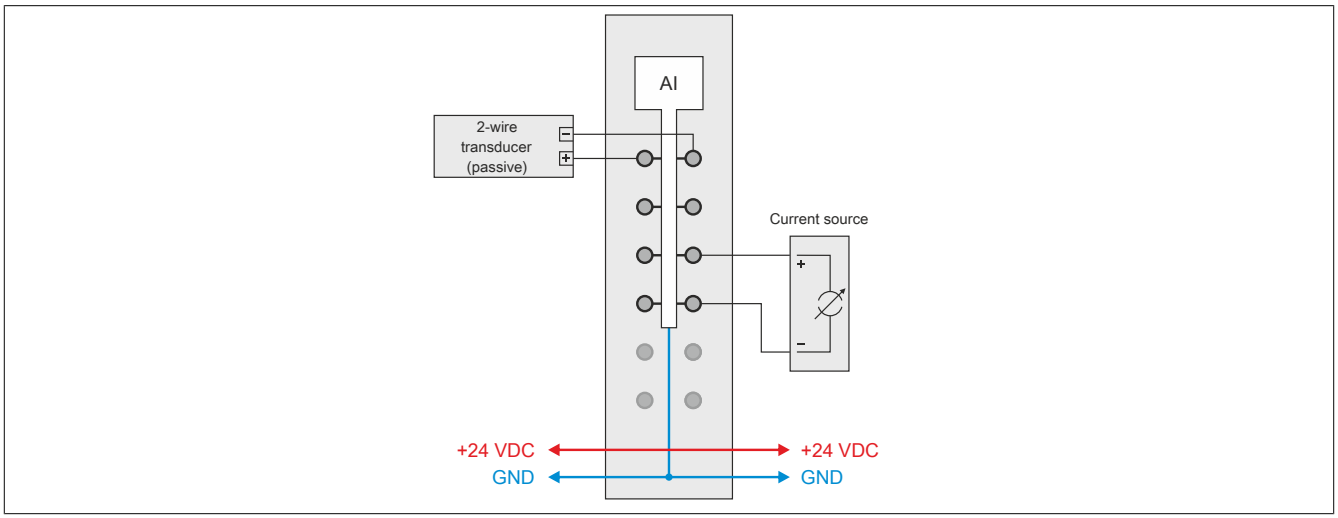


1.8.3.4 Connection examples

2-wire connections

A 2-wire connection can be implemented as follows:

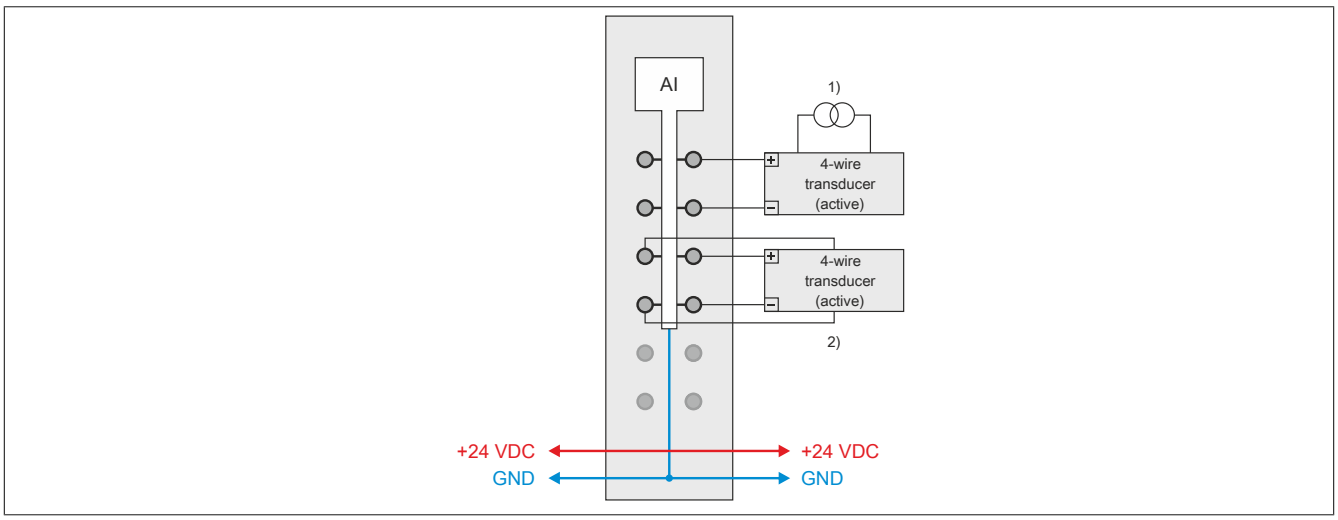
- 2-wire transducer
- Active current source



4-wire connections

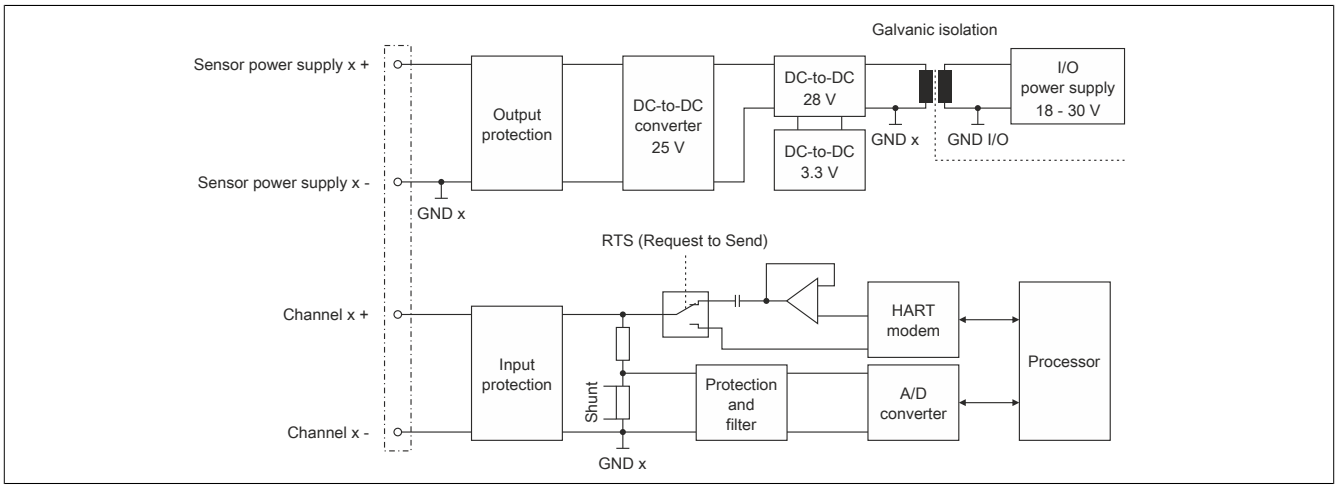
A 4-wire connection can be implemented as follows:

- 4-wire transducer with external supply
- 4-wire transducer supplied by the module



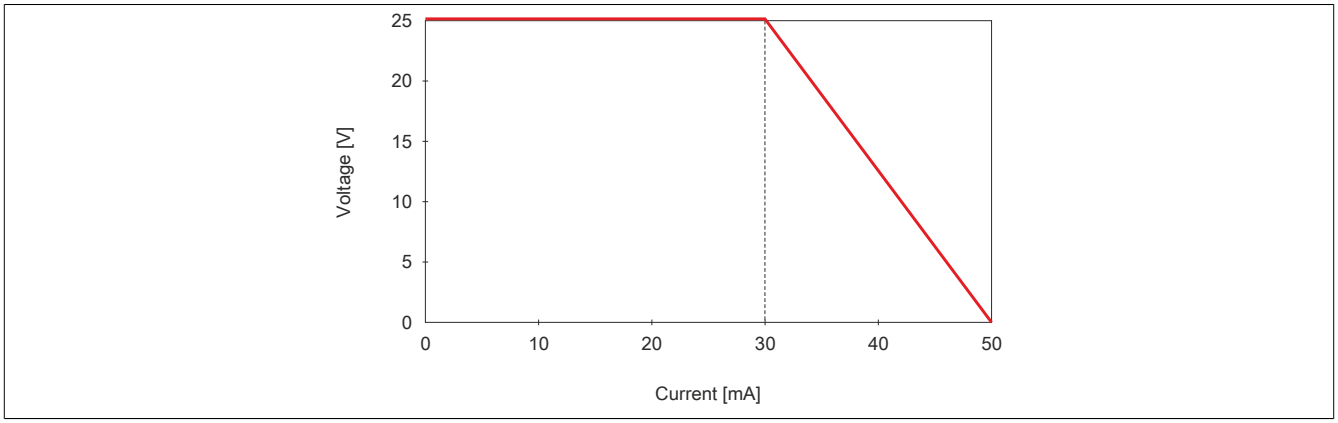
1) With external power supply.
2) With internal power supply. The internal power supply is only permitted to be loaded with max. 30 mA.

1.8.3.5 Input circuit diagram



1.8.3.6 Behavior in the event of short circuit

In the event of a short circuit, the output current for the sensor supply is limited according to the following diagram.



1.8.3.7 Usage after the X20IF1091-1

If this module is operated after X2X Link module X20IF1091-1, delays may occur during the Flatstream transfer. For detailed information, see section "Data transfer on the Flatstream" in X20IF1091-1.

1.8.4 Register description

1.8.4.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 System user's manual.

1.8.4.2 Register overview - Function model 0 (standard)

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration						
386 426	AnMode_1 AnMode_2	UINT				•
390 430	Samplerate_1 Samplerate_2	UINT				•
394 434	OpenLoopLimit_1 OpenLoopLimit_2	(U)INT				•
398 438	LowerLimit_1 LowerLimit_2	(U)INT				•
402 442	UpperLimit_1 UpperLimit_2	(U)INT				•
406 446	Hysteres_1 Hysteres_2	(U)INT				•
410 450	ReplacementLower_1 ReplacementLower_2	(U)INT				•
414 454	ReplacementUpper_1 ReplacementUpper_2	(U)INT				•
418 458	ErrorDelay_1 ErrorDelay_2	UINT				•
422 462	SumErrorDelay_1 SumErrorDelay_2	UINT				•
466 482	PreparationInterval_1 PreparationInterval_2	UINT				•
Analog signal - Communication						
266 270	AnalogInput01 (if replacement value strategy on) AnalogInput02 (if replacement value strategy on)	(U)INT	•			
258 262	AnalogInput01 (if replacement value strategy off) AnalogInput02 (if replacement value strategy off)	(U)INT	•			
282 290	AnalogSampletime01 (16-bit) AnalogSampletime02 (16-bit)	INT	•			
284 292	AnalogSampletime01 (32-bit) AnalogSampletime02 (32-bit)	DINT	•			
30 31	AnalogStatus01 AnalogStatus02	USINT	•			
	UnderflowAnalogInput01 or 02	Bit 0				
	OverflowAnalogInput01 or 02	Bit 1				
	OpenLineAnalogInput01 or 02	Bit 2				
	ConversionErrorAnalogInput01 or 02	Bit 3				
	SumErrorAnalogInput01 or 02	Bit 4				
	SensorErrorAnalogInput01 or 02	Bit 6				
	IoSuppErrorAnalogInput01 or 02	Bit 7				
HART - Configuration						
1537 1665	HartNodeCnt_1 HartNodeCnt_2	USINT				•
1539 1667	HartMode_1 HartMode_2	USINT				•
1541 1669	HartBurstNode_1 HartBurstNode_2	USINT				•
HART - Extended configuration						
1558 1686	HartNodeDisable_1 HartNodeDisable_2	UINT				•
1546 1674	HartProtTimeOut_1 HartProtTimeOut_2	UINT				•
1550 1678	HartProtRetry_1 HartProtRetry_2	UINT				•
1554 1682	HartPreamble_1 HartPreamble_2	UINT				•
HART - Communication (P2P)						
612 + N*24 1124 + N*24	PvInput01_0N (index N = 1 to 4) PvInput02_0N (index N = 1 to 4)	REAL	•	•		
617 + N*24 1129 + N*24	PvUnit01_0N (index N = 1 to 4) PvUnit02_0N (index N = 1 to 4)	USINT	•	•		
628 1140	PvSampleTime01 PvSampleTime02	DINT	•	•		

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
626 1138	PvSampleTime01 PvSampleTime02	INT	•			
566 1078	PvNodeComStatus01 PvNodeComStatus02	DINT		•		
HART - Communication (multidrop)						
612 + N*24 1124 + N*24	PvInput01_N (index N = 01 to 15) PvInput02_N (index N = 01 to 15)	REAL	•	•		
617 + N*24 1129 + N*24	PvUnit01_N (index N = 01 to 15) PvUnit02_N (index N = 01 to 15)	USINT	•	•		
604 + N*24 1116 + N*24	PvSampleTime01_N (index N = 01 to 15) PvSampleTime02_N (index N = 01 to 15)	DINT	•	•		
602 + N*24 1114 + N*24	PvSampleTime01_N (index N = 01 to 15) PvSampleTime02_N (index N = 01 to 15)	INT	•			
562 + N*4 1074 + N*4	PvNodeComStatus01_N (index N = 01 to 15) PvNodeComStatus02_N (index N = 01 to 15)	DINT		•		
HART - Extended communication						
522 1034	PvCountHartRequest01 PvCountHartRequest02	UINT	•			
530 1042	PvCountHartTimeout01 PvCountHartTimeout02	UINT	•			
538 1050	PvCountHartRxError01 PvCountHartRxError02	UINT	•			
546 1058	PvCountHartFrameError01 PvCountHartFrameError02	UINT	•			
554 1066	PvNodeFound01 PvNodeFound02	UINT	•			
558 1070	PvNodeError01 PvNodeError02	UINT	•			
Flatstream - Configuration						
1793	OutputMTU	USINT				•
1795	InputMTU	USINT				•
1797	FlatstreamMode	USINT				•
1799	Forward	USINT				•
1801	ForwardDelay	UINT				•
Flatstream - Communication						
1857	InputSequence	USINT	•			
1857 + N*2	RxByteN (index N = 1 to 15)	USINT	•			
1889	OutputSequence	USINT			•	
1889 + N*2	TxByteN (index N = 1 to 15)	USINT			•	

1.8.4.3 Register overview - Function model 254 (bus controller)

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration							
386 426	- -	AnMode_1 AnMode_2	UINT				•
390 430	- -	Samplerate_1 Samplerate_2	UINT				•
394 434	- -	OpenLoopLimit_1 OpenLoopLimit_2	(U)INT				•
398 438	- -	LowerLimit_1 LowerLimit_2	(U)INT				•
402 442	- -	UpperLimit_1 UpperLimit_2	(U)INT				•
406 446	- -	Hysteres_1 Hysteres_2	(U)INT				•
410 450	- -	ReplacementLower_1 ReplacementLower_2	(U)INT				•
414 454	- -	ReplacementUpper_1 ReplacementUpper_2	(U)INT				•
418 458	- -	ErrorDelay_1 ErrorDelay_2	UINT				•
422 462	- -	SumErrorDelay_1 SumErrorDelay_2	UINT				•
466 482	- -	PreparationInterval_1 PreparationInterval_2	UINT				•
Analog signal - Communication							
266 270	0 8	AnalogInput01 (if replacement value strategy on) AnalogInput02 (if replacement value strategy on)	(U)INT	•			
258 262	- -	AnalogInput01 (if replacement value strategy off) AnalogInput02 (if replacement value strategy off)	(U)INT		•		

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
30 31	- -	AnalogStatus01 AnalogStatus02	USINT		•		
		UnderflowAnalogInput01 or 02	Bit 0				
		OverflowAnalogInput01 or 02	Bit 1				
		OpenLineAnalogInput01 or 02	Bit 2				
		ConversionErrorAnalogInput01 or 02	Bit 3				
		SumErrorAnalogInput01 or 02	Bit 4				
		SensorErrorAnalogInput01 or 02	Bit 6				
		IoSuppErrorAnalogInput01 or 02	Bit 7				
HART - Configuration							
1537 1665	- -	HartNodeCnt_1 HartNodeCnt_2	USINT				•
1539 1667	- -	HartMode_1 HartMode_2	USINT				•
1541 1669	- -	HartBurstNode_1 HartBurstNode_2	USINT				•
HART - Extended configuration							
1558 1686	- -	HartNodeDisable_1 HartNodeDisable_2	UINT				•
1546 1674	- -	HartProtTimeOut_1 HartProtTimeOut_2	UINT				•
1550 1678	- -	HartProtRetry_1 HartProtRetry_2	UINT				•
1554 1682	- -	HartPreamble_1 HartPreamble_2	UINT				•
HART - Communication (P2P)							
636 1148	4 12	PvInput01_01 PvInput02_01	REAL	•			
612 + N*24 1124 + N*24	- -	PvInput01_0N (index N = 2 to 4) PvInput02_0N (index N = 2 to 4)	REAL		•		
641 1153	2 10	PvUnit01_01 PvUnit02_01	USINT	•			
617 + N*24 1129 + N*24	- -	PvUnit01_0N (index N = 2 to 4) PvUnit02_0N (index N = 2 to 4)	USINT		•		
566 1078	- -	PvNodeComStatus01 PvNodeComStatus02	DINT		•		
HART - Communication (multidrop)							
636 1148	4 12	PvInput01_01 PvInput02_01	REAL	•			
612 + N*24 1124 + N*24	- -	PvInput01_N (index N = 02 to 15) PvInput02_N (index N = 02 to 15)	REAL		•		
641 1153	2 10	PvUnit01_01 PvUnit02_01	USINT	•			
617 + N*24 1129 + N*24	- -	PvUnit01_N (index N = 02 to 15) PvUnit02_N (index N = 02 to 15)	USINT		•		
562 + N*4 1074 + N*4	- -	PvNodeComStatus01_N (index N = 01 to 15) PvNodeComStatus02_N (index N = 01 to 15)	DINT		•		
HART - Extended communication							
522 1034	- -	PvCountHartRequest01 PvCountHartRequest02	UINT		•		
530 1042	- -	PvCountHartTimeout01 PvCountHartTimeout02	UINT		•		
538 1050	- -	PvCountHartRxError01 PvCountHartRxError02	UINT		•		
546 1058	- -	PvCountHartFrameError01 PvCountHartFrameError02	UINT		•		
554 1066	- -	PvNodeFound01 PvNodeFound02	UINT		•		
558 1070	- -	PvNodeError01 PvNodeError02	UINT		•		

1) The offset specifies the position of the register within the CAN object.

1.8.4.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

1.8.4.3.2 CAN I/O bus controller

The module occupies 2 analog logical slots on CAN I/O.

1.8.4.4 General information

This module is equipped with two independent electrically isolated channels with integrated HART modems. Both channels can be used to read in an analog signal and handle HART communication. All registers necessary for this have a dual design so that the channels can be configured and operated independently of one another.
The current input signals (0 to 25 mA) can be displayed in various formats and used as conventional analog inputs. The integrated HART modems retrieve digital information from the memory on the HART slave using the same physical lines that modulate the HART signals.

When using the 0 to 25 mA current input variant, the module is conceived as a HART master for 2 channels (loops), with FSK modulation of the HART protocol and sensor supply for up to 15 slaves per channel.

Each channel can use one of the following connection variants:

- Connection of one HART node (point-to-point) with evaluation of the analog signal and output of 4 HART process variables OR
- Connection of up to 15 HART nodes in multidrop mode with output of the primary HART variable from activated nodes

Specific features:

- Channels electrically isolated
- Up to 15 HART input variables per channel
- Configurable sampling rate (input filter) to transfer HART and analog signal without interference (default: 50 Hz or 20 ms)
- Internal supply with short circuit protection <30 mA per channel
- Selective line monitoring can be enabled for: open line (<2 mA), underflow (<3.6 mA) or overflow (>21 mA) of a configurable threshold
- Selectable error strategy (static replacement value or retention of the last permitted value)
- Cyclic "HART status" polling (HART command 0), the status information received is made available for channel diagnostics
- Compatible with an additional secondary master in the HART network (module acts as the primary master)
- "HART communication error bit" (shows loss of HART connection if a connection had already been established successfully)
- Optional: Burst mode for one node per channel
- Optional: Cyclic polling of "HART variables" (HART command 3 or 9)
- Optional: Sensor power supply for max. 15 nodes per channel in the multidrop variant
- Optional: Flatstream functionality (module acts as bridge for HART packets)

Information:

Maximum number of HART nodes per channel:

- **5 nodes (when using HART nodes with a nominal current of 4 mA)**
- **Up to 15 HART nodes (taking into account the maximum permissible input signal or nominal output current of the sensor power supply of 25 mA)**

1.8.4.5 Analog signal - Configuration

How the analog signal is displayed can be adapted to the requirements of the application. Separate configuration registers per channel are available to aid in this.

1.8.4.5.1 Channel parameters

Name:
AnMode_1 to AnMode_2

These registers are used to predefine the operating parameters that the module will be using for the respective channel. Each channel must be enabled individually and can be configured and operated independently.

Information:

Different limit values must be configured for any display normalizing that needs to take place.

Data type	Values	Bus controller default setting
UINT	See bit structure.	29

Bit structure:

Bit	Name	Value	Information
0	Channel	0	Channel 0x turned off
		1	Channel 0x enabled (bus controller default setting)
1	Open line detection	0	Open line monitoring turned off
		1	Open circuit monitoring enabled (bus controller default setting)
2	Underflow detection	0	Underflow detection turned off
		1	Underflow detection enabled (bus controller default setting)
3	Replacement value strategy	0	Use replacement values in the event of error (bus controller default setting)
		1	Keep the last valid converted value
4 - 5	Normalization	00	Displays 0 to 25 mA as 0 to 32767
		01	Display 0 to 25 mA as 0 to 25000 [µA] (bus controller default setting)
		10	Displays 4 to 20 mA as 0 to 32767
		11	Displays 0 to 25 mA as 0 to 65535
6 - 15	Reserved	-	

1.8.4.5.2 Sample rate

Name:
Samplerate_1 to Samplerate_2

A conversion rate can be configured independently for the two analog inputs. Based on the desired sampling frequency, the following formula results for this parameter:

Sampling rate for A/D converter = (4920000 / 1024) / Sampling frequency

Data type	Value	Information
UINT	4 to 1023	Sample rate **Examples of configurable values** **Value ... Time ... Frequency** 960 ... 200 ms ... 5 Hz 480 ... 100 ms ... 10 Hz 320 ... 66.7 ms ... 15 Hz 192 ... 40 ms ... 25 Hz 160 ... 33.3 ms ... 30 Hz 96 ... 20 ms ... 50 Hz (bus controller default setting) 80 ... 16.7 ms ... 60 Hz 48 ... 10 ms ... 100 Hz 9 ... 2 ms ... 500 Hz 4 ... 1 ms ... 1000 Hz

The fastest sample rate of 10 ms for the analog inputs is predefined by the cutoff frequency of the hardware filter. When using HART communication, however, a sample rate not faster than 100 ms is recommended.

1.8.4.5.3 Limit value for open line detection

Name:
OpenLoopLimit_1 to OpenLoopLimit_2

The limit value for the respective analog input must be set when open circuit monitoring is enabled and if required by the configured normalization.

Data type	Value	Information
INT	-32767 to 32767	Open circuit limit value. Bus controller default setting: 2621
UINT	0 to 65535	Open circuit limit value

If limit value monitoring is active, the corresponding error status is output after a configured delay when falling below this value. Using a default value of 2000 µA, the following values and formulas result for this parameter:

- Displays 0 to 25 mA as 0 to 25000: 2000
- Displays 0 to 25 mA as 0 to 32767: 2621, limit value = ([µA] * 32767) / 25000
- Displays 4 to 20 mA as 0 to 32767: -4096, limit value = (([µA] * 1.31068) - 5242.72) * 1.5625
- Displays 0 to 25 mA as 0 to 65535: 5243, limit value = ([µA] * 65535) / 25000

1.8.4.5.4 Preparation time for the measured values

Name:
PreparationInterval01 to PreparationInterval02

If the last valid measured value should be kept when violating the limit value, then PreparationInterval must be defined. The measured values continue to be acquired and converted according to the configured I/O update time. They are then checked and discarded if they do not meet the specifications. When an error does not occur, therefore, the measured value acquired 2 preparation intervals ago is constantly output.

Data type	Value	Information
UINT	0 to 65535	In 0.1 ms. Bus controller default setting: 0

Functionality:
Measured values are continuously converted and stored to measured value memory. The current contents of the measured value memory are checked within the configured interval. If a permissible value is present, then the contents of the buffer memory are passed to output memory and the contents of the measured value memory are passed to the buffer.
If the check turns up an impermissible value, then the contents of the measured value memory are discarded. The copy direction between output and buffer memory reverses and the last valid value continues to be output.

Information:

If configured to keep the last valid value, the delay time from measuring to outputting the value will be at least twice the preparation interval. In the worst case scenario, this can also take twice the interval time plus the configured conversion rate of the A/D converter.

"Application" Value being measured (analog)	
↓	Condition: - Conversion interval (A/D converter) elapsed
"Measured value memory" Measured value (digital)	
↓	Condition: - PreparationInterval elapsed - Measured value permissible
"Buffer" Last valid value	
↓	Condition: - PreparationInterval elapsed - Measured value permissible
"Output memory" Next-to-last valid/ displayed value	

1.8.4.5.5 Lower replacement value

Name:
ReplacementLower_1 to ReplacementLower_2

This register is used to define the lower static values to be displayed instead of the current measured value when the lower limit is violated.

Data type	Value	Information
INT	-32767 to 32767	Bus controller default setting: 4718
UINT	0 to 65535	

If the replacement strategy "Use replacement values when an error occurs" is enabled, the replacement value must be set for the respective analog input taking the configured normalization into account as well. When an overflow or underflow error status occurs, the "AnalogInput0x" on page 202 channel is replaced with the corresponding value. Using a default value of 3600 µA, the following values and formulas result for this parameter:

- Displays 0 to 25 mA as 0 to 25000: 3600
- Displays 0 to 25 mA as 0 to 32767: 4718, limit value = ([µA] * 32767) / 25000
- Displays 4 to 20 mA as 0 to 32767: -819, limit value = (([µA] * 1.31068) - 5242.72) * 1.5625
- Displays 0 to 25 mA as 0 to 65535: 9437, limit value = ([µA] * 65535) / 25000

1.8.4.5.6 Upper replacement value

Name:
ReplacementUpper_1 to ReplacementUpper_2

These registers are used to specify the upper static values that are displayed instead of the current measured value when a limit value is exceeded.

Data type	Value	Information
INT	-32767 to 32767	Bus controller default setting: 27524
UINT	0 to 65535	

If the replacement strategy "Use replacement values when an error occurs" is activated, the replacement value must be set for the respective analog input taking the configured normalization into account as well. When an overflow or underflow error status occurs, the "AnalogInput0x" on page 202 channel is replaced with the corresponding value. Using a default value of 21000 µA, the following values and formulas result for this parameter:

- Displays 0 to 25 mA as 0 to 25000: 21000
- Displays 0 to 25 mA as 0 to 32767: 27524, limit value = ([µA] * 32767) / 25000
- Displays 4 to 20 mA as 0 to 32767: 32767, limit value = (([µA] * 1.31068) - 5242.72) * 1.5625
- Displays 0 to 25 mA as 0 to 65535: 55049, limit value = ([µA] * 65535) / 25000

1.8.4.5.7 Lower limit value

Name:
LowerLimit_1 to LowerLimit_2

If the value range needs to be restricted further, this register can be used to enter new user-specific lower limit values.

Data type	Value	Information
INT	-32767 to 32767	Bus controller default setting: 4718
UINT	0 to 65535	

The limit value must be set for the respective analog input depending on the configured normalization. After the configured delay time has passed, the corresponding error status is given if the respective value is overrun or underrun. When this error state occurs, the "AnalogInput0x" on page 202 channel is evaluated according to the replacement value strategy. Using a default value of 3600 µA, the following values and formulas result for this parameter:

- Displays 0 to 25 mA as 0 to 25000: 3600
- Displays 0 to 25 mA as 0 to 32767: 4718, limit value = ([µA] * 32767) / 25000
- Displays 4 to 20 mA as 0 to 32767: -819, limit value = (([µA] * 1.31068) - 5242.72) * 1.5625
- Displays 0 to 25 mA as 0 to 65535: 9437, limit value = ([µA] * 65535) / 25000

1.8.4.5.8 Upper limit value

Name:
UpperLimit_1 to UpperLimit_2

If the value range needs to be restricted further, this register can be used to enter new user-specific upper limit values.

Data type	Value	Information
INT	-32767 to 32767	Bus controller default setting: 27524
UINT	0 to 65535	

The limit value must be set for the respective analog input depending on the configured normalization. After the configured delay time has passed, the corresponding error status is given if the respective value is overrun or underrun. When this error state occurs, the "AnalogInput0x" on page 202 channel is evaluated according to the replacement value strategy. Using a default value of 21000 µA, the following values and formulas result for this parameter:

- Displays 0 to 25 mA as 0 to 25000: 21000
- Displays 0 to 25 mA as 0 to 32767: 27524, limit value = ([µA] * 32767) / 25000
- Displays 4 to 20 mA as 0 to 32767: 32767, limit value = (([µA] * 1.31068) - 5242.72) * 1.5625
- Displays 0 to 25 mA as 0 to 65535: 55049, limit value = ([µA] * 65535) / 25000

1.8.4.5.9 Hysteresis

Name:
Hysteres_1 to Hysteres_2

If the user-specific limit values are being used, then a hysteresis range should also be defined. These registers configure how far a limit value can be exceeded before a response is triggered.

Data type	Value	Information
INT	-32767 to 32767	Bus controller default setting: 131
UINT	0 to 65535	

The hysteresis value must be set for the respective analog input depending on the configured normalization. The error status is cleared if the actual analog value changes by at least this hysteresis value from the limit value in the allowed direction. Using a default value of 100 µA, the following values and formulas result for this parameter:

- Displays 0 to 25 mA as 0 to 25000: 100
- Displays 0 to 25 mA as 0 to 32767: 131, limit value = ([µA] * 32767) / 25000
- Displays 4 to 20 mA as 0 to 32767: 156, limit value = [µA] * 1.5625
- Displays 0 to 25 mA as 0 to 65535: 262, limit value = ([µA] * 65535) / 25000

1.8.4.5.10 Delaying error messages

Name:
ErrorDelay_1 to ErrorDelay_2

This register specifies the number of consecutive conversion procedures where an error is pending until the corresponding individual error status bit is set. The delay applies to underflow, overflow and open circuit errors. This delay can be used to hide temporary measured value deviations, for example.

Data type	Value	Information
UINT	0 to 10	Error formation delay in conversion cycles. Bus controller default setting: 2

1.8.4.5.11 Time for composite error bit

Name:
SumErrorDelay_1 to SumErrorDelay_2

This register specifies the time in milliseconds that one of the individual error bits must be pending until the composite error status bit is set.

Data type	Value	Information
UINT	0 to 65535	Composite error bit delay in ms. Bus controller default setting: 4000

1.8.4.6 Analog signal - Communication

1.8.4.6.1 Analog input values

Name:
AnalogInput01 to AnalogInput02

The analog input value is mapped in this register.

Data type	Value	Information
INT	0 to 25000	Normalizing option 0 to 25 mA
	0 to 32,767	Normalizing option 0 to 25 mA
	-8192 to 32767	Normalizing option 4 to 20 mA (value 0 corresponds to 4 mA)
UINT	0 to 65535	Normalizing option 0 to 25 mA

Predefining values and timing
If a replacement value strategy was configured, value "0" (zero) is output from the beginning until a valid measured value has been calculated.

The timing of the measured value acquisition is determined by the converter hardware and the set sampling rate. The two channels are converted independently and not synchronized with the X2X Link network.

Conversion time
Channel 0x sampling rate

1.8.4.6.2 Sample time

Name:
AnalogSampletime01 to AnalogSampletime02

These registers return the timestamp for when the module reads the current channel mapping. The values are provided as signed 2-byte or 4-byte values.

For additional information about NetTime and timestamps, see "NetTime Technology" on page 239.

Data type	Values	Information
INT	-32,768 to 32767	NetTime timestamp of the current input value in µs
DINT	-2147483648 to 2147483647	NetTime timestamp of the current input value in µs

1.8.4.6.3 Status of the inputs

Name:
AnalogStatus01 to AnalogStatus02
UnderflowAnalogInput01 to UnderflowAnalogInput02
OverflowAnalogInput01 to OverflowAnalogInput02
OpenLineAnalogInput01 to OpenLineAnalogInput02
ConversionErrorAnalogInput01 to ConversionErrorAnalogInput02
SumErrorAnalogInput01 to SumErrorAnalogInput02
SensorErrorAnalogInput01 to SensorErrorAnalogInput02
IoSuppErrorAnalogInput01 to IoSuppErrorAnalogInput02

The current error state of the module channels is indicated in this register regardless of the configured replacement value strategy. Some error information is delayed according to the previously configured condition.

Setting "Format of status information" makes it possible to define in Automation Studio whether the status information is transferred as USINT or bitwise.

Data type	Values
USINT	See bit structure.

Bit structure:

Bit	Name	Values	Information
0	UnderflowAnalogInput01 or 02	0	No error
		1	Lower limit value undershot
1	OverflowAnalogInput01 or 02	0	No error
		1	Upper limit value overshot
2	OpenLineAnalogInput01 or 02	0	No error
		1	Open circuit determined
3	ConversionErrorAnalogInput01 or 02	0	No error
		1	Conversion error determined
4	SumErrorAnalogInput01 or 02	0	No error
		1	Composite error determined
5	Reserved	-	
6	SensorErrorAnalogInput01 or 02	0	Sensor voltage OK
		1	Sensor load too high
7	IoSuppErrorAnalogInput01 or 02	0	I/O power supply OK
		1	Error in I/O power supply determined

UnderflowAnalogInput

The signal underflow error state is represented here based on the configuration. This error information is enabled as a multiple of the conversion cycles only after the configurable delay time has passed (see register "ErrorDelay" on page 201).

OverflowAnalogInput

The signal overflow error status state is represented here based on the configuration. This error information is enabled as a multiple of the conversion cycles only after the configurable delay time has passed (see register "ErrorDelay" on page 201).

OpenLineAnalogInput

Based on the configuration, the measurement information is checked for values <2 mA (register "OpenLoopLimit" on page 199) to detect a failure signal. Open circuit detection is performed using a configurable hysteresis value (default: 100 µA, register "Hysteresis" on page 201). It is possible to disable open circuit detection (register "AnalogMode" on page 198) to suppress the generation of alarms when hardware is missing. This error information is enabled as a multiple of the conversion cycles only after the configurable delay time has passed (register "ErrorDelay" on page 201).

ConversionErrorAnalogInput

This error state is triggered when the hardware overshoots the conversion time.

SumErrorAnalogInput

This error information is derived from the state of individual errors and enabled only after the configurable delay time has passed [ms] (see register "SumErrorDelay" on page 201). Linking this error information in an application makes it possible to hide temporary overshoots or undershoots of the temperature value, for example.

SensorErrorAnalogInput

This error is enabled immediately after a fault is detected in the internal sensor power supply.

IoSuppErrorAnalogInput

This error is enabled immediately after a supply voltage undershoot is detected (<20 VDC).

1.8.4.7 HART

HART (Highway Addressable Remote Transducer) is a protocol for communicating with intelligent field devices. It was developed in order to more efficiently use the infrastructure for transferring analog signals. The digital HART notifications are modulated to the analog signal using Frequency Shift Keying (FSK). HART can thus use the same physical line as the analog signal without influencing the original function.
HART slaves are able to determine different process data independently and prepare HART concordantly. This protocol supports polling of the value of a process variable as well as its unit and status. Field devices usually supply their information after the master requests it. In newer revisions, it is also possible to transfer configuration data.

There are 2 different types of HART networks. In a *point-to-point* network, only one slave is connected to a HART master. Here, the analog signal and the HART signal can be transferred over the same line. Managing several slaves with HART requires what is known as a *multidrop* network. Here, each HART slave is assigned and identified by a unique address. Classic analog signals cannot be clearly traced in bus systems. As a result, the HART protocol does not support analog information transfers in multidrop networks up to and including HART Revision 5.

1.8.4.7.1 HART - Configuration

HART modules are analog modules equipped with a HART modem. For each channel, a separate HART network can be managed by the module, which acts as a primary master. Once configured successfully, the HART information is stored in the module where it can then be used by the PLC.

The number of HART slaves must be specified in the configuration.
If only one slave is connected to the HART channel, then it is part of a point-to-point network. The module can then prepare up to 4 process variables from the connected slave.
Multidrop mode allows up to 15 HART slaves to be connected. The primary process variable from each slave is then retrieved.

1.8.4.7.1.1 HartBurstNode

Name:
HartBurstNode_1 to HartBurstNode_2

In addition to the type of network, the user can also choose from 2 different types of communication behavior. Conventional HART communication relies on polling. The module queries the data from the HART slave individually and receives the corresponding information from the slave as a response. If a HART node should be queried in short time intervals, the user can configure burst mode for a node on each channel. In this case, the slave transmits the information from this node cyclically without a new request by the master.
The node numbers (short address) whose information should be queried using burst mode are entered by channel in the "HartBurstNode" registers. Burst mode is enabled using register "HartMode" on page 205.

Data type	Value	Information
USINT	0 to 15	Point-to-point. Bus controller default setting: 0

1.8.4.7.1.2 HartMode

Name:
HartMode_1 to HartMode_2

The user can use these registers to configure the communication behavior of each of the HART channels. Generally, the HART nodes are polled individually. This register can still be used to start or stop burst mode when needed. In burst mode, a node transmits its information cyclically instead of continuously. As a result, the HART standard allows the simultaneous usage of both burst mode and polling.

Information:

Register "HartBurstNode" on page 204 must be configured correctly for burst queries.

Data type	Values	Bus controller default setting
UINT	See bit structure.	0

Bit structure:

Bit	Name	Value	Information
0	Slave polling mode	0	Polling mode enabled (bus controller default setting)
		1	Polling mode disabled
1	Start slave burst mode	0	No response to burst (bus controller default setting)
		1	Enables burst mode in the "HartBurstNode" on page 204 node
2	Stop slave burst mode	0	No response to burst (bus controller default setting)
		1	Disables burst mode, if enabled
3 - 7	Reserved	-	

1.8.4.7.1.3 HartNodeCnt

Name:
HartNodeCnt_1 to HartNodeCnt_2

These registers tell the module how many HART slaves are connected to a channel.

Information:

If a slave is not connected to one of the HART channels, the value "0" should be defined in this register. This shortens the I/O update time and avoids superfluous error messages.

Data type	Value	Information	
USINT	0	HART communication disabled for this channel	
	1	Point-to-point	Standard HART communication (bus controller default setting)
	2 to 15	Multidrop	Number of HART slave nodes

1.8.4.7.2 HART - Communication

After the configuration is completed, the information is retrieved automatically and transferred to the module registers. A separate register is implemented in the module for each piece of information. HART modules are designed to query up to 15 pieces of information per channel. The module reads in the data, stores it in temporary memory and prepares it for retrieval. When the X2X master accesses the module registers, it is irrelevant whether the HART data originates from a point-to-point or multidrop network.

Overview of internal module mapping

	Point-to-point network (1 HART slave)	*Multidrop network (2 to 15 HART slaves)*
(Pv)Input_01	Primary piece of information from HART node 1	Primary piece of information from HART node 1
(Pv)Input_02	Secondary piece of information from HART node 1	Primary piece of information from HART node 2
...	...	...
(Pv)Input_04	Quaternary piece of information from HART node 1	Primary piece of information from HART node 4
(Pv)Input_05	Reserved	Primary piece of information from HART node 5
...	...	...
(Pv)Input_15	Reserved	Primary piece of information from HART node 15

The HART specifications stipulates that information from a HART node be split into various pieces. The value of a process variable is stored to the respective "PvInput" on page 206 register and has a size of 4 bytes (REAL) per the HART specification. Due to the length limitation of 30 bytes on the X2X Link network, there are limitations to the number of possible cyclic variables. It is recommended to transfer a maximum of 2 "PvInput" on page 206 registers cyclically to the X2X master. All other information should be read in a different way. To access HART information, the user can choose between the following methods:

- **Acyclic** - If library AsIOAcc is used, information is queried acyclically only when it is needed, i.e. communication can be adapted to the program sequence of the X2X master. In this way, all of the necessary module registers on the X2X Link network can be queried despite the length limitation.
  This type of information exchange is not real-time capable.
- **Cyclic:** Data points configured for cyclic transfer are read once per bus cycle. This procedure allows real-time capable information exchange between the module and X2X master. The length limitation may prevent all data from being queried within one cycle, however.
- **Multiplexed** - A runtime driver can be used to transfer the HART data points in the I/O mapping. In this case, the HART process data is transmitted alternately (time multiplexed). Communication remains real-time capable. Multiple bus cycles are needed to update all data points, however.

  > **Information:**
  >
  > **This mode cannot be used when using the module after a bus controller.**
  >
  > **"Multiplexed" data transfer is used exclusively for HART data points.**
  >
  > **Information from the analog inputs/outputs is always transferred cyclically (see above).**

- **Flatstream** - HART modules are equipped with a Flatstream interface. When using Flatstream communication, the module is used as a bridge between the X2X master and HART slave, i.e. the X2X master communicates directly with the HART slave (see "Flatstream communication" on page 214).
  Flatstream communication is also not real-time capable. It allows unrestricted access to the HART slave. The user must have sufficient knowledge of the HART protocol command set as well as the capabilities of the corresponding HART slave.

1.8.4.7.2.1 PvInput

Name:
PvInput01_01 to PvInput01_15
PvInput02_01 to PvInput02_15

These registers return the current value of the process variable that has been read.

> **Information:**
>
> **These registers are of data type REAL, which means that the available bytes on the X2X Link are filled more quickly when operated cyclically. If information from several slave nodes is needed, it must be retrieved acyclically or using Flatstream .**

Data type	Value	Information
REAL	IEEE745 SPF	32-bit data type with valid value
	0x7FA00000	Not a number (NaN) with invalid value

1.8.4.7.2.2 PvUnit

Name:
PvUnit01_01 to PvUnit01_15
PvUnit02_01 to PvUnit02_15

These registers return a HART-specific code that specifies the unit for the measured value. The coding for this is established in the HART specification.

Data type	Value
USINT	See description of the HART slave See HART specification

1.8.4.7.2.3 PvSampleTime

Name:
PvSampleTime01 to PvSampleTime02
PvSampleTime01_01 to PvSampleTime01_15
PvSampleTime02_01 to PvSampleTime02_15

These registers return the timestamp for when the module reads the current channel mapping. The values are provided as signed 2-byte or 4-byte values.

For additional information about NetTime and timestamps, see "NetTime Technology" on page 239.

Data type	Values	Information
INT	-32,768 to 32767	NetTime timestamp of the current input value in µs
DINT	-2147483648 to 2147483647	NetTime timestamp of the current input value in µs

This refers to the point in time when the HART master receives the slave's response. This is a way to check whether new HART information has been read since the last X2X cycle.

Information:

The cycle times of a HART network are relatively long so that it is not possible to reliably determine when the measured value is retrieved with just this information.

1.8.4.7.2.4 PvNodeComStatus

Name:
PvNodeComStatus01 to PvNodeComStatus02
PvNodeComStatus01_01 to PvNodeComStatus01_15
PvNodeComStatus02_01 to PvNodeComStatus02_15

These registers provide information about whether a read value is valid. Per the HART specification, this type of status register consists of 2 parts. The "response code" is stored in the high byte; the "field device status" is stored in the low byte. This makes it possible to check the current state of a read process variable.

These registers can be checked before further processing information in temporary storage. If the current value is 0x0000, an error was not detected during the HART transfer and the information from the checked node can be used. If a different value is present, the situation in the HART network should be checked. This can be done using an extension register, for example.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Quality - Node information 2 to n	0	Digital measured value okay
		1	Measured value outside the permissible operating range
1	Quality - Node information 1	0	Digital measured value okay
		1	Measured value outside the permissible operating range
2	Limit violation	0	Parameter okay
		1	Invalid measured value(s) or encoder supply value
3	Static analog signal	0	Normal value change/fluctuation
		1	Constant analog value of Node 1 slave
4	Additional status information (only supported by a few slaves)	0	Not available
		1	Available (only using Flatstream command #48)
5	Restart	0	Normal operation
		1	Field device restarts
6	Device ID	0	Unchanged
		1	Changed
7	Device error	0	Measured value okay
		1	Questionable measured value information
8 - 14	Response code, if relevant	x	See **HART-specific response code**
15	Error - Communication	0	Error-free communication (response code irrelevant)
		1	Faulty communication (response code relevant)

HART-specific response code (excerpt):

0x82 … Receive buffer overflow 0x88 … Checksum incorrect 0x90 … Faulty protocol structure 0xA0 … Overrun 0xC0 … Parity not allowed 0xFF … Timeout	If a HART communication error occurs, the response code is written. Bit 15 is always set.

Retrieving information that has been read

After the node data has been transferred to the module registers, the information can be retrieved from the module. A separate register in the module is implemented for each piece of information.

1.8.4.7.2.5 PvCountHartRequest

Name:
PvCountHartRequest01 to PvCountHartRequest02

This register is increased as soon as the module is ready to transmit a message on the corresponding channel.

Data type	Value
UINT	0 to 65535

1.8.4.7.2.6 PvCountHartTimeout

Name:
PvCountHartTimeout01 to PvCountHartTimeout02

This register is increased if the slave exceeds the maximum permissible time to respond a request from the module.

Data type	Value
UINT	0 to 65535

1.8.4.7.2.7 PvCountHartRxError

Name:
PvCountHartRxError01 to PvCountHartRxError02

This register is increased if communication errors occur on layer 1 of the OSI model (e.g. transfer error according to the parity bit).

Data type	Value
UINT	0 to 65535

1.8.4.7.2.8 PvCountHartFrameError

Name:
PvCountHartFrameError01 to PvCountHartFrameError02

This register is increased if communication errors occur on layer 2 of the OSI model (e.g. invalid telegram structure).

Data type	Value
UINT	0 to 65535

1.8.4.7.2.9 PvNodeFound

Name:
PvNodeFound01 to PvNodeFound02

These registers provide information about which nodes were detected on which channel (slave identified successfully).

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Node 0 (default mode) Node 1 (multidrop mode)	0	Not detected as valid
		1	Detected as valid
1	Node 2 (multidrop mode)	0	Not detected as valid
		1	Detected as valid
...		...	
13	Node 14 (multidrop mode)	0	Not detected as valid
		1	Detected as valid
14	Node 15 (multidrop mode)	0	Not detected as valid
		1	Detected as valid
15	Reserved	-	

1.8.4.7.2.10 PvNodeError

Name:
PvNodeError01 to PvNodeError02

These registers contain the HART communications error bits. These bits are set if the connection to a node was established successfully but the node at some point no longer responds as it should (e.g. the HART slave exceeds the configured timeout / number of retries).

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Node 0 (default mode) Node 1 (multidrop mode)	0	Detected as having no errors
		1	Detected as having errors
1	Node 2 (multidrop mode)	0	Detected as having no errors
		1	Detected as having errors
...		...	
13	Node 14 (multidrop mode)	0	Detected as having no errors
		1	Detected as having errors
14	Node 15 (multidrop mode)	0	Detected as having no errors
		1	Detected as having errors
15	Reserved	-	

1.8.4.7.3 Extended configuration

The additional configuration registers are specified values when the module is started. In most systems, the user does not need to make any adjustments here. Register values should only be changed if HART network communication is not taking place satisfactorily.

1.8.4.7.3.1 HartNodeDisable

Name:
HartNodeDisable_1 to HartNodeDisable_2

These registers are intended for things like maintenance. They make it possible to cut off configured HART nodes to suppress error messages for a certain period of time. During normal operation, the configured nodes must be switched active to guarantee that the procedure runs smoothly.

Data type	Values	Bus controller default setting
UINT	See bit structure.	0x3FFF

Bit structure:

Bit	Name	Value	Information
0	Node 0 (default mode) Node 1 (multidrop mode)	0	Enabled (bus controller default setting)
		1	Disabled
1	Node 2 (multidrop mode)	0	Enabled
		1	Disabled (bus controller default setting)
...		...	
13	Node 14 (multidrop mode)	0	Enabled
		1	Disabled (bus controller default setting)
14	Node 15 (multidrop mode)	0	Enabled
		1	Disabled (bus controller default setting)
15	Reserved	-	

1.8.4.7.3.2 HartProtTimeOut

Name:
HartProtTimeOut_1 to HartProtTimeOut_2

These registers specify the time span within which the slave must respond for the response to be valid.

Data type	Values [ms]	Information
UINT	0 to 65535	Bus controller default setting: 256 [ms]

1.8.4.7.3.3 HartProtRetry

Name:
HartProtRetry_1 to HartProtRetry_2

These registers determine how many times the master retries a request if it receives an invalid response or no response at all.

Data type	Value	Information
UINT	0 to 65535	Bus controller default setting: 3 attempts

1.8.4.7.3.4 HartPreamble

Name:
HartPreamble_1 to HartPreamble_2

The length of the preamble can be set in these registers. The preamble is used to synchronize the receiver to the transmitter. The longer the declared preamble, the less chance that a communication error will occur. Nevertheless, a useful signal is not transmitted during synchronization so the preamble should be kept as short as possible.

Data type	Value	Information
UINT	5 to 20	Bus controller default setting: 20

1.8.4.7.4 HART with Flatstream

When using Flatstream communication, the module acts as a bridge between the X2X master and an intelligent field device connected to the module. Flatstream mode can be used for either point-to-point connections as well as for multidrop systems. Specific algorithms such as timeout and checksum monitoring are usually managed automatically. During normal operation, the user does not have access to these details.

HART is considered a master-slave network where half-duplex communication takes place asynchronously. Various features have been included to ensure that signals are transmitted without errors.
For example, the user can increase the length of the preamble, thus making the transmission more secure. However, this also has an effect on the percentage of payload data and overhead.

Additional information about HART can be found at www.HARTcomm.org.

How it works

The module has 2 independent channels. When using Flatstream , the channel number must therefore be specified. The general structure of a Flatstream frame is extended as follows.

Input/Output sequence	Tx/Rx bytes		
(unchanged)	Control byte (unchanged)	Channel number	HART frame (without preamble and checksum)

HART frame with Flatstream					
Startup	ADDR	CMD	BCNT	(STS)	(DATA)

Startup Start identification
ADDR Address within the HART network
CMD HART command
BCNT Byte counters (number of remaining bytes)
*STS Status of the last command received. Information about the working mode of the HART Slave and communication errors (if supported, return data from the HART Slave)
*DATA Data (if necessary for the command)

Examples of HART commands

Command	Function
0x00	Read slave ID
0x03	Read current value and up to 4 variables
0x09	Read up to 4 variables including status
0x21	Read variables

1.8.4.8 Flatstream registers

At the absolute minimum, registers "InputMTU" and "OutputMTU" must be set. All other registers are filled in with default values at the beginning and can be used immediately. These registers are used for additional options, e.g. to transfer data in a more compact way or to increase the efficiency of the general procedure.

Information:

For detailed information about Flatstream, see "Flatstream communication" on page 214.

1.8.4.8.1 Number of enabled Tx and Rx bytes

Name:
OutputMTU
InputMTU

These registers define the number of enabled Tx or Rx bytes and thus also the maximum size of a sequence. The user must consider that the more bytes made available also means a higher load on the bus system.

Data type	Values
USINT	See the register overview.

1.8.4.8.2 Transporting payload data and control bytes

Name:
TxByte1 to TxByteN
RxByte1 to RxByteN

(The value the number N is different depending on the bus controller model used.)

The Tx and Rx bytes are cyclic registers used to transport the payload data and the necessary control bytes. The number of active Tx and Rx bytes is taken from the configuration of registers "OutputMTU" and "InputMTU", respectively.

- "T" - "Transmit" → Controller *transmits* data to the module.
- "R" - "Receive" → Controller *receives* data from the module.

Data type	Values
USINT	0 to 255

1.8.4.8.3 Communication status of the controller

Name:
OutputSequence

This register contains information about the communication status of the controller. It is written by the controller and read by the module.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	OutputSequenceCounter	0 - 7	Counter for the sequences issued in the output direction
3	OutputSyncBit	0	Output direction (disable)
		1	Output direction (enable)
4 - 6	InputSequenceAck	0 - 7	Mirrors InputSequenceCounter
7	InputSyncAck	0	Input direction not ready (disabled)
		1	Input direction ready (enabled)

OutputSequenceCounter

The OutputSequenceCounter is a continuous counter of sequences that have been issued by the controller. The controller uses OutputSequenceCounter to direct the module to accept a sequence (the output direction must be synchronized when this happens).

OutputSyncBit

The controller uses OutputSyncBit to attempt to synchronize the output channel.

InputSequenceAck

InputSequenceAck is used for acknowledgment. The value of InputSequenceCounter is mirrored if the controller has received a sequence successfully.

InputSyncAck

The InputSyncAck bit acknowledges the synchronization of the input channel for the module. This indicates that the controller is ready to receive data.

1.8.4.8.4 Communication status of the module

Name:
InputSequence

This register contains information about the communication status of the module. It is written by the module and should only be read by the controller.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	InputSequenceCounter	0 - 7	Counter for sequences issued in the input direction
3	InputSyncBit	0	Not ready (disabled)
		1	Ready (enabled)
4 - 6	OutputSequenceAck	0 - 7	Mirrors OutputSequenceCounter
7	OutputSyncAck	0	Not ready (disabled)
		1	Ready (enabled)

InputSequenceCounter

The InputSequenceCounter is a continuous counter of sequences that have been issued by the module. The module uses InputSequenceCounter to direct the controller to accept a sequence (the input direction must be synchronized when this happens).

InputSyncBit

The module uses InputSyncBit to attempt to synchronize the input channel.

OutputSequenceAck

OutputSequenceAck is used for acknowledgment. The value of OutputSequenceCounter is mirrored if the module has received a sequence successfully.

OutputSyncAck

The OutputSyncAck bit acknowledges the synchronization of the output channel for the controller. This indicates that the module is ready to receive data.

1.8.4.8.5 Flatstream mode

Name:
FlatstreamMode

A more compact arrangement can be achieved with the incoming data stream using this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	MultiSegmentMTU	0	Not allowed (default)
		1	Permitted
1	Large segments	0	Not allowed (default)
		1	Permitted
2 - 7	Reserved		

1.8.4.8.6 Number of unacknowledged sequences

Name:
Forward

With register "Forward", the user specifies how many unacknowledged sequences the module is permitted to transmit.

Recommendation:
X2X Link: Max. 5
POWERLINK: Max. 7

Data type	Values
USINT	1 to 7 Default: 1

1.8.4.8.7 Delay time

Name:
ForwardDelay

This register is used to specify the delay time in microseconds.

Data type	Values
UINT	0 to 65535 [µs] Default: 0

1.8.4.9 Flatstream communication

1.8.4.9.1 Introduction

B&R offers an additional communication method for some modules. "Flatstream" was designed for X2X and POWERLINK networks and allows data transfer to be adapted to individual demands. Although this method is not 100% real-time capable, it still allows data transfer to be handled more efficiently than with standard cyclic polling.

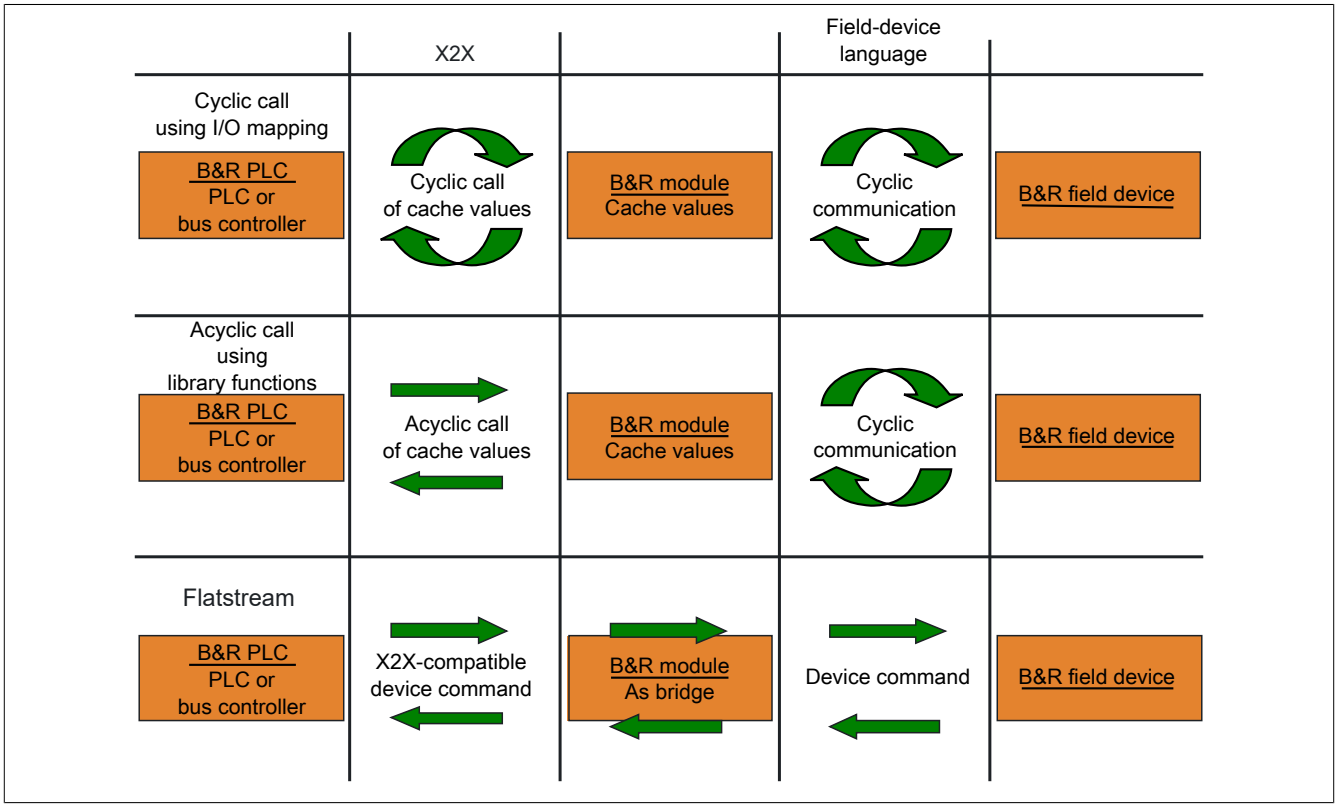


Figure 13: 3 types of communication

Flatstream extends cyclic and acyclic data queries. With Flatstream communication, the module acts as a bridge. The module is used to pass controller requests directly on to the field device.

1.8.4.9.2 Message, segment, sequence, MTU

The physical properties of the bus system limit the amount of data that can be transmitted during one bus cycle. With Flatstream communication, all messages are viewed as part of a continuous data stream. Long data streams must be broken down into several fragments that are sent one after the other. To understand how the receiver puts these fragments back together to get the original information, it is important to understand the difference between a message, a segment, a sequence and an MTU.

Message

A message refers to information exchanged between 2 communicating partner stations. The length of a message is not restricted by the Flatstream communication method. Nevertheless, module-specific limitations must be considered.

Segment (logical division of a message):

A segment has a finite size and can be understood as a section of a message. The number of segments per message is arbitrary. So that the recipient can correctly reassemble the transferred segments, each segment is preceded by a byte with additional information. This control byte contains information such as the length of a segment and whether the approaching segment completes the message. This makes it possible for the receiving station to interpret the incoming data stream correctly.

Sequence (how a segment must be arranged physically):

The maximum size of a sequence corresponds to the number of enabled Rx or Tx bytes (later: "MTU"). The transmitting station splits the transmit array into valid sequences. These sequences are then written successively to the MTU and transferred to the receiving station where they are lined up together again. The receiver stores the incoming sequences in a receive array, obtaining an image of the data stream in the process.
With Flatstream communication, the number of sequences sent are counted. Successfully transferred sequences must be acknowledged by the receiving station to ensure the integrity of the transfer.

MTU (Maximum Transmission Unit) - Physical transport:

MTU refers to the enabled USINT registers used with Flatstream. These registers can accept at least one sequence and transfer it to the receiving station. A separate MTU is defined for each direction of communication. OutputMTU defines the number of Flatstream Tx bytes, and InputMTU specifies the number of Flatstream Rx bytes. The MTUs are transported cyclically via the X2X Link network, increasing the load with each additional enabled USINT register.

Properties

Flatstream messages are not transferred cyclically or in 100% real time. Many bus cycles may be needed to transfer a particular message. Although the Rx and Tx registers are exchanged between the transmitter and the receiver cyclically, they are only processed further if explicitly accepted by register "InputSequence" or "OutputSequence".

Behavior in the event of an error (brief summary)

The protocol for X2X and POWERLINK networks specifies that the last valid values should be retained when disturbances occur. With conventional communication (cyclic/acyclic data queries), this type of error can generally be ignored.
In order for communication to also take place without errors using Flatstream, all of the sequences issued by the receiver must be acknowledged. If Forward functionality is not used, then subsequent communication is delayed for the length of the disturbance.
If Forward functionality is being used, the receiving station receives a transmission counter that is incremented twice. The receiver stops, i.e. it no longer returns any acknowledgments. The transmitting station uses SequenceAck to determine that the transfer was faulty and that all affected sequences must be repeated.

1.8.4.9.3 The Flatstream principle

Requirement

Before Flatstream can be used, the respective communication direction must be synchronized, i.e. both communication partners cyclically query the sequence counter on the remote station. This checks to see if there is new data that should be accepted.

Communication

If a communication partner wants to transmit a message to its remote station, it should first create a transmit array that corresponds to Flatstream conventions. This allows the Flatstream data to be organized very efficiently without having to block other important resources.

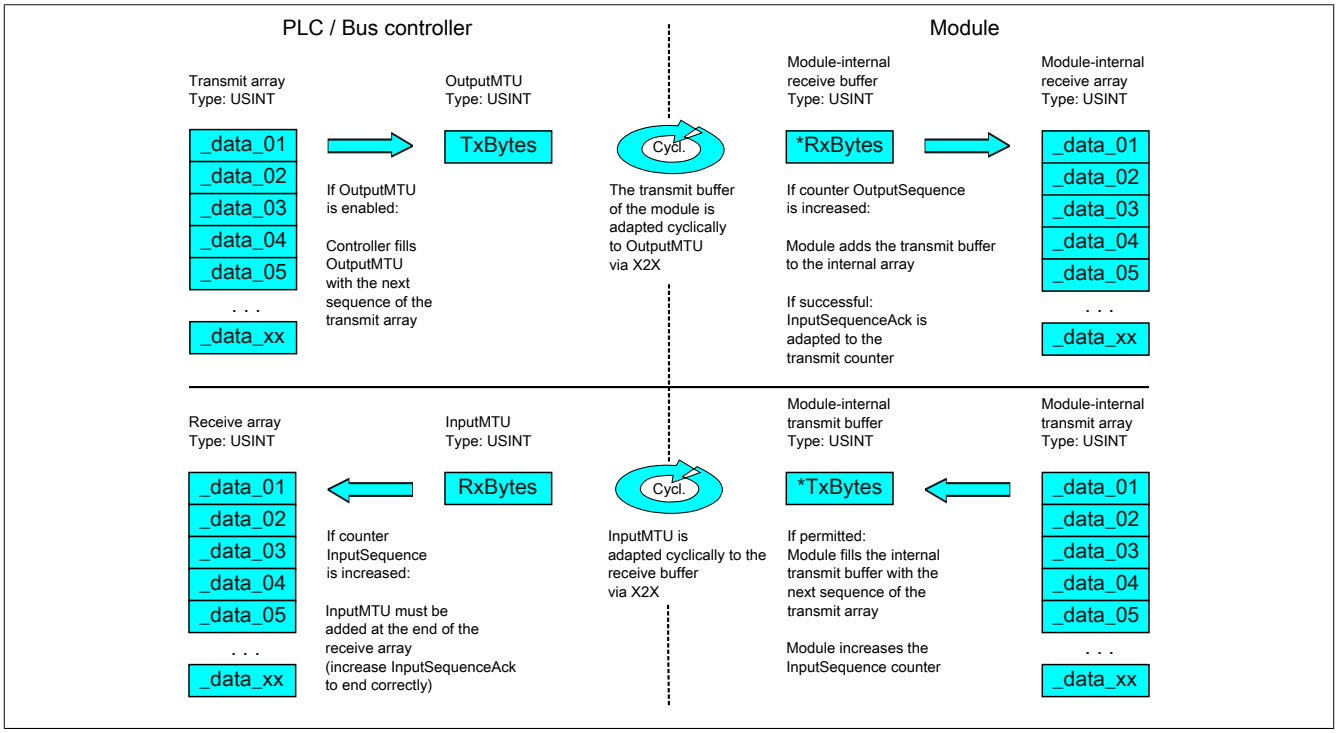


Figure 14: Flatstream communication

Procedure

The first thing that happens is that the message is broken into valid segments of up to 63 bytes, and the corresponding control bytes are created. The data is formed into a data stream made up of one control bytes per associated segment. This data stream can be written to the transmit array. The maximum size of each array element matches that of the enabled MTU so that one element corresponds to one sequence.
If the array has been completely created, the transmitter checks whether the MTU is permitted to be refilled. It then copies the first element of the array or the first sequence to the Tx byte registers. The MTU is transported to the receiver station via X2X Link and stored in the corresponding Rx byte registers. To signal that the data should be accepted by the receiver, the transmitter increases its SequenceCounter.
If the communication direction is synchronized, the remote station detects the incremented SequenceCounter. The current sequence is appended to the receive array and acknowledged by SequenceAck. This acknowledgment signals to the transmitter that the MTU can now be refilled.

If the transfer is successful, the data in the receive array will correspond 100% to the data in the transmit array. During the transfer, the receiving station must detect and evaluate the incoming control bytes. A separate receive array should be created for each message. This allows the receiver to immediately begin further processing of messages that are completely transferred.

1.8.4.9.4 Registers for Flatstream mode

5 registers are available for configuring Flatstream. The default configuration can be used to transmit small amounts of data relatively easily.

Information:

The controller communicates directly with the field device via registers "OutputSequence" and "InputSequence" as well as the enabled Tx and RxBytes bytes. For this reason, the user must have sufficient knowledge of the communication protocol being used on the field device.

1.8.4.9.4.1 Flatstream configuration

To use Flatstream, the program sequence must first be expanded. The cycle time of the Flatstream routines must be set to a multiple of the bus cycle. Other program routines should be implemented in Cyclic #1 to ensure data consistency.

At the absolute minimum, registers "InputMTU" and "OutputMTU" must be set. All other registers are filled in with default values at the beginning and can be used immediately. These registers are used for additional options, e.g. to transfer data in a more compact way or to increase the efficiency of the general procedure.

The Forward registers extend the functionality of the Flatstream protocol. This functionality is useful for substantially increasing the Flatstream data rate, but it also requires quite a bit of extra work when creating the program sequence.

Information:

In the rest of this description, the names "OutputMTU" and "InputMTU" do not refer to the registers names. Instead, they are used as synonyms for the currently enabled Tx or Rx bytes.

Information:

Registers are described in section "Flatstream registers" on page 211.

1.8.4.9.4.2 Flatstream operation

When using Flatstream, the communication direction is very important. For transmitting data to a module (output direction), Tx bytes are used. For receiving data from a module (input direction), Rx bytes are used.
Registers "OutputSequence" and "InputSequence" are used to control or secure communication, i.e. the transmitter uses them to give instructions to apply data and the receiver confirms a successfully transferred sequence.

Information:

Registers are described in section "Flatstream registers" on page 211.

Format of input and output bytes

Name:

"Format of Flatstream" in Automation Studio

On some modules, this function can be used to set how the Flatstream input and output bytes (Tx or Rx bytes) are transferred.

- **Packed:** Data is transferred as an array.
- **Byte-by-byte:** Data is transferred as individual bytes.

Transport of payload data and control bytes

The Tx and Rx bytes are cyclic registers used to transport the payload data and the necessary control bytes. The number of active Tx and Rx bytes is taken from the configuration of registers "OutputMTU" and "InputMTU", respectively.
In the user program, only the Tx and Rx bytes from the controller can be used. The corresponding counterparts are located in the module and are not accessible to the user. For this reason, the names were chosen from the point of view of the controller.

- "T" - "Transmit" → Controller *transmits* data to the module.
- "R" - "Receive" → Controller *receives* data from the module.

Control bytes

In addition to the payload data, the Tx and Rx bytes also transfer the necessary control bytes. These control bytes contain additional information about the data stream so that the receiver can reconstruct the original message from the transferred segments.

Bit structure of a control byte

Bit	Name	Value	Information
0 - 5	SegmentLength	0 - 63	Size of the subsequent segment in bytes (default: Max. MTU size - 1)
6	nextCBPos	0	Next control byte at the beginning of the next MTU
		1	Next control byte directly after the end of the current segment
7	MessageEndBit	0	Message continues after the subsequent segment
		1	Message ended by the subsequent segment

SegmentLength

The segment length lets the receiver know the length of the coming segment. If the set segment length is insufficient for a message, then the information must be distributed over several segments. In these cases, the actual end of the message is detected using bit 7 (control byte).

Information:

The control byte is not included in the calculation to determine the segment length. The segment length is only derived from the bytes of payload data.

nextCBPos

This bit indicates the position where the next control byte is expected. This information is especially important when using option "MultiSegmentMTU".
When using Flatstream communication with MultiSegmentMTUs, the next control byte is no longer expected in the first Rx byte of the subsequent MTU, but transferred directly after the current segment.

MessageEndBit

"MessageEndBit" is set if the subsequent segment completes a message. The message has then been completely transferred and is ready for further processing.

Information:

In the output direction, this bit must also be set if one individual segment is enough to hold the entire message. The module will only process a message internally if this identifier is detected.
The size of the message being transferred can be calculated by adding all of the message's segment lengths together.

Flatstream formula for calculating message length:

Message [bytes] = Segment lengths (all CBs without ME) + Segment length (of the first CB with ME)	CB	Control byte
	ME	MessageEndBit

Communication status

The communication status is determined via registers "OutputSequence" and "InputSequence".

- OutputSequence contains information about the communication status of the controller. It is written by the controller and read by the module.
- InputSequence contains information about the communication status of the module. It is written by the module and should only be read by the controller.

Relationship between OutputSequence and InputSequence

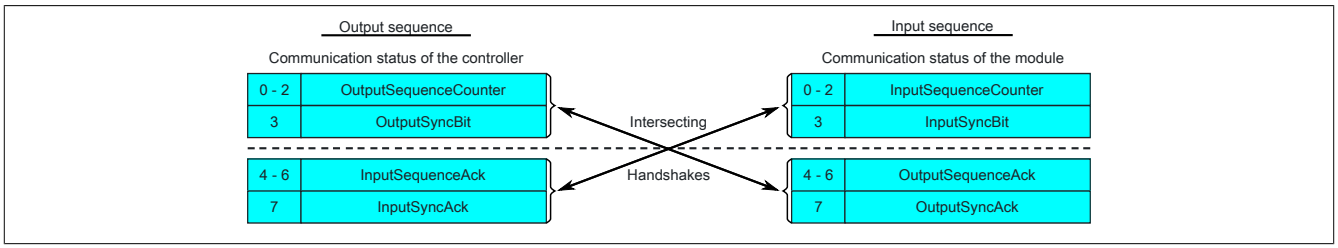


Figure 15: Relationship between OutputSequence and InputSequence

Registers "OutputSequence" and "InputSequence" are logically composed of 2 half-bytes. The low part indicates to the remote station whether a channel should be opened or whether data should be accepted. The high part is to acknowledge that the requested action was carried out.

SyncBit and SyncAck

If SyncBit and SyncAck are set in one communication direction, then the channel is considered "synchronized", i.e. it is possible to send messages in this direction. The status bit of the remote station must be checked cyclically. If SyncAck has been reset, then SyncBit on that station must be adjusted. Before new data can be transferred, the channel must be resynchronized.

SequenceCounter and SequenceAck

The communication partners cyclically check whether the low nibble on the remote station changes. When one of the communication partners finishes writing a new sequence to the MTU, it increments its SequenceCounter. The current sequence is then transmitted to the receiver, which acknowledges its receipt with SequenceAck. In this way, a "handshake" is initiated.

Information:

If communication is interrupted, segments from the unfinished message are discarded. All messages that were transferred completely are processed.

1.8.4.9.4.3 Synchronization

During synchronization, a communication channel is opened. It is important to make sure that a module is present and that the current value of SequenceCounter is stored on the station receiving the message.
Flatstream can handle full-duplex communication. This means that both channels / communication directions can be handled separately. They must be synchronized independently so that simplex communication can theoretically be carried out as well.

Synchronization in the output direction (controller as the transmitter):

The corresponding synchronization bits (OutputSyncBit and OutputSyncAck) are reset. Because of this, Flatstream cannot be used at this point in time to transfer messages from the controller to the module.

Algorithm

1) The controller must write 000 to OutputSequenceCounter and reset OutputSyncBit. The controller must cyclically query the high nibble of register "InputSequence" (checks for 000 in OutputSequenceAck and 0 in OutputSyncAck).
The module does not accept the current contents of InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
2) If the controller registers the expected values in OutputSequenceAck and OutputSyncAck, it is permitted to increment OutputSequenceCounter. The controller continues cyclically querying the high nibble of register "OutputSequence" (checks for 001 in OutputSequenceAck and 0 in InputSyncAck).
The module does not accept the current contents of InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
3) If the controller registers the expected values in OutputSequenceAck and OutputSyncAck, it is permitted to increment OutputSequenceCounter. The controller continues cyclically querying the high nibble of register "OutputSequence" (checks for 001 in OutputSequenceAck and 1 in InputSyncAck). **Note:** Theoretically, data can be transferred from this point forward. However, it is still recommended to wait until the output direction is completely synchronized before transferring data.
The module sets OutputSyncAck.
The output direction is synchronized, and the controller can transmit data to the module.

Synchronization in the input direction (controller as the receiver):

The corresponding synchronization bits (InputSyncBit and InputSyncAck) are reset. Because of this, Flatstream cannot be used at this point in time to transfer messages from the module to the controller.

Algorithm

The module writes 000 to InputSequenceCounter and resets InputSyncBit. *The module monitors the high nibble of register "OutputSequence" and expects 000 in InputSequenceAck and 0 in InputSyncAck.*
1) The controller is not permitted to accept the current contents of InputMTU since the channel is not yet synchronized. The controller must match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it increments InputSequenceCounter. *The module monitors the high nibble of register "OutputSequence" and expects 001 in InputSequenceAck and 0 in InputSyncAck.*
2) The controller is not permitted to accept the current contents of InputMTU since the channel is not yet synchronized. The controller must match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it sets InputSyncBit. *The module monitors the high nibble of register "OutputSequence" and expects 1 in InputSyncAck.*
3) The controller is permitted to set InputSyncAck. **Note:** Theoretically, data could already be transferred in this cycle. If InputSyncBit is set and InputSequenceCounter has been increased by 1, the values in the enabled Rx bytes must be accepted and acknowledged (see also "Communication in the input direction").
The input direction is synchronized, and the module can transmit data to the controller.

1.8.4.9.4.4 Transmitting and receiving

If a channel is synchronized, then the remote station is ready to receive messages from the transmitter. Before the transmitter can send data, it must first create a transmit array in order to meet Flatstream requirements.

The transmitting station must also generate a control byte for each segment created. This control byte contains information about how the subsequent part of the data being transferred should be processed. The position of the next control byte in the data stream can vary. For this reason, it must be clearly defined at all times when a new control byte is being transmitted. The first control byte is always in the first byte of the first sequence. All subsequent positions are determined recursively.

Flatstream formula for calculating the position of the next control byte:

Position (of the next control byte) = Current position + 1 + Segment length

Example

3 autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The rest of the configuration corresponds to the default settings.

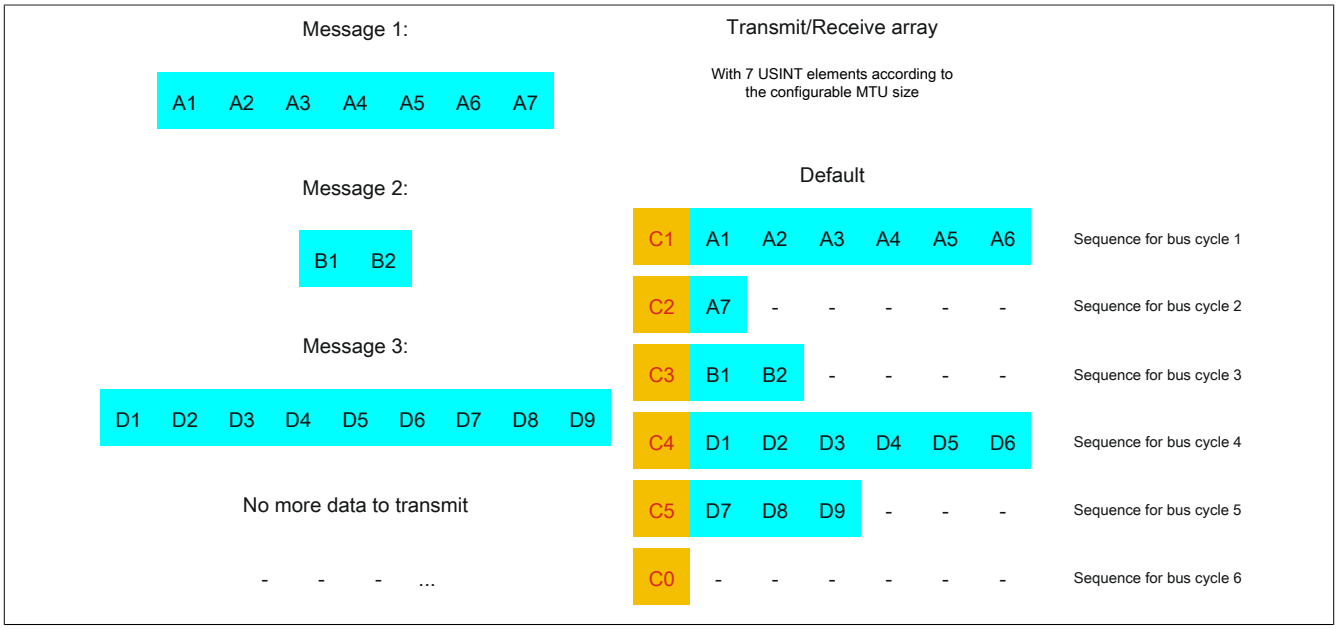


Figure 16: Transmit/Receive array (default)

The messages must first be split into segments. In the default configuration, it is important to ensure that each sequence can hold an entire segment, including the associated control byte. The sequence is limited to the size of the enable MTU. In other words, a segment must be at least 1 byte smaller than the MTU.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 1 data byte
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 3 data bytes
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C0 (control byte 0)			**C1 (control byte 1)**			**C2 (control byte 2)**		
- SegmentLength (0)	=	0	- SegmentLength (6)	=	6	- SegmentLength (1)	=	1
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (0)	=	0	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	0	Control byte	Σ	6	Control byte	Σ	129

Table 39: Flatstream determination of the control bytes for the default configuration example (part 1)

C3 (control byte 3)			**C4 (control byte 4)**			**C5 (control byte 5)**		
- SegmentLength (2)	=	2	- SegmentLength (6)	=	6	- SegmentLength (3)	=	3
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	130	Control byte	Σ	6	Control byte	Σ	131

Table 40: Flatstream determination of the control bytes for the default configuration example (part 2)

Transmitting data to a module (output)

When transmitting data, the transmit array must be generated in the application program. Sequences are then transferred one by one using Flatstream and received by the module.

> **Information:**
>
> **Although all B&R modules with Flatstream communication always support the most compact transfers in the output direction, it is recommended to use the same design for the transfer arrays in both communication directions.**

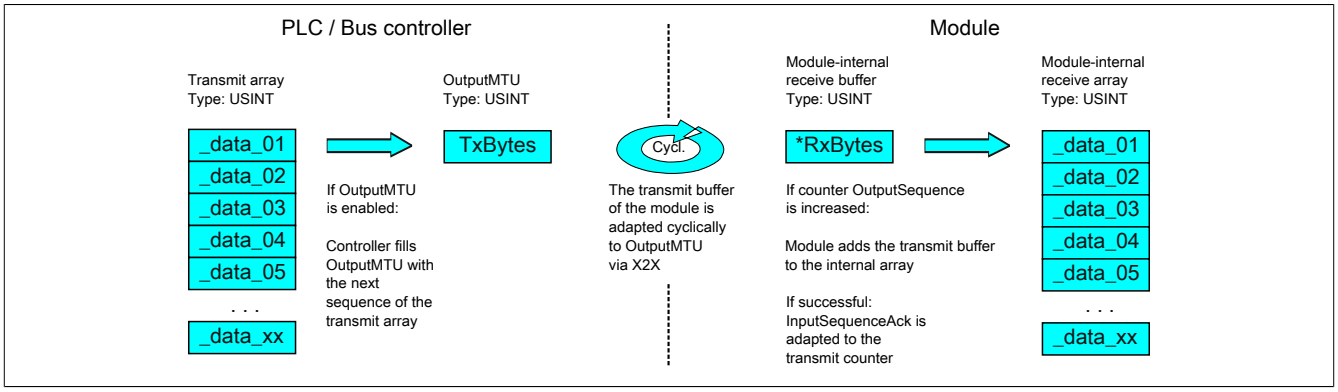


Figure 17: Flatstream communication (output)

Message smaller than OutputMTU

The length of the message is initially smaller than OutputMTU. In this case, one sequence would be sufficient to transfer the entire message and the necessary control byte.

Algorithm

Cyclic status query: *- The module monitors OutputSequenceCounter.*
0) Cyclic checks: - The controller must check OutputSyncAck. → If OutputSyncAck = 0: Reset OutputSyncBit and resynchronize the channel. - The controller must check whether OutputMTU is enabled. → If OutputSequenceCounter > InputSequenceAck: MTU is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The controller must split up the message into valid segments and create the necessary control bytes. - The controller must add the segments and control bytes to the transmit array.
2) Transmit: - The controller transfers the current element of the transmit array to OutputMTU. → OutputMTU is transferred cyclically to the module's transmit buffer but not processed further. - The controller must increase OutputSequenceCounter.
Reaction: *- The module accepts the bytes from the internal receive buffer and adds them to the internal receive array.* *- The module transmits acknowledgment and writes the value of OutputSequenceCounter to OutputSequenceAck.*
3) Completion: - The controller must monitor OutputSequenceAck. → A sequence is only considered to have been transferred successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transfer errors in the last sequence as well, it is important to make sure that the length of the *Completion* phase is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transfer can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost. (The relationship of bus to task cycle can be influenced by the user so that the threshold value must be determined individually.) - Subsequent sequences are only permitted to be transmitted in the next bus cycle after the completion check has been carried out successfully.

Message larger than OutputMTU

The transmit array, which must be created in the program sequence, consists of several elements. The user must arrange the control and data bytes correctly and transfer the array elements one after the other. The transfer algorithm remains the same and is repeated starting at the point *Cyclic checks*.

General flowchart

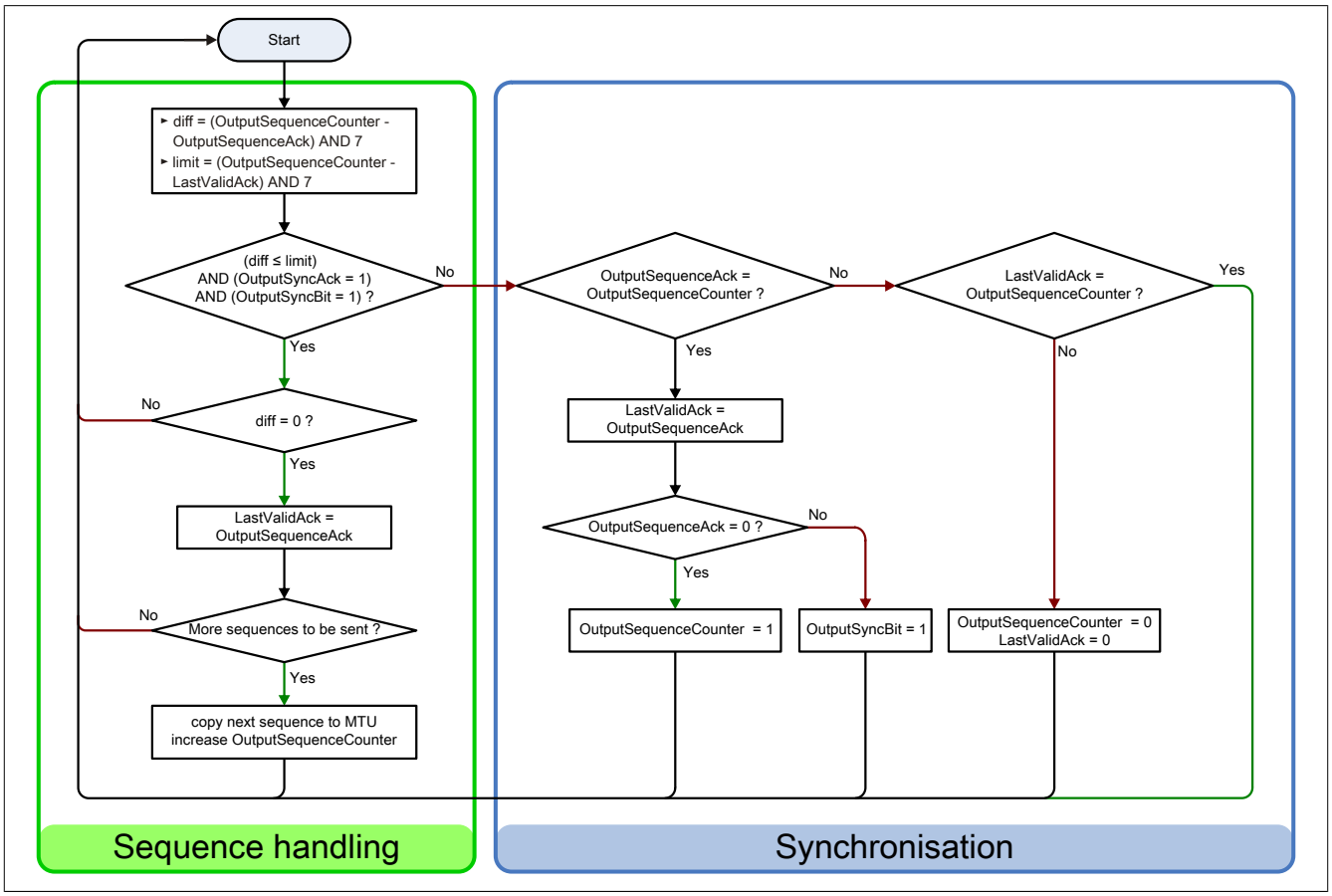


Figure 18: Flowchart for the output direction

Receiving data from a module (input)

When receiving data, the transmit array is generated by the module, transferred via Flatstream and must then be reproduced in the receive array. The structure of the incoming data stream can be set with the mode register. The algorithm for receiving the data remains unchanged in this regard.

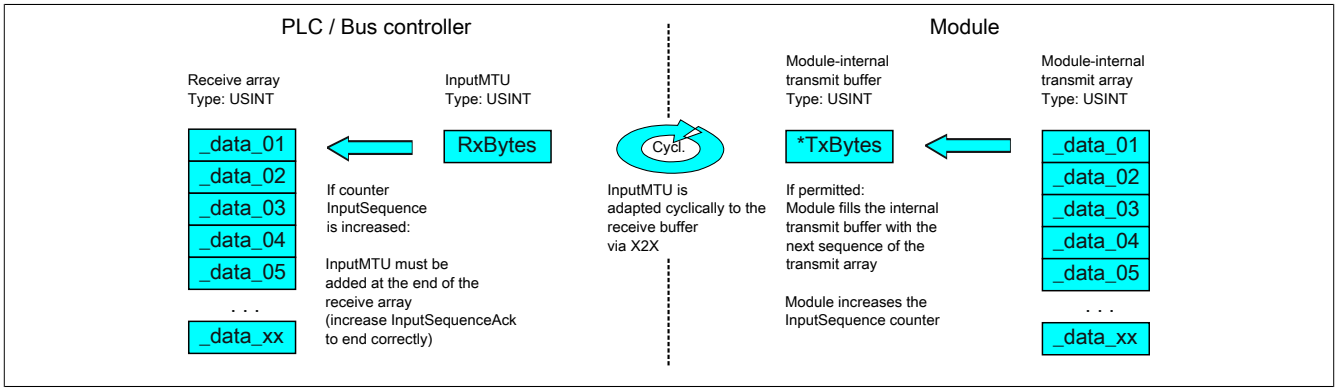


Figure 19: Flatstream communication (input)

Algorithm

0) Cyclic status query: - The controller must monitor InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck.* *- The module checks InputSequenceAck.*
Preparation: *- The module forms the segments and control bytes and creates the transmit array.*
Action: *- The module transfers the current element of the internal transmit array to the internal transmit buffer.* *- The module increases InputSequenceCounter.*
1) Receiving (as soon as InputSequenceCounter is increased): - The controller must apply data from InputMTU and append it to the end of the receive array. - The controller must match InputSequenceAck to InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck.* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.* *- Subsequent sequences are only transmitted in the next bus cycle after the completion check has been carried out successfully.*

General flowchart

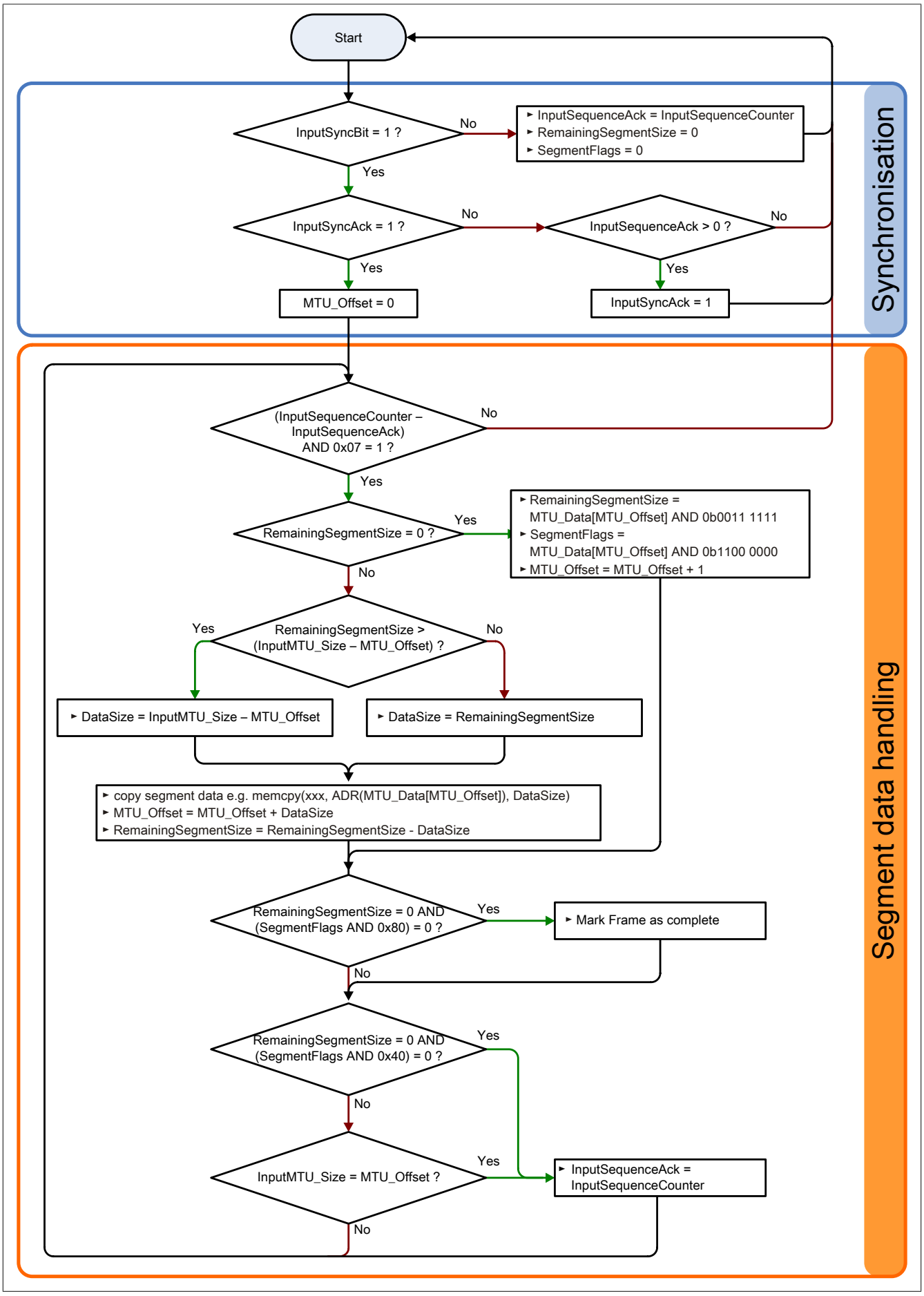


Figure 20: Flowchart for the input direction

Details

It is recommended to store transferred messages in separate receive arrays.

After a set MessageEndBit is transmitted, the subsequent segment should be added to the receive array. The message is then complete and can be passed on internally for further processing. A new/separate array should be created for the next message.

Information:

When transferring with MultiSegmentMTUs, it is possible for several small messages to be part of one sequence. In the program, it is important to make sure that a sufficient number of receive arrays can be managed. The acknowledge register is only permitted to be adjusted after the entire sequence has been applied.

If SequenceCounter is incremented by more than one counter, an error is present.

In this case, the receiver stops. All additional incoming sequences are ignored until the transmission with the correct SequenceCounter is retried. This response prevents the transmitter from receiving any more acknowledgments for transmitted sequences. The transmitter can identify the last successfully transferred sequence from the remote station's SequenceAck and continue the transfer from this point.

Information:

This situation is very unlikely when operating without "Forward" functionality.

Acknowledgments must be checked for validity.

If the receiver has successfully accepted a sequence, it must be acknowledged. The receiver takes on the value of SequenceCounter sent along with the transmission and matches SequenceAck to it. The transmitter reads SequenceAck and registers the successful transmission. If the transmitter acknowledges a sequence that has not yet been dispatched, then the transfer must be interrupted and the channel resynchronized. The synchronization bits are reset and the current/incomplete message is discarded. It must be sent again after the channel has been resynchronized.

1.8.4.9.4.5 Flatstream mode

In the input direction, the transmit array is generated automatically. Flatstream mode offers several options to the user that allow an incoming data stream to have a more compact arrangement. These include:

- Standard
- MultiSegmentMTU allowed
- Large segments allowed:

Once enabled, the program code for evaluation must be adapted accordingly.

Information:

All B&R modules that offer Flatstream mode support options "Large segments" and "MultiSegmentMTU" in the output direction. Compact transfer must be explicitly allowed only in the input direction.

Standard

By default, both options relating to compact transfer in the input direction are disabled.

1. The module only forms segments that are at least one byte smaller than the enabled MTU. Each sequence begins with a control byte so that the data stream is clearly structured and relatively easy to evaluate.
2. Since a Flatstream message is permitted to be any length, the last segment of the message frequently does not fill up all of the MTU's space. By default, the remaining bytes during this type of transfer cycle are not used.

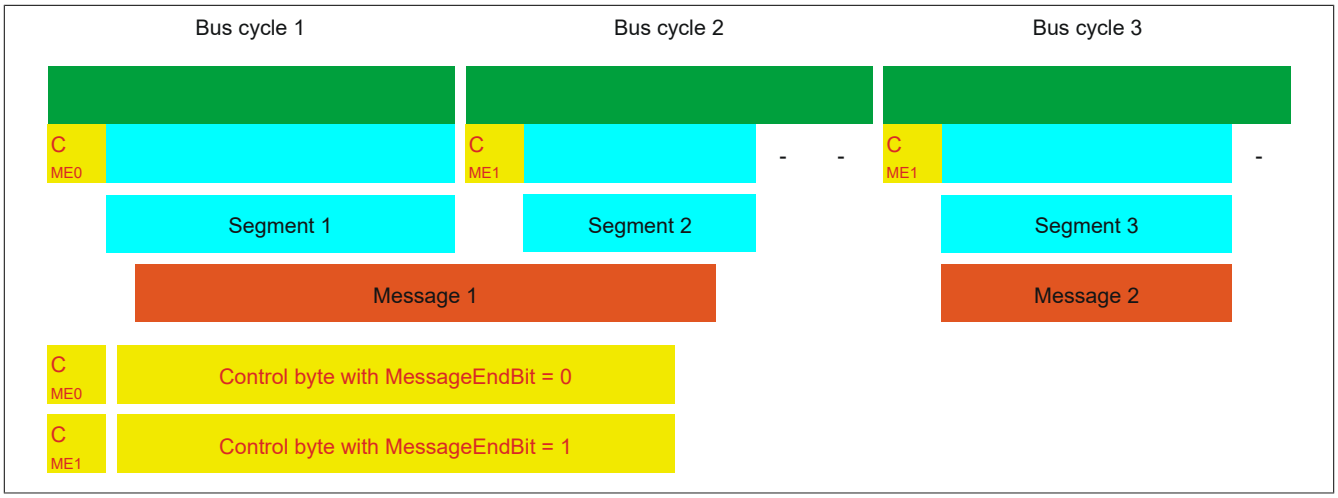


Figure 21: Message arrangement in the MTU (default)

MultiSegmentMTU allowed

With this option, InputMTU is completely filled (if enough data is pending). The previously unfilled Rx bytes transfer the next control bytes and their segments. This allows the enabled Rx bytes to be used more efficiently.

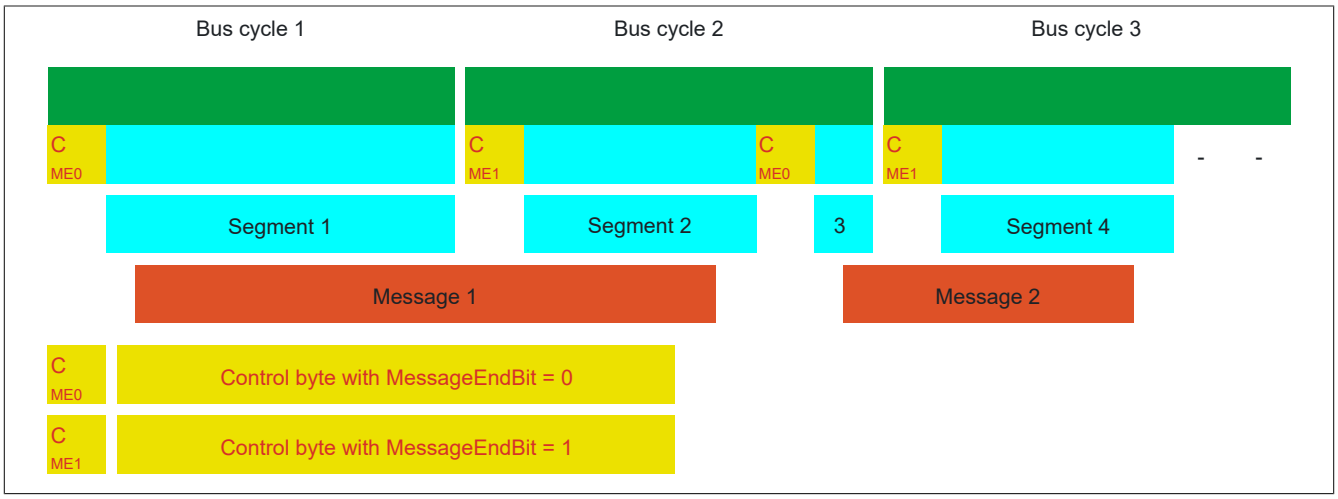


Figure 22: Arrangement of messages in the MTU (MultiSegmentMTU)

Large segments allowed:

When transferring very long messages or when enabling only very few Rx bytes, then a great many segments must be created by default. The bus system is more stressed than necessary since an additional control byte must be created and transferred for each segment. With option "Large segments", the segment length is limited to 63 bytes independently of InputMTU. One segment is permitted to stretch across several sequences, i.e. it is possible for "pure" sequences to occur without a control byte.

Information:

It is still possible to split up a message into several segments, however. If this option is used and messages with more than 63 bytes occur, for example, then messages can still be split up among several segments.

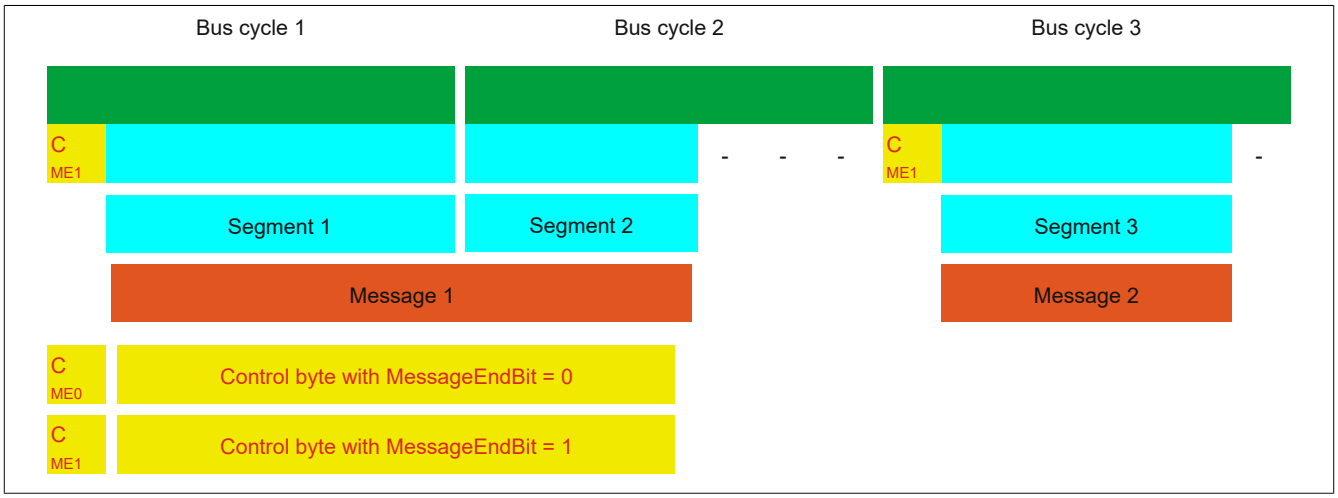


Figure 23: Arrangement of messages in the MTU (large segments)

Using both options

Using both options at the same time is also permitted.

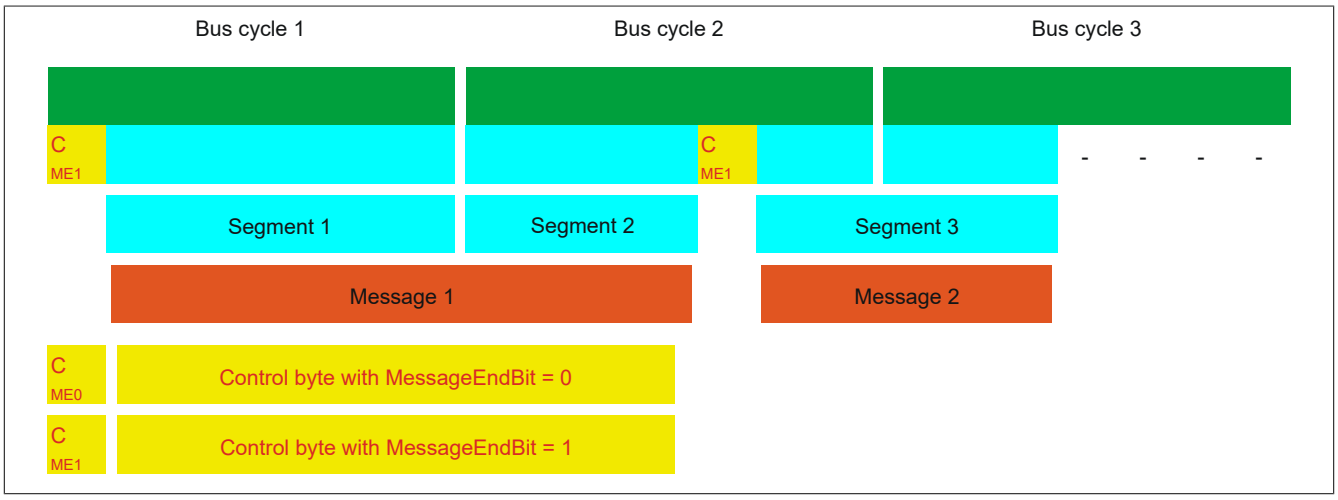


Figure 24: Arrangement of messages in the MTU (large segments and MultiSegmentMTU)

1.8.4.9.4.6 Adjusting the Flatstream

If the way messages are structured is changed, then the way data in the transmit/receive array is arranged is also different. The following changes apply to the example given earlier.

MultiSegmentMTU

If MultiSegmentMTUs are allowed, then "open positions" in an MTU can be used. These "open positions" occur if the last segment in a message does not fully use the entire MTU. MultiSegmentMTUs allow these bits to be used to transfer the subsequent control bytes and segments. In the program sequence, the "nextCBPos" bit in the control byte is set so that the receiver can correctly identify the next control byte.

Example

3 autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows the transfer of MultiSegmentMTUs.

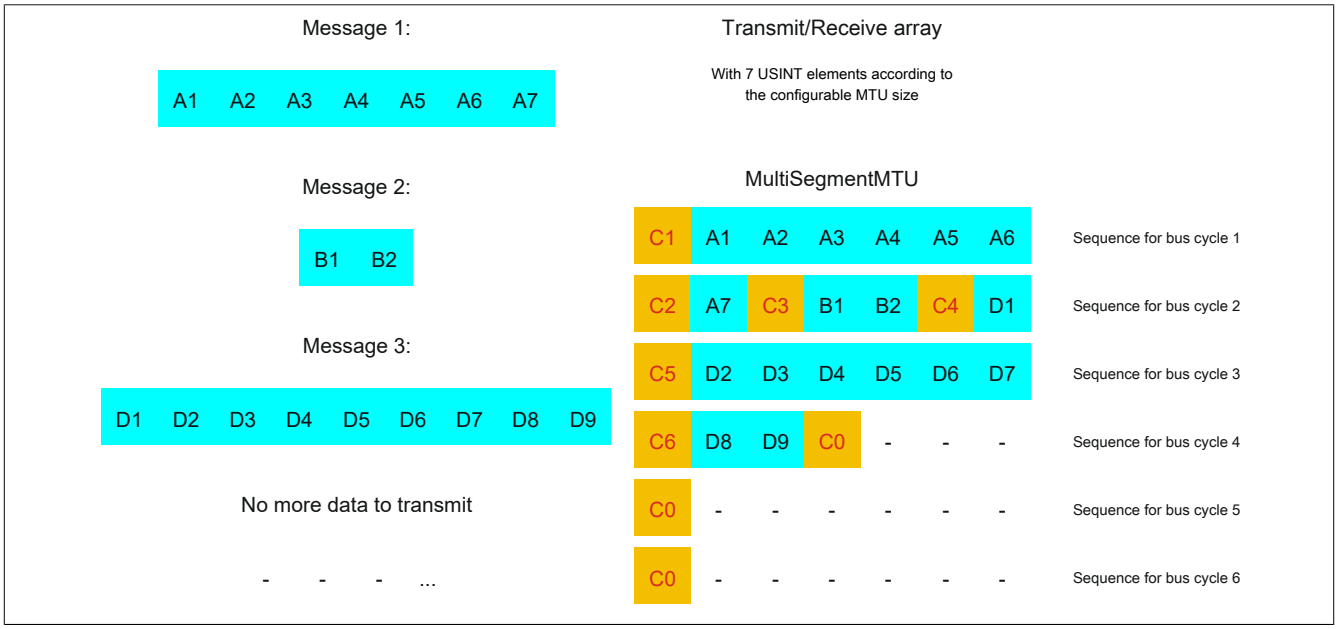


Figure 25: Transmit/receive array (MultiSegmentMTUs)

First, the messages must be split into segments. As in the default configuration, it is important for each sequence to begin with a control byte. The free bits in the MTU at the end of a message are filled with data from the following message, however. With this option, the "nextCBPos" bit is always set if payload data is transferred after the control byte.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Second segment = Control byte + 1 byte of data (MTU still has 5 open bytes)
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data (MTU still has 2 open bytes)
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 1 byte of data (MTU full)
  - ⇨ Second segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Third segment = Control byte + 2 bytes of data (MTU still has 4 open bytes)
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (6)	=	6	- SegmentLength (1)	=	1	- SegmentLength (2)	=	2
- nextCBPos (1)	=	64	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	70	Control byte	Σ	193	Control byte	Σ	194

Table 41: Flatstream determination of the control bytes for the MultiSegmentMTU example (part 1)

Warning!

The second sequence is only permitted to be acknowledged via SequenceAck if it has been completely processed. In this example, there are 3 different segments within the second sequence, i.e. the program must include enough receive arrays to handle this situation.

C4 (control byte 4)			C5 (control byte 5)			C6 (control byte 6)		
- SegmentLength (1)	=	1	- SegmentLength (6)	=	6	- SegmentLength (2)	=	2
- nextCBPos (6)	=	6	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	7	Control byte	Σ	70	Control byte	Σ	194

Table 42: Flatstream determination of the control bytes for the MultiSegmentMTU example (part 2)

Large segments

Segments are limited to a maximum of 63 bytes. This means they can be larger than the active MTU. These large segments are divided among several sequences when transferred. It is possible for sequences to be completely filled with payload data and not have a control byte.

Information:

It is still possible to subdivide a message into several segments so that the size of a data packet does not also have to be limited to 63 bytes.

Example

3 autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows the transfer of large segments.

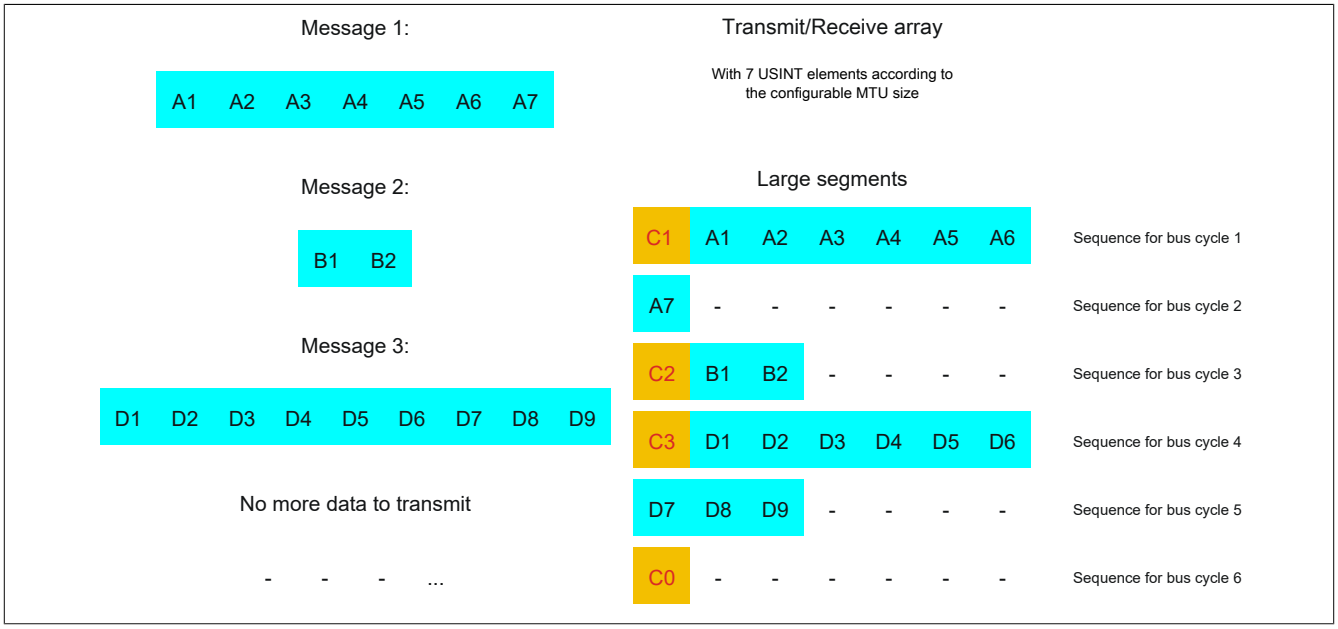


Figure 26: Transmit/receive array (large segments)

First, the messages must be split into segments. The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 7 bytes of data
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 9 bytes of data
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 43: Flatstream determination of the control bytes for the large segment example

Large segments and MultiSegmentMTU

Example

3 autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transfer of large segments as well as MultiSegmentMTUs.

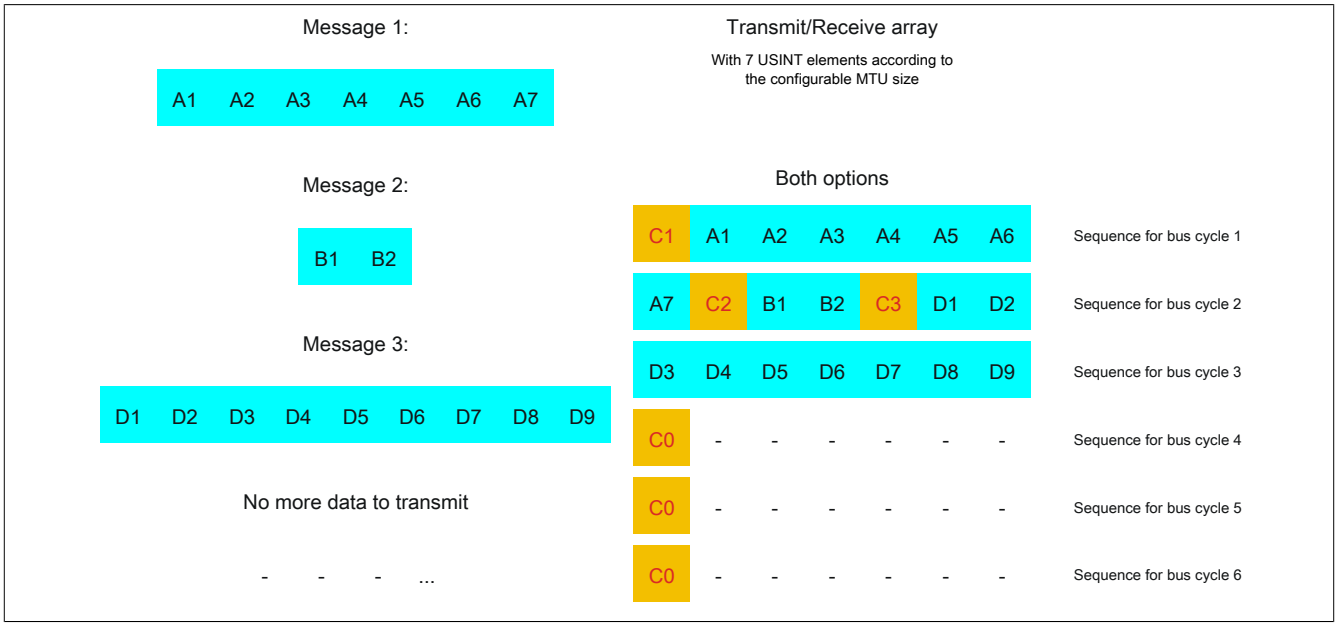


Figure 27: Transmit/receive array (large segments and MultiSegmentMTUs)

First, the messages must be split into segments. If the last segment of a message does not completely fill the MTU, it is permitted to be used for other data in the data stream. Bit "nextCBPos" must always be set if the control byte belongs to a segment with payload data.
The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated. Control bytes are generated in the same way as with option "Large segments".

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 7 bytes of data
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 9 bytes of data
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 44: Flatstream determination of the control bytes for the large segment and MultiSegmentMTU example

1.8.4.9.5 Example of function "Forward" with X2X Link

Function "Forward" is a method that can be used to substantially increase the Flatstream data rate. The basic principle is also used in other technical areas such as "pipelining" for microprocessors.

1.8.4.9.5.1 Function principle

X2X Link communication cycles through 5 different steps to transfer a Flatstream sequence. At least 5 bus cycles are therefore required to successfully transfer the sequence.

	Step I	Step II	Step III	Step IV	Step V
Actions	Transfer sequence from transmit array, increase SequenceCounter	Cyclic synchronization of MTU and module buffer	Append sequence to receive array, adjust SequenceAck	Cyclic synchronization MTU and module buffer	Check SequenceAck
Resource	Transmitter (task to transmit)	Bus system (direction 1)	Recipients (task to receive)	Bus system (direction 2)	Transmitter (task for Ack checking)

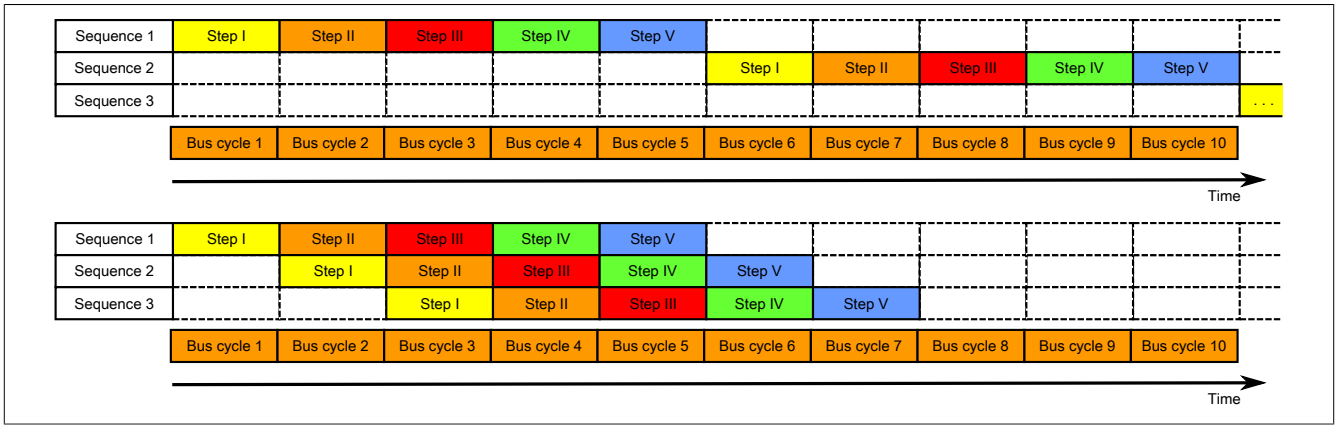


Figure 28: Comparison of transfer without/with Forward

Each of the 5 steps (tasks) requires different resources. If Forward functionality is not used, the sequences are executed one after the other. Each resource is then only active if it is needed for the current sub-action.
With Forward, a resource that has executed its task can already be used for the next message. The condition for enabling the MTU is changed to allow for this. Sequences are then passed to the MTU according to the timing. The transmitting station no longer waits for an acknowledgment from SequenceAck, which means that the available bandwidth can be used much more efficiently.
In the most ideal situation, all resources are working during each bus cycle. The receiver must still acknowledge every sequence received. Only when SequenceAck has been changed and checked by the transmitter is the sequence considered as having been transferred successfully.

1.8.4.9.5.2 Configuration

The Forward function must only be enabled for the input direction. Flatstream modules have been optimized in such a way that they support this function. In the output direction, the Forward function can be used as soon as the size of OutputMTU is specified.

Information:

Registers are described in section "Flatstream registers" on page 211.

Delay time

The delay time is specified in microseconds. This is the amount of time the module must wait after sending a sequence until it is permitted to write new data to the MTU in the following bus cycle. The program routine for receiving sequences from a module can therefore be run in a task class whose cycle time is slower than the bus cycle.

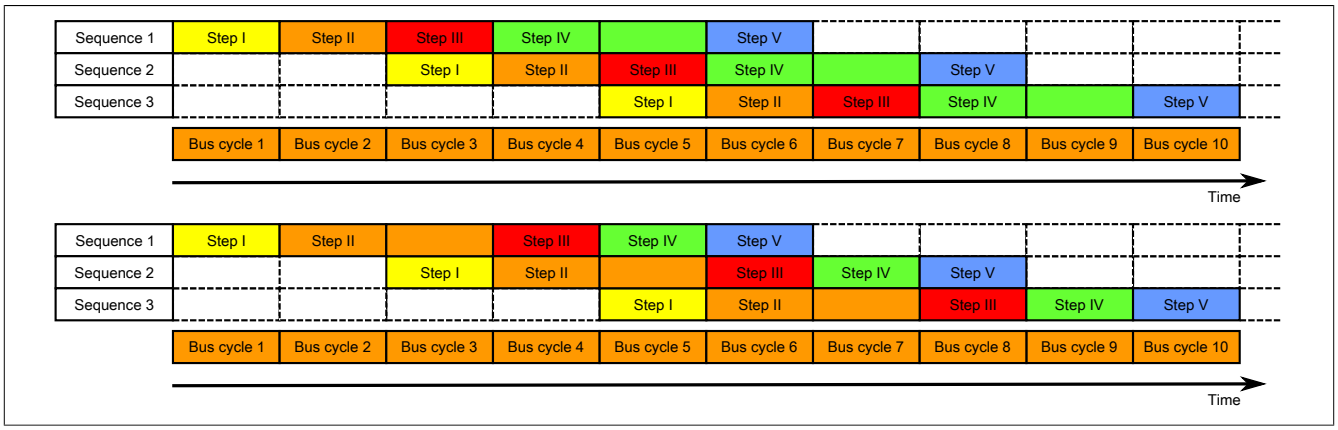


Figure 29: Effect of ForwardDelay when using Flatstream communication with the Forward function

In the program, it is important to make sure that the controller is processing all of the incoming InputSequences and InputMTUs. The ForwardDelay value causes delayed acknowledgment in the output direction and delayed reception in the input direction. In this way, the controller has more time to process the incoming InputSequence or InputMTU.

1.8.4.9.5.3 Transmitting and receiving with Forward

The basic algorithm for transmitting and receiving data remains the same. With the Forward function, up to 7 unacknowledged sequences can be transmitted. Sequences can be transmitted without having to wait for the previous message to be acknowledged. Since the delay between writing and response is eliminated, a considerable amount of additional data can be transferred in the same time window.

Algorithm for transmitting

Cyclic status query: *- The module monitors OutputSequenceCounter.*
0) Cyclic checks: - The controller must check OutputSyncAck. → If OutputSyncAck = 0: Reset OutputSyncBit and resynchronize the channel. - The controller must check whether OutputMTU is enabled. → If OutputSequenceCounter > OutputSequenceAck + 7, then it is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The controller must split up the message into valid segments and create the necessary control bytes. - The controller must add the segments and control bytes to the transmit array.
2) Transmit: - The controller must transfer the current part of the transmit array to OutputMTU. - The controller must increase OutputSequenceCounter for the sequence to be accepted by the module. - The controller is then permitted to *transmit* in the next bus cycle if the MTU has been enabled.
The module responds since OutputSequenceCounter > OutputSequenceAck: *- The module accepts data from the internal receive buffer and appends it to the end of the internal receive array.* *- The module is acknowledged and the currently received value of OutputSequenceCounter is transferred to OutputSequenceAck.* *- The module queries the status cyclically again.*
3) Completion (acknowledgment): - The controller must check OutputSequenceAck cyclically. → A sequence is only considered to have been transferred successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transfer errors in the last sequence as well, it is important to make sure that the algorithm is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transfer can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost (the relationship of bus to task cycle can be influenced by the user so that the threshold value must be determined individually).

Algorithm for receiving

0) Cyclic status query: - The controller must monitor InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck.* *- The module checks if InputMTU for enabling.* *→ Enabling criteria: InputSequenceCounter > InputSequenceAck + Forward*
Preparation: *- The module forms the control bytes / segments and creates the transmit array.*
Action: *- The module transfers the current part of the transmit array to the receive buffer.* *- The module increases InputSequenceCounter.* *- The module waits for a new bus cycle after time from ForwardDelay has expired.* *- The module repeats the action if InputMTU is enabled.*
1) Receiving (InputSequenceCounter > InputSequenceAck): - The controller must apply data from InputMTU and append it to the end of the receive array. - The controller must match InputSequenceAck to InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck.* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.*

Details/Background

1. Illegal SequenceCounter size (counter offset)
   Error situation: MTU not enabled
   If the difference between SequenceCounter and SequenceAck during transmission is larger than permitted, a transfer error occurs. In this case, all unacknowledged sequences must be repeated with the old Sequence-Counter value.
2. Checking an acknowledgment
   After an acknowledgment has been received, a check must verify whether the acknowledged sequence has been transmitted and had not yet been unacknowledged. If a sequence is acknowledged multiple times, a severe error occurs. The channel must be closed and resynchronized (same behavior as when not using Forward).

   > **Information:**
   >
   > **In exceptional cases, the module can increment OutputSequenceAck by more than 1 when using Forward.**
   > **An error does not occur in this case. The controller is permitted to consider all sequences up to the one being acknowledged as having been transferred successfully.**

3. Transmit and receive arrays
   The Forward function has no effect on the structure of the transmit and receive arrays. They are created and must be evaluated in the same way.

1.8.4.9.5.4 Errors when using Forward

In industrial environments, it is often the case that many different devices from various manufacturers are being used side by side. The electrical and/or electromagnetic properties of these technical devices can sometimes cause them to interfere with one another. These kinds of situations can be reproduced and protected against in laboratory conditions only to a certain point.

Precautions have been taken for transfer via X2X Link in case such interference should occur. For example, if an invalid checksum occurs, the I/O system will ignore the data from this bus cycle and the receiver receives the last valid data once more. With conventional (cyclic) data points, this error can often be ignored. In the following cycle, the same data point is again retrieved, adjusted and transferred.

Using Forward functionality with Flatstream communication makes this situation more complex. The receiver receives the old data again in this situation as well, i.e. the previous values for SequenceAck/SequenceCounter and the old MTU.

Loss of acknowledgment (SequenceAck)

If a SequenceAck value is lost, then the MTU was already transferred properly. For this reason, the receiver is permitted to continue processing with the next sequence. The SequenceAck is aligned with the associated SequenceCounter and sent back to the transmitter. Checking the incoming acknowledgments shows that all sequences up to the last one acknowledged have been transferred successfully (see sequences 1 and 2 in the image).

Loss of transmission (SequenceCounter, MTU):

If a bus cycle drops out and causes the value of SequenceCounter and/or the filled MTU to be lost, then no data reaches the receiver. At this point, the transmission routine is not yet affected by the error. The time-controlled MTU is released again and can be rewritten to.
The receiver receives SequenceCounter values that have been incremented several times. For the receive array to be put together correctly, the receiver is only permitted to process transmissions whose SequenceCounter has been increased by one. The incoming sequences must be ignored, i.e. the receiver stops and no longer transmits back any acknowledgments.
If the maximum number of unacknowledged sequences has been sent and no acknowledgments are returned, the transmitter must repeat the affected SequenceCounter and associated MTUs (see sequence 3 and 4 in the image).

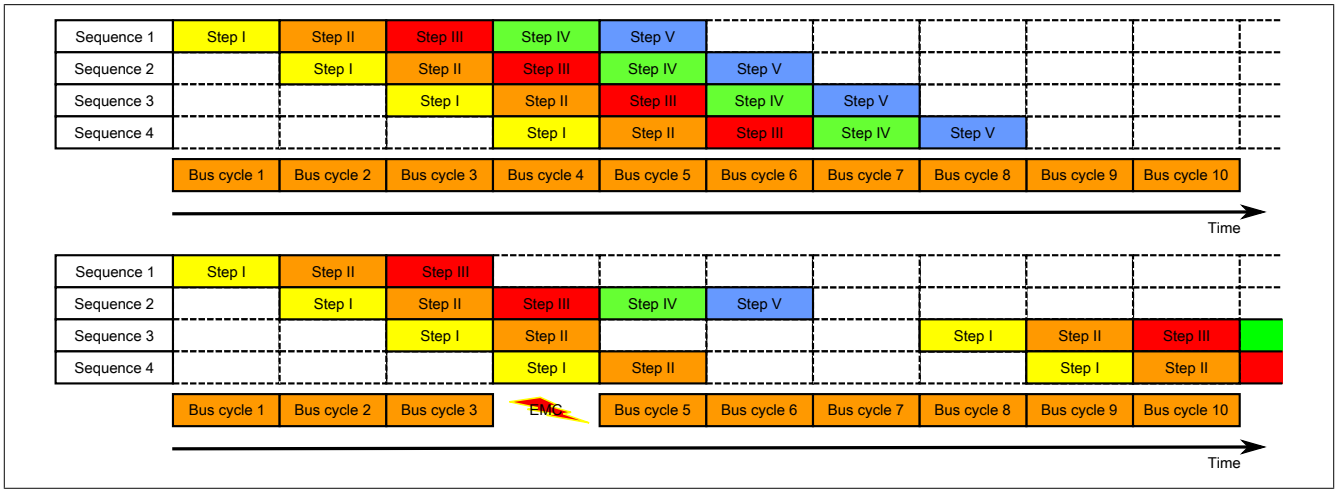


Figure 30: Effect of a lost bus cycle

Loss of acknowledgment

In sequence 1, the acknowledgment is lost due to disturbance. Sequences 1 and 2 are therefore acknowledged in Step V of sequence 2.

Loss of transmission

In sequence 3, the entire transmission is lost due to disturbance. The receiver stops and no longer sends back any acknowledgments.
The transmitting station continues transmitting until it has issued the maximum permissible number of unacknowledged transmissions.
5 bus cycles later at the earliest (depending on the configuration), it begins resending the unsuccessfully sent transmissions.

1.8.4.10 NetTime Technology

NetTime refers to the ability to precisely synchronize and transfer system times between individual components of the controller or network (controller, I/O modules, X2X Link, POWERLINK, etc.).

This allows the moment that events occur to be determined system-wide with microsecond precision. Upcoming events can also be executed precisely at a specified moment.

1.8.4.10.1 Time information

Various time information is available in the controller or on the network:

- System time (on the PLC, Automation PC, etc.)
- X2X Link time (for each X2X Link network)
- POWERLINK time (for each POWERLINK network)
- Time data points of I/O modules

The NetTime is based on 32-bit counters, which are increased with microsecond resolution. The sign of the time information changes after 35 min, 47 s, 483 ms and 648 µs; an overflow occurs after 71 min, 34 s, 967 ms and 296 µs.

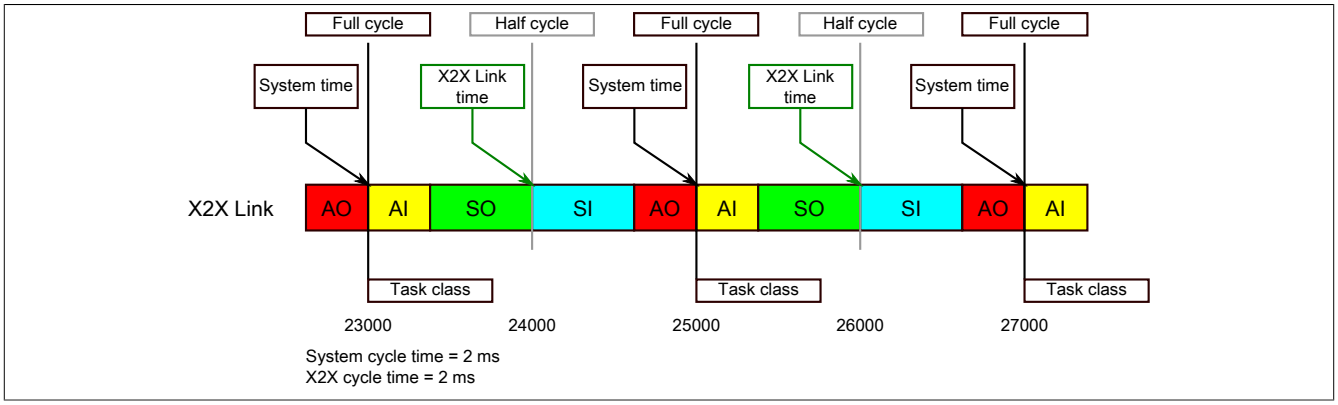
The initialization of the times is based on the system time during the startup of the X2X Link, the I/O modules or the POWERLINK interface.

Current time information in the application can also be determined via library AsIOTime.

1.8.4.10.1.1 Controller data points

The NetTime I/O data points of the controller are latched to each system clock and made available.

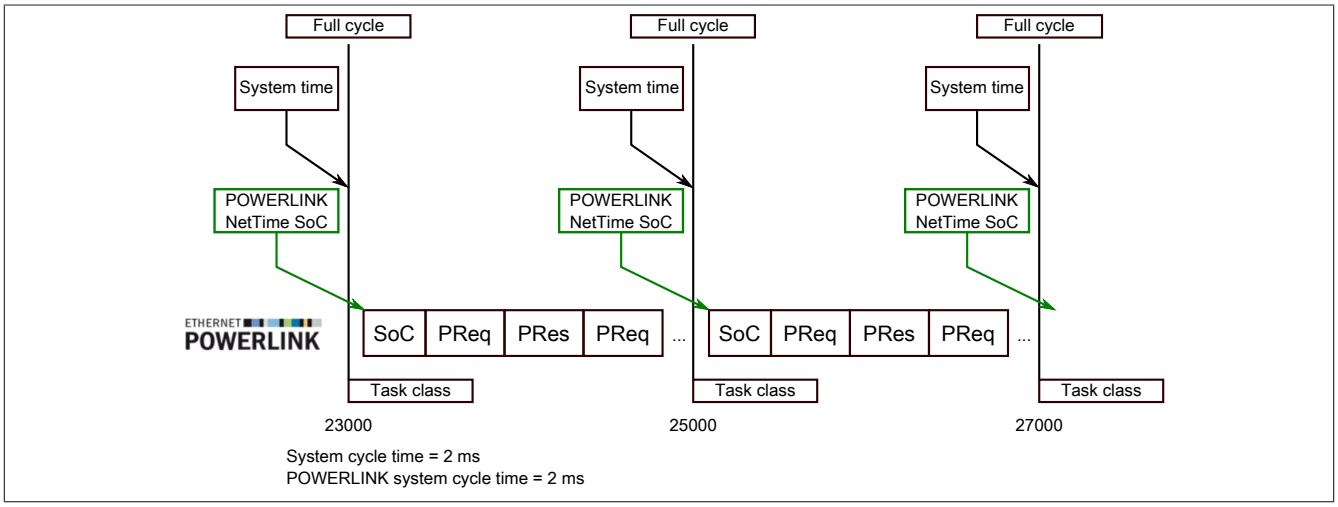
1.8.4.10.1.2 X2X Link - Reference time point



The reference time point on the X2X Link network is always calculated at the half cycle of the X2X Link cycle. This results in a difference between the system time and the X2X Link reference time point when the reference time is read out.

In the example above, this results in a difference of 1 ms, i.e. if the system time and X2X Link reference time are compared at time 25000 in the task, then the system time returns the value 25000 and the X2X Link reference time returns the value 24000.

1.8.4.10.1.3 POWERLINK - Reference time point

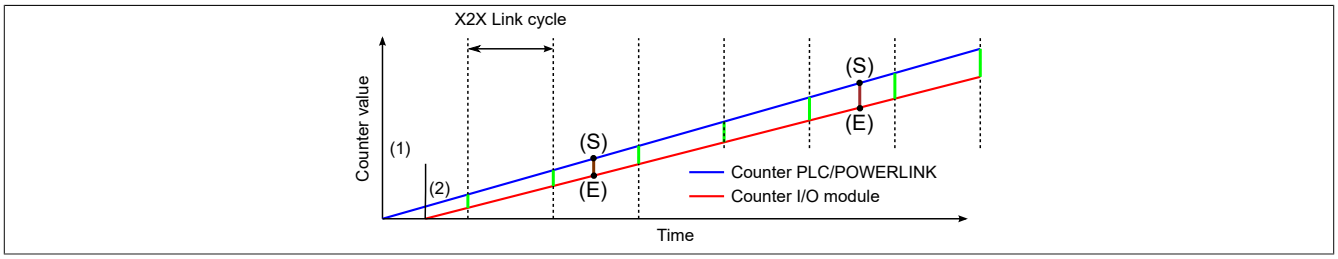


The reference time point on the POWERLINK network is always calculated at the start of cycle (SoC) of the POWERLINK network. The SoC starts 20 µs after the system clock due to the system. This results in the following difference between the system time and the POWERLINK reference time:

POWERLINK reference time = System time - POWERLINK cycle time + 20 µs.

In the example above, this means a difference of 1980 µs, i.e. if the system time and POWERLINK reference time are compared at time 25000 in the task, then the system time returns the value 25000 and the POWERLINK reference time returns the value 23020.

1.8.4.10.1.4 Synchronization of system time/POWERLINK time and I/O module



At startup, the internal counters for the controller/POWERLINK (1) and the I/O module (2) start at different times and increase the values with microsecond resolution.

At the beginning of each X2X Link cycle, the controller or POWERLINK network sends time information to the I/O module. The I/O module compares this time information with the module's internal time and forms a difference (green line) between the two times and stores it.

When a NetTime event (E) occurs, the internal module time is read out and corrected with the stored difference value (brown line). This means that the exact system moment (S) of an event can always be determined, even if the counters are not absolutely synchronous.

Note

The deviation from the clock signal is strongly exaggerated in the picture as a red line.

1.8.4.10.2 Timestamp functions

NetTime-capable modules provide various timestamp functions depending on the scope of functions. If a timestamp event occurs, the module immediately saves the current NetTime. After the respective data is transferred to the controller, including this precise moment, the controller can then evaluate the data using its own NetTime (or system time), if necessary.

1.8.4.10.2.1 Time-based inputs

NetTime Technology can be used to determine the exact moment of a rising edge at an input. The rising and falling edges can also be detected and the duration between 2 events can be determined.

Information:

The determined moment always lies in the past.

1.8.4.10.2.2 Time-based outputs

NetTime Technology can be used to specify the exact moment of a rising edge on an output. The rising and falling edges can also be specified and a pulse pattern generated from them.

Information:

The specified time must always be in the future, and the set X2X Link cycle time must be taken into account for the definition of the moment.

1.8.4.10.2.3 Time-based measurements

NetTime Technology can be used to determine the exact moment of a measurement that has taken place. Both the starting and end moment of the measurement can be transmitted.

1.8.4.11 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without causing a communication error or impaired functionality. It should be noted that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

1.8.4.12 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

Minimum I/O update time	
Analog inputs	1 ms

Minimum I/O update time for HART communication	
Point-to-point	500 ms
Multidrop	500 ms * Number of stations

1.9 X20AI2622

1.9.1 General information

The module is equipped with 2 inputs with 13-bit (including sign) digital converter resolution. It is possible to select between the current and voltage signal using different terminals.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

- 2 analog inputs
- Either current or voltage signal possible
- 13-bit digital converter resolution

1.9.2 Order data

Order number	Short description	Figure
	Analog inputs	
X20AI2622	X20 analog input module, 2 inputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution, configurable input filter	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 45: X20AI2622 - Order data

1.9.3 Technical data

Order number	X20AI2622
Short description	
I/O module	2 analog inputs ±10 V or 0 to 20 mA / 4 to 20 mA
General information	
B&R ID code	0x1B9E
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Channel type	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	0.8 W [1]
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
KC	Yes
EAC	Yes
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
DNV GL	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
LR	ENV1
Analog inputs	
Input	±10 V or 0 to 20 mA / 4 to 20 mA, via different terminal connections
Input type	Differential input
Digital converter resolution	
Voltage	±12-bit
Current	12-bit
Conversion time	300 µs for all inputs
Output format	
Data type	INT
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0008 = 2.441 mV
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0008 = 4.883 µA
Input impedance in signal range	
Voltage	20 MΩ
Current	-
Load	
Voltage	-
Current	<400 Ω
Input protection	Protection against wiring with supply voltage
Permissible input signal	
Voltage	Max. ±30 V
Current	Max. ±50 mA
Output of digital value during overload	Configurable
Conversion procedure	SAR
Input filter	3rd-order low pass / cutoff frequency 1 kHz
Max. error at 25°C	
Voltage	
Gain	0.08% [2]
Offset	0.015% [3]
Current	
Gain	0 to 20 mA = 0.08 % / 4 to 20 mA = 0.1 % [2]
Offset	0 to 20 mA = 0.03 % / 4 to 20 mA = 0.16 % [4]
Max. gain drift	
Voltage	0.006 %/°C [2]
Current	0 to 20 mA = 0.009 %/°C 4 to 20 mA = 0.0113 %/°C [2]
Max. offset drift	
Voltage	0.002 %/°C [3]
Current	0 to 20 mA = 0.004 %/°C 4 to 20 mA = 0.005 %/°C [4]

Table 46: X20AI2622 - Technical data

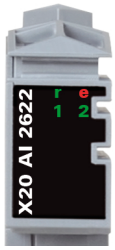
Order number	X20AI2622
Common-mode rejection	
DC	70 dB
50 Hz	70 dB
Common-mode range	±12 V
Crosstalk between channels	<-70 dB
Nonlinearity	
Voltage	<0.025% 3)
Current	<0.05% 4)
Insulation voltage between channel and bus	500 V_{eff}
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Pitch	$12.5^{+0.2}$ mm

Table 46: X20AI2622 - Technical data

1) To reduce power dissipation, B&R recommends bridging unused inputs on the terminals or configuring them as current signals.
2) Based on the current measured value.
3) Based on the 20 V measurement range.
4) Based on the 20 mA measurement range.

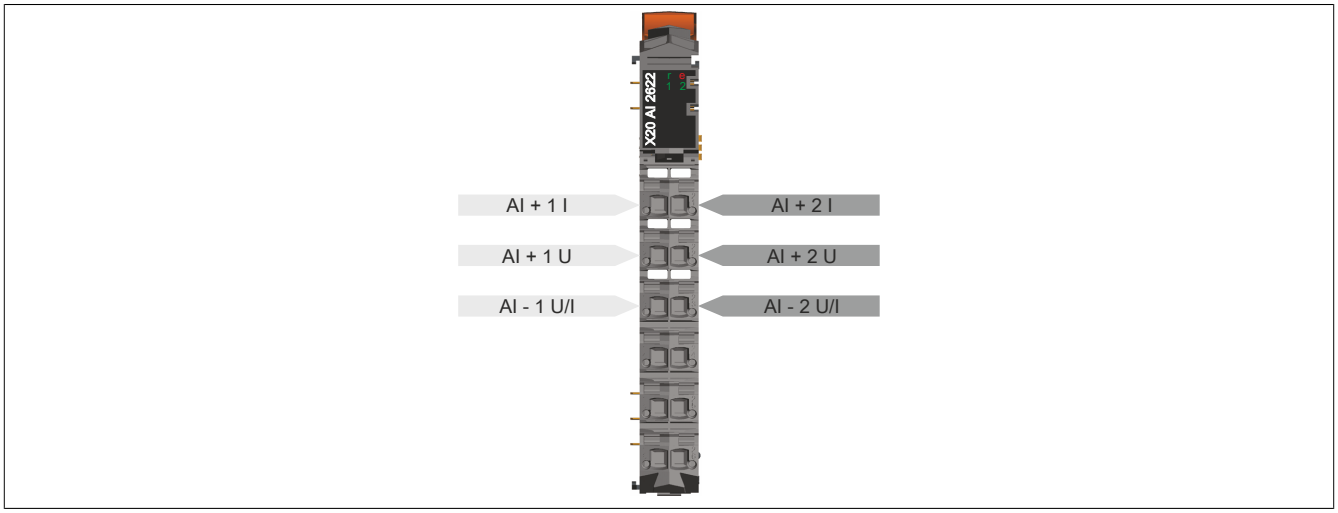
1.9.4 LED status indicators

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 system user's manual.

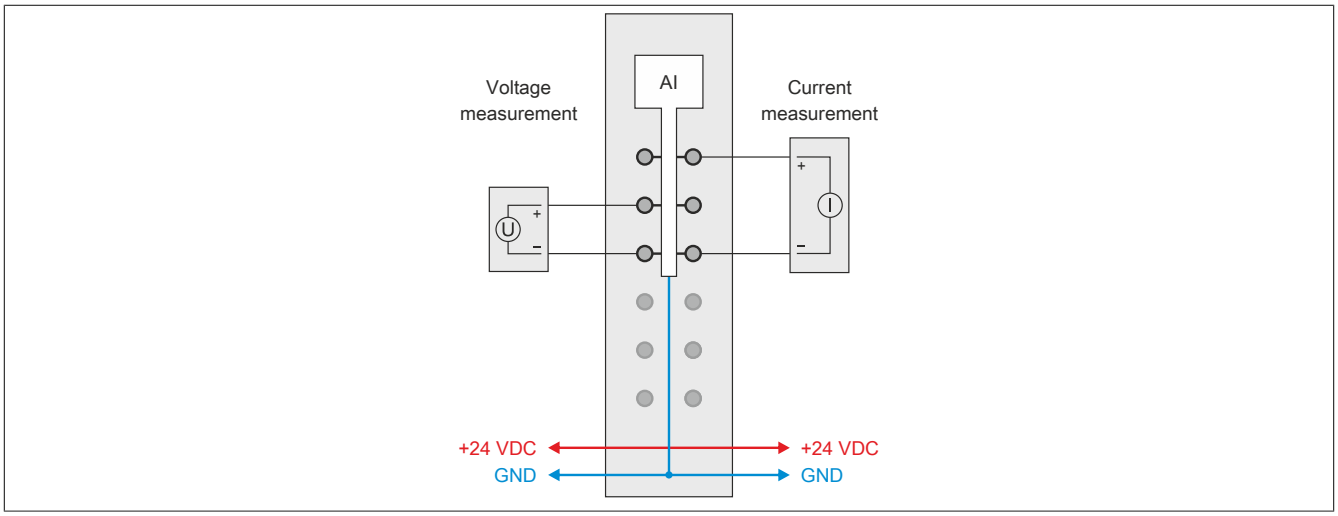
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 2	Green	Off	Open line1) or sensor is disconnected
			Blinking	Input signal overflow or underflow
			On	Analog/digital converter running, value OK

1) Open line detection only possible when measuring voltage.

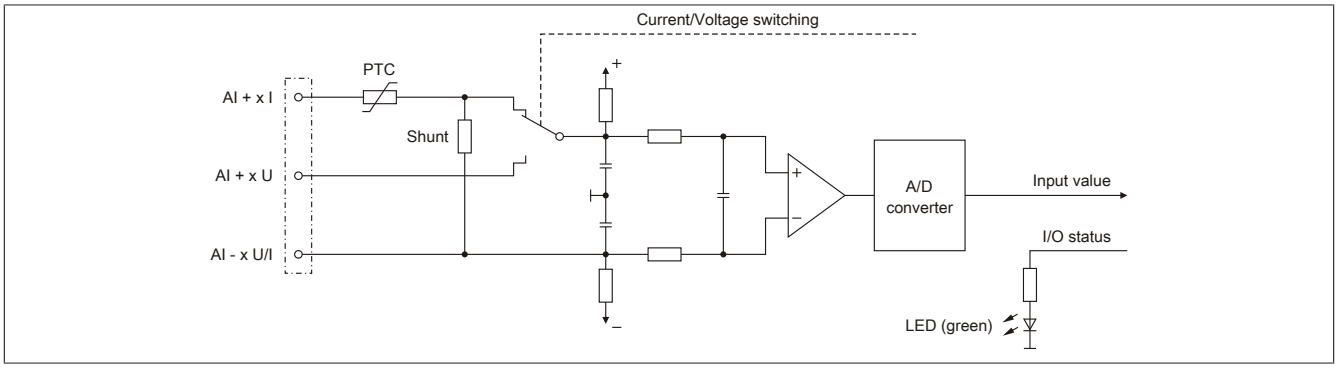
1.9.5 Pinout



1.9.6 Connection example



1.9.7 Input circuit diagram



1.9.8 Register description

1.9.8.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 system user's manual.

1.9.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
16	ConfigOutput01 (Input filter)	USINT				•
18	ConfigOutput02 (Channel type)	USINT				•
20	ConfigOutput03 (Lower value)	INT				•
22	ConfigOutput04 (Upper limit value)	INT				•
Communication						
0	AnalogInput01	INT	•			
2	AnalogInput02	INT	•			
30	StatusInput01	USINT	•			

1.9.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
16	-	ConfigOutput01 (Input filter)	USINT				•
18	-	ConfigOutput02 (Channel type)	USINT				•
20	-	ConfigOutput03 (Lower limit value)	INT				•
22	-	ConfigOutput04 (Upper limit value)	INT				•
Communication							
0	0	AnalogInput01	INT	•			
2	2	AnalogInput02	INT	•			
30	-	StatusInput01	USINT		•		

1) The offset specifies the position of the register within the CAN object.

1.9.8.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

1.9.8.3.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

1.9.8.4 Analog inputs

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

1.9.8.5 Analog input values

Name:
AnalogInput01 to AnalogInput02

The analog input value are mapped to this register depending on the configured operating mode.

Data type	Value	Input signal:
INT	-32768 to 32767	Voltage signal -10 to 10 VDC
	0 to 32767	Current signal 0 to 20 mA
	-8192 to 32767	Current signal 4 to 20 mA (value 0 corresponds to 4 mA)

1.9.8.6 Input filter

This module is equipped with a configurable input filter. The minimum X2X cycle time must be >500 µs. Filtering is disabled for shorter X2X cycle times.

If the input filter is active, then the channels are scanned in 1 ms cycles. The time offset between the channels is 200 µs. Conversion is performed acyclically to the X2X cycle.

Information:

The filter sampling time is fixed at 1 ms and is acyclic to the X2X cycle.

1.9.8.6.1 Input ramp limiting

Input ramp limiting can only be performed in conjunction with filtering. Input ramp limiting is performed before filtering.

The difference of the input value change is checked for exceeding the specified limit. In the event of overshoot, the tracked input value is equal to the old value ± the limit value.

Configurable limit values:

Value	Limit value
0	The input value is used without limitation.
1	0x3FFF = 16383
2	0x1FFF = 8191
3	0x0FFF = 4095
4	0x07FF = 2047
5	0x03FF = 1023
6	0x01FF = 511
7	0x00FF = 255

Input ramp limiting is well suited for suppressing disturbances (spikes). The following examples show the functionality of input ramp limiting based on an input step and a disturbance.

Example 1

The input value jumps from 8000 to 17000. The diagram shows the tracked input value with the following settings:

Input ramp limiting = 4 = 0x07FF = 2047

Filter level = 2

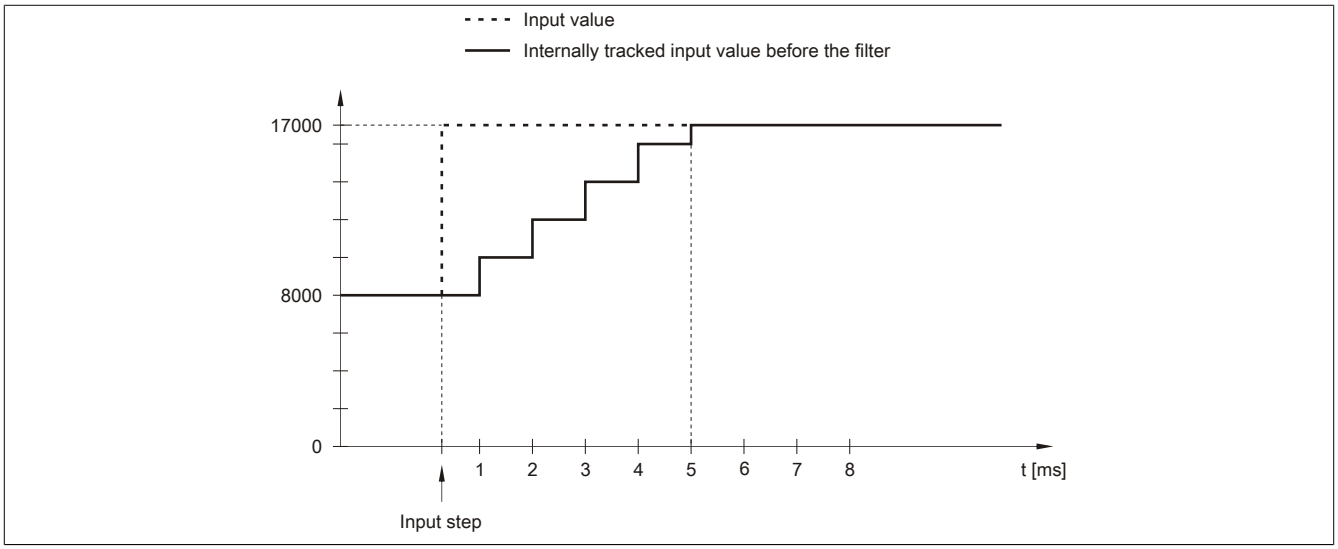


Figure 31: Tracked input value for input step

Example 2

A disturbance interferes with the input value. The diagram shows the tracked input value with the following settings:

Input ramp limiting = 4 = 0x07FF = 2047

Filter level = 2

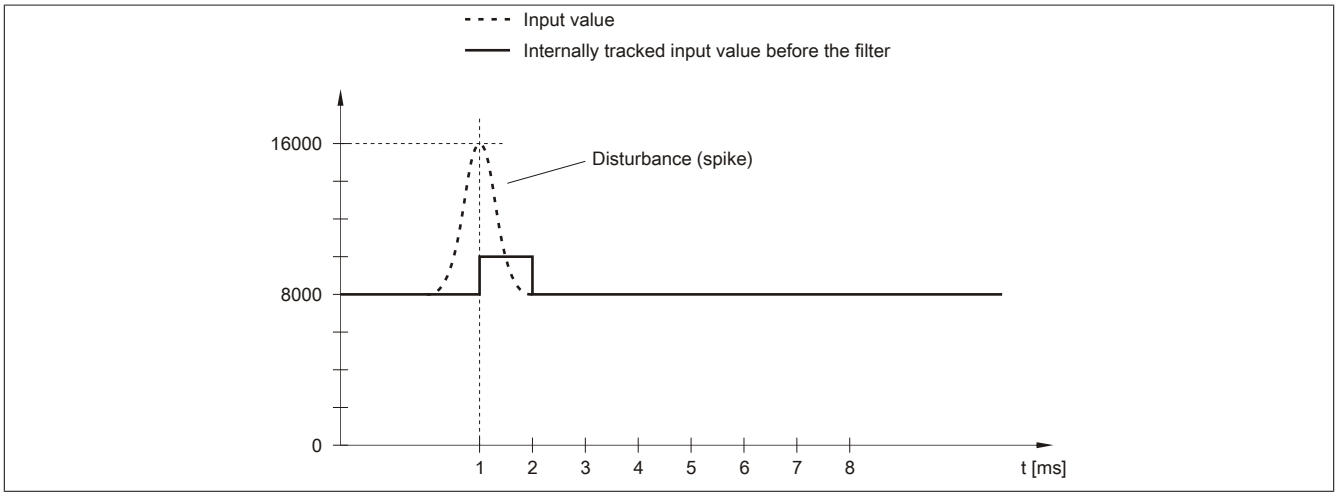


Figure 32: Tracked input value for disturbance

1.9.8.6.2 Filter level

A filter can be defined to prevent large input steps. This filter is used to bring the input value closer to the actual analog value over a period of several milliseconds.
Filtering takes place after any input ramp limiting has been carried out.

Formula for calculating the input value:

$$\text{Value}_{\text{New}} = \text{Value}_{\text{Old}} - \frac{\text{Value}_{\text{Old}}}{\text{Filter level}} + \frac{\text{Input value}}{\text{Filter level}}$$

Adjustable filter levels:

Value	Filter level
0	Filter switched off
1	Filter level 2
2	Filter level 4
3	Filter level 8
4	Filter level 16
5	Filter level 32
6	Filter level 64
7	Filter level 128

The following examples show the functionality of the filter based on an input step and a disturbance.

Example 1

The input value jumps from 8000 to 16000. The diagram shows the calculated value with the following settings:

Input ramp limiting = 0

Filter level = 2 or 4

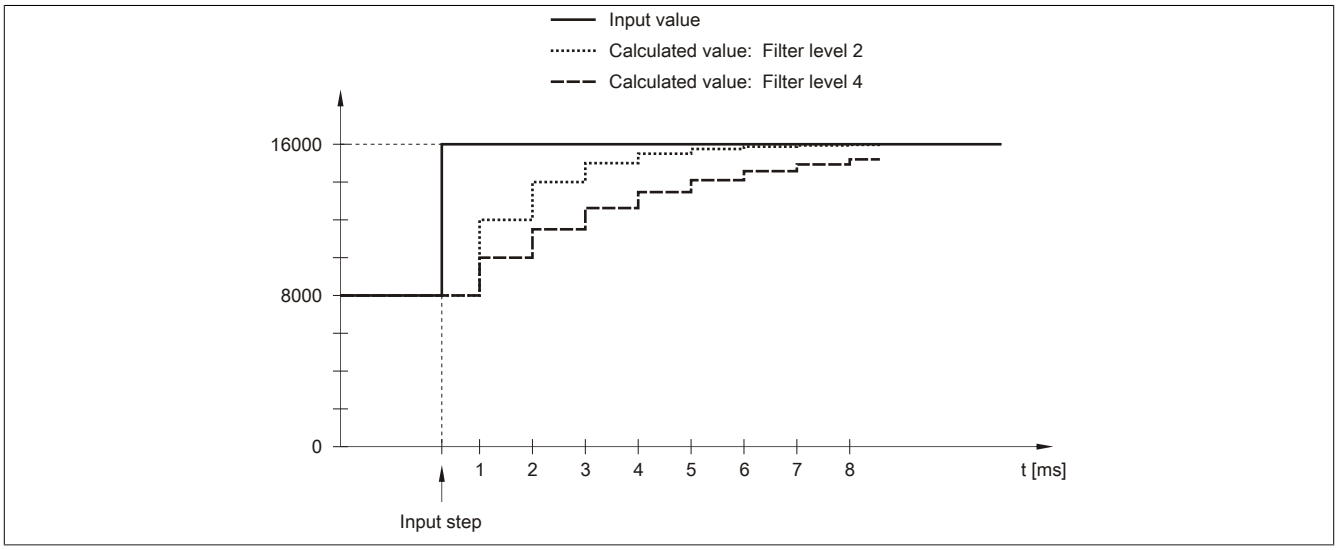


Figure 33: Calculated value during input step

Example 2

A disturbance interferes with the input value. The diagram shows the calculated value with the following settings:

Input ramp limiting = 0

Filter level = 2 or 4

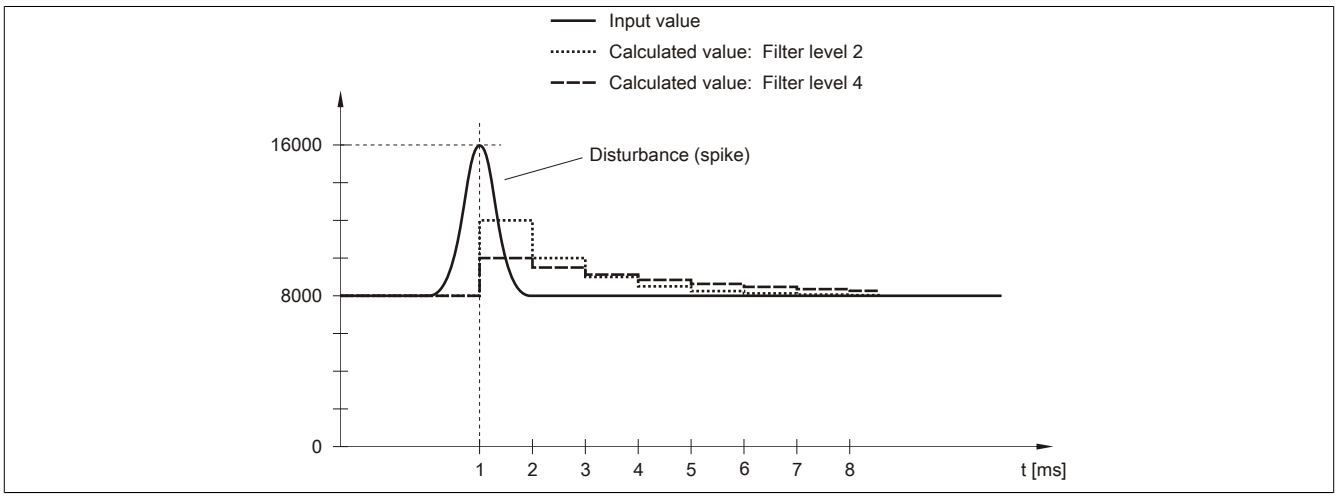


Figure 34: Calculated value during disturbance

1.9.8.7 Configuring the input filter

Name:
ConfigOutput01

The filter level and input ramp limiting of the input filter are set in this register.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter disabled (bus controller default setting)
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines input ramp limiting	000	The input value is applied without limitation (bus controller default setting)
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

1.9.8.8 Channel type

Name:
ConfigOutput02

The type and range of signal measurement can be set in this register.

The individual channels are designed for current and voltage signals. This differentiation is made using different terminals and an integrated switch in the module. The switch is automatically activated by the module depending on the specified configuration. The following input signals can be set:

- ±10 V voltage signal (default)
- 0 to 20 mA current signal
- 4 to 20 mA current signal

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Voltage signal (bus controller default setting)
		1	Current signal, measurement range corresponding to bit 4
1	Channel 2	0	Voltage signal
		1	Current signal, measurement range corresponding to bit 5
2 - 3	Reserved	0	
4	Channel 1: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal
5	Channel 2: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal
6 - 7	Reserved	0	

1.9.8.9 Limit values

The input signal is monitored at the upper and lower limit values. These must be defined according to the operating mode:

Limit value (default)	Voltage signal ±10 V		Current signal 0 to 20 mA		Current signal 4 to 20 mA	
Upper maximum limit value	+10 V	+32767 (0x7FFF)	20 mA	+32767 (0x7FFF)	20 mA	+32767 (0x7FFF)
Lower minimum limit value	-10 V	-32767 (0x8001)	0 mA	0[1)]	4 mA	0[2)]

1) The analog value is limited down to 0.
2) The analog value is limited down to 0 at currents <4 mA. The status bit for the lower limit is set.

Other limit values can be defined if necessary. The limit values apply to all channels. These are enabled automatically by writing to the limit value registers. From this point on, the analog values will be monitored and limited according to the new limits. The results of monitoring are displayed in the status register.

Examples of limit value settings

Use case	Limit value settings
Current signal: 4 to 20 mA	If values <4 mA should be measured for a current signal with 4 to 20 mA, a negative limit value must be set: 0 mA corresponds to value -8192 (0xE000).
Mixed voltage and current signal	The set limit values apply to all channels. A compromise must therefore be made for mixed operation (voltage and current signal mixed). The following setting has proven to be effective: Upper limit value = +32767, lower limit value = -32767 This also allows negative voltage values to be measured. With a lower limit value of 0, the voltage value would be limited to 0.
Current signal on all channels	All channels are configured for current measurement. The limit value setting in Automation Studio is not adjusted automatically. This means that +32767 is set for the upper limit value and -32767 for the lower limit value. The necessary adjustments must be made by the user, e.g. lower limit value = 0

1.9.8.9.1 Lower limit value

Name:
ConfigOutput03

The lower limit value for analog values can be set in this register. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Values	Information
INT	-32768 to 32767	Bus controller default setting: -32768

Information:

- **The default value of -32767 corresponds to the minimum default value of -10 VDC.**
- **For a 0 to 20 mA configuration, this value should be set to 0.**
- **For a 4 to 20 mA configuration, this value can be set to -8192 (corresponds to 0 mA) in order to display values <4 mA.**

Information:

It is important to note that this setting applies to all channels!

1.9.8.9.2 Upper limit value

Name:
ConfigOutput04

The upper limit value for analog values can be set in this register. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Values	Information
INT	-32767 to 32767	Bus controller default setting: 32767

Information:

The default value 32767 corresponds to the maximum default value at 20 mA or +10 VDC.

Information:

It is important to note that this setting applies to all channels!

1.9.8.10 Input status

Name:
StatusInput01

The module inputs are monitored in this register. A change in the monitoring status is actively transmitted as an error message. The following states are monitored depending on the settings:

Value	Voltage signal ±10 V	Current signal 0 to 20 mA	Current signal 4 to 20 mA
0	No error	No error	No error
1	Lower limit value undershot	Default setting The input value has a lower limit of 0x0000. Underflow monitoring is therefore not necessary. After lower limit value change The input value is limited to the configured value. The status bit is set when the value falls below the lower limit.	Lower limit value undershot
2	Upper limit value overshot	Upper limit value overshot	Upper limit value overshot
3	Open circuit	-	-

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
2 - 3	Channel 2	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
4 - 7	Reserved	0	

Limiting the analog value

In addition to the status information, the analog value is fixed to the values listed below by default in an error state. The analog value is limited to the new values if the limit values were changed.

Error state	Digital value on error (default values)
Open circuit	+32767 (0x7FFF)
Upper limit value overshot	+32767 (0x7FFF)
Lower limit value undershot	-32767 (0x8001)
Invalid value	-32768 (0x8000)

1.9.8.11 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
Inputs without filtering	100 µs
Inputs with filtering	500 µs

1.9.8.12 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

	Minimum I/O update time
Inputs without filtering	300 µs for all inputs
Inputs with filtering	1 ms

1.10 X20AI2632

1.10.1 General information

1.10.1.1 Other applicable documents

For additional and supplementary information, see the following documents.

Other applicable documents

Document name	Title
MAX20	X20 System user's manual
MAEMV	Installation / EMC guide

1.10.1.2 Order data

Order number	Short description	Figure
	Analog inputs	
X20AI2632	X20 analog input module, 2 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 47: X20AI2632 - Order data

1.10.1.3 Module description

The module is equipped with 2 inputs with 16-bit digital converter resolution and very fast conversion time. It is possible to select between the current and voltage signal using different terminals.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

Functions:

- Scaling
- Filtering
- Error monitoring
- Analysis functions

Scaling

The A/D converter data can optionally be scaled by the user to ensure the greatest possible flexibility.

Input filter

An input filter can be configured for each individual analog input.

Error monitoring

The input signal is monitored for range overshoot, synchronization errors and invalid sampling cycles. User-defined limit values can also be defined.

Analysis functions

In addition to sampling the analog input signal, the values determined can also be analyzed:

- Limit value analysis
- Recording the sampled values
- Trace

1.10.2 Technical description

1.10.2.1 Technical data

Order number	X20AI2632
Short description	
I/O module	2 analog inputs ±10 V or 0 to 20 mA
General information	
B&R ID code	0x1BA0
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using LED status indicator and software
Inputs	Yes, using LED status indicator and software
Channel type	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	1.2 W [1)]
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
UKCA	Yes
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
DNV	Temperature: **B** (0 to 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
LR	ENV1
KR	Yes
ABS	Yes
BV	**EC33B** Temperature: 5 - 55°C Vibration: 4 g EMC: Bridge and open deck
EAC	Yes
KC	Yes
Analog inputs	
Input	±10 V or 0 to 20 mA, via different terminal connections
Input type	Differential input
Digital converter resolution	
Voltage	±15-bit
Current	15-bit
Conversion time	50 µs for all inputs
Output format	INT
Output format	
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0001 = 305.176 µV
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 610.352 nA
Input impedance in signal range	
Voltage	20 MΩ
Current	-
Load	
Voltage	-
Current	<400 Ω
Input protection	Protection against wiring with supply voltage
Permissible input signal	
Voltage	Max. ±30 V
Current	Max. ±50 mA
Output of digital value during overload	
Undershoot	
Voltage	0x8001
Current	0x0000
Overshoot	
Voltage	0x7FFF
Current	0x7FFF
Conversion procedure	SAR
Input filter	Hardware - Third-order low-pass filter / cutoff frequency 10 kHz

Table 48: X20AI2632 - Technical data

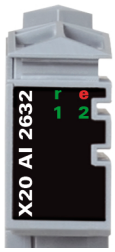
Order number	X20AI2632
Max. error	
Voltage	
Gain	0.08% 2)
Offset	0.01% 3)
Current	
Gain	0.08% 2)
Offset	0.02% 4)
Max. gain drift	
Voltage	0.01%/°C 2)
Current	0.01%/°C 2)
Max. offset drift	
Voltage	0.001%/°C 3)
Current	0.002%/°C 4)
Common-mode rejection	
DC	70 dB
50 Hz	70 dB
Common-mode range	±12 V
Crosstalk between channels	<-70 dB
Nonlinearity	
Voltage	<0.01% 3)
Current	<0.015% 4)
Insulation voltage between channel and bus	500 V_{eff}
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x terminal block X20TB06 or X20TB12 separately. Order 1x bus module X20BM11 separately.
Pitch	$12.5^{+0.2}$ mm

Table 48: X20AI2632 - Technical data

1) To reduce power dissipation, B&R recommends bridging unused inputs on the terminals or configuring them as current signals.
2) Based on the current measured value.
3) Based on the 20 V measurement range.
4) Based on the 20 mA measurement range.

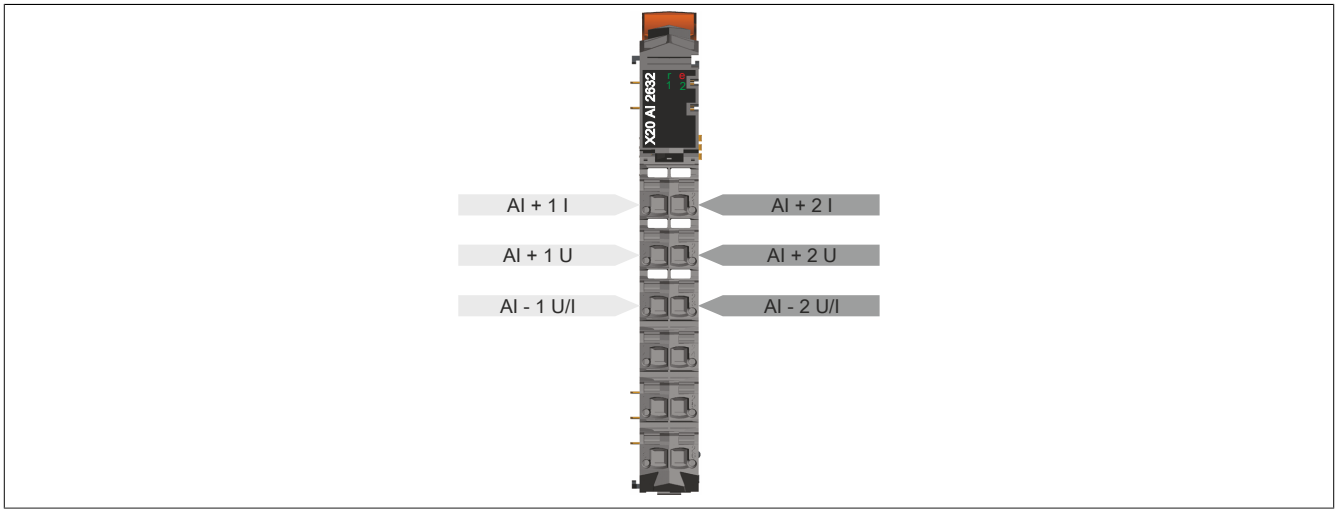
1.10.2.2 LED status indicators

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 System user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Double flash	System error: • Violation of the scan time • Synchronization error
	1 - 2	Green	Off	Open line[2] or sensor is disconnected
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.
2) Open line detection only possible when measuring voltage.

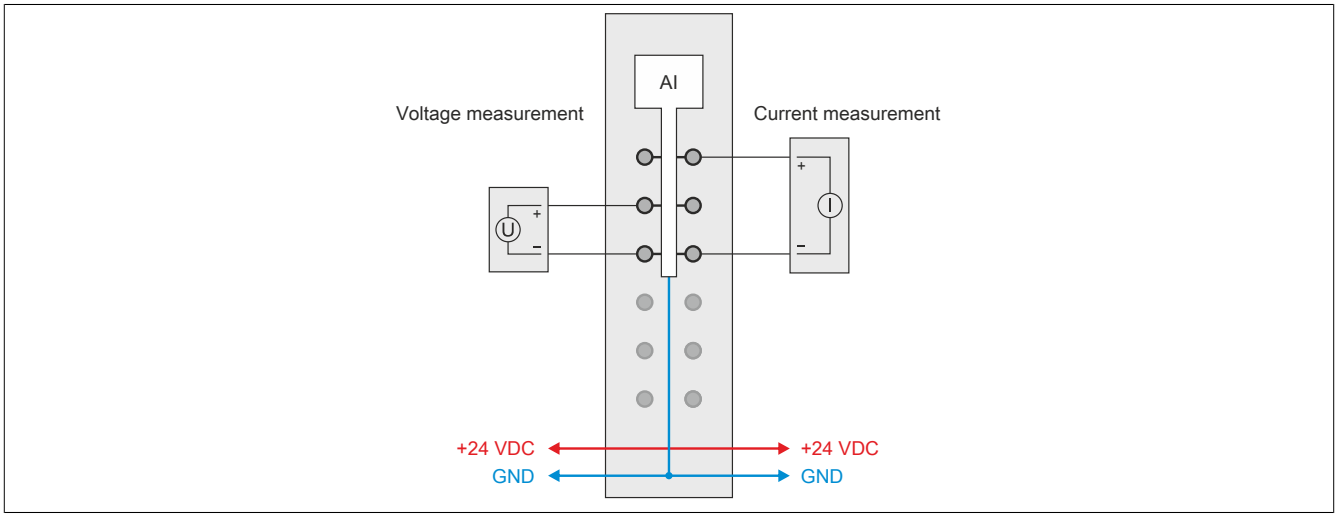
1.10.2.3 Pinout



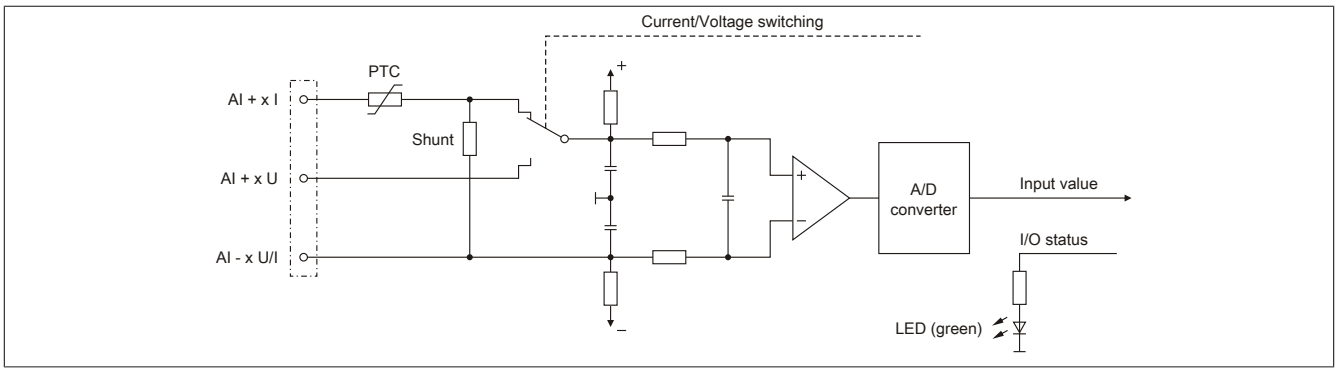
1.10.2.4 Connection example

To prevent disturbances, the following modules must be separated by at least one module:

- Bus receiver X20BR9300
- Supply module X20PS3300/X20PS3310
- Supply module X20PS9400/X20PS9402
- Power supply module X20PS9600/X20PS9602
- Controller



1.10.2.5 Input circuit diagram



1.10.3 Function description

1.10.3.1 Analog inputs

The module is equipped with analog inputs with connected 16-bit A/D converters. Each of the inputs can be configured separately for either voltage or current input for the following ranges:

- Permissible voltage: ±10 V
- Permissible current: 0 to 20 mA

Configuration must take place in addition to using suitable terminals.

> **Information:**
>
> **The register is described in "Channel configuration" on page 267.**

1.10.3.1.1 Scaling

The A/D converter data can optionally be scaled by the user. The following additional registers are available for this:

- Gain = ku
- Offset = du

Scaling calculation:

Scaled value = k * A/C value + d

Gain $k = k_{Calibration} * ku$

Offset $d = d_{Calibration} + du$

The value must be limited since it can exceed the 16-bit constraints. If the application requires a restriction of the range of values, the user can define custom limit values. These are also used for the module's error statistics.

> **Information:**
>
> **Within the module, 32-bit numbers are used for the limit values. A limit value violation can therefore also be detected if the permissible range of values of -32768 to 32767 has been defined.**

> **Information:**
>
> **The registers are described in "User-defined scaling" on page 268.**

1.10.3.1.2 Filtering

If filtering has been enabled, the basic data of the A/D converters is filtered per channel. The filter order and respective cutoff frequency of the low-pass filter can be configured for this.

Internal filter orders greater than 1 are implemented as cascaded first-order filters.

Calculating the cutoff frequency of an nth-order filter:

Cutoff frequency = Cutoff frequency$_{n}$ / ((2 ^ (1 / n) - 1) ^ 0.5)

Approximate calculation

yn = a * xn + b * y(n-1)

a = Sampling time$_{Sec}$ / (Sampling time$_{Sec}$ + 1 / (2 Pi * Cutoff frequency$_{Hz}$))

b = 1 - a

Information:

Since low-pass filtering takes place using an approximation procedure with fixed-point arithmetic, there are discrepancies to the effective cutoff frequency that depend on the sampling cycle and filter sequence.

Information:

The registers are described in "Filtering" on page 267.

1.10.3.2 Error monitoring

There are various counter registers in the module that can be used to record the occurrence of certain errors.

The counters in these registers follow the rules of the event error counter, i.e. each occurrence or reset of an error increases the counter value. The last bit of the counter indicates the error state:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

The following errors are monitored:

- **Synchronization error**
  This error shows how often the conversion task was triggered more than 5 µs after the previous X2X cycle.
- **Invalid sampling cycles**
  This error indicates a cycle time violation. The error occurs if the conversion task triggers a sampling task before the last sampling cycle has been completed.
- **Workspace overshoots**
  This indicates errors outside the maximum possible measurement range of the module.
- **Range undershoots**
  This indicates range undershoots below the value set as "Minimum limit value".
- **Range overshoots**
  This indicates range overshoots above the value set as "Maximum limit value".

Overshoots and undershoots

These counters are only operated if the static error counters are enabled in the channel configuration.

Information:

The registers are described in "Error monitoring and counters" on page 269.

1.10.3.3 Analysis functions

In addition to sampling the analog input signal, this module can also be used to perform additional analysis of the values obtained.

1.10.3.3.1 Limit value analysis

Limit value analysis must be enabled for the desired channel. The sampled value of the channel is then compared with the minimum and maximum values stored internally within the module. If a new measurement period is triggered, the values from the last measuring period can be read out from the registers provided for this purpose.

If limit value analysis has been enabled for a channel, the sampled minimum and maximum values are latched within the module. A measurement period can be triggered via the control byte. If the corresponding configured edge is generated by the application, the limit values of the last measurement period are displayed and the internal latch registers are reset.

Information:

The registers are described in "Limit values" on page 273.

1.10.3.3.2 Recording the sampled values

If the recording of sampled values has been enabled for a channel, the sampled values are also recorded in a module-internal FIFO memory. When the configured event occurs, the contents of the FIFO memory are transmitted to the application.

Information:

Recording of sampled values can only be used if the module is operated on an X2X master that is a type SG4 controller.

The analog signal is sampled in 2 steps.

- **Conversion task**

  The A/D converter digitalizes the inputs signals for the enabled inputs once per conversion cycle. Then the results are available internally in the module. To ensure that this process is executed without delays, the corresponding task will be handled with very high priority.

  The timespan needed for conversion results from the set sampling time.
- **Processing task**

  The converted A/D converter values are further processed according to the user settings (filtering, scaling, limit values, error statistics, min/max analysis, hysteresis comparison). The task for this process has low priority. The timespan needed for further processing depends on the configured functions and is the second portion of the sampling time.

Cycle time violation

In normal operation, further processing is triggered after each conversion. The conversion and sampling tasks run synchronous to one another. If the predefined sampling time is not sufficient to convert all enabled channels and complete the configured functions, a cycle time violation occurs.

Information:

The register is described in "Sampling time" on page 267.

1.10.3.3.3 Trace

If the module is operated on a type SG4 controller, the digitized input values can be recorded by the module. Module monitoring must be enabled to use measured value recording.

Recording must be enabled for the desired channel. The enable bits can then control the recording at runtime. The sampled values are recorded in the module's internal FIFO memory.

If the previously defined state occurs on the channel, the contents of the FIFO memory are transmitted to the application. Whether the FIFO memory continued to be filled depends on how recording is configured.

Information:

The trace mechanism cannot be used if the module is operated behind a bus controller, but only when it is directly connected to the controller.

Information:

The registers are described in "Trace" on page 273.

Library "AsIOTrc" is used to read out the trace data.

Register "TraceChannelEnable" on page 273 determines the structure of the trace buffer.

Example of the structure of the trace buffer:

Both channels of the module are used in this example. Both channels are sampled per trigger and stored one after the other in the trace buffer.

Channel sequence
1
2
1
2
1
2
:

The length of the trace buffer is determined with registers "TraceTriggerStart" on page 277 and "TraceTriggerStop" on page 277.

Parameter "Number of trace buffers" must be defined in Automation Studio in order to configure the trace function block.

1.10.3.3.3.1 Comparator for trigger conditions

In order to adapt the trace as closely as possible to the requirements of the application, the trace function can also be controlled using the comparator. Threshold values (hysteresis) can be defined within the permitted range of values to do so. 2 status bits are then generated for each enabled channel:

- **InRange bit**
  The InRange status is "1" if the measured value falls within the defined limits.
  The InRange status is "0" if the measured value falls outside the defined limits.
- **Threshold value bit**
  The threshold value bit is "1" if the measured value exceeds the upper threshold value.
  The threshold value bit is "0" if the measured value falls below the lower threshold value.

The InRange and threshold bits of all channels are combined in the least significant byte of register CompState-Collection. In addition, the states of the previous sampling are stored in the high-order byte.

The 4 status messages of each channel can be linked via a link mask using AND or OR operators according to the following logic and used as triggers for recordings.

```
delta = (Current_HysteresisStatus ^ NominalValues)// Difference between current status and preset
cond = delta & Selected_HysteresisStatusBits// Eliminate irrelevant status messages
cond = Selected_HysteresisStatusBits (Current_HysteresisStatus ^ NominalValues)
if((0==(cond & ~LogicalOperators)) &&
(0!=(~cond & LogicalOperators))) {=> Generate trigger event}
```

	Corresponds to register:
Selected_HysteresisStatusBits	cfgComp_EnableMask
Current_HysteresisStatus	CompStateCollection
Nominal values	cfgComp_NominalState
Logical operators	cfgComp_ConditionTypeMask

Information:

The registers are described in "Comparator for trigger conditions" on page 275.

1.10.3.3.3.2 Recording measured values

The module has 16 kB available for the trace. The limitation of the FIFO memory means that a maximum of 8192 analog values can be recorded. The memory is divided evenly between the enabled channels. The actual maximum number of possible recordings therefore depends on the number of channels registered for the trace:

1 channel enabled: Maximum 8192 recordings
2 channels enabled: Maximum 4096 recordings per channel

Time-shifted recording

If the recording should be defined with a time offset to the trigger, additional conditions can be defined for shifting the start and stop time.

Information:

The registers are described in "Time-offset trace" on page 277.

1.10.4 Commissioning

1.10.4.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

1.10.4.1.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

1.10.5 Register description

1.10.5.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 System user's manual.

1.10.5.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration - Frame size						
-	AsynSize	-				
Configuration						
257	ConfigOutput01 (channel configuration)	USINT				•
289	ConfigOutput06 (channel configuration)	USINT				•
	Sampling time					
390	ConfigOutput24 (sampling time)	UINT				•
	Filtering					
259	ConfigOutput26 (filter order)	USINT				•
291	ConfigOutput28 (filter order)	USINT				•
262	ConfigOutput27 (filter cutoff frequency)	UINT				•
294	ConfigOutput29 (filter cutoff frequency)	UINT				•
	Scaling					
276	ConfigOutput04 (user-defined gain)	DINT				•
308	ConfigOutput09 (user-defined gain)	DINT				•
284	ConfigOutput05 (user-defined offset)	DINT				•
316	ConfigOutput10 (user-defined offset)	DINT				•
	User-defined limit values					
266	ConfigOutput02 (minimum limit value)	UINT				•
298	ConfigOutput07 (minimum limit value)	UINT				•
270	ConfigOutput03 (maximum limit value)	UINT				•
302	ConfigOutput08 (maximum limit value)	UINT				•
Communication						
0	AnalogInput01	INT	•			
4	AnalogInput02	INT	•			
650	SampleCycleCounter	UINT		•		
	Error monitoring and counters					
641	Channel status	USINT	•			
	Channel01OK	Bit 0				
	Channel02OK	Bit 1				
	SyncStatus	Bit 6				
	ConvertionCycle	Bit 7				
654	SampleCycleViolationErrorCounter	UINT		•		
658	SynchronizationViolationErrorCounter	UINT		•		
2097	Range undershoot and overshoot	USINT	•			
	Channel01underflow	Bit 0				
	Channel02underflow	Bit 1				
	Channel01overflow	Bit 4				
	Channel02overflow	Bit 5				
2099	Workspace overshoot	USINT	•			
	Channel01outofrange	Bit 0				
	Channel02outofrange	Bit 1				
518	Ch01OutOfRange	UINT		•		
550	Ch02OutOfRange	UINT		•		
522	Ch01Underflow	UINT		•		
554	Ch02Underflow	UINT		•		
526	Ch01Overflow	UINT		•		
558	Ch02Overflow	UINT		•		
Additional analysis functions						
133	ConfigOutput21 (trigger condition on falling edge)	USINT				•
135	ConfigOutput22 (trigger condition on rising edge)	USINT				•
129	Analysis control byte	USINT			•	
	TraceTrigger01	Bit 0				
	MinMaxStart01	Bit 4				
	MinMaxStart02	Bit 5				
129	Analysis status byte	USINT	•			
	MinMaxStart01Readback	Bit 4				
	MinMaxStart02Readback	Bit 5				
	Limit values					
530	MinInput01	INT	•			

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
562	MinInput02	INT	•			
534	MaxInput01	INT	•			
566	MaxInput02	INT	•			
538	Ch01MinMaxLatchCounter	UINT		•		
570	Ch02MinMaxLatchCounter	UINT		•		
	Trace configuration					
1026	TraceChannelEnable	USINT				•
1030	TraceSampleDepth	UINT				•
4157	ConfigOutput25 (trace priority)	USINT				•
1037	Enabling the trace function	USINT			•	
	TraceEnable01	Bit 0				
1089	Trace status	USINT	•			
	TraceEnabled	Bit 0				
	TraceWriteActive	Bit 2				
	TraceReadActive	Bit 3				
	ReadyForTrigger	Bit 4				
	TriggerActive	Bit 5				
	TraceOK	Bit 6				
	TraceError	Bit 7				
1094	FreeBufferSize	UINT	•			
1098	TriggerCount	UINT	•			
1102	TriggerFailCount	UINT	•			
	Comparator					
450	cfgComp_LowLimitCh01	INT			(•)	•
458	cfgComp_LowLimitCh02	INT			(•)	•
454	cfgComp_HighLimitCh01	INT			(•)	•
462	cfgComp_HighLimitCh02	INT			(•)	•
662	CompStateCollection	UINT	•			
490	cfgComp_NominalState	UINT				•
482	cfgComp_EnableMask	UINT				•
486	cfgComp_ConditionTypeMask	UINT				•
	Time-offset trace					
1042	TraceTriggerStart	INT				•
1046	TraceTriggerStop	UINT				•

1.10.5.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration - Frame size							
-	-	AsynSize	-				
Configuration							
257	-	ConfigOutput01 (channel configuration)	USINT				•
289	-	ConfigOutput06 (channel configuration)	USINT				•
	Sampling time						
390	-	ConfigOutput24 (sampling time)	UINT				•
	Filtering						
259	-	ConfigOutput26 (filter order)	USINT				•
291	-	ConfigOutput28 (filter order)	USINT				•
262	-	ConfigOutput27 (filter cutoff frequency)	UINT				•
294	-	ConfigOutput29 (filter cutoff frequency)	UINT				•
	Scaling						
276	-	ConfigOutput04 (user-defined gain)	DINT				•
308	-	ConfigOutput09 (user-defined gain)	DINT				•
284	-	ConfigOutput05 (user-defined offset)	DINT				•
316	-	ConfigOutput10 (user-defined offset)	DINT				•
	User-defined limit values						
266	-	ConfigOutput02 (minimum limit value)	UINT				•
298	-	ConfigOutput07 (minimum limit value)	UINT				•
270	-	ConfigOutput03 (maximum limit value)	UINT				•
302	-	ConfigOutput08 (maximum limit value)	UINT				•
Communication							
0	0	AnalogInput01	INT	•			
4	2	AnalogInput02	INT	•			
650	-	SampleCycleCounter	UINT		•		
	Error monitoring and counters						
641	-	Channel status	USINT		•		
		Channel01OK	Bit 0				
		Channel02OK	Bit 1				
		SyncStatus	Bit 6				
		ConvertionCycle	Bit 7				
654	-	SampleCycleViolationErrorCounter	UINT		•		
658	-	SynchronizationViolationErrorCounter	UINT		•		
2097	-	Range undershoot and overshoot	USINT		•		
		Channel01underflow	Bit 0				
		Channel02underflow	Bit 1				
		Channel01overflow	Bit 4				
		Channel02overflow	Bit 5				
2099	-	Workspace overshoot	USINT		•		
		Channel01outofrange	Bit 0				
		Channel02outofrange	Bit 1				
518	-	Ch01OutOfRange	UINT		•		
550	-	Ch02OutOfRange	UINT		•		
522	-	Ch01Underflow	UINT		•		
554	-	Ch02Underflow	UINT		•		
526	-	Ch01Overflow	UINT		•		
558	-	Ch02Overflow	UINT		•		
Additional analysis functions							
133	-	ConfigOutput21 (trigger condition on falling edge)	USINT				•
135	-	ConfigOutput22 (trigger condition on rising edge)	USINT				•
129	-	Analysis control byte	USINT				•
		TraceTrigger01	Bit 0				
		MinMaxStart01	Bit 4				
		MinMaxStart02	Bit 5				
129	-	Analysis status byte	USINT		•		
		MinMaxStart01Readback	Bit 4				
		MinMaxStart02Readback	Bit 5				
	Limit values						
530	-	MinInput01	INT		•		
562	-	MinInput02	INT		•		
534	-	MaxInput01	INT		•		
566	-	MaxInput02	INT		•		
538	-	Ch01MinMaxLatchCounter	UINT		•		
570	-	Ch02MinMaxLatchCounter	UINT		•		

1) The offset specifies the position of the register within the CAN object.

1.10.5.4 Configuration

1.10.5.4.1 Channel configuration

Name:
ConfigOutput01 for channel 1
ConfigOutput06 for channel 2

The individual inputs for processing the current or voltage signal are configured in these registers. This configuration must be made in addition to using suitable terminals.

Filtering, analysis and error monitoring (bits 4 to 6) can only be used if the channel is enabled (bit 7 = 0).

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	Terminal selector	0	Voltage terminal for ±10 VDC (bus controller default setting)
		1	Current terminal for 0 to 20 mA
1	Gain selector	0	Voltage ±10 VDC (bus controller default setting)
		1	Current 0 to 20 mA
2 - 3	Reserved	-	
4	Filtering active	0	Inactive (bus controller default setting)
		1	Active
5	Minimum/Maximum analysis active	0	Inactive (bus controller default setting)
		1	Active
6	Error monitoring active	0	Inactive (bus controller default setting)
		1	Active
7	Enables channel	0	Channel enabled (bus controller default setting)
		1	Channel disabled

1.10.5.4.2 Sampling time

Name:
ConfigOutput24

The sampling time is set to µs in this register. This makes it possible to improve the sampling cycle (resolution = 1 µs). The lowest configurable cycle time is 50 µs.

Data type	Value	Information
UINT	50 to 10,000	Bus controller default setting: 100

Information:

Values that are too low for the cycle time will result in cycle time violations.

1.10.5.4.3 Filtering

1.10.5.4.3.1 Filter order

Name:
ConfigOutput26 for channel 1
ConfigOutput28 for channel 2

The filter order is specified in this register. The "Filter cutoff frequency" on page 268 register is used to configure the respective cutoff frequency of the filter.

Data type	Value	Information
USINT	1 to 4	Bus controller default setting: 0

1.10.5.4.3.2 Filter cutoff frequency

Name:
ConfigOutput27 for channel 1
ConfigOutput29 for channel 2

The cutoff frequency of the respective filter is configured in these registers.

Data type	Value	Information
UINT	1 to 65,535	Cutoff frequency in hertz. Bus controller default setting: 0

Information:

The highest cutoff frequency is limited by the Nyquist Shannon sampling theorem (based on the sampling cycle time). The system does not check for violations of this sampling theorem.

1.10.5.4.4 User-defined scaling

1.10.5.4.4.1 User-defined gain

Name:
ConfigOutput04 for channel 1
ConfigOutput09 for channel 2

The user-defined gain for the A/D converter data of the respective physical channel can be specified in these registers.

The value 65536 (0x10000) corresponds to a gain of 1.

Data type	Values	Information
DINT	-2,147,483,648 to 2,147,483,647	Bus controller default setting: 65536

1.10.5.4.4.2 User-defined offset

Name:
ConfigOutput05 for channel 1
ConfigOutput10 for channel 2

The user-defined offset for the A/D converter data of the respective physical channel can be specified in this register.

The value 65536 (0x10000) corresponds to an offset of 1.

Data type	Values	Information
DINT	-2,147,483,648 to 2,147,483,647	Bus controller default setting: 0

1.10.5.4.5 User-defined limit values

1.10.5.4.5.1 Minimum limit value

Name:
ConfigOutput02 for channel 1
ConfigOutput07 for channel 2

The minimum limit value is configured in this register. This limit value is also used for the undershoot error statistics (see register "Ch0xUnderflow" on page 271).

Data type	Values	Information
INT	-32768 to 32767	Bus controller default setting: -32768

1.10.5.4.5.2 Maximum limit value

Name:
ConfigOutput03 for channel 1
ConfigOutput08 for channel 2

The maximum limit value is configured in this register. This limit value is also used for the overflow error statistics (see register "Ch0xOverflow" on page 271).

Data type	Values	Information
INT	-32767 to 32767	Bus controller default setting: 32767

1.10.5.5 Communication - General

The analog inputs of the module convert the current or voltage values with a resolution of 16 bits. The information can be used by the application via the registers described here.

1.10.5.5.1 Analog inputs

Name:
AnalogInput01 to AnalogInput02

The analog input value is mapped in this register depending on the configured operating mode.

Data type	Value	Input signal
INT	-32,768 to 32,767	Voltage signal ±10 VDC
	0 to 32,767	Current signal 0 to 20 mA

1.10.5.5.2 Sampling cycle counter

Name:
SampleCycleCounter

The number of times the input signal has been sampled is provided in this register.

Data type	Values
UINT	0 to 65535

1.10.5.6 Error monitoring and counters

1.10.5.6.1 Channel status

Name:
Channel01OK to Channel02OK
SyncStatus
ConvertionCycle

This register collects error messages synchronously with the network cycle. Temporary error states that were registered in a conversion cycle remain active for at least 2 network cycles. In order to receive detailed error information, the corresponding error counters and X2X network events should also be observed.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01OK	0	OK
		1	Errors
1	Channel02OK	0	OK
		1	Errors
2 - 5	Reserved	-	
6	SyncStatus[1)]	0	OK
		1	Not synchronized
7	ConvertionCycle[2)]	0	OK
		1	Errors

1) Identical to bit 0 of the registers "SynchronizationViolationErrorCounter" on page 270.
2) Identical to bit 0 of the registers "SampleCycleViolationErrorCounter" on page 270.

1.10.5.6.2 Workspace overshoot

Name:
Channel01outofrange to Channel02outofrange

This register indicates whether the input value overshoots the module's maximum measurement range. The individual bits in this register are identical to the value of the lowest bit of register "Ch0xOutOfRange" on page 271.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01outofrange	0	No error
		1	Working range violation (pos.) of channel 1
1	Channel02outofrange	0	No error
		1	Working range violation (pos.) of channel 2
2 - 7	Reserved	-	

1.10.5.6.3 Range undershoot and overshoot

Name:
Channel01underflow to Channel02underflow
Channel01overflow to Channel02overflow

This register indicates whether the limit values defined by registers "Minimum limit value" on page 268 and "Maximum limit value" on page 268 have been overshot or undershot. The individual bits in this register are identical to the value of the lowest bit of registers "Ch0xUnderflow" on page 271 and "Ch0xOverflow" on page 271.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01underflow	0	No error
		1	Range exceeded (.neg) on channel 1
1	Channel02underflow	0	No error
		1	Range exceeded (.neg) on channel 2
2 - 3	Reserved	-	
4	Channel01overflow	0	No error
		1	Range exceeded (.pos) on channel 1
5	Channel02overflow	0	No error
		1	Range exceeded (.pos) on channel 2
6 - 7	Reserved	-	

1.10.5.6.4 Counter for synchronization errors

Name:
SynchronizationViolationErrorCounter

This register counts how often the conversion task was triggered more than 5 µs after the next-coming X2X cycle. In this case, the module is considered being no longer synchronized with X2X Link.

Data type	Value	Information[1)]
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

1) For details, see "Error monitoring" on page 259.

1.10.5.6.5 Counter for faulty sampling cycles

Name:
SampleCycleViolationErrorCounter

This register is used to indicate the number of cycle time violations that have occurred thus far. A cycle time violation occurs if the conversion tasks initiates a sampling task before the last sampling cycle has finished. See "Recording the sampled values" on page 260.

Data type	Value	Information[1)]
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

1) For details, see "Error monitoring" on page 259.

1.10.5.6.6 Counter for workspace overshoots

Name:
Ch01OutOfRange to Ch02OutOfRange

This register indicates errors outside the maximum possible measurement range of the module. These errors result in a final deflection of the A/D converter.

Data type	Value	Information[1)]
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

1) For details, see "Error monitoring" on page 259.

1.10.5.6.7 Counter for range exceeded violations (neg.)

Name:
Ch01Underflow to Ch02Underflow

This register indicates the range undershoots below the value set in register "Minimum limit value" on page 268.

Data type	Value	Information[1)]
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

1) For details, see "Error monitoring" on page 259.

1.10.5.6.8 Counter for range exceeded violations (pos.)

Name:
Ch01Overflow to Ch02Overflow

This register indicates the range overshoots above the value set in register "Maximum limit value" on page 268.

Data type	Value	Information[1)]
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

1) For details, see "Error monitoring" on page 259.

1.10.5.7 Analysis functions

In addition to sampling the analog input signal, this module can also be used to perform additional analysis of the values obtained.

1.10.5.7.1 Trigger condition on falling edge

Name:
ConfigOutput21

This register can be used to configure whether the falling edge is used to trigger the trace and determine the input value in register "Analysis control byte" on page 272.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	No trigger (bus controller default setting)
		1	Falling edge active as trigger
1 - 3	Reserved	-	
4	MinMaxStart01	0	No determination (bus controller default setting)
		1	Falling edge determines input value of channel 1
5	MinMaxStart02	0	No determination (bus controller default setting)
		1	Falling edge determines input value of channel 2
6 - 7	Reserved	0	

1.10.5.7.2 Trigger condition on rising edge

Name:
ConfigOutput22

This register can be used to configure whether the rising edge is used to trigger the trace and determine the input value in register "Analysis control byte" on page 272.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	Trigger not initiated on positive edge (bus controller default setting)
		1	Rising edge active as trigger
1 - 3	Reserved	-	
4	MinMaxStart01	0	No determination (bus controller default setting)
		1	Rising edge determines input value of channel 1
5	MinMaxStart02	0	No determination (bus controller default setting)
		1	A positive edge determines the input value of channel 2.
6 - 7	Reserved	0	

1.10.5.7.3 Analysis control byte

Name:
TraceTrigger01
MinMaxStart01 to MinMaxStart02

The trace function and determination of the minimum/maximum input values can be started in this register. Whether the rising and/or falling edge is used to trigger the functions can be configured using the registers "Trigger condition on falling edge" on page 271 and "Trigger condition on rising edge" on page 272.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	Trigger/Trace not triggered (bus controller default setting)
		1	Initiates trigger/trace
1 - 3	Reserved	-	
4	MinMaxStart01	0	Determination not triggered (bus controller default setting)
		1	Determination of the input value of channel 1 is triggered.
5	MinMaxStart02	0	Determination not triggered (bus controller default setting)
		1	Determination of the input value of channel 2 is triggered.
6 - 7	Reserved	-	

Information:

To reduce the cyclic data transfer, this register combines the trace and limit value determination functions.

1.10.5.7.4 Analysis status byte

Name:
MinMaxStart01Readback to MinMaxStart02Readback

The currently requested module-internal analyses can be checked in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Reserved	-	
4	MinMaxStart01Readback	0 or 1	Current state of the trigger bits for determining the limit values on channel 1
5	MinMaxStart02Readback	0 or 1	Current state of the trigger bits for determining the limit values on channel 2
6 - 7	Reserved	-	

1.10.5.8 Limit values

1.10.5.8.1 Minimum input values

Name:
MinInput01 to MinInput02

The minimum value of the preceding trigger period is saved in this register based on the filtered, scaled and user-defined limit values. The register value is 0 if the channel is inactive.

Data type	Value
INT	-32,768 to 32,767

1.10.5.8.2 Maximum input values

Name:
MaxInput01 to MaxInput02

The maximum value of the preceding trigger period is saved in this register based on the filtered, scaled and user-defined limit values. The register value is 0 if the channel is inactive.

Data type	Value
INT	-32,768 to 32,767

1.10.5.8.3 Limit value trigger counter

Name:
Ch01MinMaxLatchCounter to Ch02MinMaxLatchCounter

The number of valid events that trigger a new measurement period for the limit value analysis is counted in this register.

Data type	Value
UINT	0 to 65535

1.10.5.9 Trace

1.10.5.9.1 Enabling channels

Name:
TraceChannelEnable

The respective channel is enabled for the trace with this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Channel disabled
		1	Channel enabled
1	Channel 2	0	Channel disabled
		1	Channel enabled
2 - 7	Reserved	-	

1.10.5.9.2 Trace FIFO configuration

Name:
TraceSampleDepth

The module has 16 kB available for the trace. The limitation of the FIFO memory means that a maximum of 8192 analog values can be recorded. The memory is divided evenly between the enabled channels. The actual maximum number of possible recordings therefore depends on the number of channels registered for the trace.

Data type	Value
UINT	2 to 8192

1.10.5.9.3 Trace priority

Name:
ConfigOutput25

The priority of the trace can be increased with this register.

Data type	Value	Function
USINT	3	Standard
	6	Trace priority higher than X2X Link communication

1.10.5.9.4 Enabling the trace function

Name:

TraceEnable01

This register can be used to enable recording according to the edge control or comparator specifications.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	TraceEnable01	0	Disables the trace function
		1	Enables the trace function
1 - 7	Reserved	-	

1.10.5.9.5 Trace status

Name:
TraceEnabled
TraceWriteActive
TraceReadActive
ReadyForTrigger
TriggerActive
TraceOk
TraceError

The status of the trace is represented in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	TraceEnabled	0	Trace inactive
		1	Trace active
1	Reserved	-	
2	TraceWriteActive	0	Data not recorded
		1	Data recorded
3	TraceReadActive	0	Data not output/read
		1	Data output/read
4	ReadyForTrigger	0	Not ready for triggering
		1	Ready for triggering
5	TriggerActive	0	No trigger active or already executed
		1	Trigger active
6	TraceOk	0	Overflow or inactive
		1	No overflow
7	TraceError	0	No error or inactive
		1	Trace buffer full

1.10.5.9.6 Free trace buffer

Name:
FreeBufferSize

Specifies the free FIFO memory area for the trace in bytes.

Data type	Values
UINT	0 to 65535

1.10.5.9.7 Counter for trigger events

Name:
TriggerCount

This register indicates the number of trigger events that have occurred since the start of the recording.

Data type	Values
UINT	0 to 65535

1.10.5.9.8 Counter for invalid trigger events

Name:
TriggerFailCount

Counts the trigger events for which the trace could not be carried out.

Data type	Values
UINT	0 to 65535

1.10.5.9.9 Comparator for trigger conditions

1.10.5.9.9.1 Lower limit value for hysteresis

Name:
cfgComp_LowLimitCh01 to cfgComp_LowLimitCh02

The lower limit value for hysteresis is configured in this register.

Data type	Values
INT	-32768 to 32767

1.10.5.9.9.2 Upper limit value for hysteresis

Name:
cfgComp_HighLimitCh01 to cfgComp_HighLimitCh02

The upper limit value for hysteresis is configured in this register.

Data type	Values
INT	-32768 to 32767

1.10.5.9.9.3 Hysteresis status of the channels

Name:
CompStateCollection

The hysteresis status of the input channels for the current and last cycle are represented in this register.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
1	Channel01 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
2	Channel02 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
3	Channel02 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
4 - 7	Reserved	-	
8	Channel01 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
9	Channel01 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
10	Channel02 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
11	Channel02 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
12 - 15	Reserved	-	

1.10.5.9.9.4 Comparison state of the channels

Name:
cfgComp_NominalState

The desired comparison state for the hysteresis status is indicated in this register.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
1	Channel01 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
2	Channel02 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
3	Channel02 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
4 - 7	Reserved	-	
8	Channel01 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
9	Channel01 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
10	Channel02 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
11	Channel02 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
12 - 15	Reserved	-	

Information:

This is a positive list. This means that recording starts as soon as the current status message assumes the state specified here.

Whether one match is sufficient or whether several matches are required depends on the selection of the relevant hysteresis status bits and logical operators.

1.10.5.9.9.5 Selecting the relevant hysteresis status bits

Name:
cfgComp_EnableMask

This register can be used to select which status bits of the hysteresis comparison should be used to generate the trigger.

For more information about using this register, see "Comparator for trigger conditions" on page 262.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Do not use
		1	Use for generation
1	Channel01 InRange status in the current cycle	0	Do not use
		1	Use for generation
2	Channel02 hysteresis status in the current cycle	0	Do not use
		1	Use for generation
3	Channel02 InRange status in the current cycle	0	Do not use
		1	Use for generation
4 - 7	Reserved	-	
8	Channel01 hysteresis status in the last cycle	0	Do not use
		1	Use for generation
9	Channel01 InRange status in the last cycle	0	Do not use
		1	Use for generation
10	Channel02 hysteresis status in the last cycle	0	Do not use
		1	Use for generation
11	Channel02 InRange status in the last cycle	0	Do not use
		1	Use for generation
12 - 15	Reserved	-	

1.10.5.9.9.6 Logical connective operators for hysteresis status bits

Name:
cfgComp_ConditionTypeMask

This register is used to select the desired operators of the states with which the status bits are linked with one another to generate a trigger.

At least one OR operation must be configured, but it does not necessarily have to be located on a channel configured with "1" in the "cfgComp_EnableMask" on page 276 register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Use AND operation
		1	Use OR operation
1	Channel01 InRange status in the current cycle	0	Use AND operation
		1	Use OR operation
2	Channel02 hysteresis status in the current cycle	0	Use AND operation
		1	Use OR operation
3	Channel02 InRange status in the current cycle	0	Use AND operation
		1	Use OR operation
4 - 7	Reserved	-	
8	Channel01 hysteresis status in the last cycle	0	Use AND operation
		1	Use OR operation
9	Channel01 InRange status in the last cycle	0	Use AND operation
		1	Use OR operation
10	Channel02 hysteresis status in the last cycle	0	Use AND operation
		1	Use OR operation
11	Channel02 InRange status in the last cycle	0	Use AND operation
		1	Use OR operation
12 - 15	Reserved	-	

1.10.5.9.10 Time-offset trace

1.10.5.9.10.1 Starting the trace

Name:
TraceTriggerStart

The relative start position in relation to the configured trigger condition (pos./neg. edge) is defined in this register. Positive values mean that recording begins x samplings after the trigger condition. Negative values mean that the recording starts x samplings before the trigger condition.

With value -32768, recording is started immediately when the trace is enabled.

Data type	Value	Information
INT	-32767 to 32767	
	-32768	Continuous trace without a stopping point

1.10.5.9.10.2 Stopping the trace

Name:
TraceTriggerStop

The relative unsigned stop position in relation to the configured trigger condition is defined in this register.

- When configuring an early recording start, this value refers to the trigger event.
- When configuring a delayed start of recording, the value refers to the start of recording.

Data type	Values
UINT	0 to 65535

1.10.5.10 Acyclic frame size

Name:
AsynSize

When using the stream, the data is exchanged internally between the module and controller. A defined number of acyclic bytes is reserved for this slot for this purpose.
Increasing the acyclic frame size results in increased data throughput on this slot.

Information:

This configuration involves a driver setting that cannot be changed during runtime!

Data type	Values	Information
-	8 to 28	Acyclic frame size in bytes. Default = 24

1.10.5.11 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Standard priority	200 µs
High priority with trace function	300 µs

1.10.5.12 Minimum I/O update time

There is no limitation or dependency on the bus cycle time.

The I/O update time is defined using the "Sampling time" register. The fastest possible sampling time depends on the number of channels to be converted and the configuration.

1.11 X20AI2636

1.11.1 General information

1.11.1.1 Other applicable documents

For additional and supplementary information, see the following documents.

Other applicable documents

Document name	Title
MAX20	X20 System user's manual
MAEMV	Installation / EMC guide

1.11.1.2 Order data

Order number	Short description	Figure
	Analog inputs	
X20AI2636	X20 analog input module, 2 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oversampling functions	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 49: X20AI2636 - Order data

1.11.1.3 Module description

The module is equipped with 2 inputs with 16-bit digital converter resolution. It is possible to select between the current and voltage signal using different terminals.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

Functions:

- Physical values
- Logical values
- Oversampling
- Monitoring the inputs

Physical values

The conversion results of the analog inputs are scaled and filtered before being transferred to the higher-level system.

Logical values

The physical values can be further processed using mathematical functions and comparators. Another logical channel can also be used as a starting point for further processing for a logical function.

Oversampling

The input values of the enabled channels are stored in the module in a configurable interval independently of the X2X cycle. The memory depth is 16 analog values per physical and logical channel.

Monitoring the input signal

The input signal of the analog inputs is monitored for out-of-range, for upper and lower limit values and for filter errors.

1.11.2 Technical description

1.11.2.1 Technical data

Order number	X20AI2636
Short description	
I/O module	2 analog inputs ±10 V or 0 to 20 mA
General information	
B&R ID code	0xB3A7
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using LED status indicator and software
Inputs	Yes, using LED status indicator and software
Channel type	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	1.2 W [1)]
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
UKCA	Yes
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
DNV	Temperature: **B** (0 to 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
LR	ENV1
KR	Yes
ABS	Yes
BV	**EC33B** Temperature: 5 - 55°C Vibration: 4 g EMC: Bridge and open deck
EAC	Yes
KC	Yes
Analog inputs	
Input	±10 V or 0 to 20 mA, via different terminal connections
Input type	Differential input
Digital converter resolution	
Voltage	±15-bit
Current	15-bit
Conversion time	40 µs for all inputs
Output format	INT
Output format	
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0001 = 305.176 µV
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 610.352 nA
Input impedance in signal range	
Voltage	20 MΩ
Current	-
Load	
Voltage	-
Current	<400 Ω
Input protection	Protection against wiring with supply voltage
Permissible input signal	
Voltage	Max. ±30 V
Current	Max. ±50 mA
Output of digital value during overload	
Undershoot	
Voltage	0x8001
Current	0x0000
Overshoot	
Voltage	0x7FFF
Current	0x7FFF
Conversion procedure	SAR
Input filter	Hardware - Third-order low-pass filter / cutoff frequency 10 kHz

Table 50: X20AI2636 - Technical data

Order number	X20AI2636
Max. error	
Voltage	
Gain	0.08% 2)
Offset	0.01% 3)
Current	
Gain	0.08% 2)
Offset	0.02% 4)
Max. gain drift	
Voltage	0.01%/°C 2)
Current	0.01%/°C 2)
Max. offset drift	
Voltage	0.001%/°C 3)
Current	0.002%/°C 4)
Common-mode rejection	
DC	70 dB
50 Hz	70 dB
Common-mode range	±12 V
Crosstalk between channels	<-70 dB
Nonlinearity	
Voltage	<0.01% 3)
Current	<0.015% 4)
Insulation voltage between channel and bus	500 V_{eff}
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x terminal block X20TB06 or X20TB12 separately. Order 1x bus module X20BM11 separately.
Pitch	$12.5^{+0.2}$ mm

Table 50: X20AI2636 - Technical data

1) To reduce power dissipation, B&R recommends bridging unused inputs on the terminal.
2) Based on the current measured value.
3) Based on the 20 V measurement range.
4) Based on the 20 mA measurement range.

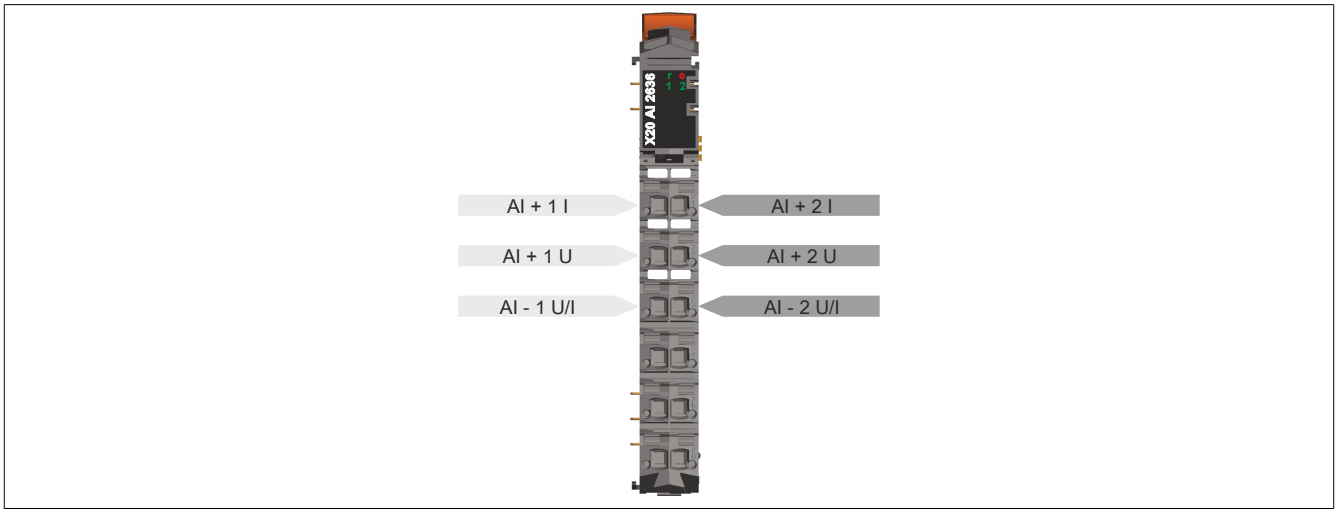
1.11.2.2 LED status indicators

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 System user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Double flash	System error: • Violation of the scan time • Synchronization error
	1 - 2	Green	Off	Open line[2] or sensor is disconnected
			Blinking	Channel error: Underflow, overflow or broken connection
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.
2) Open line detection only possible when measuring voltage.

1.11.2.3 Pinout

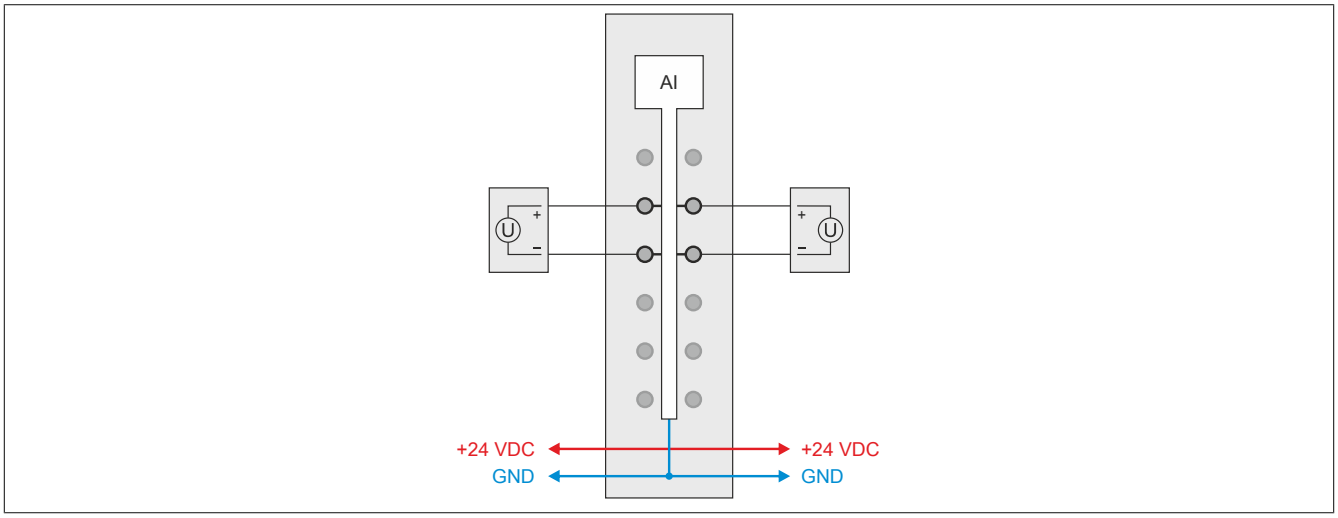


1.11.2.4 Connection example

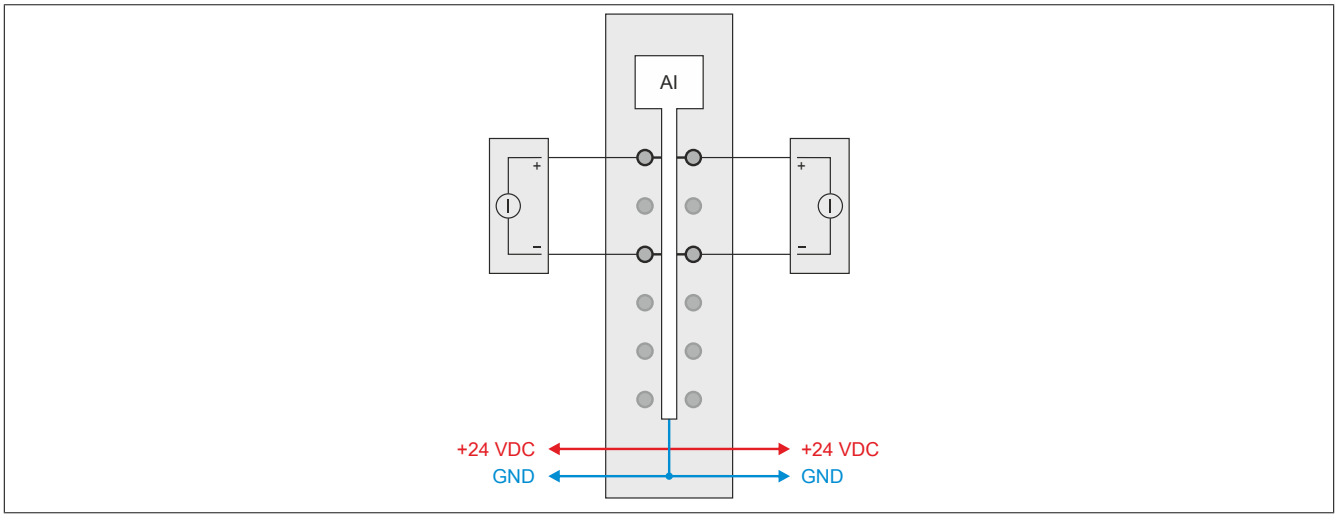
To prevent disturbances, the following modules must be separated by at least one module:

- Bus receiver X20BR9300
- Supply module X20PS3300/X20PS3310
- Supply module X20PS9400/X20PS9402
- Power supply module X20PS9600/X20PS9602
- Controller

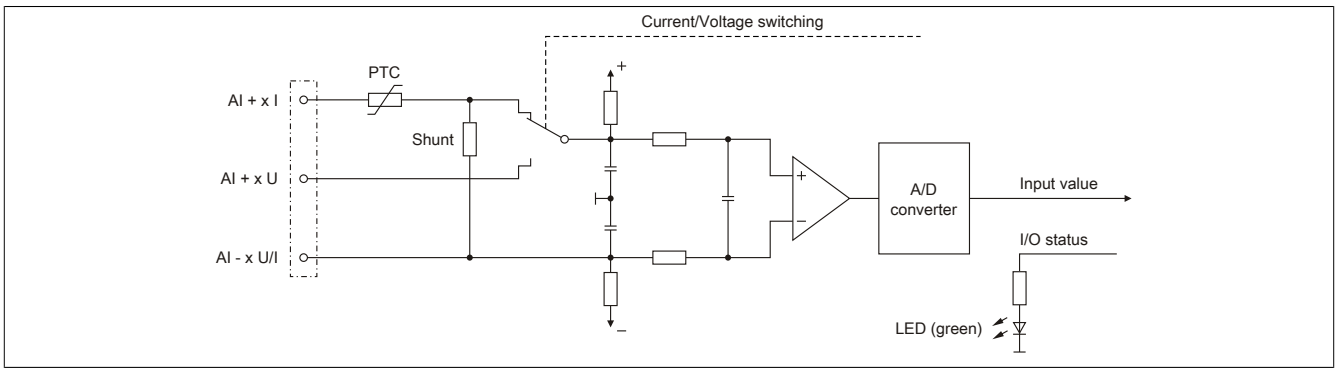
Voltage measurement



Current measurement



1.11.2.5 Input circuit diagram



1.11.3 Function description

1.11.3.1 Operating modes

1.11.3.1.1 Standard - Oversampling

The input values are recorded with a configurable sampling cycle time and saved with timestamp to the internal physical data buffer. This data range can then be read out in the cyclic data transfer using a configurable data length.

The recording and transmission system for the logical channels is identical to that for the physical channels. The functions of the logical channels are also executed in the configured sampling cycle time and saved with timestamp to the logical data buffer. The values can also be read out from here using configurable cyclic data points.

The defined sampling cycle time may not be sufficient for the sum of all physical and logical functions if using fast X2X Link cycle times, however. If influencing the physical sampling is not permitted, then a prescaler can be used to slow down the logical processing.

> **Information:**
>
> **The ability to adjust the sampling cycle time as needed on the module means there is basically no synchronization with X2X Link, regardless of whether standard inputs or an oversampling function is configured.**
>
> **If synchronization is required, then the configured sampling cycle time must be a multiple of the X2X Link cycle time!**

1.11.3.1.2 Bus controller

The module is operated as a normal analog input module in this mode. The input values are measured with a configurable sampling cycle time and saved in the internal physical data buffer with timestamp. Only the latest value is transferred in the next possible bus cycle.

It is possible to assign a logical function directly to each input channel, however. The analog data on the bus controller is mapped using the calculation options of the logical channels and configured automatically, see "Operation in the standard function model" on page 292.

Function model "Bus controller" has the following limitations compared to function model Standard:

- No oversampling function since consistency is not possible due to the small data range when operating on CAN-based bus controllers
- The sampling cycle time is set to 100 µs.
- No timestamp function
- A selection of logical functions is available with which the physical values can already be processed on the module:
    - Physical value output (standard)
    - Addition of two channels with scaling
    - Integral addition of two channels with scaling
    - Multiplication of two channels with scaling
    - Integral multiplication of two channels with scaling

1.11.3.2 Oversampling

1.11.3.2.1 Analog oversampling

With analog oversampling, the enabled channels are stored in the module in a configurable interval independently of the X2X cycle. The memory depth is 16 analog values per physical and logical channel.

These samplings are numbered from 1 to 16 in the registers. The conversions or calculations of the individual channels with the same number (i.e. sample line 1 to 16, e.g. PhysCh01Sample**10**, PhysCh02Sample**10**) originate from the same sampling cycle or logical calculation cycle and therefore have the same timestamp.

The timestamp refers to the newest data value, i.e. always to sample line 1. If a timestamp for older data points is needed, it needs to be back-calculated in the application using the sampling cycle time configured on the module. The prescaler must also be taken into account for logical channels.

Calculation example

Sample line	Calculation	
1	Timestamp	**Newest value**
2	Timestamp - Sampling cycle time	
3	Timestamp - 2 * Sampling cycle time	
4	Timestamp - 3 * Sampling cycle time	
...	...	
10	Timestamp - 9 * Sampling cycle time	
...	...	
16	Timestamp - 15 * Sampling cycle time	**Oldest value**

How the buffer is organized can be seen from this. This is not a FIFO buffer but a static buffer that the values are pushed through. Sample line 1 always contains the newest values, the next line the second newest, all the way up to sample line 16, which contains the oldest values.

The sample counter is a circular counter, with the number of new sample lines derived from the value of the last transfer cycle.

Example

A difference of 3 to the last transfer cycle means:

The data in sample line 1 and all subsequent data from the previous transfer cycle is now shifted in the current cycle beginning with sample line 4. Sample lines 1 through 3 contain the new values for further processing by the application. Sample lines 14 through 16 from the last transfer cycle are no longer in the buffer.

1.11.3.2.2 Comparator oversampling

With comparator oversampling, the results of the enabled channels are stored in the module in a configurable interval independently of the X2X cycle. The memory depth is 16 bits per logical channel.

These samplings, i.e. the result bits, are numbered consecutively from 1 to 8 and 9 to 16 for the two registers. The results of the individual channels with the same number (i.e. sample line 1 to 16, e.g. LogicCh01Sample**16_9**, LogicCh01Sample**8_1** for channel 1) originate from the same sampling cycle or logical calculation cycle and therefore have the same timestamp.

The timestamp refers to the latest data value, so always to sample line 1, i.e. bit 0 in register "LogicCh01Sample8_1". If a timestamp for the older comparator results is needed, this must be recalculated in the application using the sampling cycle time set on the module. The prescaler setting must also be taken into account.

Calculation example

Sample line	(register name)	Calculation	
1	(LogicCh01Sample8_1 bit 0)	Timestamp	**Newest value**
2	(LogicCh01Sample8_1 bit 1)	Timestamp - Sampling cycle time	
3	(LogicCh01Sample8_1 bit 2)	Timestamp - 2 * Sampling cycle time	
4	(LogicCh01Sample8_1 bit 3)	Timestamp - 3 * Sampling cycle time	
...			
10	(LogicCh01Sample16_9 bit 1)	Timestamp - 9 * Sampling cycle time	
...			
16	(LogicCh01Sample16_9 bit 7)	Timestamp - 15 * Sampling cycle time	**Oldest value**

How the buffer is organized can be seen from this. This is not a FIFO buffer but a static buffer that the values are pushed through. Sample line 1 always contains the newest values, the next line the second newest, all the way up to sample line 16, which contains the oldest values.

The sample counter is a circular counter, with the number of new sample lines derived from the value of the last transfer cycle.

Example

A difference of 3 to the last transfer cycle means:

The comparator result in sample line 1 and all subsequent data from the previous transfer cycle is now shifted in the current cycle beginning with sample line 4. Sample lines 1 through 3 contain the new bit values for further processing by the application. Sample lines 14 through 16 from the last transfer cycle are no longer in the buffer.

1.11.3.2.3 Priorities and values

Priority of logical oversampling

- Low priority setting
  Preparation of the logical and physical buffer does not run in the same context. If the calculation time in logical oversampling is longer than the set sampling cycle time, this setting and a prescaler >1 can be used to split the logical processing over several sampling cycle times. The sample lines of the physical and logical oversampling therefore do not automatically have the same recording or calculation time. If the prescaler is configured incorrectly, logical oversampling cannot be processed successfully.
- High priority setting
  The logical and physical buffers are prepared in the same context. The sample lines of the physical and logical oversampling have the same recording or calculation time. All configured functions must be able to be executed in the set sampling cycle time; otherwise, a cycle time violation will occur and the configuration must be changed accordingly. The setting of the logical prescaler has no influence here; only the data volume in logical oversampling is limited.

Current or referenced values for logical or physical oversampling

In a busy system, jitter can occur in the sampling cycle on the module even with synchronous cycle time settings due to the necessary processing of the functions (X2X Link operation, logical and physical oversampling). This results in a different number of sample lines in the same time frames. For this reason, more samples should be configured in the cyclic image as well than is mathematically necessary.

- Current values setting
  The sample lines are transferred to the higher-level system as quickly as possible, with more or fewer new sample lines possibly occurring.
- Referenced values setting
  With this setting, jitter is minimized and a constant number of new sample lines per cycle is achieved with the optimal setting. With regard to response time, however, there may be delays of several sampling cycle times.

Information:

The register is described in "Logical oversampling and data acquisition" on page 302.

1.11.3.2.4 Data transfer

The analog conversion rate / sampling cycle time can be considerably faster than the X2X Link cycle. Saved analog or comparator data can be transferred to the higher-level system synchronously and consistently.

In terms of the application, it must be ensured that the ratio of cyclic data points, the sampling cycle time on the module and the transfer time is sufficient to read out all new data points in the higher-level system.

The sample counter can be used to check how many data values are actually new since the last transfer cycle. If the counter difference to the previous cycle is larger than the number of existing cyclic data points, then values have been overlooked and the system needs to be adjusted.

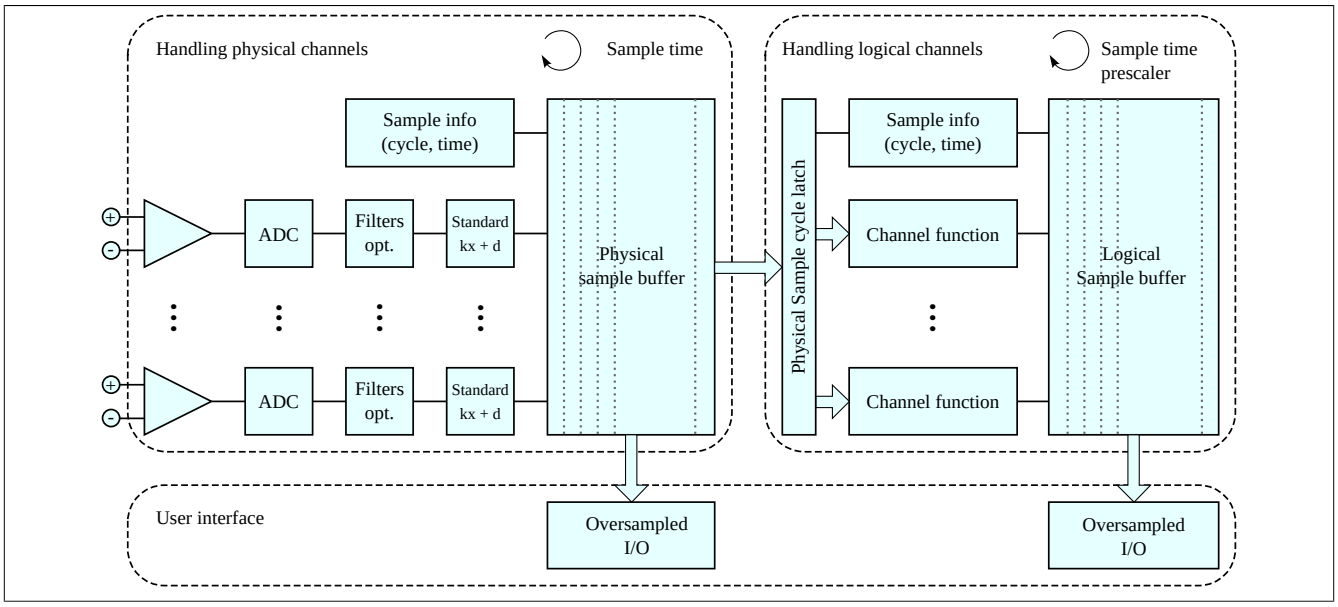
The general guideline is that a cyclic data point should be configured more than is actually required computing-wise.

Example with synchronous settings

- Sampling cycle time = 50 µs
- X2X Link cycle time = 500 µs

Samples 1 to 10 of a channel are possible to calculate in this example. Sample 11 should also be configured as a cyclic data point, however.
The reason for this is the possible jitter in the module caused by interruptions, e.g. from the X2X Link transfer. For the current cycle, this can mean that only 9 new values are available and that 11 values will have to be transferred in the next cycle.

For logical comparator functions, this problem doesn't exist since the maximum number is always transferred in the cycle data range.



1.11.3.3 Physical values

The conversion results are scaled and filtered before being transferred to the higher-level system. No further processing takes place.

Information:

The registers are described in "Physical configuration" on page 305.

1.11.3.3.1 Physical sampling

This module has a data buffer with 16 entries for each of the physical input channels. This buffer is processed according to the configured sampling cycle time.

A maximum of only 30 bytes is available for cyclic transfer on the X2X bus, however. Minus the status and sample counter, this allows only a selection of 14 samples (with a 16-bit data width) from the physical and logical buffer to be transferred.
Data loss can therefore occur with an imprecise selection and configuration.

Example

Displaying continuous sample lines.

- Sampling cycle time = 100 µs
- X2X cycle time = 500 µs

Sample line 1	PhysCh0xSample1
Sample line 2	PhysCh0xSample2
Sample line 3	PhysCh0xSample3
Sample line 4	PhysCh0xSample4
Sample line 5	PhysCh0xSample5
Sample line 6	PhysCh0xSample6
Difference SampleCount = 1	New value in sample line 1
Difference SampleCount = 2	New values in sample line 1 and sample line 2
...	
Difference SampleCount = 5	New values in sample line 1 to sample line 5

Information:

It is important to note that the sample counter refers to the update of the sample lines in the data buffer and not to the number of values transferred cyclically.

Display every second sample line to bridge a longer recording duration:

- Sampling cycle time = 100 µs
- X2X cycle time = 1000 µs

Sample line 1	PhysCh0xSample1
Sample line 3	PhysCh0xSample3
Sample line 5	PhysCh0xSample5
Sample line 7	PhysCh0xSample7
Sample line 9	PhysCh0xSample9
Sample line 11	PhysCh0xSample11
Difference SampleCount = 1	New value in sample line 1
Difference SampleCount = 3	New values in sample line 1 and sample line 3
...	
Difference SampleCount = 5	New values in sample line 1 to sample line 5
...	
Difference SampleCount = 9	New values in sample line 1 to sample line 9

1.11.3.3.2 Input filter

This module is equipped with an individually configurable input filter for each channel. The following filters can be selected:

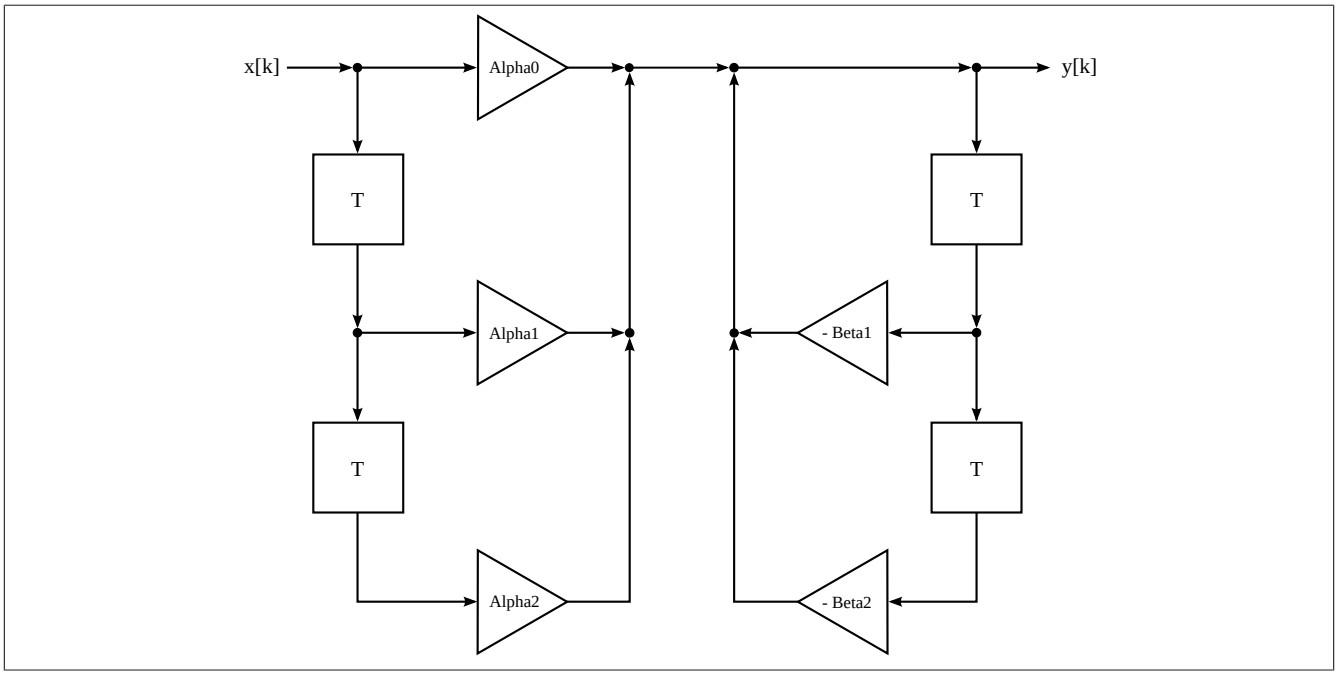
- 1st-order low pass
- 2nd-order low pass
- 2nd-order IIR

The cutoff frequency for the first-order and second-order low-pass filters is configurable. Coefficients Alpha0, Alpha1, Alpha2, Beta1 and Beta2 must be configured for the IIR filter.

Image as a z-transfer function

The second-order z-transfer function is specified in coefficient form (denominator polynomial Beta1, Beta2 and numerator polynomial Alpha0, Alpha1, Alpha2). The transfer method is calculated with the sampling cycle time.

$$S(Z) = \frac{a(Z)}{b(Z)} = \frac{Alpha0 + Alpha1 * Z^{-1} + Alpha2 * Z^{-2}}{1 + Beta1 * Z^{-1} + Beta2 * Z^{-2}}$$



Information:

The registers are described in "Filtering" on page 303.

1.11.3.3.3 Scaling

The analog input channels are calibrated and scaled when delivered (gain = k, offset = d).

User-defined scaling (gain = ku, offset = du) is also available. The calculation is optimized by combining the factors.

Normalization calculation:

nom = k * RawValue + d

k = k * ku

d = k * d + du

The values calculated here are limited to 16 bits.

Information:

The registers are described in "Scaling" on page 303.

1.11.3.4 Logical values

The physical values can be further processed using mathematical functions and comparators. Another logical channel can also be used as a starting point for further processing for a logical function.

Information:

The registers are described in "Logical configuration" on page 305.

1.11.3.4.1 Logical sampling

The module has a data buffer with 16 entries for each of the 6 logical channels. This buffer is processed according to the configured sampling cycle time. In addition, it's also possible to adjust the logical execution cycle using a prescaler for the sampling cycle time.

A maximum of only 30 bytes is available for cyclic transfer on the X2X bus, however. Minus the status and sample counter, this allows only a selection of 14 samples (with a 16-bit data width) from the physical and logical buffer to be transferred. For the logical channels, it is also possible to configure a 32-bit data width.
Data loss can therefore occur with an imprecise selection and configuration.

Example

Displaying continuous sample lines.

- Sampling cycle time = 100 µs
- X2X cycle time = 500 µs

Sample line 1	LogicCh0xSample1
Sample line 2	LogicCh0xSample2
Sample line 3	LogicCh0xSample3
Sample line 4	LogicCh0xSample4
Sample line 5	LogicCh0xSample5
Sample line 6	LogicCh0xSample6
Difference SampleCount = 1	New value in sample line 1
Difference SampleCount = 2	New values in sample line 1 and sample line 2
...	
Difference SampleCount = 5	New values in sample line 1 to sample line 5

Information:

It is important to note that the sample counter refers to the update of the sample lines in the data buffer and not to the number of values transferred cyclically.

Display every second sample line to bridge a longer recording duration:

- Sampling cycle time = 100 µs
- X2X cycle time = 1000 µs

Sample line 1	LogicCh0xSample1
Sample line 3	LogicCh0xSample3
Sample line 5	LogicCh0xSample5
Sample line 7	LogicCh0xSample7
Sample line 9	LogicCh0xSample9
Sample line 11	LogicCh0xSample11
Difference SampleCount = 1	New value in sample line 1
Difference SampleCount = 3	New values in sample line 1 and sample line 3
...	
Difference SampleCount = 5	New values in sample line 1 to sample line 5
...	
Difference SampleCount = 9	New values in sample line 1 to sample line 9

1.11.3.4.2 Operation in the standard function model

6 logical channels are available on the module. Each channel can be configured with one of the following functions:

- "Addition of two channels with scaling" on page 293
- "Integral addition of two channels with scaling" on page 294
- "Multiplication of two channels with scaling" on page 295
- "Integral multiplication of two channels with scaling" on page 296
- "Comparator function of two channels" on page 296
- "Hysteresis comparator of one channel " on page 296

The sources to be used for each logical channel are selected using register "CfO_LogCh0NSource0x". The additionally required function parameters are configured in the "CfO_LogCh0NFuncPar0x" registers. "N" stands for the logical channel to be used; "x" stands for the source or function 0 or 1.

The following links can be made:

- Addition: Result = (Source0 * FunctionParameter0) + (Source1 * FunctionParameter1)
- Integral of the addition: Result = Σ(Source0 * FunctionParameter0) + (Source1 * FunctionParameter1)
- Multiplication: Result = Source0 * Source1 * FunctionParameter0
- Integral of the multiplication: Result = Σ(Source0 * Source1 * FunctionParameter0)
- Channel comparator: Result = Comparison of Source0 with Source1
- Hysteresis comparator: Result = Comparison of Source0 with (Lower threshold value = FunctionParameter0) and (Upper threshold value = FunctionParameter1)
- Physical value display: Result = (Source0 * 1) + (Source1 * 0)

With logical oversampling, 32-bit data points are available in addition to the 16-bit data points due to the possible calculation results. Which ones are used can be selected via the Automation Studio I/O configuration or the data point mapping.

If there is no need for 32-bit data points or this would result in a large restriction in the number of data points, scaling can be used to limit the number range to 16 bits.

The buffer depth for the digital comparator is also able to handle 16 results. Since these are Boolean results, these 16 bits are compressed into 2-byte data points and transferred that way.

1.11.3.4.2.1 Addition

This function can be used to determine the sum or difference of two channels. Only negative scaling of a channel must be configured for calculating the difference.

Calculation

Sample line = (Channel 1 * Scaling 1) + (Channel 2 * Scaling 2)

The addition calculation is performed internally with 32 bits in 16.16 format; the data from the source channels is evaluated as integers (applied to the high word), with decimal places possible due to scaling. When displayed as a logical 32-bit result, these decimal places are visible. When displayed as a 16-bit value, only the integral high word is used.

Example

Channel 1 = 2000
Channel 2 = 1000
Both scalings = 1

Results

3000.x = (2000.x * 1.0) + (1000.x * 1.0)
32-bit representation = 196608000 = 0xBB80000
16-bit representation = 3000 = 0xBB8

Information:

The maximum value for channels 1 and 2 can only be 32767; otherwise, an additional overflow occurs. If values greater than 32767 are possible, the range of values must be limited with scaling.

1.11.3.4.2.2 Integral of addition

This function can be used in the application to establish the average value of the channels or to calculate the deviation/difference between two channels over n samples. In each cycle, addition of the channels is carried out first; the summed result is then saved with the previous value in the current sample line. Depending on the result data type used (16-bit or 32-bit), the calculation overflows sooner or later after n samples due to continuous integration. Due to the signed result value, it must be ensured by the application that number n of samples is chosen small enough so that the integral calculation is less than half the range of values. If this is done, determining the average value can be carried out despite an overflow.

Calculation

Sample line result = Integral ((Channel 1 * Scaling 1) + (Channel 2 * Scaling 2))

The addition calculation is performed internally with 32 bits in 16.16 format; the data from the source channels is evaluated as integers (applied to the high word), with decimal places possible due to scaling. When displayed as a logical 32-bit result, these decimal places are visible. When displayed as a 16-bit value, only the integral high word is used.

Example

Channel 1 = 2000
Channel 2 = 1000
Both scalings = 1

Results

3000.x = (2000.x * 1.0) + (1000.x * 1.0)
32-bit representation = 196608000 = 0xBB80000.
16-bit representation = 3000 = 0xBB8

The average value can now be calculated as follows:

n = Number of samples / sample line
$Value_x$ = Value from sample line x → Newer value
$Value_{(x-n)}$ = Value from sample line x-n → Older value, n samplings back

Average value = ($Value_x$ - $Value_{(x-n)}$) / n

Information:

The maximum value for channels 1 and 2 can only be 32767; otherwise, an additional overflow occurs. If values greater than 32767 are possible, the range of values must be limited with scaling.

1.11.3.4.2.3 Multiplication

This function can be used to calculate the current effective power P = U * I.

Calculation

Sample line = Channel 1 * Channel 2 * Scaling

Multiplication is calculated internally as a 32-bit value; the 16-bit data from the source channels is passed to the low word. When displayed as a logical 32-bit value, the entire result is visible (no multiplication overflow possible when scaling ≤1). When displayed as a 16-bit value, only the high word is used. Though there is a loss of precision, the 16-bit values allow more data points to be transferred.

Example

Channel 1 = 2000
Channel 2 = 1000
Scaling = 1

Results

2000000 = (2000 * 1000 * 1.0)
32-bit representation = 2000000 = 0x1E8480
16-bit representation = 30 = 0x1E

Information:

If higher accuracy is required for the 16-bit value, scaling can be used to shift the bit value in steps of 2^n (... *128, * 256, ...). It is important to ensure that the input values of the source channels are limited here as well; otherwise, there will be an overflow in the multiplication.

1.11.3.4.2.4 Integral of multiplication

This function can be used to calculate the average of the active power in the application. In each cycle, multiplication of the channels is carried out first; the summed result is then saved with the previous value in the current sample line. Depending on the result data type used (16-bit or 32-bit), the calculation overflows sooner or later after n samples due to continuous integration. Due to the signed result value, it must be ensured by the application that number n of samples is chosen small enough so that the integral calculation is less than half the range of values. If this is done, determining the average value can be carried out despite an overflow.

Calculation

Sample line = Integral (Channel 1 * Channel 2 * Scaling)

Multiplication is calculated internally as a 32-bit value; the 16-bit data from the source channels is passed to the low word. When displayed as a logical 32-bit value, the entire result is visible (no multiplication overflow possible when scaling ≤1). When displayed as a 16-bit value, only the high word is used. Though there is a loss of precision, the 16-bit values allow more data points to be transferred.

Example

Channel 1 = 2000
Channel 2 = 1000
Scaling = 1

Results

2000000 = (2000 * 1000 * 1.0)
32-bit representation = 2000000 = 0x1E8480
16-bit representation = 30 = 0x1E

The average value can now be calculated as follows:

n = Number of samples / sample line
$Value_x$ = Value from sample line x → Newer value
$Value_{(x-n)}$ = Value from sample line x-n → Older value, n samplings back

Average value = ($Value_x$ - $Value_{(x-n)}$) / n

Information:

If higher accuracy is required for the 16-bit value, scaling can be used to shift the bit value in steps of 2^n (... *128, * 256, ...). It is important to ensure that the input values of the source channels are limited here as well; otherwise, there will be an overflow in the multiplication.

1.11.3.4.2.5 Channel comparator

This function can be used to compare channel values. The following applies:

- Channel 1 > Channel 2 = 1
- Channel 1 < Channel 2 = 0
- Channel 1 = Channel 2 = State before values are the same

Calculation

Sample line (bit) = Comparison (channel value 1 with channel value 2)

1.11.3.4.2.6 Hysteresis comparator

This function can be used to monitor channel limit violations. The following applies:

- Channel > Upper threshold value = 1
- Channel < Lower threshold value = 0
- Channel within threshold = Value before occurrence

Calculation

Sample line (bit) = Comparison (channel value with lower threshold value) and (channel value with upper threshold value))

1.11.3.4.3 Operation in the bus controller function model

When used on the bus controller, there are 4 logical functions available for each of the analog input channels in addition to the physical value output. Each channel can be configured with one of the following functions:

- "Output of physical values" on page 297 (default setting)
- "Addition of two channels with scaling" on page 293
- "Integral addition of two channels with scaling" on page 294
- "Multiplication of two channels with scaling" on page 295
- "Integral multiplication of two channels with scaling" on page 296
- "Comparator function of two channels" on page 296
- "Hysteresis comparator of one channel " on page 296

In contrast to the standard function model, oversampling and the two digital comparators are not supported. As a result, there is only one newly generated value per channel in each update cycle. Another difference is that there are only 4 logical calculation channels instead of 6.

The logical functions addition, integral of addition, multiplication and integral of multiplication do not differ from the standard function model in their configuration and function when operating on the bus controller.

1.11.3.4.3.1 Value display in bus controller operating mode

The physical value display in the bus controller function model is initialized automatically and represents a special form of the logical function "Addition" with defined scaling factors.

Calculation

Result = Channel value
Formula used for addition: Result = (Channel value 1 * 1) + (Channel value 2 * 0)

Information:

In this function model, only the 2 physical input channels are available, and the scaling factors have fixed values.

1.11.3.5 Monitoring the inputs

The module's inputs are monitored. The standard and extended error messages must be enabled individually for each channel.

The following areas are monitored:

- **Out of range:** The analog input signal is outside the specified operating range.
- **Filter error:** The set filter theorem cannot be calculated (parameter error).
- **Underflow:** The input signal is less than the lower limit value.
- **Overflow:** The input signal is greater than the upper limit value.

Value	Information
0	No error occurred
1	Error occurred

The composite errors of the channels are derived from the individual extended error states, e.g. underflow, overflow of the input range on the analog value. The error state of the oversampling results from a cycle time violation of the set sampling cycle time. All configured physical and logical oversampling functions must be able to be carried out in the configured sampling cycle time; otherwise, an error message will be displayed.

Any error messages that occur must be acknowledged by setting the corresponding bits.

Information:

The registers are described in "Error monitoring" on page 309.

1.11.4 Commissioning

1.11.4.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

1.11.4.1.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

1.11.5 Register description

1.11.5.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 System user's manual.

1.11.5.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
System configuration						
513	CfO_BaseConfig	USINT				•
15364	CfO_CycleTime	UDINT				•
15370	CfO_SyncOffset	UINT				•
15374	CfO_Prescaler	UINT				•
Error messages - Configuration						
385	CfO_ErrorID0007	USINT				•
389	CfO_ErrorID1017	USINT				•
Physical channel configuration						
8194 8450	CfO_ModeCh01 CfO_ModeCh02	UINT				•
8204 8460	CfO_UserGainCh01 CfO_UserGainCh02	DINT				•
8212 8468	CfO_UserOffsetCh01 CfO_UserOffsetCh02	DINT				•
8220 8476	CfO_Alpha0Ch01 CfO_Alpha0Ch02	DINT				•
8228 8484	CfO_Alpha1Ch01 CfO_Alpha1Ch02	DINT				•
8236 8492	CfO_Alpha2Ch01 CfO_Alpha2Ch02	DINT				•
8244 8500	CfO_Beta1Ch01 CfO_Beta1Ch02	DINT				•
8252 8508	CfO_Beta2Ch01 CfO_Beta2Ch02	DINT				•
8198 8454	CfO_CutOffFrequCh01 CfO_CutOffFrequCh02	UINT				•
Logical channel configuration						
10242 + (N-1) * 256	CfO_LogCh0NMode (index N = 1 to 6)	UINT				•
10245 + (N-1) * 256	CfO_LogCh0NSource00 (index N = 1 to 6)	USINT				•
10247 + (N-1) * 256	CfO_LogCh0NSource01 (index N = 1 to 6)	USINT				•
10260 + (N-1) * 256	CfO_LogCh0NFuncPar00 (index N = 1 to 6)	UDINT				•
10268 + (N-1) * 256	CfO_LogCh0NFuncPar01 (index N = 1 to 6)	UDINT				•
Analog inputs - Communication						
5062 5070	AnalogInput01 AnalogInput02	INT	•			
Error messages - Communication						
261	Composite error	USINT	•			
	Channel01Error	Bit 0				
	Channel02Error	Bit 1				
	PhysicalError	Bit 4				
	LogicalError	Bit 5				
325	Acknowledging standard errors	USINT			•	
	AckChannel01Error	Bit 0				
	AckChannel01Error	Bit 1				
	AckPhysicalError	Bit 4				
	AckLogicalError	Bit 5				
257	Extended channel error messages	USINT	•			
	Channel01OutOfRange	Bit 0				
	Channel01FilterError	Bit 1				
	Channel01Underflow	Bit 2				
	Channel01Overflow	Bit 3				
	Channel02OutOfRange	Bit 4				
	Channel02FilterError	Bit 5				
	Channel02Underflow	Bit 6				
	Channel02Overflow	Bit 7				

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
321	Acknowledging extended channel error messages	USINT			•	
	AckChannel01OutOfRange	Bit 0				
	AckChannel01FilterError	Bit 1				
	AckChannel01Underflow	Bit 2				
	AckChannel01Overflow	Bit 3				
	AckChannel02OutOfRange	Bit 4				
	AckChannel02FilterError	Bit 5				
	AckChannel02Underflow	Bit 6				
	AckChannel02Overflow	Bit 7				
Physical analog sample display						
4102 + (16-N) * 64	PhysCh01SampleN (index N = 1 to 16)	INT	•			
4110 + (16-N) * 64	PhysCh02SampleN (index N = 1 to 16)	INT	•			
5106	PhysTimestamp	INT	•			
5108	PhysTimestamp	DINT	•			
5113	PhysSampleCount	SINT	•			
5114	PhysSampleCount	INT	•			
Logical analog and digital sample display						
6148 + (16-N) * 64	LogicCh01SampleN (index N = 1 to 16) (32-bit)	DINT	•			
6150 + (16-N) * 64	LogicCh01SampleN (index N = 1 to 16) (16-bit)	INT	•			
6156 + (16-N) * 64	LogicCh02SampleN (index N = 1 to 16) (32-bit)	DINT	•			
6158 + (16-N) * 64	LogicCh02SampleN (index N = 1 to 16) (16-bit)	INT	•			
6164 + (16-N) * 64	LogicCh03SampleN (index N = 1 to 16) (32-bit)	DINT	•			
6166 + (16-N) * 64	LogicCh03SampleN (index N = 1 to 16) (16-bit)	INT	•			
6172 + (16-N) * 64	LogicCh04SampleN (index N = 1 to 16) (32-bit)	DINT	•			
6174 + (16-N) * 64	LogicCh04SampleN (index N = 1 to 16) (16-bit)	INT	•			
6180 + (16-N) * 64	LogicCh05SampleN (index N = 1 to 16) (32-bit)	DINT	•			
6182 + (N-16) * 64	LogicCh05SampleN (index N = 1 to 16) (16-bit)	INT	•			
6188 + (16-N) * 64	LogicCh06SampleN (index N = 1 to 16) (32-bit)	DINT	•			
6190 + (16-N) * 64	LogicCh06SampleN (index N = 1 to 16) (16-bit)	INT	•			
7109 + (N-1) * 8	LogicCh0NSample16_9 (index N = 1 to 5)	USINT	•			
7151	LogicCh06Sample16_9	USINT	•			
7111 + (N-1) * 8	LogicCh0NSample8_1 (index N = 1 to 5)	USINT	•			
7149	LogicCh06Sample8_1	USINT	•			
7154	LogicTimestamp	INT	•			
7156	LogicTimestamp	DINT	•			
7161	LogicSampleCount	SINT	•			
7162	LogicSampleCount	INT	•			

1.11.5.3 Function model 254 - Bus controller

Function model "Bus controller" has limitations compared to function model Standard. For details, see "Operating modes " on page 284.

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
System configuration							
513	-	CfO_BaseConfig	USINT				•
15364	-	CfO_CycleTime	UDINT				•
15370	-	CfO_SyncOffset	UINT				•
15374	-	CfO_Prescaler	UINT				•
Error messages - Configuration							
385	-	CfO_ErrorID0007	USINT				•
389	-	CfO_ErrorID1017	USINT				•
Physical channel configuration							
8194 8450	-	CfO_ModeCh01 CfO_ModeCh02	UINT				•
8204 8460	-	CfO_UserGainCh01 CfO_UserGainCh02	DINT				•
8212 8468	-	CfO_UserOffsetCh01 CfO_UserOffsetCh02	DINT				•
8220 8476	-	CfO_Alpha0Ch01 CfO_Alpha0Ch02	DINT				•
8228 8484	-	CfO_Alpha1Ch01 CfO_Alpha1Ch02	DINT				•
8236 8492	-	CfO_Alpha2Ch01 CfO_Alpha2Ch02	DINT				•
8244 8500	-	CfO_Beta1Ch01 CfO_Beta1Ch02	DINT				•
8252 8508	-	CfO_Beta2Ch01 CfO_Beta2Ch02	DINT				•
8198 8454	-	CfO_CutOffFrequCh01 CfO_CutOffFrequCh02	UINT				•
Logical channel configuration							
10242 + (N-1) * 256	-	CfO_LogCh0NMode (index N = 1 to 6)	UINT				•
10245 + (N-1) * 256	-	CfO_LogCh0NSource00 (index N = 1 to 6)	USINT				•
10247 + (N-1) * 256	-	CfO_LogCh0NSource01 (index N = 1 to 6)	USINT				•
10260 + (N-1) * 256	-	CfO_LogCh0NFuncPar00 (index N = 1 to 6)	UDINT				•
10268 + (N-1) * 256	-	CfO_LogCh0NFuncPar01 (index N = 1 to 6)	UDINT				•
Analog inputs - Communication							
5062 5070	0 2	AnalogInput01 AnalogInput02	INT	•			
Error messages - Communication							
261	-	Composite error	USINT		•		
		Channel01Error	Bit 0				
		Channel02Error	Bit 1				
		PhysicalError	Bit 4				
		LogicalError	Bit 5				
325	-	Acknowledging standard errors	USINT				•
		AckChannel01Error	Bit 0				
		AckChannel01Error	Bit 1				
		AckPhysicalError	Bit 4				
		AckLogicalError	Bit 5				
257	-	Extended channel error messages	USINT		•		
		Channel01OutOfRange	Bit 0				
		Channel01FilterError	Bit 1				
		Channel01Underflow	Bit 2				
		Channel01Overflow	Bit 3				
		Channel02OutOfRange	Bit 4				
		Channel02FilterError	Bit 5				
		Channel02Underflow	Bit 6				
		Channel02Overflow	Bit 7				

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
321	-	Acknowledging extended channel error messages	USINT				•
		AckChannel01OutOfRange	Bit 0				
		AckChannel01FilterError	Bit 1				
		AckChannel01Underflow	Bit 2				
		AckChannel01Overflow	Bit 3				
		AckChannel02OutOfRange	Bit 4				
		AckChannel02FilterError	Bit 5				
		AckChannel02Underflow	Bit 6				
		AckChannel02Overflow	Bit 7				

1) The offset specifies the position of the register within the CAN object.

1.11.5.4 Configuration

Configuration must take place in addition to using suitable terminals.

1.11.5.4.1 System configuration

The following registers are used to configure the module's system settings.

1.11.5.4.1.1 Logical oversampling and data acquisition

Name:
CfO_BaseConfig

This register can be used to configure settings relating to handling logical oversampling and data acquisition. For details, see "Priorities and values" on page 287.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	49

Bit structure:

Bit	Description	Value	Information
0	"Display configuration for logical values active/inactive" in the Automation Studio I/O configuration	0	Inactive
		1	Active (bus controller default setting)
1	"Logical handling priority" in the Automation Studio I/O configuration	0	Low (bus controller default setting)
		1	High
2 - 3	Reserved	-	
4	"Physical input mode" in the Automation Studio I/O configuration	0	Newest value
		1	Referenced value (reference = prescaled system timer) (bus controller default setting)
5	"Logical input mode" in the Automation Studio I/O configuration	0	Newest value
		1	Referenced value (reference = prescaled system timer) (bus controller default setting)
6 - 7	Reserved	-	

1.11.5.4.1.2 Sampling cycle time

Name:
CfO_CycleTime
"Physical sample time" in the Automation Studio I/O configuration.

This register is used to set the sampling cycle time on the module. The format is a 16.16-bit unsigned 4-byte value, where the high word is the microseconds integer and the low word is the decimal places. The decimal places allow a more precise adjustment to the X2X cycle time. The absolute resolution is 1 µs.

Input value = Time in µs * 65536 data type

Data type	Value	Information
UDINT	2,621,440 to 2,147,483,647	40 µs to 32 ms sampling cycle time. Bus controller default setting: 6,553,600 = 100 µs

1.11.5.4.1.3 Prescaler of the logical channel processing time

Name:
CfO_Prescaler

This register contains the prescaler for configuring the logical channel processing time. The actual logical cycle time will be calculated from the multiple of the sampling cycle time that is defined here. If a very short sampling cycle time is required for physical samples, then the module load can be reduced using the second time base for the logical samples.

Data type	Value	Information
UINT	1 to 10	Multiples of the physical sampling cycle for logical processing Bus controller default setting: 2

1.11.5.4.1.4 Synchronization offset

Name:
CfO_SyncOffset
"Synchronization offset" in the Automation Studio I/O configuration.

The system cycle can be offset in 1 µs steps in this register.

Data type	Value	Information
UINT	-32,768 to 32,767	Synchronization offset in µs. Bus controller default setting: 0

1.11.5.4.2 Scaling

The analog input channels are calibrated and scaled when delivered. User-defined scaling is also available.

1.11.5.4.2.1 Gain

Name:
CfO_UserGainCh01 to CfO_UserGainCh02
"Configuration channel 0x / gain" in the Automation Studio I/O configuration

These registers are used to set the gain for the corresponding channel. The format is a 16.16-bit signed 4-byte value, where the high word is the integer and the low word is the decimal places.

Input value = Gain ku * 65536

Value 65535 corresponds to a gain of 1.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	Gain. Bus controller default setting: 65535

1.11.5.4.2.2 Offset

Name:
CfO_UserOffsetCh01 to CfO_UserOffsetCh02
"Configuration channel 0x / offset" in the Automation Studio I/O configuration

These registers are used to set the offset for the corresponding channel. The format is a 16.16-bit signed 4-byte value, where the high word is the integer and the low word is the decimal places.

Input value = Offset du * 65536

Value 65536 corresponds to an offset of 1.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	Offset. Bus controller default setting: 0

1.11.5.4.3 Filtering

The module is equipped with an individually configurable input filter for each individual channel.

1.11.5.4.3.1 Coefficients

Name:
CfO_Alpha0Ch01 to CfO_Alpha0Ch02
CfO_Alpha1Ch01 to CfO_Alpha1Ch02
CfO_Alpha2Ch01 to CfO_Alpha2Ch02
CfO_Beta1Ch01 to CfO_Beta1Ch02
CfO_Beta1Ch01 to CfO_Beta1Ch02

These registers are used to set the coefficients for the IIR filter.

Data type	Values	
DINT	-2,147,483,648 to 2,147,483,647	IIR filter coefficient. Bus controller default setting: 0

1.11.5.4.3.2 Cutoff frequency

Name:
CfO_CutOffFrequCh01 to CfO_CutOffFrequCh02

These registers are used to configure the limit frequency in hertz for a 1st- or 2nd-order low pass for the corresponding channel.

Data type	Value	Information
UINT	0 to 65535	Cutoff frequency for 1st- or 2nd-order low pass [Hz]. Bus controller default setting: 1000

1.11.5.4.4 Physical configuration

The conversion results are scaled and filtered before being transferred to the higher-level system. To do this, the operating mode must be set for each channel.

1.11.5.4.4.1 Operating mode

Name:
CfO_ModeCh01 to CfO_ModeCh02

The operating mode for each physical channel can be configured in this register.

Data type	Values	Bus controller default setting
UINT	See the bit structure.	256

Bit structure:

Bit	Description	Value	Information
0 - 2	Connection configuration **This value must be set the same for each register!**	000	Voltage signal (bus controller default setting)
		111	Current signal
3 - 7	Reserved	0	
8 - 10	Operating mode	000	Channel disabled
		001	No filtering (bus controller default setting)
		010	2nd-order IIR (configurableAlpha and Beta coefficients)
		011	1st-order low pass (configurable limit frequency)
		100	2nd-order low pass (configurable limit frequency)
		101 to 111	Reserved
11 - 15	Reserved	0	

1.11.5.4.5 Logical configuration

The physical values can be further processed using mathematical functions and comparators. Various settings must be made for this.

1.11.5.4.5.1 Operating mode

Name:
CfO_LogCh01Mode to CfO_LogCh06Mode
"Logical configuration channel 0x / Addition" in the Automation Studio I/O configuration.
"Logical configuration channel 0x / Integral of addition" in the Automation Studio I/O configuration.
"Logical configuration channel 0x / Multiplication" in the Automation Studio I/O configuration.
"Logical configuration channel 0x / Integral of multiplication" in the Automation Studio I/O configuration.
"Logical configuration channel 0x / Channel comparator" in the Automation Studio I/O configuration.
"Logical configuration channel 0x / Hysteresis comparator" in the Automation Studio I/O configuration.
"Logical configuration channel 0x / Physical value display" in the Automation Studio I/O configuration.

The operating mode for each logical channel can be configured in this register.

The sources to be used for each logical channel are selected using the "CfO_LogCh0NSource0x" on page 306 registers. The additionally required function parameters are configured in the "CfO_LogCh0NFuncPar0x" on page 306 registers. "N" stands for the logical channel to be used; "x" stands for the source or function 0 or 1.

Data type	Value	Information
UINT	0	Channel switched off. Bus controller default setting: Channel 3 to 6
	256	Addition or physical value display[1]. Bus controller default setting: Channel 1 to 2
	257	Integral of addition
	512	Multiplication
	513	Integral of multiplication
	768	Channel comparator
	1024	Hysteresis comparator

1) Only registers CfO_LogCh01Mode to CfO_LogCh02Mode are used for physical value display.

1.11.5.4.5.2 Source registers

Name:
CfO_LogCh01Source00 to CfO_LogCh06Source00
CfO_LogCh01Source01 to CfO_LogCh06Source01

These registers can be used to select the source registers for the operating mode of the logical channel configured in the register "CfO_LogCh0NMode" on page 305.
In the name, "Source00" stands for source register 0; "Source01" stands for source register 1.

In Value display in bus controller operating mode mode, the same channel number is written to both source registers.

Data type	Value	Information
USINT	0	Physical channel 01. Bus controller default setting[1)]
	1	Physical channel 02. Bus controller default setting[1)]
	8	Logical channel 01[1)]
	...	...
	13	Logical channel 06

1) **Values**

Channel 1: 0
Channel 2: 1
Channels 3 to 6: 0

2) Logical channels cannot be used in the bus controller function model.

1.11.5.4.5.3 Additional function parameters

Name:
CfO_LogCh01FuncPar00 to CfO_LogCh06FuncPar00
CfO_LogCh01FuncPar01 to CfO_LogCh06FuncPar01

These registers can be used to store additional function parameters for the operating modes of the logical channel set in register "CfO_LogCh0NMode" on page 305.

The meaning of the function parameter varies depending on the operating mode.

Operating mode	Parameter 1	Parameter 2
(Integral of) addition	Scaling factor	Scaling factor
(Integral of) multiplication	Scaling factor	-
Channel comparator	-	-
Hysteresis comparator	Upper threshold value	Lower threshold value
Output of physical values	Fixed scaling factor = 65536	Defined scaling factor = 0

Value 65536 corresponds to scaling or a threshold value of 1.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Scaling factor or threshold value. Bus controller default setting: Register "...FuncPar00" Channels 1 to 4 65536 Channels 5 to 6 0 Register "...FuncPar01" All 0

1.11.5.5 Communication - General

The analog inputs of the module convert the current or voltage values with a resolution of 16 bits.

1.11.5.5.1 Analog inputs

Name:
AnalogInput01 to AnalogInput02

This module can be configured and operated as a normal analog input module without logical auxiliary functions. The physical values from the last sampling cycle are used as input values in this case.

Analog input values are displayed as signed 16-bit values depending on the configured operating mode.

Data type	Value	Information
INT	-32,768 to 32,767	Voltage signal ±10 VDC
	0 to 32,767	Current signal 0 to 20 mA

Information:

It is important to note that the oversampling function is not available in function model "Bus controller" due to the amount of data and lack of consistency!

1.11.5.5.2 Physical sampling

The module has a data buffer with 16 entries for each of the physical input channels. This buffer is processed with the set sampling cycle time.

1.11.5.5.2.1 Physical data buffer

Name:
PhysCh01Sample1 to PhysCh01Sample16
PhysCh02Sample1 to PhysCh02Sample16

These registers are the physical buffer registers of the analog channels. 16 registers are available for each channel. Sample 1 is the newest value; sample 16 is the oldest.

Data type	Value	Information
INT	-32,768 to 32,767	Voltage signal ±10 VDC
	0 to 32,767	Current signal 0 to 20 mA

1.11.5.5.2.2 Physical sample counter

Name:
PhysSampleCount

This register is an integer counter that is increased as soon as the module has saved a new physical sample line. The number of new sample lines is calculated from the difference to the previous cycle.

Data type	Value
SINT	-128 to 127
INT	-32,768 to 32,767

1.11.5.5.2.3 Physical timestamp

Name:
PhysTimestamp

This register returns the timestamp of the values currently being determined as signed values in µs. This data point is the timestamp of the physical sample line 1.

Data type	Values
INT	-32768 to 32767
DINT	-2,147,483,648 to 2,147,483,647

1.11.5.5.3 Logical sampling

The physical values can be further processed using mathematical functions and comparators. The module has a data buffer with 16 entries for each of the 6 logical channels.

1.11.5.5.3.1 Logical data buffer

Name:
LogicCh01Sample1 to LogicCh01Sample16
...
LogicCh06Sample1 to LogicCh06Sample16

These registers are the buffer registers of the logical input channels. 16 registers are available for each channel. Sample 1 is the newest value; sample 16 is the oldest.

The calculated values are displayed as signed 16-bit or 32-bit values depending on the register used.

Data type	Values
INT	-32768 to 32767
DINT	-2,147,483,648 to 2,147,483,647

1.11.5.5.3.2 Results 9-16 of the comparator comparison

Name:
LogicCh01Sample16_9 to LogicCh06Sample16_9

The results of samples 9 to 16 of the logical digital comparator of the logical channels are contained in these registers. Each of these bits corresponds to a sample line, with sample 9 the newest and sample 16 the oldest comparator comparison. The results of samples 1 to 8 are contained in register "LogicCHSample8_1" on page 308.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Comparator result	x	Sample 9
...	...		
7	Comparator result	x	Sample 16

1.11.5.5.3.3 Results 1-8 of the comparator comparison

Name:
LogicCh01Sample8_1 to LogicCh06Sample8_1

These registers are used to represent the results of samples 1 to 8 of the logical digital comparator for the logical channels. Each of these bits corresponds to a sample line, with sample 1 the newest and Sample 8 the oldest comparator comparison. The results of samples 9 to 16 are represented in register "LogicSample16_9" on page 308.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Comparator result	x	Sample 1
...	...		
7	Comparator result	x	Sample 8

1.11.5.5.3.4 Logical sample counter

Name:
LogicSampleCount

This register is an integer counter that is increased as soon as the module has saved a new logical sample line. The number of new sample lines is calculated from the difference to the previous cycle.

Data type	Value
SINT	-128 to 127
INT	-32,768 to 32,767

1.11.5.5.3.5 Logical timestamp

Name:
LogicTimestamp

This register provides the timestamp of the currently determined values as a signed 2-byte or 4-byte value in microseconds. This data point is the timestamp of logical sample line 1.

Data type	Values
INT	-32768 to 32767
DINT	-2,147,483,648 to 2,147,483,647

1.11.5.6 Error monitoring

The registers for displaying and acknowledging errors are transferred either cyclically or acyclically depending on the function model.

1.11.5.6.1 Enabling standard error messages

Name:
CfO_ErrorID1017
Automatic enabling by the Automation Studio I/O configuration.

This register can be used to enable the standard error messages. The composite errors of the channels are derived from the individual extended error states, e.g. underflow, overflow of the input range on the analog value. The error status of the oversampling results from a cycle time violation of the set sampling cycle time.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	63

Bit structure:

Bit	Description	Value	Information
0	Composite errors on channel 01	0	Error generation disabled
		1	Error generation enabled (bus controller default setting)
1	Composite errors on channel 02	0	Error generation disabled
		1	Error generation enabled (bus controller default setting)
2 - 3	Reserved	0	
4	Physical sample error status	0	Error generation disabled
		1	Error generation enabled (bus controller default setting)
5	Logical sample error status	0	Error generation disabled
		1	Error generation enabled (bus controller default setting)
6 - 7	Reserved	0	

1.11.5.6.2 Enabling extended error messages

Name:
CfO_ErrorID0007
Automatic enabling in the Automation Studio I/O configuration by selecting "Extended error status information" and channel activation.

This register can be used to enable the extended error messages for analog channels 1 and 2.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	Channel 1: Range exceeded violation (pos.)	0	Error generation disabled (bus controller default setting)
		1	Range exceeded violation (pos.) enabled
1	Channel 1: Filter error	0	Error generation disabled (bus controller default setting)
		1	Filter error enabled
2	Channel 1: Underflow	0	Error generation disabled (bus controller default setting)
		1	Underflow enabled
3	Channel 1: Overrun	0	Error generation disabled (bus controller default setting)
		1	Overflow enabled
4	Channel 2: Range exceeded violation (pos.)	0	Error generation disabled (bus controller default setting)
		1	Range exceeded violation (pos.) enabled
5	Channel 2: Filter error	0	Error generation disabled (bus controller default setting)
		1	Filter error enabled
6	Channel 2: Underflow	0	Error generation disabled (bus controller default setting)
		1	Underflow enabled
7	Channel 2: Overrun	0	Error generation disabled (bus controller default setting)
		1	Overflow enabled

1.11.5.6.3 Composite error

Name:
Channel01Error to Channel02Error
PhysicalError
LogicalError

Composite errors are mapped to this register.

All configured physical and logical oversampling functions must be able to be carried out in the configured sampling cycle time; otherwise, these error messages will be displayed. The system can be further adjusted with settings for the processing priority and the prescaler for logical oversampling.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01Error	0	No error
		1	Composite errors on channel 1
1	Channel02Error	0	No error
		1	Composite errors on channel 2
2 - 3	Reserved	0	
4	PhysicalError	0	No error
		1	Physical sample error status, sampling cycle time too short
5	LogicalError	0	No error
		1	Logical sample error status, sampling cycle time too short or prescaler configured too low
6 - 7	Reserved	0	

1.11.5.6.4 Acknowledging standard errors

Name:
AckChannel01Error to AckChannel02Error
AckPhysicalError
AckLogicalError

In this register, error messages from register "Composite error" on page 310 can be acknowledged by setting the corresponding bits.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	AckChannel01Error	0	No change
		1	Acknowledge error
1	AckChannel02Error	0	No change
		1	Acknowledge error
2 - 3	Reserved	0	
4	AckPhysicalError	0	No change
		1	Acknowledge error
5	AckLogicalError	0	No change
		1	Acknowledge error
6 - 7	Reserved	0	

1.11.5.6.5 Extended channel error messages

Name:
Channel01OutOfRange to Channel02OutOfRange
Channel01FilterError to Channel02FilterError
Channel01Underflow to Channel02Underflow
Channel01Overflow to Channel02Overflow

The error states of input channels 1 and 2 are represented in these registers.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01OutOfRange	0	No error
		1	Range exceeded violation (pos.) occurred
1	Channel01FilterError	0	No error
		1	Filter error occurred
2	Channel01Underflow	0	No error
		1	Underflow occurred
3	Channel01Overflow	0	No error
		1	Overflow occurred
4	Channel02OutOfRange	0	No error
		1	Range exceeded violation (pos.) occurred
5	Channel02FilterError	0	No error
		1	Filter error occurred
6	Channel02Underflow	0	No error
		1	Underflow occurred
7	Channel02Overflow	0	No error
		1	Overflow occurred

1.11.5.6.6 Acknowledging extended channel error messages

Name:
AckChannel01OutOfRange to AckChannel02OutOfRange
AckChannel01FilterError to AckChannel02FilterError
AckChannel01Underflow to AckChannel02Underflow
AckChannel01Overflow to AckChannel02Overflow

These registers can be used to acknowledge the error messages from the "ExtendedChannelErrorMessages" on page 311 registers by setting the corresponding bit.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	AckChannel01OutOfRange	0	No change
		1	Acknowledge error
1	AckChannel01FilterError	0	No change
		1	Acknowledge error
2	AckChannel01Underflow	0	No change
		1	Acknowledge error
3	AckChannel01Overflow	0	No change
		1	Acknowledge error
4	AckChannel02OutOfRange	0	No change
		1	Acknowledge error
5	AckChannel02FilterError	0	No change
		1	Acknowledge error
6	AckChannel02Underflow	0	No change
		1	Acknowledge error
7	AckChannel02Overflow	0	No change
		1	Acknowledge error

1.11.5.7 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

1.11.5.8 Minimum I/O update time

There is no limitation or dependency on the bus cycle time.

The I/O update time is defined using the "Sampling time" register. The fastest possible sampling time depends on the number of channels to be converted and the configuration.

1.12 X20AI4222

1.12.1 General information

The module is equipped with 4 inputs with 13-bit (including sign) digital converter resolution. It can be used to capture voltage signals in the range from ±10 V.

- 4 analog inputs ±10 V
- 13-bit digital converter resolution

1.12.2 Order data

Order number	Short description	Figure
	Analog inputs	
X20AI4222	X20 analog input module, 4 inputs, ±10 V, 13-bit converter resolution, configurable input filter	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 51: X20AI4222 - Order data

1.12.3 Technical data

Order number	X20AI4222
Short description	
I/O module	4 analog inputs ±10 V
General information	
B&R ID code	0xCAB1
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1.1 W [1]
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
EAC	Yes
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
DNV GL	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
LR	ENV1
KR	Yes
Analog inputs	
Input	±10 V
Input type	Differential input
Digital converter resolution	±12-bit
Conversion time	400 µs for all inputs
Output format	
Data type	INT
Voltage	0x8001 - 0x7FFF / 1 LSB = 0x0008 = 2.441 mV
Input impedance in signal range	20 MΩ
Input protection	Protection against wiring with supply voltage
Permissible input signal	Max. ±30 V
Output of digital value during overload	Configurable
Conversion procedure	SAR
Input filter	3rd-order low pass / cutoff frequency 1 kHz
Max. error at 25°C	
Gain	0.08% [2]
Offset	0.015% [3]
Max. gain drift	0.006 %/°C [2]
Max. offset drift	0.002 %/°C [3]
Common-mode rejection	
DC	70 dB
50 Hz	70 dB
Common-mode range	±12 V
Crosstalk between channels	-70 dB
Nonlinearity	<0.025% [3]
Isolation voltage between channel and bus	500 V_{eff}
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20

Table 52: X20AI4222 - Technical data

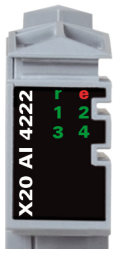
Order number	X20AI4222
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5$^{+0.2}$ mm

Table 52: X20AI4222 - Technical data

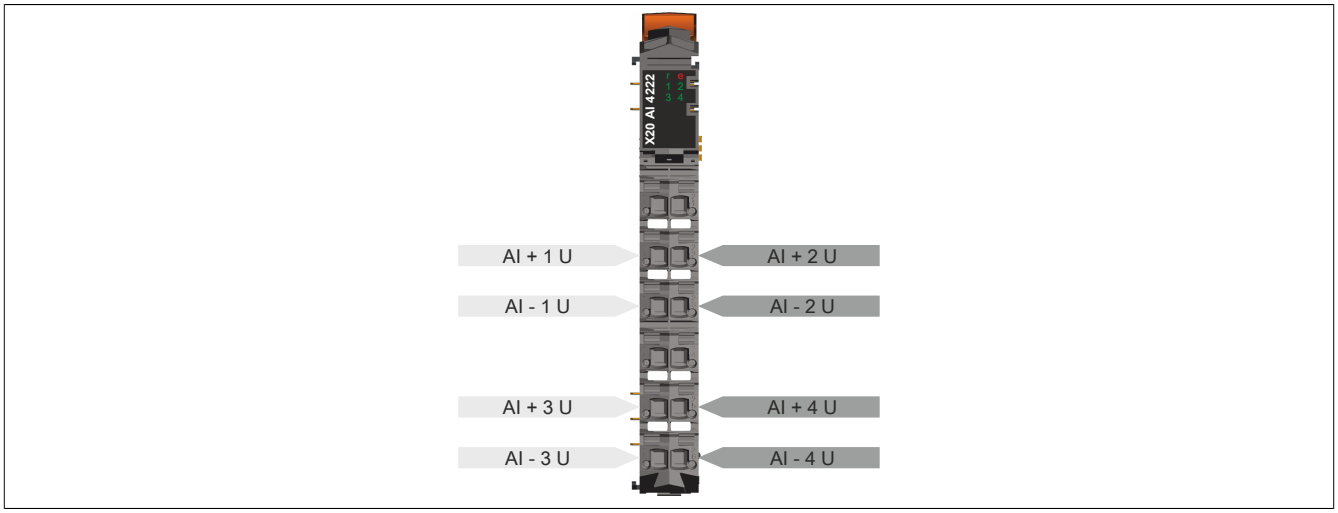
1) To reduce power dissipation, B&R recommends bridging unused inputs on the terminals.
2) Based on the current measured value.
3) Based on the 20 V measurement range.

1.12.4 LED status indicators

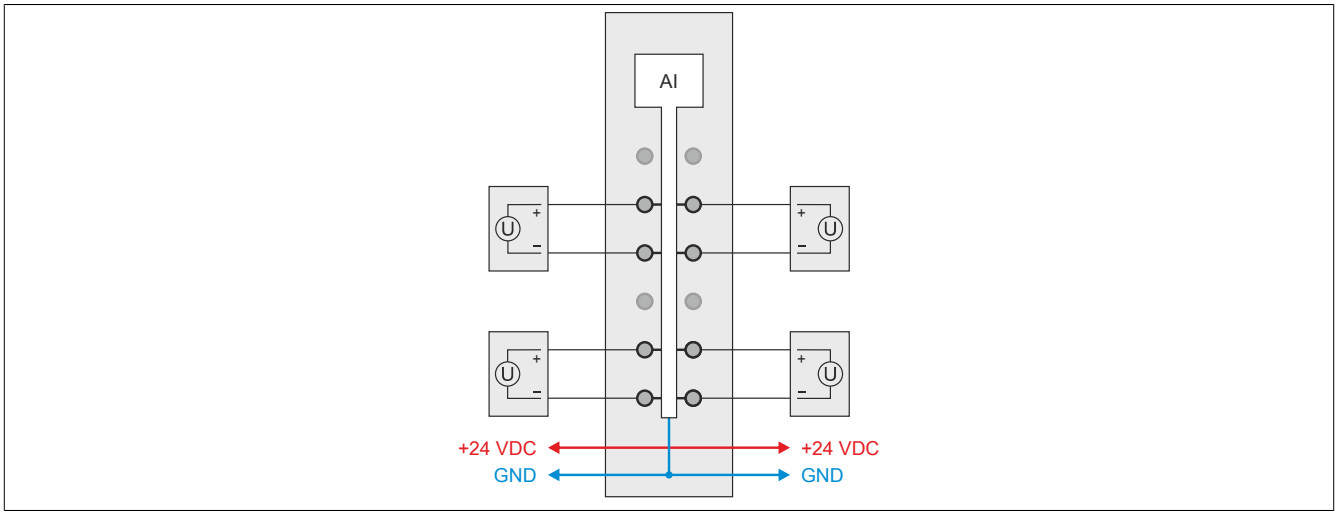
For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 system user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Green	Off	Open line or sensor is disconnected
			Blinking	Input signal overflow or underflow
			On	Analog/digital converter running, value OK

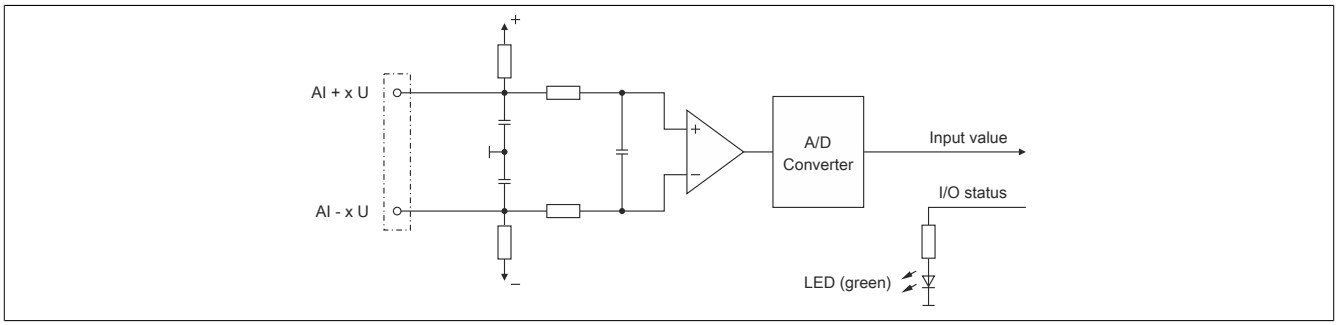
1.12.5 Pinout



1.12.6 Connection example



1.12.7 Input circuit diagram



1.12.8 Register description

1.12.8.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 system user's manual.

1.12.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration						
16	ConfigOutput01 (Input filter)	USINT				•
20	ConfigOutput03 (Lower limit value)	INT				•
22	ConfigOutput04 (Upper limit value)	INT				•
Analog signal - Communication						
Index * 2 - 2	AnalogInput0N (Index N = 1 to 4)	INT	•			
30	StatusInput01	USINT	•			

1.12.8.3 Function model 254 - Bus controller

Register	Offset	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration							
16	-	ConfigOutput01 (Input filter)	USINT				•
20	-	ConfigOutput03 (Lower limit value)	INT				•
22	-	ConfigOutput04 (Upper limit value)	INT				•
Analog signal - Communication							
Index * 2 - 2	Index * 2 - 2	AnalogInput0N (Index N = 1 to 4)	INT	•			
30	-	StatusInput01	USINT		•		

1) The offset specifies the position of the register within the CAN object.

1.12.8.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

1.12.8.3.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

1.12.8.4 Analog inputs

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

1.12.8.5 Analog input values

Name:
AnalogInput01 to AnalogInput04

The analog input values are mapped to this register.

Data type	Value	Input signal:
INT	-32,768 to 32,767	Voltage signal -10 to 10 VDC

1.12.8.6 Input filter

This module is equipped with a configurable input filter. The minimum cycle time must be >500 µs. Filtering is disabled for shorter cycle times.

If the input filter is active, then the scan rate for the channels is measured in ms. The time offset between the channels is 200 µs. The conversion takes place asynchronously to the network cycle.

1.12.8.6.1 Input ramp limiting

Input ramp limiting can only be performed in conjunction with filtering. Input ramp limiting is performed before filtering.

The difference of the input value change is checked for exceeding the specified limit. In the event of overshoot, the tracked input value is equal to the old value ± the limit value.

Configurable limit values:

Value	Limit value
0	The input value is used without limitation.
1	0x3FFF = 16383
2	0x1FFF = 8191
3	0x0FFF = 4095
4	0x07FF = 2047
5	0x03FF = 1023
6	0x01FF = 511
7	0x00FF = 255

Input ramp limiting is well suited for suppressing disturbances (spikes). The following examples show the functionality of input ramp limiting based on an input step and a disturbance.

Example 1

The input value jumps from 8000 to 17000. The diagram shows the tracked input value with the following settings:

Input ramp limiting = 4 = 0x07FF = 2047

Filter level = 2

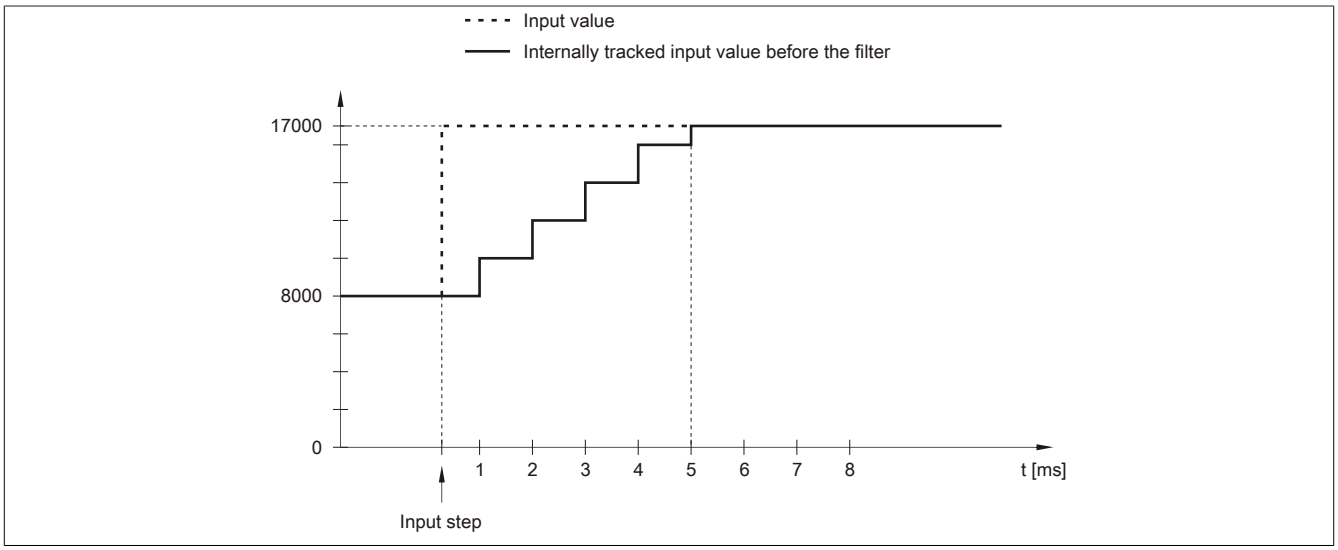


Figure 35: Tracked input value for input step

Example 2

A disturbance interferes with the input value. The diagram shows the tracked input value with the following settings:

Input ramp limiting = 4 = 0x07FF = 2047

Filter level = 2

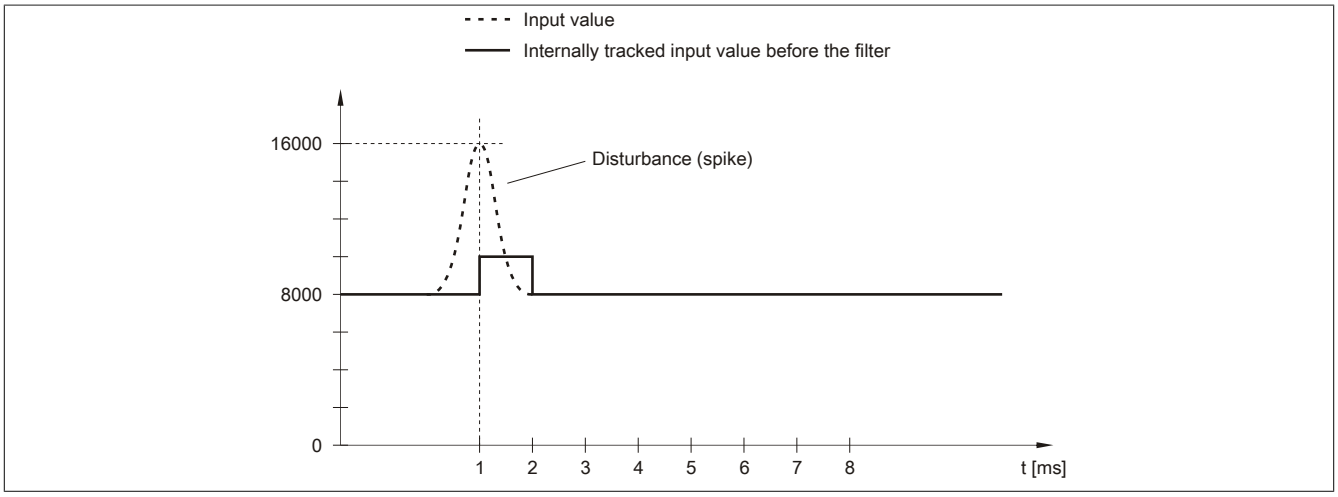


Figure 36: Tracked input value for disturbance

1.12.8.6.2 Filter level

A filter can be defined to prevent large input steps. This filter is used to bring the input value closer to the actual analog value over a period of several bus cycles.
Filtering takes place after any input ramp limiting has been carried out.

Formula for calculating the input value:

$$\text{Value}_{\text{New}} = \text{Value}_{\text{Old}} - \frac{\text{Value}_{\text{Old}}}{\text{Filter level}} + \frac{\text{Input value}}{\text{Filter level}}$$

Adjustable filter levels:

Value	Filter level
0	Filter switched off
1	Filter level 2
2	Filter level 4
3	Filter level 8
4	Filter level 16
5	Filter level 32
6	Filter level 64
7	Filter level 128

The following examples show the functionality of the filter based on an input step and a disturbance.

Example 1

The input value jumps from 8000 to 16000. The diagram shows the calculated value with the following settings:

Input ramp limiting = 0

Filter level = 2 or 4

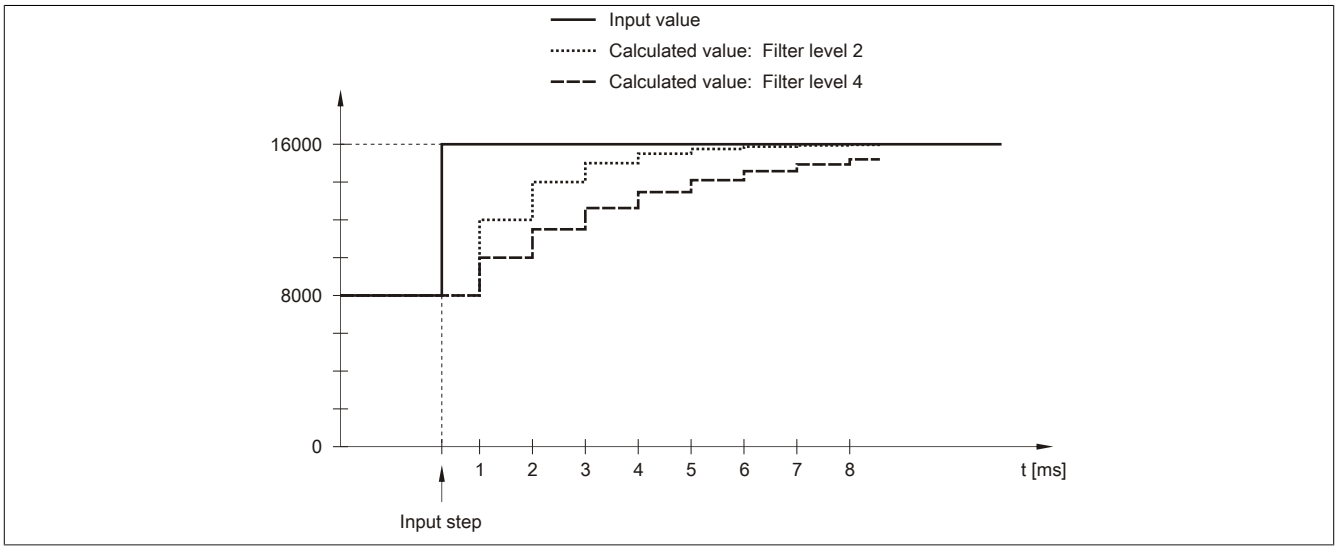


Figure 37: Calculated value during input step

Example 2

A disturbance interferes with the input value. The diagram shows the calculated value with the following settings:

Input ramp limiting = 0

Filter level = 2 or 4

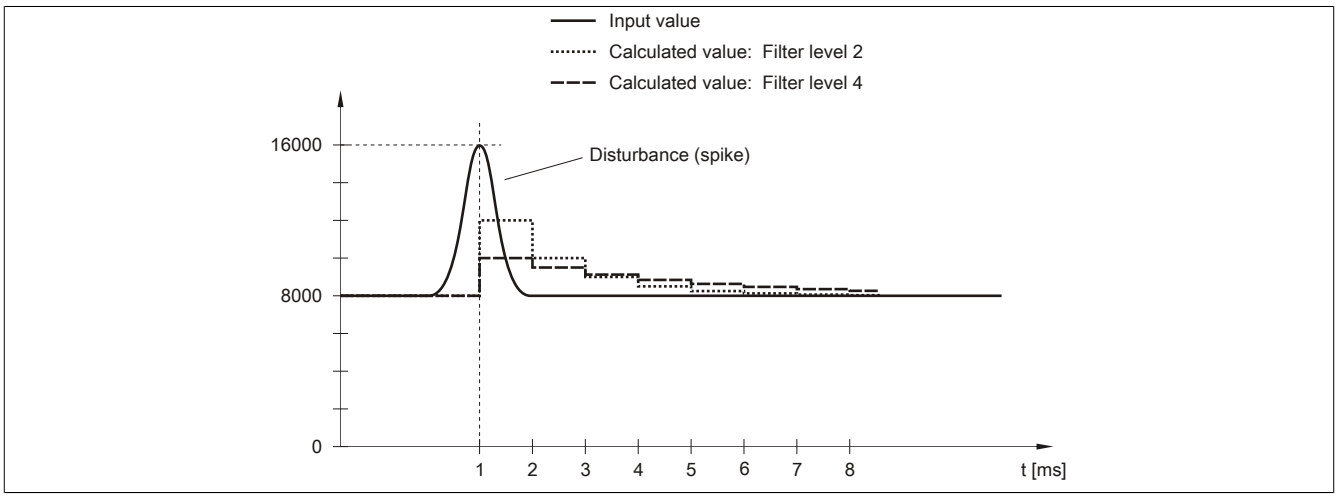


Figure 38: Calculated value during disturbance

1.12.8.7 Configuring the input filter

Name:
ConfigOutput01

The filter level and input ramp limiting of the input filter are set in this register.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter disabled (bus controller default setting)
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines input ramp limiting	000	The input value is applied without limitation (bus controller default setting)
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

1.12.8.8 Lower limit value

Name:
ConfigOutput03

The lower limit value for analog values can be set in this register. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Values	Information
INT	-32767 to 32767	Bus controller default setting: -32767

Information:

The default value of -32767 corresponds to the minimum default value of -10 VDC.

It is important to note that this setting applies to all channels!

1.12.8.9 Upper limit value

Name:
ConfigOutput04

The upper limit value for analog values can be set in this register. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Values	Information
INT	-32767 to 32767	Bus controller default setting: 32767

Information:

Default value 32767 corresponds to the maximum default value at +10 VDC.

It is important to note that this setting applies to all channels!

1.12.8.10 Input status

Name:
StatusInput01

This register is used to monitor the module inputs. A change in the monitoring status generates an error message.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
...		...	
6 - 7	Channel 4	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line

Limiting the analog value

In addition to the status information, the analog value is fixed to the values listed below by default in an error state. The analog value is limited to the new values if the limit values were changed.

Error state	Digital value on error (default values)
Open circuit	+32767 (0x7FFF)
Upper limit value overshot	+32767 (0x7FFF)
Lower limit value undershot	-32767 (0x8001)
Invalid value	-32768 (0x8000)

1.12.8.11 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
Inputs without filtering	100 µs
Inputs with filtering	500 µs

1.12.8.12 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

	Minimum I/O update time
Inputs without filtering	400 µs for all inputs
Inputs with filtering	1 ms

1.13 X20AI4322

1.13.1 General information

The module is equipped with 4 inputs with 12-bit digital converter resolution. It is possible to select between the two current ranges 0 to 20 mA and 4 to 20 mA.

- 4 analog inputs, 0 to 20 mA or 4 to 20 mA
- 12-bit digital converter resolution

1.13.2 Order data

Order number	Short description	Figure
	Analog inputs	
X20AI4322	X20 analog input module, 4 inputs, 0-20 mA / 4-20 mA, 12-bit converter resolution, configurable input filter	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 53: X20AI4322 - Order data

1.13.3 Technical data

Order number	X20AI4322
Short description	
I/O module	4 analog inputs 0 to 20 mA / 4 to 20 mA
General information	
B&R ID code	0xCAB3
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1.1 W
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
EAC	Yes
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
DNV GL	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
LR	ENV1
Analog inputs	
Input	0 to 20 mA/4 to 20 mA
Input type	Differential input
Digital converter resolution	12-bit
Conversion time	400 µs for all inputs
Output format	
Data type	INT
Current	0x0000 - 0x7FFF / 1 LSB = 0x0008 = 4.883 µA
Load	<400 Ω
Input protection	Protection against wiring with supply voltage
Permissible input signal	Max. ±50 mA
Output of digital value during overload	Configurable
Conversion procedure	SAR
Input filter	3rd-order low pass / cutoff frequency 1 kHz
Max. error at 25°C	
Gain	
0 to 20 mA	0.08% [1]
4 to 20 mA	0.1% [1]
Offset	
0 to 20 mA	0.03% [2]
4 to 20 mA	0.16% [2]
Max. gain drift	
0 to 20 mA	0.009 %/°C [1]
4 to 20 mA	0.0113 %/°C [1]
Max. offset drift	
0 to 20 mA	0.004 %/°C [2]
4 to 20 mA	0.005 %/°C [2]
Common-mode rejection	
DC	70 dB
50 Hz	70 dB
Common-mode range	±12 V
Crosstalk between channels	-70 dB
Nonlinearity	<0.05% [2]
Insulation voltage between channel and bus	500 V_{eff}
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes

Table 54: X20AI4322 - Technical data

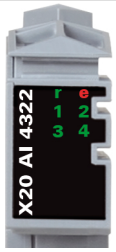
Order number	X20AI4322
Installation elevation above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Pitch	12.5$^{+0.2}$ mm

Table 54: X20AI4322 - Technical data

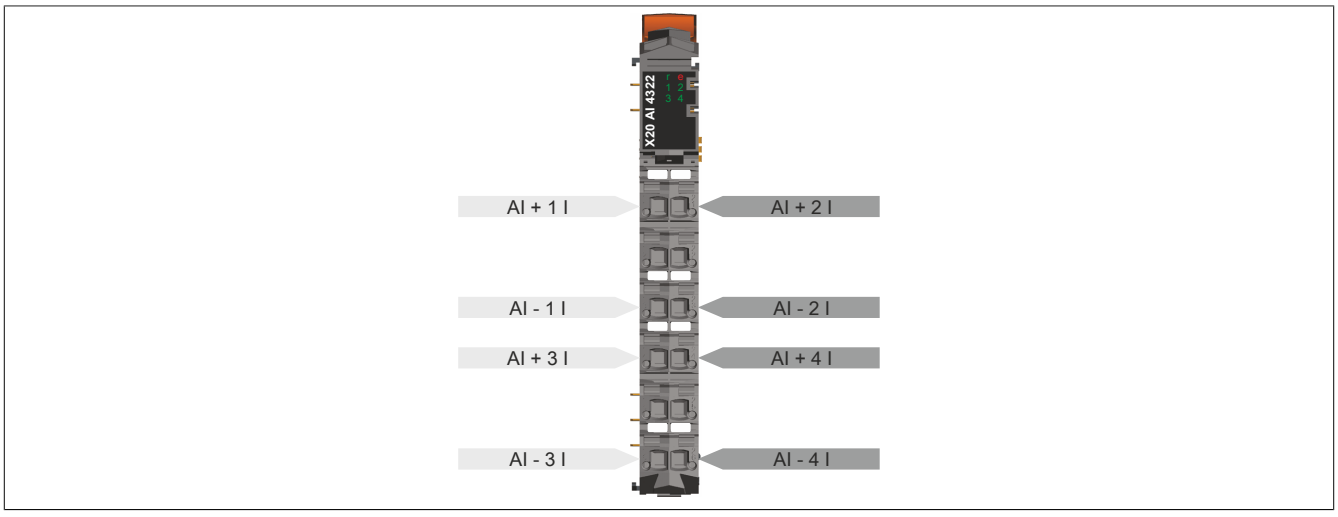
1) Based on the current measured value.
2) Based on the 20 mA measurement range.

1.13.4 LED status indicators

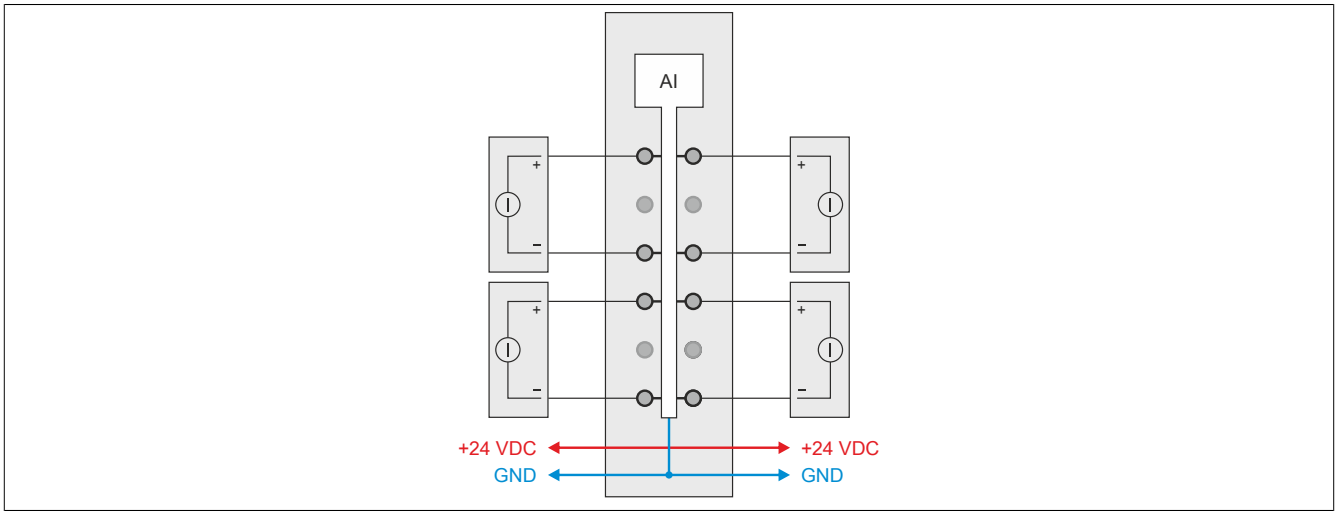
For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 system user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Green	Blinking	Input signal overflow or underflow
			On	Analog/digital converter running, value OK

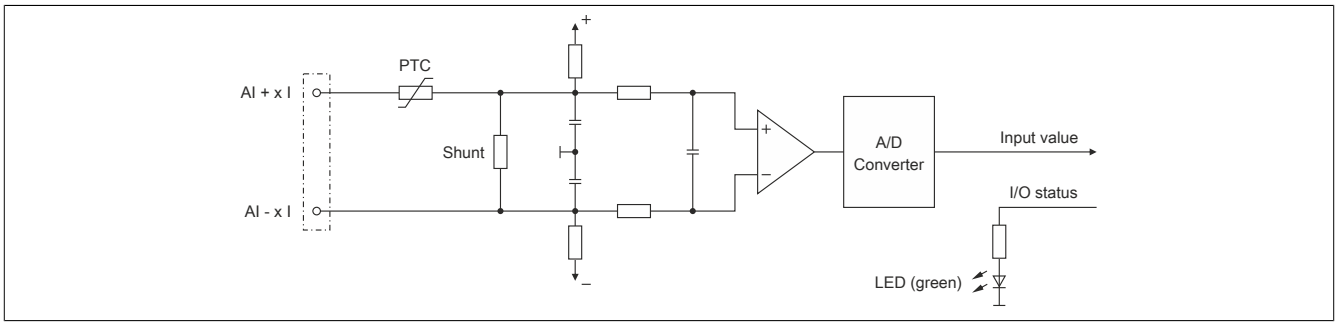
1.13.5 Pinout



1.13.6 Connection example



1.13.7 Input circuit diagram



1.13.8 Register description

1.13.8.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 system user's manual.

1.13.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration						
16	ConfigOutput01 (Input filter)	USINT				•
18	ConfigOutput02 (Channel type)	USINT				•
20	ConfigOutput03 (Lower limit value)	INT				•
22	ConfigOutput04 (Upper limit value)	INT				•
Analog signal - Communication						
Index * 2 - 2	AnalogInput0N (Index N = 1 to 4)	INT	•			
30	StatusInput01	USINT	•			

1.13.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration							
16	-	ConfigOutput01 (Input filter)	USINT				•
18	-	ConfigOutput02 (Channel type)	USINT				•
20	-	ConfigOutput03 (Lower limit value)	INT				•
22	-	ConfigOutput04 (Upper limit value)	INT				•
Analog signal - Communication							
Index * 2 - 2	Index * 2 - 2	AnalogInput0N (Index N = 1 to 4)	INT	•			
30	-	StatusInput01	USINT		•		

1) The offset specifies the position of the register within the CAN object.

1.13.8.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

1.13.8.3.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

1.13.8.4 Analog inputs

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

1.13.8.5 Analog input values

Name:
AnalogInput01 to AnalogInput04

The analog input values are mapped to this register.

Data type	Value	Input signal:
INT	0 to 32767	Current signal 0 to 20 mA
	-8192 to 32767	Current signal 4 to 20 mA (value 0 corresponds to 4 mA)

1.13.8.6 Input filter

This module is equipped with a configurable input filter. The minimum cycle time must be >500 µs. Filtering is disabled for shorter cycle times.

If the input filter is active, then the scan rate for the channels is measured in ms. The time offset between the channels is 200 µs. The conversion takes place asynchronously to the network cycle.

1.13.8.6.1 Input ramp limiting

Input ramp limiting can only be performed in conjunction with filtering. Input ramp limiting is performed before filtering.

The difference of the input value change is checked for exceeding the specified limit. In the event of overshoot, the tracked input value is equal to the old value ± the limit value.

Configurable limit values:

Value	Limit value
0	The input value is used without limitation.
1	0x3FFF = 16383
2	0x1FFF = 8191
3	0x0FFF = 4095
4	0x07FF = 2047
5	0x03FF = 1023
6	0x01FF = 511
7	0x00FF = 255

Input ramp limiting is well suited for suppressing disturbances (spikes). The following examples show the functionality of input ramp limiting based on an input step and a disturbance.

Example 1

The input value jumps from 8000 to 17000. The diagram shows the tracked input value with the following settings:

Input ramp limiting = 4 = 0x07FF = 2047

Filter level = 2

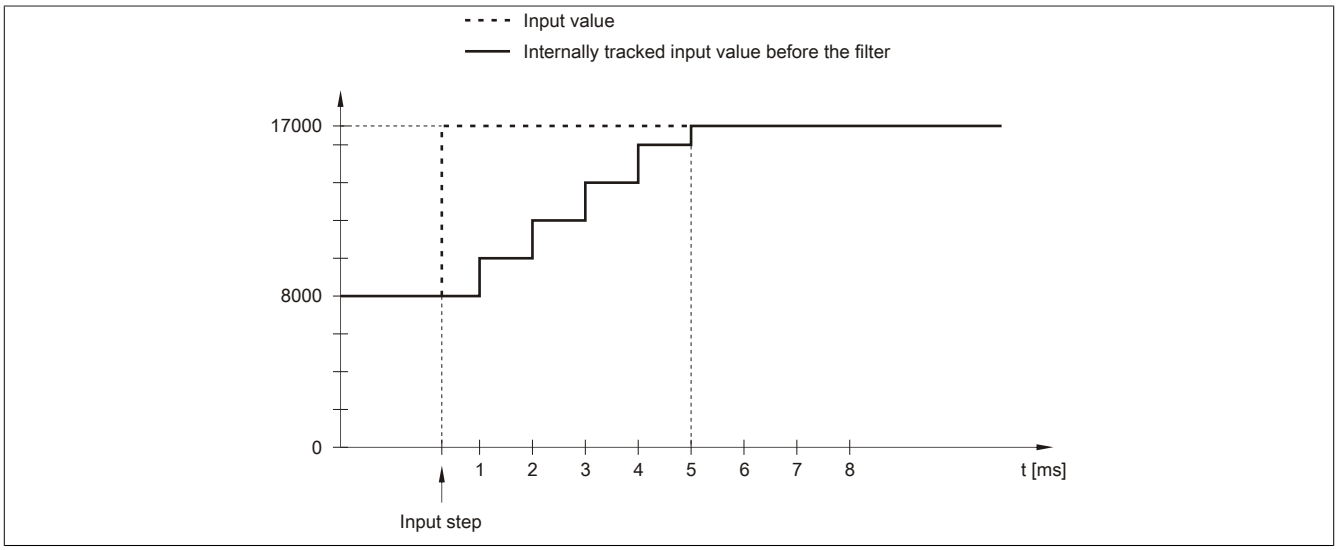


Figure 39: Tracked input value for input step

Example 2

A disturbance interferes with the input value. The diagram shows the tracked input value with the following settings:

Input ramp limiting = 4 = 0x07FF = 2047

Filter level = 2

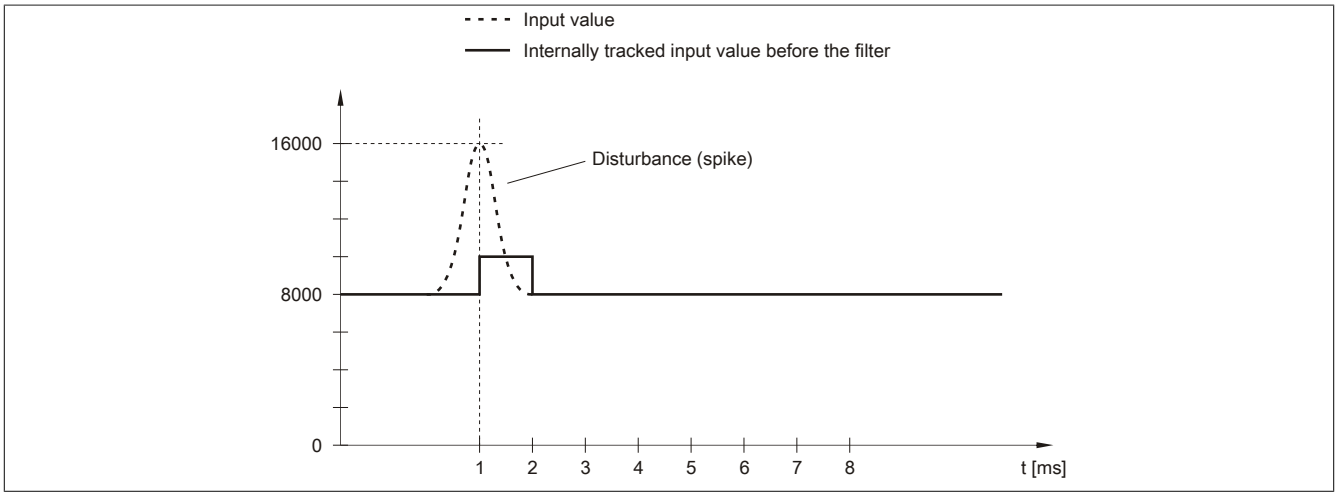


Figure 40: Tracked input value for disturbance

1.13.8.6.2 Filter level

A filter can be defined to prevent large input steps. This filter is used to bring the input value closer to the actual analog value over a period of several bus cycles.
Filtering takes place after any input ramp limiting has been carried out.

Formula for calculating the input value:

$$\text{Value}_{\text{New}} = \text{Value}_{\text{Old}} - \frac{\text{Value}_{\text{Old}}}{\text{Filter level}} + \frac{\text{Input value}}{\text{Filter level}}$$

Adjustable filter levels:

Value	Filter level
0	Filter switched off
1	Filter level 2
2	Filter level 4
3	Filter level 8
4	Filter level 16
5	Filter level 32
6	Filter level 64
7	Filter level 128

The following examples show the functionality of the filter based on an input step and a disturbance.

Example 1

The input value jumps from 8000 to 16000. The diagram shows the calculated value with the following settings:

Input ramp limiting = 0

Filter level = 2 or 4

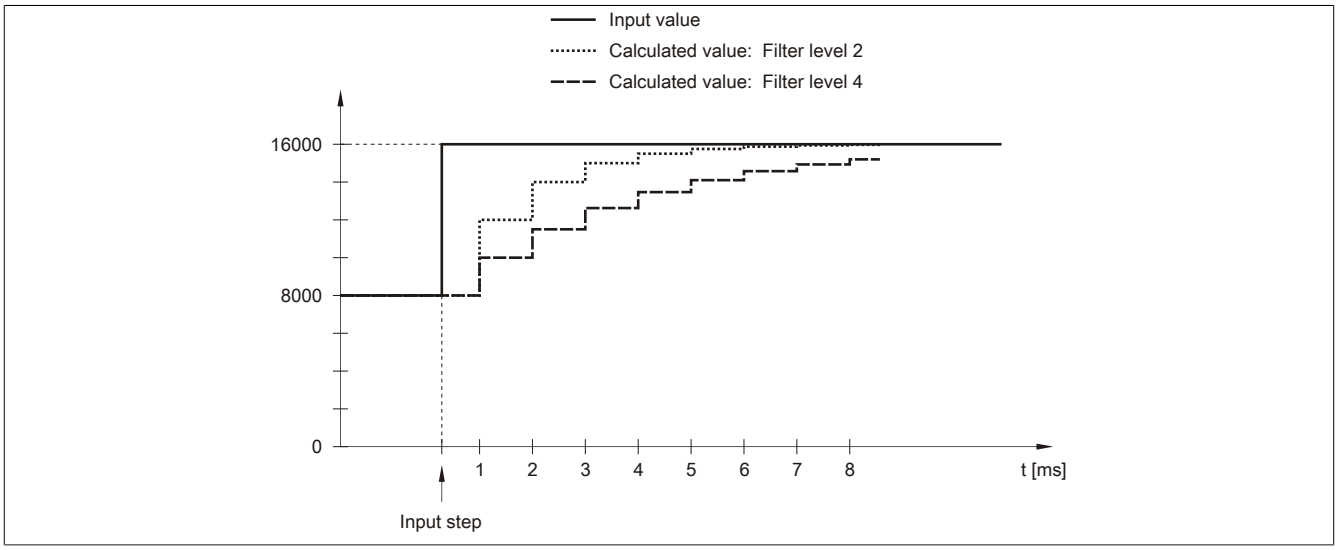


Figure 41: Calculated value during input step

Example 2

A disturbance interferes with the input value. The diagram shows the calculated value with the following settings:

Input ramp limiting = 0

Filter level = 2 or 4

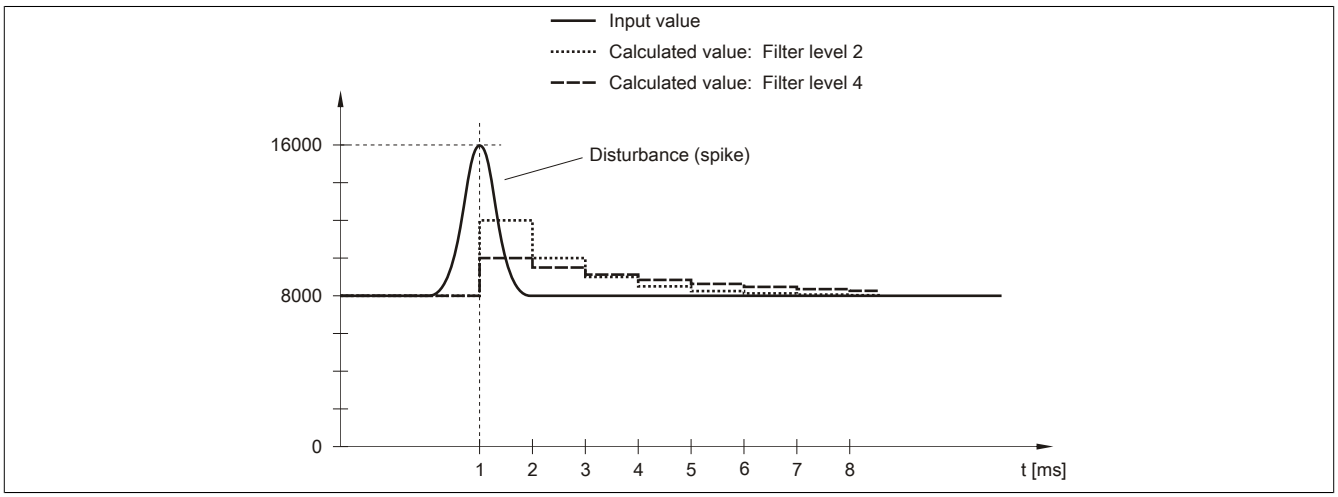


Figure 42: Calculated value during disturbance

1.13.8.7 Configuring the input filter

Name:
ConfigOutput01

The filter level and input ramp limiting of the input filter are set in this register.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter disabled (bus controller default setting)
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines input ramp limiting	000	The input value is applied without limitation (bus controller default setting)
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

1.13.8.8 Channel type

Name:
ConfigOutput02

This register can be used to set the range of the current signal. This is determined by how they are configured. The following input signals can be set:

- 0 to 20 mA current signal
- 4 to 20 mA current signal

Data type	Values	Bus controller default setting
USINT	See the bit structure.	15

Bit structure:

Bit	Description	Value	Information
0 - 3	Reserved	1	
4	Channel 1: Current measurement range	0	0 to 20 mA current signal (bus controller default setting)
		1	4 to 20 mA current signal
...		...	
7	Channel 4: Current measurement range	0	0 to 20 mA current signal (bus controller default setting)
		1	4 to 20 mA current signal

1.13.8.9 Lower limit value

Name:
ConfigOutput03

This register can be used to configure the lower limit for analog values. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Values	Information
INT	-32768 to 32767	Bus controller default setting: -32767

Information:

- **When configured as 0 to 20 mA, this value should be set to 0.**
- **When configured as 4 to 20 mA, this value can be set to -8192 (corresponds to 0 mA) in order to display values <4 mA.**

Keep in mind that this setting applies to all channels!

1.13.8.10 Upper limit value

Name:
ConfigOutput04

This register can be used to configure the upper limit for analog values. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Values	Information
INT	-32768 to 32767	Bus controller default setting: 32767

Information:

The default value of 32767 corresponds to the maximum default value at 20 mA.

Keep in mind that this setting applies to all channels!

1.13.8.11 Input status

Name:
StatusInput01

This register is used to monitor the module inputs. A change in the monitoring status generates an error message.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
...		...	
6 - 7	Channel 4	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded

Limiting the analog value

In addition to the status information, the analog value is set to the values listed below by default when an error occurs. The analog value is limited to the new values if the limit values were changed.

Error status	Digital value for error (default values)	
	0 to 20 mA	4 to 20 mA
Upper limit value exceeded	+32767 (0x7FFF)	
Lower limit value exceeded	0	-8191 (0xE001)

1.13.8.12 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Inputs without filtering	100 µs
Inputs with filtering	500 µs

1.13.8.13 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time	
Inputs without filtering	400 µs for all inputs
Inputs with filtering	1 ms

1.14 X20(c)AI4622

1.14.1 General information

1.14.1.1 Other applicable documents

For additional and supplementary information, see the following documents.

Other applicable documents

Document name	Title
MAX20	X20 System user's manual
MAEMV	Installation / EMC guide

1.14.1.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, method 4, exposure 21 days

1.14.1.2.1 Starting temperature

The starting temperature describes the minimum permissible ambient temperature in a voltage-free state at the time the coated module is switched on. This is permitted to be as low as -40°C. During operation, the conditions as specified in the technical data continue to apply.

Information:

It is important to absolutely ensure that there is no forced cooling by air currents in the closed control cabinet, e.g. due to the use of a fan or ventilation slots.

1.14.1.3 Order data

Order number	Short description	Figure
	Analog inputs	
X20AI4622	X20 analog input module, 4 inputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution, configurable input filter	
X20cAI4622	X20 analog input module, coated, 4 inputs, ±10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution, configurable input filter	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 55: X20AI4622, X20cAI4622 - Order data

1.14.1.4 Module description

The module is equipped with 4 inputs with 13-bit (including sign) digital converter resolution. It is possible to select between the current and voltage signal using different terminals.

Functions:

- Input filter
- Setting the input signal
- Monitoring the input signal

Analog input filter

The module is equipped with a configurable input filter with input ramp limiting.

Monitoring the input signal

The input signal of the analog inputs is monitored against the upper and lower limit values as well as for open circuit.

1.14.2 Technical description

1.14.2.1 Technical data

Order number	X20AI4622	X20cAI4622
Short description		
I/O module	4 analog inputs ±10 V or 0 to 20 mA / 4 to 20 mA	
General information		
B&R ID code	0x1BAA	0xE1EF
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using LED status indicator and software	
Inputs	Yes, using LED status indicator and software	
Channel type	Yes, using software	
Power consumption		
Bus	0.01 W	
Internal I/O	1.1 W [1]	
Additional power dissipation caused by actuators (resistive) [W]	-	
Certifications		
CE	Yes	
UKCA	Yes	
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X	
UL	cULus E115267 Industrial control equipment	
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5	
DNV	Temperature: **B** (0 to 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)	
LR	ENV1	
KR	Yes	
ABS	Yes	
BV	**EC33B** Temperature: 5 - 55°C Vibration: 4 g EMC: Bridge and open deck	
EAC	Yes	
KC	Yes	-
Analog inputs		
Input	±10 V or 0 to 20 mA / 4 to 20 mA, via different terminal connections	
Input type	Differential input	
Digital converter resolution		
Voltage	±12-bit	
Current	12-bit	
Conversion time	400 µs for all inputs	
Output format	INT	
Output format		
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0008 = 2.441 mV	
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0008 = 4.883 µA	
Input impedance in signal range		
Voltage	20 MΩ	
Current	-	
Load		
Voltage	-	
Current	<400 Ω	
Input protection	Protection against wiring with supply voltage	
Permissible input signal		
Voltage	Max. ±30 V	
Current	Max. ±50 mA	
Output of digital value during overload	Configurable	
Conversion procedure	SAR	
Input filter	Third-order low-pass filter / Cutoff frequency 1 kHz	
Max. error		
Voltage		
Gain	0.08% [2]	
Offset	0.015% [3]	
Current		
Gain	0 to 20 mA = 0.08% / 4 to 20 mA = 0.1% [2]	
Offset	0 to 20 mA = 0.03% / 4 to 20 mA = 0.0375% [4]	

Table 56: X20AI4622, X20cAI4622 - Technical data

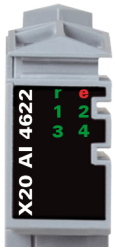
Order number	X20AI4622	X20cAI4622
Max. gain drift		
Voltage	0.006%/°C [2]	
Current	0 to 20 mA = 0.009 %/°C 4 to 20 mA = 0.0113 %/°C [2]	
Max. offset drift		
Voltage	0.002%/°C [3]	
Current	0 to 20 mA = 0.004 %/°C 4 to 20 mA = 0.005 %/°C [4]	
Common-mode rejection		
DC	70 dB	
50 Hz	70 dB	
Common-mode range	±12 V	
Crosstalk between channels	<-70 dB	
Nonlinearity		
Voltage	<0.025% [3]	
Current	<0.05% [4]	
Insulation voltage between channel and bus	500 V_{eff}	
Electrical properties		
Electrical isolation	Channel isolated from bus Channel not isolated from channel	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation elevation above sea level		
0 to 2000 m	No limitation	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
Degree of protection per EN 60529	IP20	
Ambient conditions		
Temperature		
Operation		
Horizontal mounting orientation	-25 to 60°C	
Vertical mounting orientation	-25 to 50°C	
Derating	-	
Starting temperature	-	Yes, -40°C
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical properties		
Note	Order 1x terminal block X20TB12 separately. Order 1x bus module X20BM11 separately.	Order 1x terminal block X20TB12 separately. Order 1x bus module X20cBM11 separately.
Pitch	12.5$^{+0.2}$ mm	

Table 56: X20AI4622, X20cAI4622 - Technical data

1) To reduce power dissipation, B&R recommends bridging unused inputs on the terminals or configuring them as current signals.
2) Based on the current measured value.
3) Based on the 20 V measurement range.
4) Based on the 20 mA measurement range.

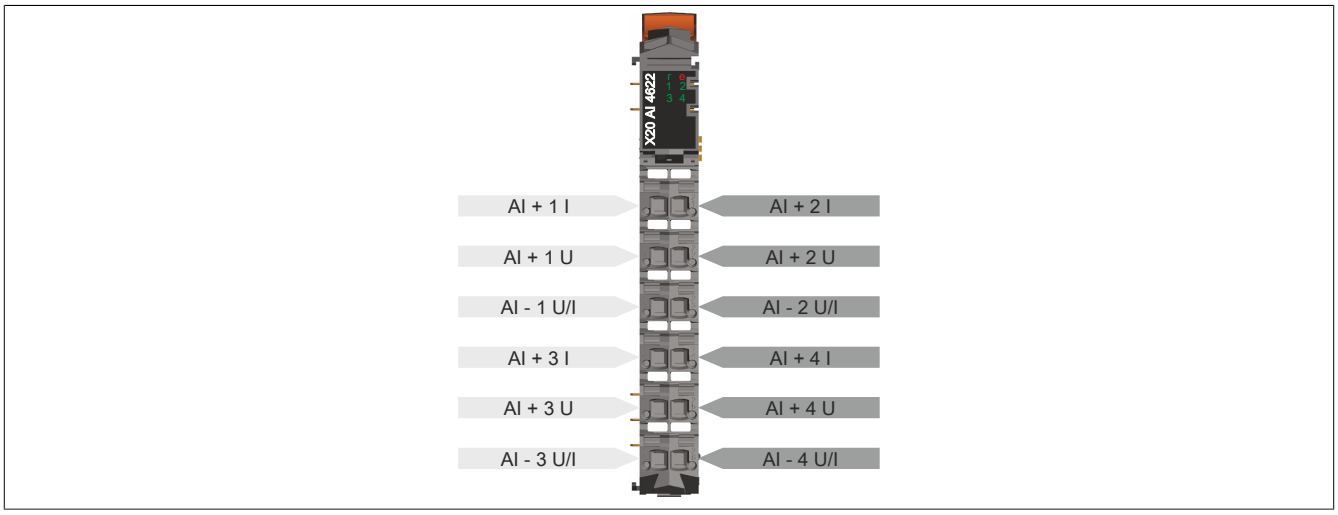
1.14.2.2 LED status indicators

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 System user's manual.

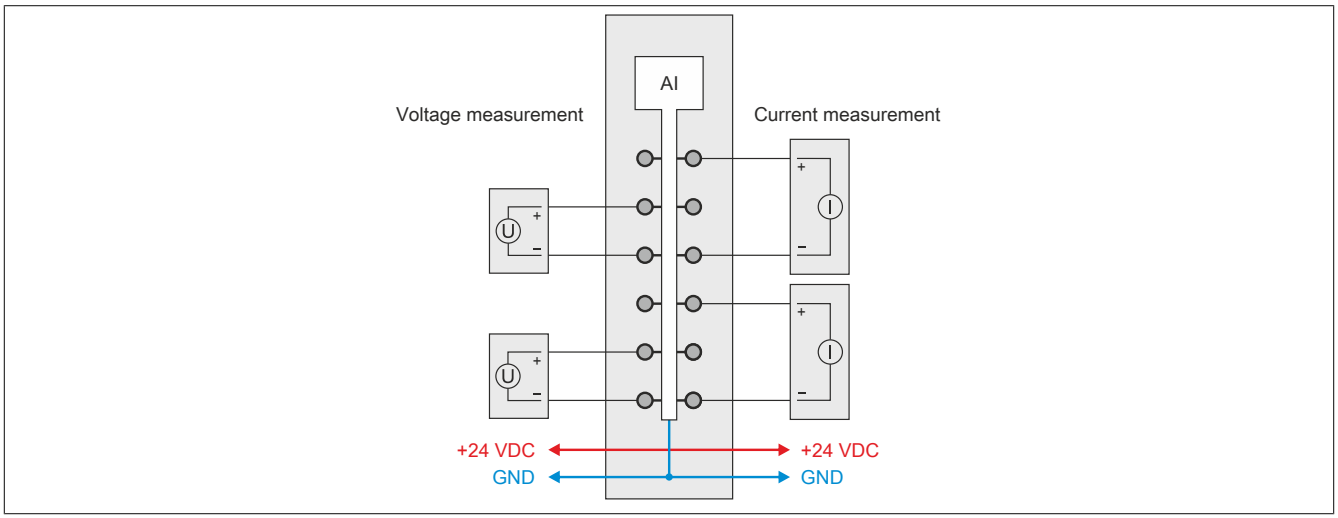
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Green	Off	Open line[1] or sensor is disconnected
			Blinking	Input signal overflow or underflow
			On	Analog/digital converter running, value OK

1) Open line detection only possible when measuring voltage.

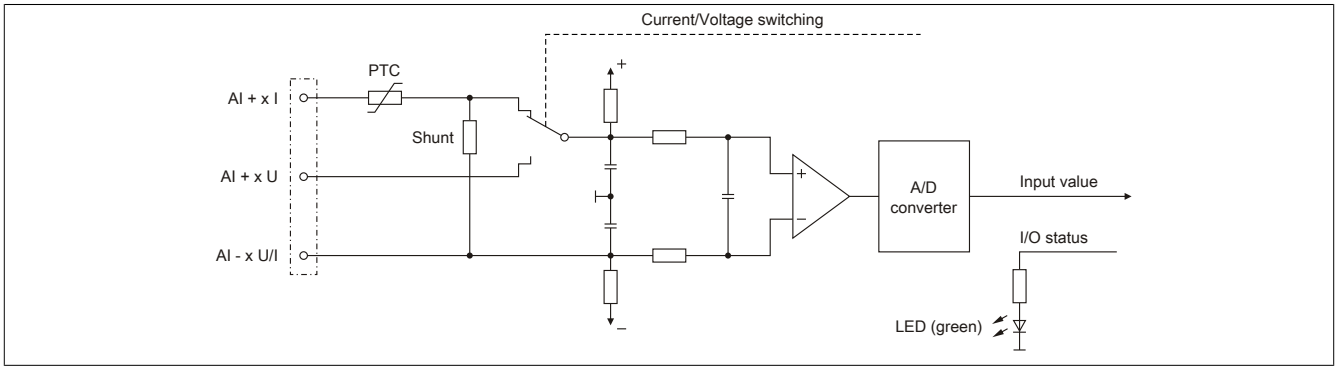
1.14.2.3 Pinout



1.14.2.4 Connection example



1.14.2.5 Input circuit diagram



1.14.3 Function description

1.14.3.1 Input filter

The module is equipped with a configurable input filter. The minimum cycle time must be >500 µs. The filter function is disabled for shorter cycle times.

When the input filter is activated, the channels are sampled at millisecond intervals. The time offset between the channels is 200 µs. The conversion takes place asynchronously to the network cycle.

Information:

The register is described in "Configuring the input filter" on page 343.

1.14.3.1.1 Input ramp limiting

Input ramp limiting can only be performed in conjunction with filtering. Input ramp limiting is performed before filtering.

The difference of the input value change is checked for exceeding the specified limit. In the event of overshoot, the tracked input value is equal to the old value ± the limit value.

Configurable limit values:

Value	Limit value
0	The input value is used without limitation.
1	0x3FFF = 16383
2	0x1FFF = 8191
3	0x0FFF = 4095
4	0x07FF = 2047
5	0x03FF = 1023
6	0x01FF = 511
7	0x00FF = 255

Input ramp limiting is well suited for suppressing disturbances (spikes). The following examples show the functionality of input ramp limiting based on an input step and a disturbance.

Example 1

The input value jumps from 8000 to 17000. The diagram shows the tracked input value with the following settings:

Input ramp limiting = 4 = 0x07FF = 2047

Filter level = 2

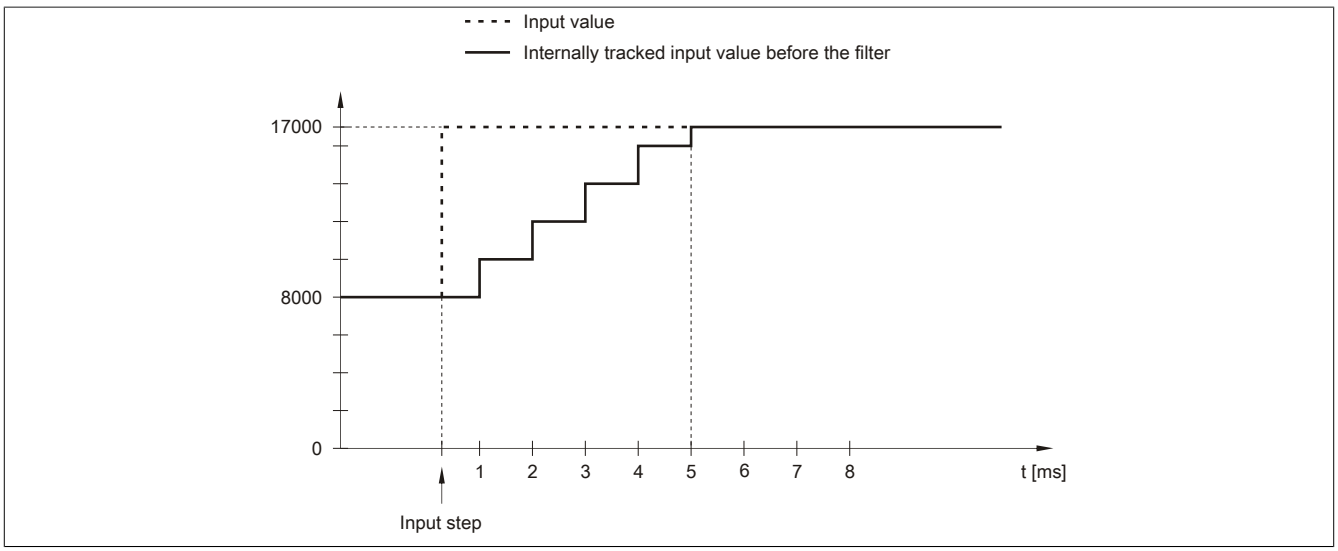


Figure 43: Tracked input value for input step

Example 2

A disturbance interferes with the input value. The diagram shows the tracked input value with the following settings:

Input ramp limiting = 4 = 0x07FF = 2047

Filter level = 2

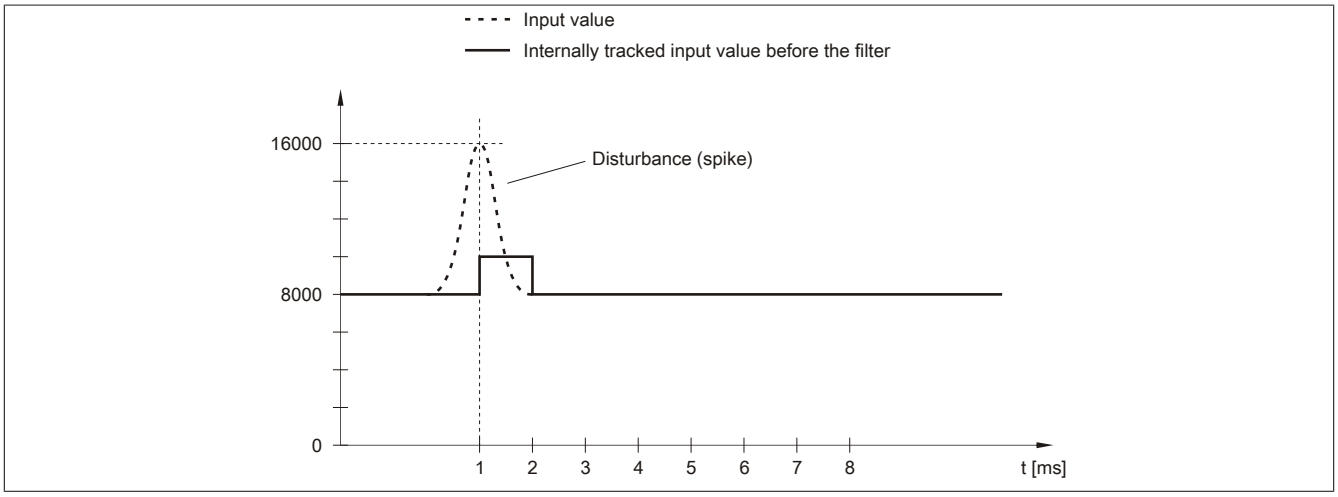


Figure 44: Tracked input value for disturbance

1.14.3.1.2 Filter level

A filter can be defined to prevent large input steps. This filter is used to bring the input value closer to the actual analog value over a period of several bus cycles.
Filtering takes place after any input ramp limiting has been carried out.

Formula for calculating the input value:

$$\text{Value}_{\text{New}} = \text{Value}_{\text{Old}} - \frac{\text{Value}_{\text{Old}}}{\text{Filter level}} + \frac{\text{Input value}}{\text{Filter level}}$$

Adjustable filter levels:

Value	Filter level
0	Filter switched off
1	Filter level 2
2	Filter level 4
3	Filter level 8
4	Filter level 16
5	Filter level 32
6	Filter level 64
7	Filter level 128

The following examples show the functionality of the filter based on an input step and a disturbance.

Example 1

The input value jumps from 8000 to 16000. The diagram shows the calculated value with the following settings:

Input ramp limiting = 0

Filter level = 2 or 4

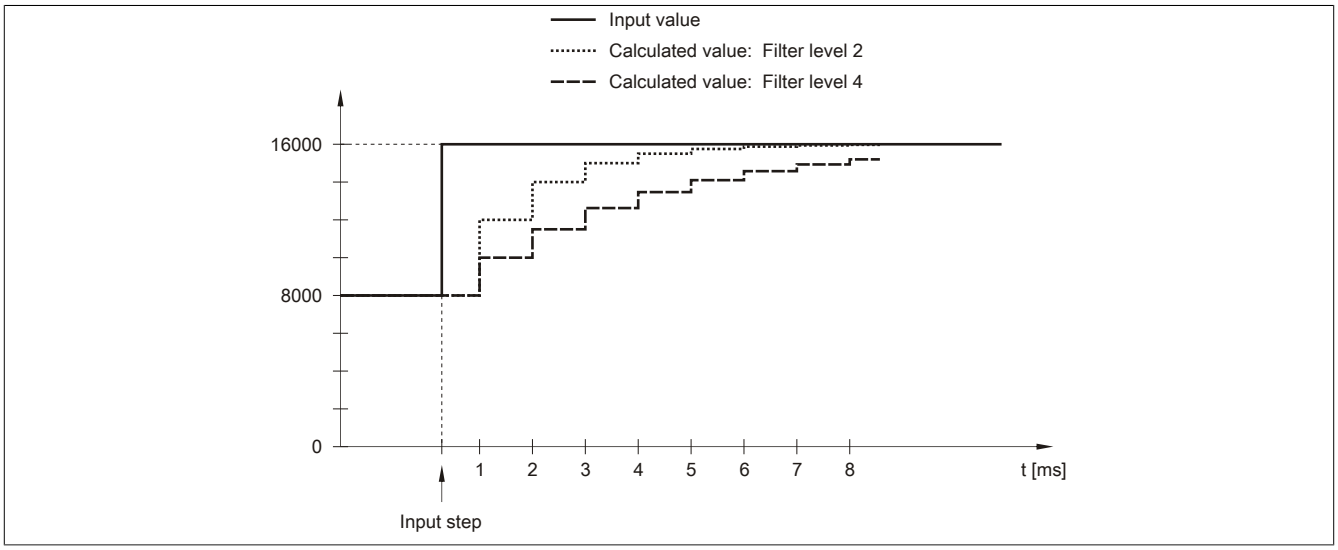


Figure 45: Calculated value during input step

Example 2

A disturbance interferes with the input value. The diagram shows the calculated value with the following settings:

Input ramp limiting = 0

Filter level = 2 or 4

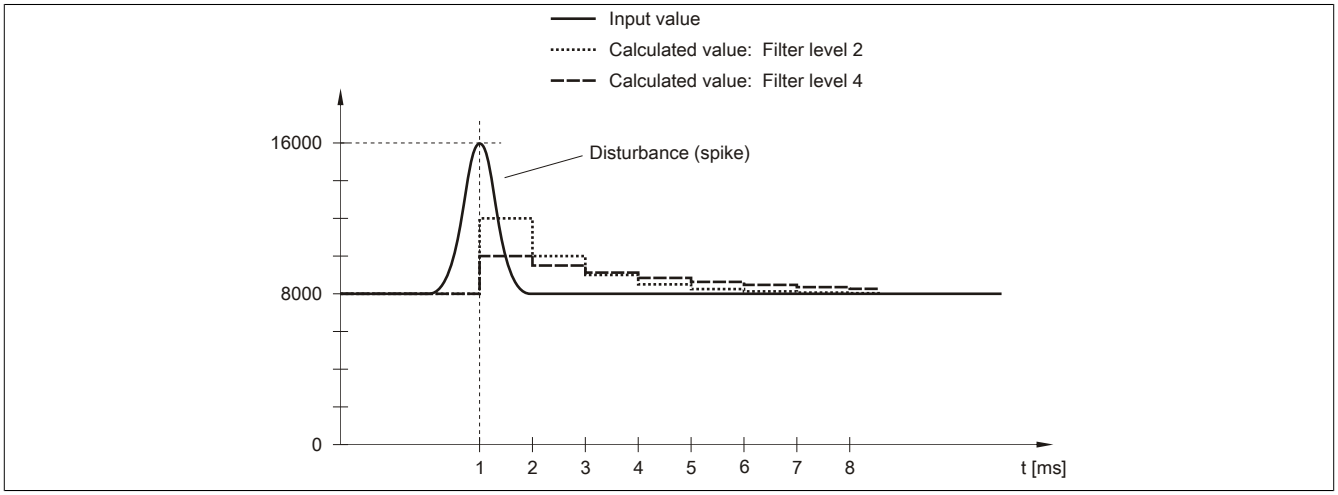


Figure 46: Calculated value during disturbance

1.14.3.2 Setting the input signal

The individual channels are designed for current and voltage signals. This differentiation is made using different terminals and an integrated switch in the module. The switch is automatically activated by the module depending on the specified configuration. The following input signals can be set:

- ±10 V voltage signal (default)
- 0 to 20 mA current signal
- 4 to 20 mA current signal

Information:

The register is described in "Channel type" on page 343.

1.14.3.3 Monitoring the input signal

The input signal is monitored at the upper and lower limit values. These must be defined according to the operating mode:

Limit value (default)	Voltage signal ±10 V		Current signal 0 to 20 mA		Current signal 4 to 20 mA	
Upper maximum limit value	+10 V	+32767 (0x7FFF)	20 mA	+32767 (0x7FFF)	20 mA	+32767 (0x7FFF)
Lower minimum limit value	-10 V	-32767 (0x8001)	0 mA	0[1)]	4 mA	0[2)]

1) • **Default setting:** The input value has a lower limit of 0x0000. Underflow monitoring is therefore not necessary.
• **After lower limit value change:** The input value is limited to the set value. The status bit is set if undershot.

2) The analog value is limited down to 0 at currents <4 mA. The status bit for the lower limit is set.

Other limit values can be defined if necessary. The limit values apply to all channels. These are enabled automatically by writing to the limit value registers. From this point on, the analog values will be monitored and limited according to the new limits. The results of monitoring are displayed in the status register.

Examples of limit value settings

Use case	Limit value settings
Current signal: 4 to 20 mA	If values <4 mA should be measured for a current signal with 4 to 20 mA, a negative limit value must be set: 0 mA corresponds to value -8192 (0xE000).
Mixed voltage and current signal	The set limit values apply to all channels. A compromise must therefore be made for mixed operation (voltage and current signal mixed). The following setting has proven to be effective: Upper limit value = +32767, lower limit value = -32767 This also allows negative voltage values to be measured. With a lower limit value of 0, the voltage value would be limited to 0.
Current signal on all channels	All channels are configured for current measurement. The limit value setting in Automation Studio is not adjusted automatically. This means that +32767 is set for the upper limit value and -32767 for the lower limit value. The necessary adjustments must be made by the user, e.g. lower limit value = 0

Limiting the analog value

In addition to the status information, the analog value is fixed to the values listed below by default in an error state. The analog value is limited to the new values if the limit values were changed.

Error state	Digital value on error (default values)
Open circuit	+32767 (0x7FFF)
Upper limit value overshot	+32767 (0x7FFF)
Lower limit value undershot	-32767 (0x8001)
Invalid value	-32768 (0x8000)

Information:

The register is described in "Status of the inputs" on page 345.

1.14.4 Register description

1.14.4.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 System user's manual.

1.14.4.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
16	ConfigOutput01 (input filter)	USINT				•
18	ConfigOutput02 (channel type)	USINT				•
20	ConfigOutput03 (lower limit value)	INT				•
22	ConfigOutput04 (upper limit value)	INT				•
Communication						
0	AnalogInput01	INT	•			
2	AnalogInput02	INT	•			
4	AnalogInput03	INT	•			
6	AnalogInput04	INT	•			
30	StatusInput01	USINT	•			

1.14.4.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
16	-	ConfigOutput01 (input filter)	USINT				•
18	-	ConfigOutput02 (channel type)	USINT				•
20	-	ConfigOutput03 (lower limit value)	INT				•
22	-	ConfigOutput04 (upper limit value)	INT				•
Communication							
0	0	AnalogInput01	INT	•			
2	2	AnalogInput02	INT	•			
4	4	AnalogInput03	INT	•			
6	6	AnalogInput04	INT	•			
30	-	StatusInput01	USINT		•		

1) The offset specifies the position of the register within the CAN object.

1.14.4.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

1.14.4.3.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

1.14.4.4 Analog signal - Configuration

1.14.4.4.1 Configuring the input filter

Name:
ConfigOutput01

The filter level and input ramp limiting of the input filter are set in this register.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter disabled (bus controller default setting)
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines input ramp limiting	000	The input value is applied without limitation (bus controller default setting)
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7	Reserved	0	

1.14.4.4.2 Channel type

Name:
ConfigOutput02

The type and range of signal measurement can be set in this register.

The individual channels are designed for current and voltage signals. This differentiation is made using different terminals and an integrated switch in the module.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Voltage signal (bus controller default setting)
		1	Current signal, measurement range corresponding to bit 4
...		...	
3	Channel 4	0	Voltage signal (bus controller default setting)
		1	Current signal, measurement range corresponding to bit 7
4	Channel 1: Current measurement range	0	0 to 20 mA current signal (bus controller default setting)
		1	4 to 20 mA current signal
...		...	
7	Channel 4: Current measurement range	0	0 to 20 mA current signal (bus controller default setting)
		1	4 to 20 mA current signal

1.14.4.4.3 Lower limit value

Name:
ConfigOutput03

The lower limit value for analog values can be set in this register. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Values	Information
INT	-32768 to 32767	Bus controller default setting: -32768

Information:

- **The default value of -32767 corresponds to the minimum default value of -10 VDC.**
- **For a 0 to 20 mA configuration, this value should be set to 0.**
- **For a 4 to 20 mA configuration, this value can be set to -8192 (corresponds to 0 mA) in order to display values <4 mA.**

Information:

It is important to note that this setting applies to all channels!

1.14.4.4.4 Upper limit value

Name:
ConfigOutput04

The upper limit value for analog values can be set in this register. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Values	Information
INT	-32767 to 32767	Bus controller default setting: 32767

Information:

The default value 32767 corresponds to the maximum default value at 20 mA or +10 VDC.

Information:

It is important to note that this setting applies to all channels!

1.14.4.5 Analog signal - Communication

1.14.4.5.1 Analog inputs

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

1.14.4.5.2 Input values of analog inputs

Name:
AnalogInput01 to AnalogInput04

This register contains the analog input value depending on the configured operating mode.

Data type	Values	Input signal:
INT	-32768 to 32767	Voltage signal -10 to 10 VDC
	0 to 32767	Current signal 0 to 20 mA
	-8192 to 32767	Current signal 4 to 20 mA (value 0 corresponds to 4 mA)

1.14.4.5.3 Status of the inputs

Name:
StatusInput01

The module inputs are monitored in this register. The analog value is permanently defined at fixed values when the monitoring state changes and in the event of error. For details, see "Monitoring the input signal" on page 341.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Channel 1	00	No error
		01	Lower limit value undershot
		10	Upper limit value overshot
		11	Open circuit[1)]
...		...	
6 - 7	Channel 4	00	No error
		01	Lower limit value undershot
		10	Upper limit value overshot
		11	Open circuit[1)]

1) Only when monitoring the voltage signal ±10 V

1.14.4.6 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
Inputs without filtering	100 µs
Inputs with filtering	500 µs

1.14.4.7 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

	Minimum I/O update time
Inputs without filtering	300 µs for all inputs
Inputs with filtering	1 ms

1.15 X20AI4632

1.15.1 General information

1.15.1.1 Other applicable documents

For additional and supplementary information, see the following documents.

Other applicable documents

Document name	Title
MAX20	X20 System user's manual
MAEMV	Installation / EMC guide

1.15.1.2 Order data

Order number	Short description	Figure
	Analog inputs	
X20AI4632	X20 analog input module, 4 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 57: X20AI4632 - Order data

1.15.1.3 Module description

The module is equipped with 4 inputs with 16-bit digital converter resolution and very fast conversion time. It is possible to select between the current and voltage signal using different terminals.

Functions:

- Scaling
- Filtering
- Error monitoring
- Analysis functions

Scaling

The A/D converter data can optionally be scaled by the user to ensure the greatest possible flexibility.

Input filter

An input filter can be configured for each individual analog input.

Error monitoring

The input signal is monitored for range overshoot, synchronization errors and invalid sampling cycles. User-defined limit values can also be defined.

Analysis functions

In addition to sampling the analog input signal, the values determined can also be analyzed:

- Limit value analysis
- Recording the sampled values
- Trace

1.15.2 Technical description

1.15.2.1 Technical data

Order number	X20AI4632
Short description	
I/O module	4 analog inputs ±10 V or 0 to 20 mA
General information	
B&R ID code	0x1BA1
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using LED status indicator and software
Inputs	Yes, using LED status indicator and software
Channel type	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	1.5 W [1)]
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
UKCA	Yes
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
DNV	Temperature: **B** (0 to 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
LR	ENV1
KR	Yes
ABS	Yes
BV	**EC33B** Temperature: 5 - 55°C Vibration: 4 g EMC: Bridge and open deck
EAC	Yes
KC	Yes
Analog inputs	
Input	±10 V or 0 to 20 mA, via different terminal connections
Input type	Differential input
Digital converter resolution	
Voltage	±15-bit
Current	15-bit
Conversion time	50 µs for all inputs
Output format	INT
Output format	
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0001 = 305.176 µV
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 610.352 nA
Input impedance in signal range	
Voltage	20 MΩ
Current	-
Load	
Voltage	-
Current	<400 Ω
Input protection	Protection against wiring with supply voltage
Permissible input signal	
Voltage	Max. ±30 V
Current	Max. ±50 mA
Output of digital value during overload	
Undershoot	
Voltage	0x8001
Current	0x0000
Overshoot	
Voltage	0x7FFF
Current	0x7FFF
Conversion procedure	SAR
Input filter	Hardware - Third-order low-pass filter / cutoff frequency 10 kHz

Table 58: X20AI4632 - Technical data

Order number	X20AI4632
Max. error	
Voltage	
Gain	0.08% 2)
Offset	0.01% 3)
Current	
Gain	0.08% 2)
Offset	0.02% 4)
Max. gain drift	
Voltage	0.01%/°C 2)
Current	0.01%/°C 2)
Max. offset drift	
Voltage	0.001%/°C 3)
Current	0.002%/°C 4)
Common-mode rejection	
DC	70 dB
50 Hz	70 dB
Common-mode range	±12 V
Crosstalk between channels	<-70 dB
Nonlinearity	
Voltage	<0.01% 3)
Current	<0.015% 4)
Insulation voltage between channel and bus	500 V_{eff}
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	See section "Derating".
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x terminal block X20TB12 separately. Order 1x bus module X20BM11 separately.
Pitch	$12.5^{+0.2}$ mm

Table 58: X20AI4632 - Technical data

1) To reduce power dissipation, B&R recommends bridging unused inputs on the terminals or configuring them as current signals.
2) Based on the current measured value.
3) Based on the 20 V measurement range.
4) Based on the 20 mA measurement range.

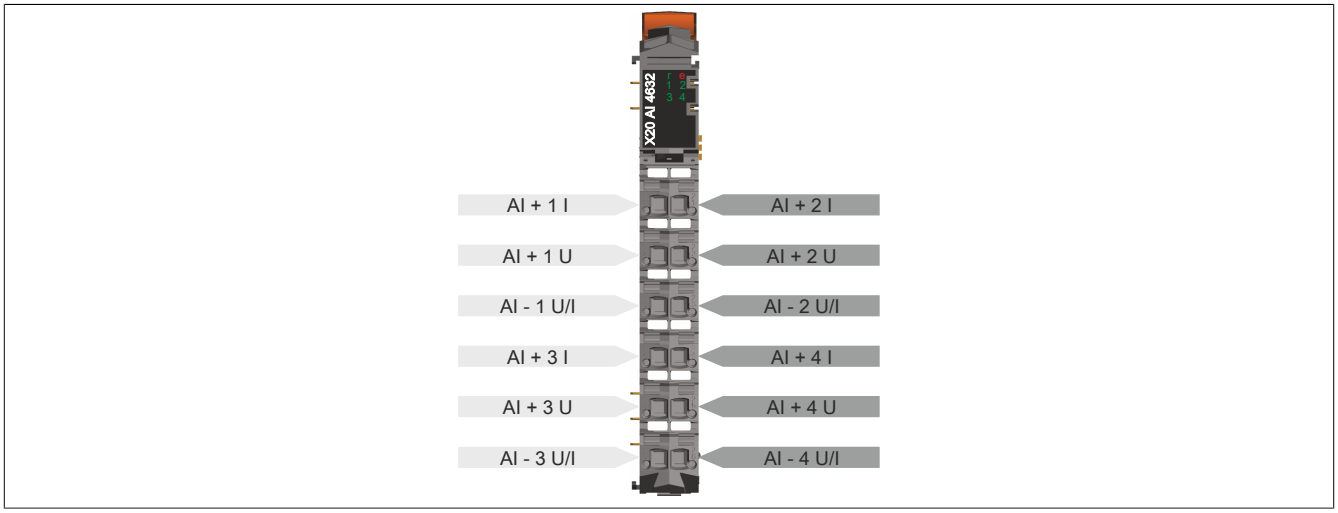
1.15.2.2 LED status indicators

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 System user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Double flash	System error: • Violation of the scan time • Synchronization error
	1 - 4	Green	Off	Open line[2] or sensor is disconnected
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.
2) Open line detection only possible when measuring voltage.

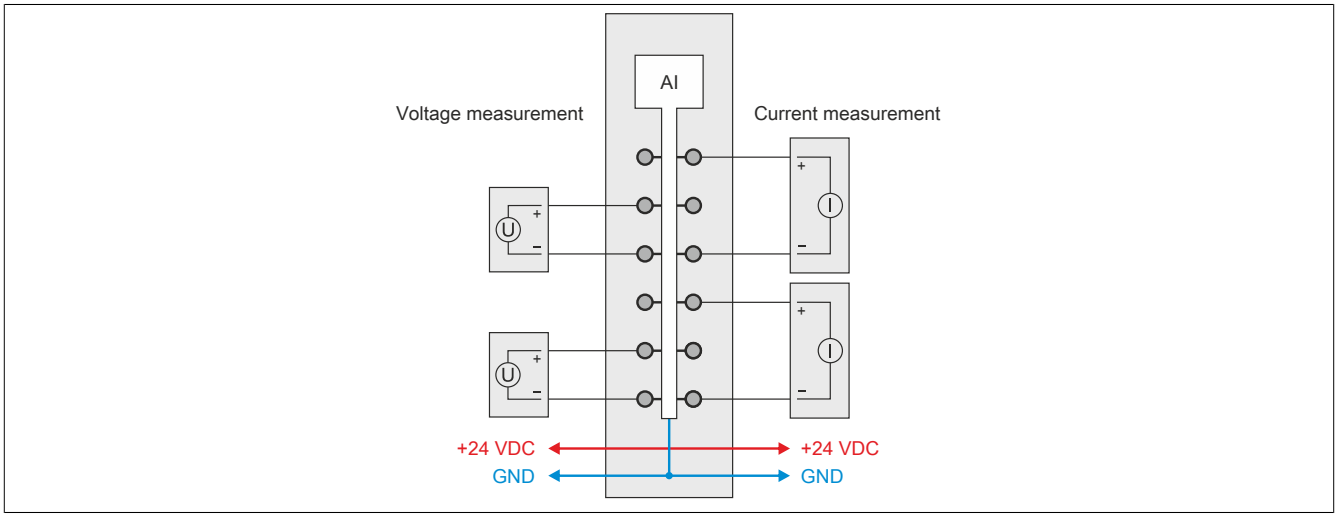
1.15.2.3 Pinout



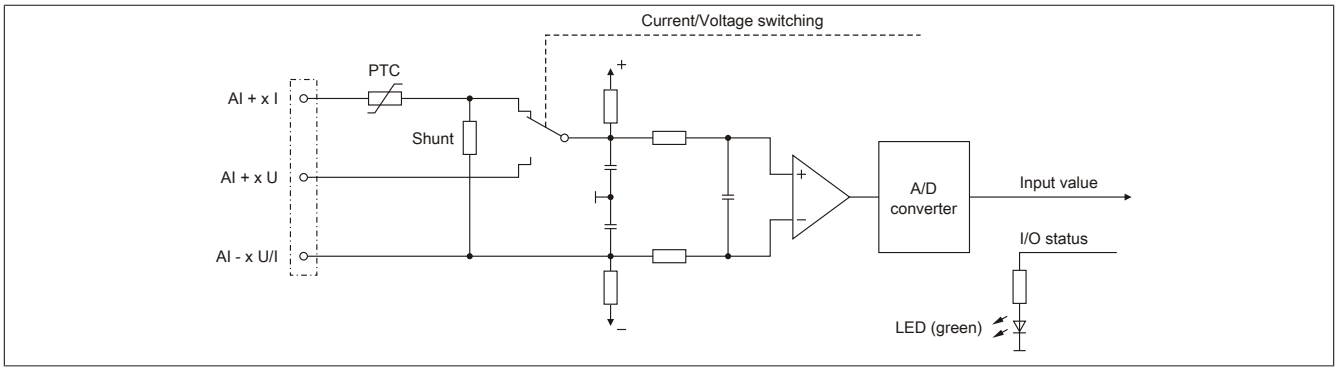
1.15.2.4 Connection example

To prevent disturbances, the following modules must be separated by at least one module:

- Bus receiver X20BR9300
- Supply module X20PS3300/X20PS3310
- Supply module X20PS9400/X20PS9402
- Power supply module X20PS9600/X20PS9602
- Controller



1.15.2.5 Input circuit diagram

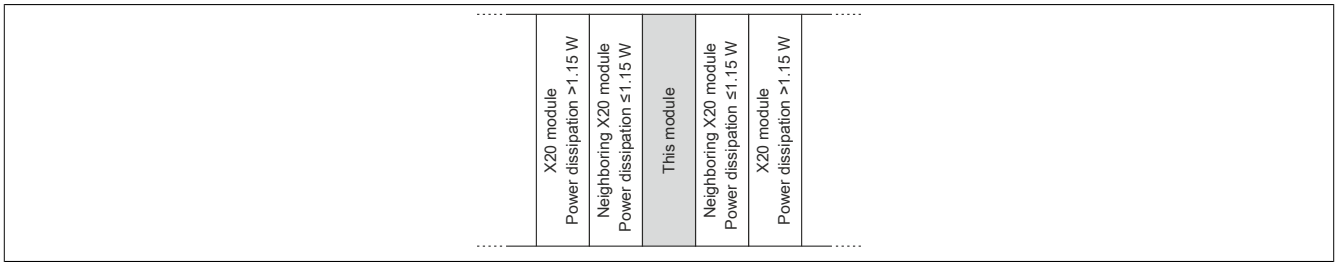


1.15.2.6 Derating

There is no derating when operated below 55°C.

When operated above 55°C, the modules to the left and right of this module are permitted to have a maximum power dissipation of 1.15 W!

For an example of calculating the power dissipation of I/O modules, see section "Mechanical and electrical configuration - Power dissipation of I/O modules" in the X20 user's manual.



1.15.3 Function description

1.15.3.1 Analog inputs

The module is equipped with analog inputs with connected 16-bit A/D converters. Each of the inputs can be configured separately for either voltage or current input for the following ranges:

- Permissible voltage: ±10 V
- Permissible current: 0 to 20 mA

Configuration must take place in addition to using suitable terminals.

Information:

The register is described in "Channel configuration" on page 361.

1.15.3.1.1 Scaling

The A/D converter data can optionally be scaled by the user. The following additional registers are available for this:

- Gain = ku
- Offset = du

Scaling calculation:

Scaled value = k * A/C value + d

Gain $k = k_{Calibration} * ku$

Offset $d = d_{Calibration} + du$

The value must be limited since it can exceed the 16-bit constraints. If the application requires a restriction of the range of values, the user can define custom limit values. These are also used for the module's error statistics.

Information:

Within the module, 32-bit numbers are used for the limit values. A limit value violation can therefore also be detected if the permissible range of values of -32768 to 32767 has been defined.

Information:

The registers are described in "User-defined scaling" on page 362.

1.15.3.1.2 Filtering

If filtering has been enabled, the basic data of the A/D converters is filtered per channel. The filter order and respective cutoff frequency of the low-pass filter can be configured for this.

Internal filter orders greater than 1 are implemented as cascaded first-order filters.

Calculating the cutoff frequency of an nth-order filter:

Cutoff frequency = Cutoff frequency$_{n}$ / ((2 ^ (1 / n) - 1) ^ 0.5)

Approximate calculation

yn = a * xn + b * y(n-1)

a = Sampling time$_{Sec}$ / (Sampling time$_{Sec}$ + 1 / (2 Pi * Cutoff frequency$_{Hz}$))

b = 1 - a

Information:

Since low-pass filtering takes place using an approximation procedure with fixed-point arithmetic, there are discrepancies to the effective cutoff frequency that depend on the sampling cycle and filter sequence.

Information:

The registers are described in "Filtering" on page 362.

1.15.3.2 Error monitoring

There are various counter registers in the module that can be used to record the occurrence of certain errors.

The counters in these registers follow the rules of the event error counter, i.e. each occurrence or reset of an error increases the counter value. The last bit of the counter indicates the error state:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

The following errors are monitored:

- **Synchronization error**
  This error shows how often the conversion task was triggered more than 5 µs after the previous X2X cycle.
- **Invalid sampling cycles**
  This error indicates a cycle time violation. The error occurs if the conversion task triggers a sampling task before the last sampling cycle has been completed.
- **Workspace overshoots**
  This indicates errors outside the maximum possible measurement range of the module.
- **Range undershoots**
  This indicates range undershoots below the value set as "Minimum limit value".
- **Range overshoots**
  This indicates range overshoots above the value set as "Maximum limit value".

Overshoots and undershoots

These counters are only operated if the static error counters are enabled in the channel configuration.

Information:

The registers are described in "Error monitoring and counters" on page 364.

1.15.3.3 Analysis functions

In addition to sampling the analog input signal, this module can also be used to perform additional analysis of the values obtained.

1.15.3.3.1 Limit value analysis

Limit value analysis must be enabled for the desired channel. The sampled value of the channel is then compared with the minimum and maximum values stored internally within the module. If a new measurement period is triggered, the values from the last measuring period can be read out from the registers provided for this purpose.

If limit value analysis has been enabled for a channel, the sampled minimum and maximum values are latched within the module. A measurement period can be triggered via the control byte. If the corresponding configured edge is generated by the application, the limit values of the last measurement period are displayed and the internal latch registers are reset.

Information:

The registers are described in "Limit values" on page 368.

1.15.3.3.2 Recording the sampled values

If the recording of sampled values has been enabled for a channel, the sampled values are also recorded in a module-internal FIFO memory. When the configured event occurs, the contents of the FIFO memory are transmitted to the application.

Information:

Recording of sampled values can only be used if the module is operated on an X2X master that is a type SG4 controller.

The analog signal is sampled in 2 steps.

- **Conversion task**

  The A/D converter digitalizes the inputs signals for the enabled inputs once per conversion cycle. Then the results are available internally in the module. To ensure that this process is executed without delays, the corresponding task will be handled with very high priority.

  The timespan needed for conversion results from the set sampling time.
- **Processing task**

  The converted A/D converter values are further processed according to the user settings (filtering, scaling, limit values, error statistics, min/max analysis, hysteresis comparison). The task for this process has low priority. The timespan needed for further processing depends on the configured functions and is the second portion of the sampling time.

Cycle time violation

In normal operation, further processing is triggered after each conversion. The conversion and sampling tasks run synchronous to one another. If the predefined sampling time is not sufficient to convert all enabled channels and complete the configured functions, a cycle time violation occurs.

Information:

The register is described in "Sampling time" on page 361.

1.15.3.3.3 Trace

If the module is operated on a type SG4 controller, the digitized input values can be recorded by the module. Module monitoring must be enabled to use measured value recording.

Recording must be enabled for the desired channel. The enable bits can then control the recording at runtime. The sampled values are recorded in the module's internal FIFO memory.

If the previously defined state occurs on the channel, the contents of the FIFO memory are transmitted to the application. Whether the FIFO memory continued to be filled depends on how recording is configured.

Information:

The trace mechanism cannot be used if the module is operated behind a bus controller, but only when it is directly connected to the controller.

Information:

The registers are described in "Trace" on page 368.

Library "AsIOTrc" is used to read out the trace data.

Register "TraceChannelEnable" on page 368 determines the structure of the trace buffer.

Example of the structure of the trace buffer:

3 channels of the module are used in this example. All 3 channels are sampled per trigger and stored one after the other in the trace buffer.

Channel sequence
1
2
3
1
2
3
:

The length of the trace buffer is determined with registers "TraceTriggerStart" on page 372 and "TraceTriggerStop" on page 372.

Parameter "Number of trace buffers" must be defined in Automation Studio in order to configure the trace function block.

1.15.3.3.3.1 Comparator for trigger conditions

In order to adapt the trace as closely as possible to the requirements of the application, the trace function can also be controlled using the comparator. Threshold values (hysteresis) can be defined within the permitted range of values to do so. 2 status bits are then generated for each enabled channel:

- **InRange bit**
  The InRange status is "1" if the measured value falls within the defined limits.
  The InRange status is "0" if the measured value falls outside the defined limits.
- **Threshold value bit**
  The threshold value bit is "1" if the measured value exceeds the upper threshold value.
  The threshold value bit is "0" if the measured value falls below the lower threshold value.

The InRange and threshold bits of all channels are combined in the least significant byte of register CompState-Collection. In addition, the states of the previous sampling are stored in the high-order byte.

The 4 status messages of each channel can be linked via a link mask using AND or OR operators according to the following logic and used as triggers for recordings.

```
delta = (Current_HysteresisStatus ^ NominalValues)// Difference between current status and preset
cond = delta & Selected_HysteresisStatusBits// Eliminate irrelevant status messages
cond = Selected_HysteresisStatusBits (Current_HysteresisStatus ^ NominalValues)
if((0==(cond & ~LogicalOperators)) &&
(0!=(~cond & LogicalOperators))) {=> Generate trigger event}
```

	Corresponds to register:
Selected_HysteresisStatusBits	cfgComp_EnableMask
Current_HysteresisStatus	CompStateCollection
Nominal values	cfgComp_NominalState
Logical operators	cfgComp_ConditionTypeMask

Information:

The registers are described in "Comparator for trigger conditions" on page 370.

1.15.3.3.3.2 Recording measured values

The module has 16 kB available for the trace. The limitation of the FIFO memory means that a maximum of 8192 analog values can be recorded. The memory is divided evenly between the enabled channels. The actual maximum number of possible recordings therefore depends on the number of channels registered for the trace:

1 channel enabled: Maximum 8192 recordings
2 channels enabled: Maximum 4096 recordings per channel
3 channels enabled: Maximum 2730 recordings per channel
4 channels enabled: Maximum 2048 recordings per channel

Time-shifted recording

If the recording should be defined with a time offset to the trigger, additional conditions can be defined for shifting the start and stop time.

Information:

The registers are described in "Time-offset trace" on page 372.

1.15.4 Commissioning

1.15.4.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

1.15.4.1.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

1.15.5 Register description

1.15.5.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 System user's manual.

1.15.5.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration - Frame size						
-	AsynSize	-				
Configuration						
257 289 321 353	ConfigOutput01 (channel configuration) ConfigOutput06 ConfigOutput11 ConfigOutput16	USINT				•
	Sampling time					
390	ConfigOutput24 (sampling time)	UINT				•
	Filtering					
259 291 323 355	ConfigOutput26 (order for low-pass filter) ConfigOutput28 ConfigOutput30 ConfigOutput32	USINT				•
262 294 326 358	ConfigOutput27 (cutoff frequency of low-pass filter) ConfigOutput29 ConfigOutput31 ConfigOutput33	UINT				•
	Scaling					
276 308 340 372	ConfigOutput04 (user-defined gain) ConfigOutput09 ConfigOutput14 ConfigOutput19	DINT				•
284 316 348 380	ConfigOutput05 (user-defined offset) ConfigOutput10 ConfigOutput15 ConfigOutput20	DINT				•
	User-defined limit values					
266 298 330 362	ConfigOutput02 (minimum limit value) ConfigOutput07 ConfigOutput12 ConfigOutput17	UINT				•
270 302 334 366	ConfigOutput03 (maximum limit value) ConfigOutput08 ConfigOutput13 ConfigOutput18	UINT				•
Communication						
0 + (N-1) * 4	AnalogInput0N (index N = 1 to 4)	INT	•			
650	SampleCycleCounter	UINT		•		
	Error monitoring and counters					
641	Channel status	USINT	•			
	Channel01OK	Bit 0				
	...	...				
	Channel04OK	Bit 3				
	SyncStatus	Bit 6				
	ConvertionCycle	Bit 7				
654	SampleCycleViolationErrorCounter	UINT		•		
658	Counter for synchronization errors	UINT		•		
2097	Range undershoot and overshoot	USINT	•			
	Channel01underflow	Bit 0				
	...					
	Channel04underflow	Bit 3				
	Channel01overflow	Bit 4				
	...	...				
	Channel04overflow	Bit 7				
2099	Workspace overshoot	USINT	•			
	Channel01outofrange	Bit 0				
	...	...				
	Channel04outofrange	Bit 3				
518 + (N-1) * 32	Ch0NOutOfRange (index N = 1 to 4)	UINT		•		
522 + (N-1) * 32	Ch0NUnderflow (index N = 1 to 4)	UINT		•		

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
526 + (N-1) * 32	Ch0NOverflow (index N = 1 to 4)	UINT		•		
Additional analysis functions						
133	ConfigOutput21 (trigger reaction on falling edge)	USINT				•
135	ConfigOutput22 (trigger reaction on rising edge)	USINT				•
129	Analysis control byte	USINT			•	
	TraceTrigger01	Bit 0				
	MinMaxStart01	Bit 4				
	...	...				
	MinMaxStart04	Bit 7				
129	Analysis status byte	USINT	•			
	MinMaxStart01Readback	Bit 4				
	...	...				
	MinMaxStart04Readback	Bit 7				
	Limit values					
530 + (N-1) * 32	MinInput0N (index N = 1 to 4)	INT	•			
534 + (N-1) * 32	MaxInput0N (index N = 1 to 4)	INT	•			
538 + (N-1) * 32	Ch0NMinMaxLatchCounter (index N = 1 to 4)	UINT		•		
	Trace configuration					
1026	TraceChannelEnable	USINT				•
1030	TraceSampleDepth	UINT				•
4157	ConfigOutput25 (trace priority)	USINT				•
1037	Enabling the trace function	USINT			•	
	TraceEnable01	Bit 0				
1089	Trace status	USINT	•			
	TraceEnabled	Bit 0				
	TraceWriteActive	Bit 2				
	TraceReadActive	Bit 3				
	ReadyForTrigger	Bit 4				
	TriggerActive	Bit 5				
	TraceOK	Bit 6				
	TraceError	Bit 7				
1094	FreeBufferSize	UINT	•			
1098	TriggerCount	UINT	•			
1102	TriggerFailCount	UINT	•			
	Comparator					
450 + (N-1) * 8	cfgComp_LowLimitCh0N (index N = 1 to 4)	INT			(•)	•
454 + (N-1) * 8	cfgComp_HighLimitCh0N (index N = 1 to 4)	INT			(•)	•
662	CompStateCollection	UINT	•			
490	cfgComp_NominalState	UINT				•
482	cfgComp_EnableMask	UINT				•
486	cfgComp_ConditionTypeMask	UINT				•
	Time-offset trace					
1042	TraceTriggerStart	INT				•
1046	TraceTriggerStop	UINT				•

1.15.5.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration - Frame size							
-	-	AsynSize	-				
Configuration							
257 289 321 353	-	ConfigOutput01 (channel configuration) ConfigOutput06 ConfigOutput11 ConfigOutput16	USINT				•
	Sampling time						
390	-	ConfigOutput24 (sampling time)	UINT				•
	Filtering						
259 291 323 355	-	ConfigOutput26 (order for low-pass filter) ConfigOutput28 ConfigOutput30 ConfigOutput32	USINT				•
262 294 326 358	-	ConfigOutput27 (cutoff frequency of low-pass filter) ConfigOutput29 ConfigOutput31 ConfigOutput33	UINT				•
	Scaling						
276 308 340 372	-	ConfigOutput04 (user-defined gain) ConfigOutput09 ConfigOutput14 ConfigOutput19	DINT				•
284 316 348 380	-	ConfigOutput05 (user-defined offset) ConfigOutput10 ConfigOutput15 ConfigOutput20	DINT				•
	User-defined limit values						
266 298 330 362	-	ConfigOutput02 (minimum limit value) ConfigOutput07 ConfigOutput12 ConfigOutput17	UINT				•
270 302 334 366	-	ConfigOutput03 (maximum limit value) ConfigOutput08 ConfigOutput13 ConfigOutput18	UINT				•
Communication							
0 + (N-1) * 4	0 + (N-1) * 2	AnalogInput0N (index N = 1 to 4)	INT	•			
650	-	SampleCycleCounter	UINT		•		
	Error monitoring and counters						
641	-	Channel status	USINT		•		
		Channel01OK	Bit 0				
		...	...				
		Channel04OK	Bit 3				
		SyncStatus	Bit 6				
		ConvertionCycle	Bit 7				
654	-	SampleCycleViolationErrorCounter	UINT		•		
658	-	Counter for synchronization errors	UINT		•		
2097	-	Range undershoot and overshoot	USINT		•		
		Channel01underflow	Bit 0				
		...					
		Channel04underflow	Bit 3				
		Channel01overflow	Bit 4				
		...	...				
		Channel04overflow	Bit 7				
2099	-	Workspace overshoot	USINT		•		
		Channel01outofrange	Bit 0				
		...	...				
		Channel04outofrange	Bit 3				
522 + (N-1) * 32	-	Ch0NUnderflow (index N = 1 to 4)	UINT		•		
526 + (N-1) * 32	-	Ch0NOverflow (index N = 1 to 4)	UINT		•		
518 + (N-1) * 32	-	Ch0NOutOfRange (index N = 1 to 4)	UINT		•		
Additional analysis functions							
133	-	Trigger reaction on falling edge	USINT				•
135	-	Trigger reaction on rising edge	USINT				•
129	-	Analysis control byte	USINT				•
		MinMaxStart01	Bit 4				
		...	...				
		MinMaxStart04	Bit 7				

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
129	-	Analysis status byte	USINT		•		
		MinMaxStart01Readback	Bit 4				
		...	...				
		MinMaxStart04Readback	Bit 7				
	Limit values						
530 + (N-1) * 32	-	MinInput0N (index N = 1 to 4)	INT		•		
534 + (N-1) * 32	-	MaxInput0N (index N = 1 to 4)	INT		•		
538 + (N-1) * 32	-	Ch0NMinMaxLatchCounter (index N = 1 to 4)	UINT		•		

1) The offset specifies the position of the register within the CAN object.

1.15.5.4 Configuration

1.15.5.4.1 Channel configuration

Name:
ConfigOutput01 for channel 1
ConfigOutput06 for channel 2
ConfigOutput11 for channel 3
ConfigOutput16 for channel 4

The individual inputs for processing the current or voltage signal are configured in these registers. This configuration must be made in addition to using suitable terminals.

Filtering, analysis and error monitoring (bits 4 to 6) can only be used if the channel is enabled (bit 7 = 0).

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	Terminal selector	0	Voltage terminal for ±10 VDC (bus controller default setting)
		1	Current terminal for 0 to 20 mA
1	Gain selector	0	Voltage ±10 VDC (bus controller default setting)
		1	Current 0 to 20 mA
2 - 3	Reserved	-	
4	Filtering active	0	Inactive (bus controller default setting)
		1	Active
5	Minimum/Maximum analysis active	0	Inactive (bus controller default setting)
		1	Active
6	Error monitoring active	0	Inactive (bus controller default setting)
		1	Active
7	Enables channel	0	Channel enabled (bus controller default setting)
		1	Channel disabled

1.15.5.4.2 Sampling time

Name:
ConfigOutput24

The sampling time is set to µs in this register. This makes it possible to improve the sampling cycle (resolution = 1 µs). The lowest configurable cycle time is 50 µs.

Data type	Value	Information
UINT	50 to 10,000	Bus controller default setting: 100

Information:

Values that are too low for the cycle time will result in cycle time violations.

1.15.5.4.3 Filtering

1.15.5.4.3.1 Filter order

Name:
ConfigOutput26 for channel 1
ConfigOutput28 for channel 2
ConfigOutput30 for channel 3
ConfigOutput32 for channel 4

The filter order is specified in this register. The "Filter cutoff frequency" on page 362 register is used to configure the respective cutoff frequency of the filter.

Data type	Value	Information
USINT	1 to 4	Bus controller default setting: 0

1.15.5.4.3.2 Filter cutoff frequency

Name:
ConfigOutput27 for channel 1
ConfigOutput29 for channel 2
ConfigOutput31 for channel 3
ConfigOutput33 for channel 4

The cutoff frequency of the respective filter is configured in these registers.

Data type	Value	Information
UINT	1 to 65,535	Cutoff frequency in hertz. Bus controller default setting: 0

Information:

The highest cutoff frequency is limited by the Nyquist Shannon sampling theorem (based on the sampling cycle time). The system does not check for violations of this sampling theorem.

1.15.5.4.4 User-defined scaling

1.15.5.4.4.1 User-defined gain

Name:
ConfigOutput04 for channel 1
ConfigOutput09 for channel 2
ConfigOutput14 for channel 3
ConfigOutput19 for channel 4

The user-defined gain for the A/D converter data of the respective physical channel can be specified in these registers.

The value 65536 (0x10000) corresponds to a gain of 1.

Data type	Values	Information
DINT	-2,147,483,648 to 2,147,483,647	Bus controller default setting: 65536

1.15.5.4.4.2 User-defined offset

Name:
ConfigOutput05 for channel 1
ConfigOutput10 for channel 2
ConfigOutput15 for channel 3
ConfigOutput20 for channel 4

The user-defined offset for the A/D converter data of the respective physical channel can be specified in this register.

The value 65536 (0x10000) corresponds to an offset of 1.

Data type	Values	Information
DINT	-2,147,483,648 to 2,147,483,647	Bus controller default setting: 0

1.15.5.4.5 User-defined limit values

1.15.5.4.5.1 Minimum limit value

Name:
ConfigOutput02 for channel 1
ConfigOutput07 for channel 2
ConfigOutput12 for channel 3
ConfigOutput17 for channel 4

The minimum limit value is configured in this register. This limit value is also used for the undershoot error statistics (see register "Ch0xUnderflow" on page 366).

Data type	Values	Information
INT	-32768 to 32767	Bus controller default setting: -32768

1.15.5.4.5.2 Maximum limit value

Name:
ConfigOutput03 for channel 1
ConfigOutput08 for channel 2
ConfigOutput13 for channel 3
ConfigOutput18 for channel 4

The maximum limit value is configured in this register. This limit value is also used for the overflow error statistics (see register "Ch0xOverflow" on page 366).

Data type	Values	Information
INT	-32767 to 32767	Bus controller default setting: 32767

1.15.5.5 Communication - General

The analog inputs of the module convert the current or voltage values with a resolution of 16 bits. The information can be used by the application via the registers described here.

1.15.5.5.1 Analog inputs

Name:
AnalogInput01 to AnalogInput04

The analog input value is mapped in this register depending on the configured operating mode.

Data type	Value	Input signal
INT	-32,768 to 32,767	Voltage signal ±10 VDC
	0 to 32,767	Current signal 0 to 20 mA

1.15.5.5.2 Sampling cycle counter

Name:
SampleCycleCounter

The number of times the input signal has been sampled is provided in this register.

Data type	Values
UINT	0 to 65535

1.15.5.6 Error monitoring and counters

1.15.5.6.1 Channel status

Name:
Channel01OK to Channel04OK
SyncStatus
ConvertionCycle

This register collects error messages synchronously with the network cycle. Temporary error states that were registered in a conversion cycle remain active for at least 2 network cycles. In order to receive detailed error information, the corresponding error counters and X2X network events should also be observed.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01OK	0	OK
		1	Errors • Range overshot • Range undershot • Workspace overshoot
...		...	
3	Channel04OK	0	OK
		1	Errors See description for bit 0.
4 - 5	Reserved	-	
6	SyncStatus[1)]	0	OK
		1	Not synchronized
7	ConvertionCycle[2)]	0	OK
		1	Errors

1) Identical to bit 0 of the registers "SynchronizationViolationErrorCounter" on page 365.
2) Identical to bit 0 of the registers "SampleCycleViolationErrorCounter" on page 365.

1.15.5.6.2 Workspace overshoot

Name:
Channel01outofrange to Channel04outofrange

This register indicates whether the input value overshoots the module's maximum measurement range. The individual bits in this register are identical to the value of the lowest bit of register "Ch0xOutOfRange" on page 365.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01outofrange	0	No error
		1	Working range violation (pos.) of channel 1
...		...	
3	Channel04outofrange	0	No error
		1	Working range violation (pos.) of channel 4
4 - 7	Reserved	-	

1.15.5.6.3 Range undershoot and overshoot

Name:
Channel01underflow to Channel04underflow
Channel01overflow to Channel04overflow

This register indicates whether the limit values defined by registers "Minimum limit value" on page 363 and "Maximum limit value" on page 363 have been overshot or undershot. The individual bits in this register are identical to the value of the lowest bit of registers "Ch0xUnderflow" on page 366 and "Ch0xOverflow" on page 366.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01underflow	0	No error
		1	Range exceeded (.neg) on channel 1
...		...	
3	Channel04underflow	0	No error
		1	Range exceeded (.neg) on channel 4
4	Channel01overflow	0	No error
		1	Range exceeded (.pos) on channel 1
...		...	
7	Channel04overflow	0	No error
		1	Range exceeded (.pos) on channel 4

1.15.5.6.4 Counter for synchronization errors

Name:
SynchronizationViolationErrorCounter

This register counts how often the conversion task was triggered more than 5 µs after the next-coming X2X cycle. In this case, the module is considered being no longer synchronized with X2X Link.

Data type	Value	Information[1)]
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

1) For details, see "Error monitoring" on page 353.

1.15.5.6.5 Counter for faulty sampling cycles

Name:
SampleCycleViolationErrorCounter

This register is used to indicate the number of cycle time violations that have occurred thus far. A cycle time violation occurs if the conversion tasks initiates a sampling task before the last sampling cycle has finished. See "Recording the sampled values" on page 354.

Data type	Value	Information[1)]
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

1) For details, see "Error monitoring" on page 353.

1.15.5.6.6 Counter for workspace overshoots

Name:
Ch01OutOfRange to Ch04OutOfRange

This register indicates errors outside the maximum possible measurement range of the module. These errors result in a final deflection of the A/D converter.

Data type	Value	Information[1)]
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

1) For details, see "Error monitoring" on page 353.

1.15.5.6.7 Counter for range exceeded violations (neg.)

Name:
Ch01Underflow to Ch04Underflow

This register indicates the range undershoots below the value set in register "Minimum limit value" on page 363.

Data type	Value	Information[1)]
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

1) For details, see "Error monitoring" on page 353.

1.15.5.6.8 Counter for range exceeded violations (pos.)

Name:
Ch01Overflow to Ch04Overflow

This register indicates range exceeded violations (pos.) of the value configured in the register "Maximum limit value" on page 363.

Data type	Value	Information[1)]
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

1) For details, see "Error monitoring" on page 353.

1.15.5.7 Analysis functions

In addition to sampling the analog input signal, this module can also be used to perform additional analysis of the values obtained.

1.15.5.7.1 Trigger condition on falling edge

Name:
ConfigOutput21

This register can be used to configure whether the falling edge is used to trigger the trace and determine the input value in register "Analysis control byte" on page 367.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	No trigger (bus controller default setting)
		1	Falling edge active as trigger
1 - 3	Reserved	-	
4	MinMaxStart01	0	No determination (bus controller default setting)
		1	Falling edge determines input value of channel 1
...	...	...	
7	MinMaxStart04	0	No determination (bus controller default setting)
		1	Falling edge determines input value of channel 4

1.15.5.7.2 Trigger condition on rising edge

Name:
ConfigOutput22

This register can be used to configure whether the rising edge is used to trigger the trace and determine the input value in register "Analysis control byte" on page 367.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	Trigger not initiated on positive edge (bus controller default setting)
		1	Rising edge active as trigger
1 - 3	Reserved	-	
4	MinMaxStart01	0	No determination (bus controller default setting)
		1	Rising edge determines input value of channel 1
...	...	...	
7	MinMaxStart04	0	No determination (bus controller default setting)
		1	A positive edge determines the input value of channel 4.

1.15.5.7.3 Analysis control byte

Name:
TraceTrigger01
MinMaxStart01 to MinMaxStart04

The trace function and determination of the minimum/maximum input values can be started in this register. Whether the rising and/or falling edge is used to trigger the functions can be configured using the registers "Trigger condition on falling edge" on page 366 and "Trigger condition on rising edge" on page 367.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	Trigger/Trace not triggered (bus controller default setting)
		1	Initiates trigger/trace
1 - 3	Reserved	-	
4	MinMaxStart01	0	Determination not triggered (bus controller default setting)
		1	Determination of the input value of channel 1 is triggered.
...	...	...	
7	MinMaxStart04	0	Determination not triggered (bus controller default setting)
		1	Determination of the input value of channel 4 is triggered.

Information:

To reduce the cyclic data transfer, this register combines the trace and limit value determination functions.

1.15.5.7.4 Analysis status byte

Name:
MinMaxStart01Readback to MinMaxStart04Readback

The currently requested module-internal analyses can be checked in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Reserved	-	
4	MinMaxStart01Readback	0 or 1	Current state of the trigger bits for determining the limit values on channel 1
...	...	...	
7	MinMaxStart04Readback	0 or 1	Current state of the trigger bits for determining the limit values on channel 4

1.15.5.8 Limit values

1.15.5.8.1 Minimum input values

Name:
MinInput01 to MinInput04

The minimum value of the preceding trigger period is saved in this register based on the filtered, scaled and user-defined limit values. The register value is 0 if the channel is inactive.

Data type	Value
INT	-32,768 to 32,767

1.15.5.8.2 Maximum input values

Name:
MaxInput01 to MaxInput04

The maximum value of the preceding trigger period is saved in this register based on the filtered, scaled and user-defined limit values. The register value is 0 if the channel is inactive.

Data type	Value
INT	-32,768 to 32,767

1.15.5.8.3 Limit value trigger counter

Name:
Ch01MinMaxLatchCounter to Ch04MinMaxLatchCounter

The number of valid events that trigger a new measurement period for the limit value analysis is counted in this register.

Data type	Value
UINT	0 to 65535

1.15.5.9 Trace

1.15.5.9.1 Enabling channels

Name:
TraceChannelEnable

The respective channel is enabled for the trace with this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Channel disabled
		1	Channel enabled
...	...	...	
3	Channel 4	0	Channel disabled
		1	Channel enabled
4 - 7	Reserved	-	

1.15.5.9.2 Trace FIFO configuration

Name:
TraceSampleDepth

The module has 16 kB available for the trace. The limitation of the FIFO memory means that a maximum of 8192 analog values can be recorded. The memory is divided evenly between the enabled channels. The actual maximum number of possible recordings therefore depends on the number of channels registered for the trace.

Data type	Value
UINT	2 to 8192

1.15.5.9.3 Trace priority

Name:
ConfigOutput25

The priority of the trace can be increased with this register.

Data type	Value	Function
USINT	3	Standard
	6	Trace priority higher than X2X Link communication

1.15.5.9.4 Enabling the trace function

Name:

TraceEnable01

This register can be used to enable recording according to the edge control or comparator specifications.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	TraceEnable01	0	Disables the trace function
		1	Enables the trace function
1 - 7	Reserved	-	

1.15.5.9.5 Trace status

Name:
TraceEnabled
TraceWriteActive
TraceReadActive
ReadyForTrigger
TriggerActive
TraceOk
TraceError

The status of the trace is represented in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	TraceEnabled	0	Trace inactive
		1	Trace active
1	Reserved	-	
2	TraceWriteActive	0	Data not recorded
		1	Data recorded
3	TraceReadActive	0	Data not output/read
		1	Data output/read
4	ReadyForTrigger	0	Not ready for triggering
		1	Ready for triggering
5	TriggerActive	0	No trigger active or already executed
		1	Trigger active
6	TraceOk	0	Overflow or inactive
		1	No overflow
7	TraceError	0	No error or inactive
		1	Trace buffer full

1.15.5.9.6 Free trace buffer

Name:
FreeBufferSize

Specifies the free FIFO memory area for the trace in bytes.

Data type	Values
UINT	0 to 65535

1.15.5.9.7 Counter for trigger events

Name:
TriggerCount

This register indicates the number of trigger events that have occurred since the start of the trace.

Data type	Values
UINT	0 to 65535

1.15.5.9.8 Counter for invalid trigger events

Name:
TriggerFailCount

Counts the trigger events for which the trace could not be carried out.

Data type	Values
UINT	0 to 65535

1.15.5.9.9 Comparator for trigger conditions

1.15.5.9.9.1 Lower limit value for hysteresis

Name:
cfgComp_LowLimitCh01 to cfgComp_LowLimitCh04

The lower limit value for hysteresis is configured in this register.

Data type	Values
INT	-32768 to 32767

1.15.5.9.9.2 Upper limit value for hysteresis

Name:
cfgComp_HighLimitCh01 to cfgComp_HighLimitCh04

The upper limit value for hysteresis is configured in this register.

Data type	Values
INT	-32768 to 32767

1.15.5.9.9.3 Hysteresis status of the channels

Name:
CompStateCollection

The hysteresis status of the input channels for the current and last cycle are represented in this register.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
1	Channel01 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
...	...	...	
6	Channel04 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
7	Channel04 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
8	Channel01 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
9	Channel01 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
...	...	...	
14	Channel04 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
15	Channel04 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.

1.15.5.9.9.4 Comparison state of the channels

Name:
cfgComp_NominalState

The desired comparison state for the hysteresis status is indicated in this register.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
1	Channel01 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
...	...	...	
6	Channel04 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
7	Channel04 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
8	Channel01 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
9	Channel01 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
...	...	...	
14	Channel04 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
15	Channel04 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.

Information:

This is a positive list. This means that recording starts as soon as the current status message assumes the state specified here.

Whether one match is sufficient or whether several matches are required depends on the selection of the relevant hysteresis status bits and logical operators.

1.15.5.9.9.5 Selecting the relevant hysteresis status bits

Name:
cfgComp_EnableMask

This register can be used to select which status bits of the hysteresis comparison should be used to generate the trigger.

For information about using this register, see "Comparator for trigger conditions" on page 356.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Do not use
		1	Use for generation
1	Channel01 InRange status in the current cycle	0	Do not use
		1	Use for generation
...	...	...	
6	Channel04 hysteresis status in the current cycle	0	Do not use
		1	Use for generation
7	Channel04 InRange status in the current cycle	0	Do not use
		1	Use for generation
8	Channel01 hysteresis status in the last cycle	0	Do not use
		1	Use for generation
9	Channel01 InRange status in the last cycle	0	Do not use
		1	Use for generation
...	...	...	
14	Channel04 hysteresis status in the last cycle	0	Do not use
		1	Use for generation
15	Channel04 InRange status in the last cycle	0	Do not use
		1	Use for generation

1.15.5.9.9.6 Logical connective operators for hysteresis status bits

Name:
cfgComp_ConditionTypeMask

This register is used to select the desired operators of the states with which the status bits are linked with one another to generate a trigger.

At least one OR operation must be configured, but it does not necessarily have to be located on a channel configured with "1" in the "cfgComp_EnableMask" on page 371 register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Use AND operation
		1	Use OR operation
1	Channel01 InRange status in the current cycle	0	Use AND operation
		1	Use OR operation
...	...	...	
6	Channel04 hysteresis status in the current cycle	0	Use AND operation
		1	Use OR operation
7	Channel04 InRange status in the current cycle	0	Use AND operation
		1	Use OR operation
8	Channel01 hysteresis status in the last cycle	0	Use AND operation
		1	Use OR operation
9	Channel01 InRange status in the last cycle	0	Use AND operation
		1	Use OR operation
...	...	...	
14	Channel04 hysteresis status in the last cycle	0	Use AND operation
		1	Use OR operation
15	Channel04 InRange status in the last cycle	0	Use AND operation
		1	Use OR operation

1.15.5.9.10 Time-offset trace

1.15.5.9.10.1 Starting the trace

Name:
TraceTriggerStart

The relative start position in relation to the configured trigger condition (pos./neg. edge) is defined in this register. Positive values mean that recording begins x samplings after the trigger condition. Negative values mean that the recording starts x samplings before the trigger condition.

With value -32768, recording is started immediately when the trace is enabled.

Data type	Value	Information
INT	-32767 to 32767	
	-32768	Continuous trace without a stopping point

1.15.5.9.10.2 Stopping the trace

Name:
TraceTriggerStop

The relative unsigned stop position in relation to the configured trigger condition is defined in this register.

- When configuring an early recording start, this value refers to the trigger event.
- When configuring a delayed start of recording, the value refers to the start of recording.

Data type	Values
UINT	0 to 65535

1.15.5.10 Acyclic frame size

Name:
AsynSize

When using the stream, the data is exchanged internally between the module and controller. A defined number of acyclic bytes is reserved for this slot for this purpose.
Increasing the acyclic frame size results in increased data throughput on this slot.

Information:

This configuration involves a driver setting that cannot be changed during runtime!

Data type	Values	Information
-	8 to 28	Acyclic frame size in bytes. Default = 24

1.15.5.11 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Standard priority	200 µs
High priority with trace function	300 µs

1.15.5.12 Minimum I/O update time

There is no limitation or dependency on the bus cycle time.

The I/O update time is defined using the "Sampling time" register. The fastest possible sampling time depends on the number of channels to be converted and the configuration.

1.16 X20(c)AI4632-1

1.16.1 General information

1.16.1.1 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, method 4, exposure 21 days

1.16.1.1.1 Starting temperature

The starting temperature describes the minimum permissible ambient temperature in a voltage-free state at the time the coated module is switched on. This is permitted to be as low as -40°C. During operation, the conditions as specified in the technical data continue to apply.

Information:

It is important to absolutely ensure that there is no forced cooling by air currents in the closed control cabinet, e.g. due to the use of a fan or ventilation slots.

1.16.1.2 Other applicable documents

For additional and supplementary information, see the following documents.

Other applicable documents

Document name	Title
MAX20	X20 System user's manual
MAEMV	Installation / EMC guide

1.16.1.3 Order data

Order number	Short description	Figure
	Analog inputs	
X20AI4632-1	X20 analog input module, 4 inputs, ±11 V or 0 to 22 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions	
X20cAI4632-1	X20 analog input module, coated, 4 inputs, ±11 V or 0 to 22 mA, 16-bit converter resolution, configurable input filter, oscilloscope functions	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 59: X20AI4632-1, X20cAI4632-1 - Order data

1.16.1.4 Module description

The module is equipped with 4 inputs with 16-bit digital converter resolution and very fast conversion time. It is possible to select between the current and voltage signal using different terminals.

Functions:

- Scaling
- Filtering
- Error monitoring
- Analysis functions

Scaling

The A/D converter data can optionally be scaled by the user to ensure the greatest possible flexibility.

Input filter

An input filter can be configured for each individual analog input.

Error monitoring

The input signal is monitored for range overshoot, synchronization errors and invalid sampling cycles. User-defined limit values can also be defined.

Analysis functions

In addition to sampling the analog input signal, the values determined can also be analyzed:

- Limit value analysis
- Recording the sampled values
- Trace

1.16.2 Technical description

1.16.2.1 Technical data

Order number	X20AI4632-1	X20cAI4632-1
Short description		
I/O module	4 analog inputs ±11 V or 0 to 22 mA	
General information		
B&R ID code	0xA29D	0xD57A
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using LED status indicator and software	
Inputs	Yes, using LED status indicator and software	
Channel type	Yes, using software	
Power consumption		
Bus	0.01 W	
Internal I/O	1.5 W [1)]	
Additional power dissipation caused by actuators (resistive) [W]	-	
Certifications		
CE	Yes	
UKCA	Yes	
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X	
UL	cULus E115267 Industrial control equipment	
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5	
DNV	Temperature: **B** (0 to 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)	
LR	ENV1	
KR	Yes	
ABS	Yes	
BV	**EC33B** Temperature: 5 - 55°C Vibration: 4 g EMC: Bridge and open deck	
EAC	Yes	
KC	Yes	-
Analog inputs		
Input	±11 V or 0 to 22 mA, via different terminal connections	
Input type	Differential input	
Digital converter resolution		
Voltage	±15-bit	
Current	15-bit	
Conversion time	50 µs for all inputs	
Output format	INT	
Output format		
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0001 = 335.693 µV	
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 671.387 nA	
Input impedance in signal range		
Voltage	20 MΩ	
Current	-	
Load		
Voltage	-	
Current	<400 Ω	
Input protection	Protection against wiring with supply voltage	
Permissible input signal		
Voltage	Max. ±30 V	
Current	Max. ±50 mA	
Output of digital value during overload		
Undershoot		
Voltage	0x8001	
Current	0x0000	
Overshoot		
Voltage	0x7FFF	
Current	0x7FFF	
Conversion procedure	SAR	
Input filter	Hardware - Third-order low-pass filter / cutoff frequency 10 kHz	

Table 60: X20AI4632-1, X20cAI4632-1 - Technical data

Order number	X20AI4632-1	X20cAI4632-1
Max. error		
Voltage		
Gain	0.08% 2)	
Offset	0.01% 3)	
Current		
Gain	0.08% 2)	
Offset	0.02% 4)	
Max. gain drift		
Voltage	0.01%/°C 2)	
Current	0.01%/°C 2)	
Max. offset drift		
Voltage	0.001%/°C 3)	
Current	0.002%/°C 4)	
Common-mode rejection		
DC	70 dB	
50 Hz	70 dB	
Common-mode range	±12 V	
Crosstalk between channels	<-70 dB	
Nonlinearity		
Voltage	<0.01% 3)	
Current	<0.015% 4)	
Insulation voltage between channel and bus	500 V_{eff}	
Electrical properties		
Electrical isolation	Channel isolated from bus Channel not isolated from channel	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation elevation above sea level		
0 to 2000 m	No limitation	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
Degree of protection per EN 60529	IP20	
Ambient conditions		
Temperature		
Operation		
Horizontal mounting orientation	-25 to 60°C	
Vertical mounting orientation	-25 to 50°C	
Derating	See section "Derating".	
Starting temperature	-	Yes, -40°C
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical properties		
Note	Order 1x terminal block X20TB12 separately. Order 1x bus module X20BM11 separately.	Order 1x terminal block X20TB12 separately. Order 1x bus module X20cBM11 separately.
Pitch	$12.5^{+0.2}$ mm	

Table 60: X20AI4632-1, X20cAI4632-1 - Technical data

1) To reduce power dissipation, B&R recommends bridging unused inputs on the terminals or configuring them as current signals.
2) Based on the current measured value.
3) Based on the 22 V measurement range.
4) Based on the 22 mA measurement range.

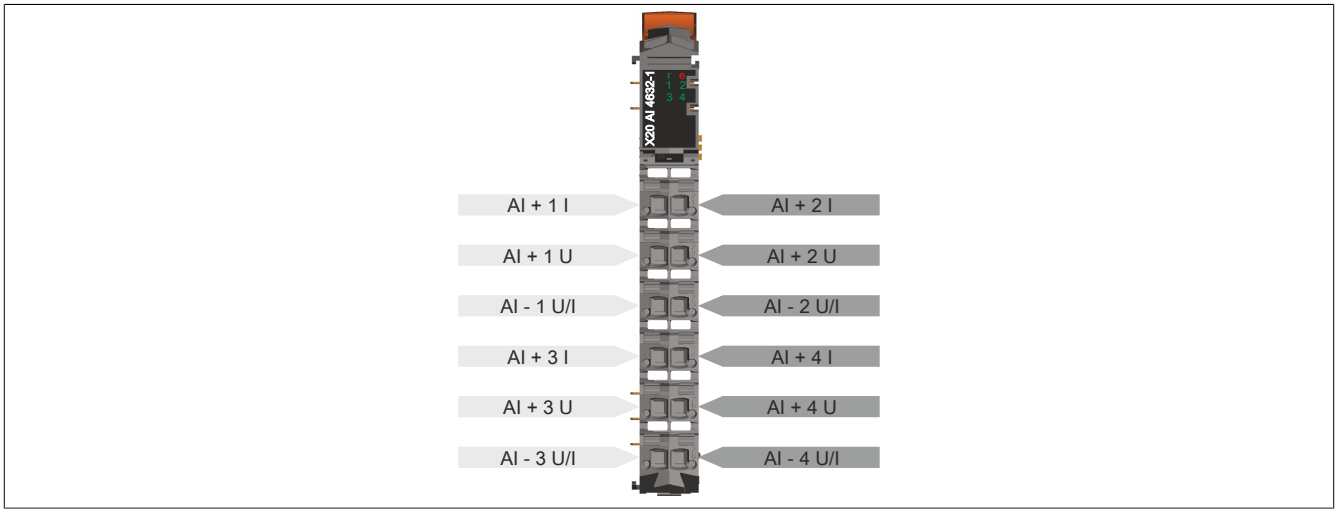
1.16.2.2 LED status indicators

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 System user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Double flash	System error: • Violation of the scan time • Synchronization error
	1 - 4	Green	Off	Open line[2] or sensor is disconnected
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.
2) Open line detection only possible when measuring voltage.

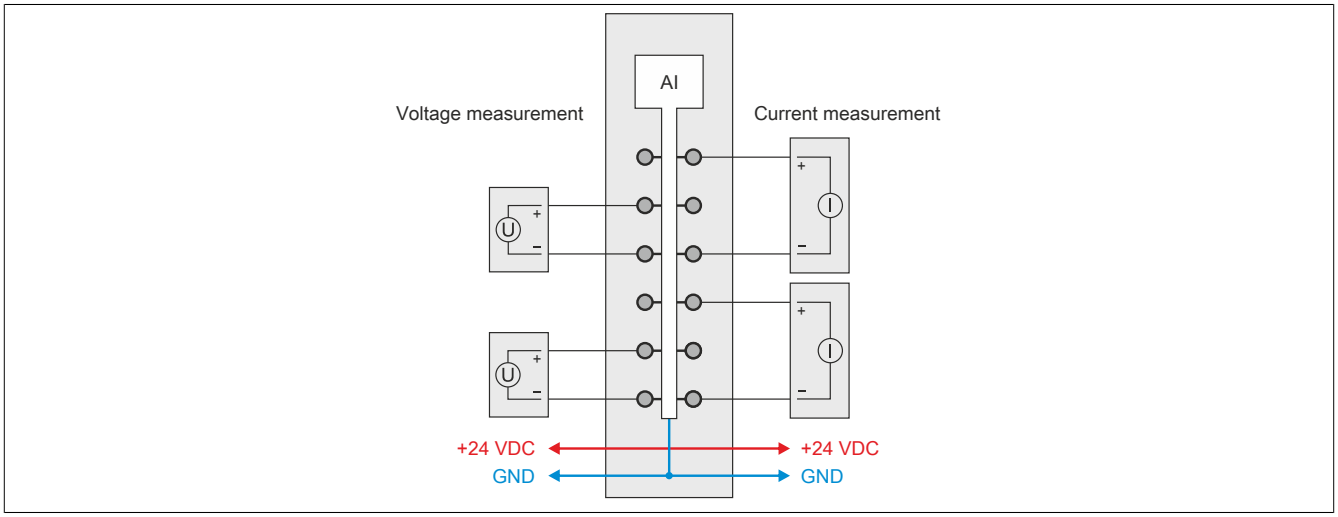
1.16.2.3 Pinout



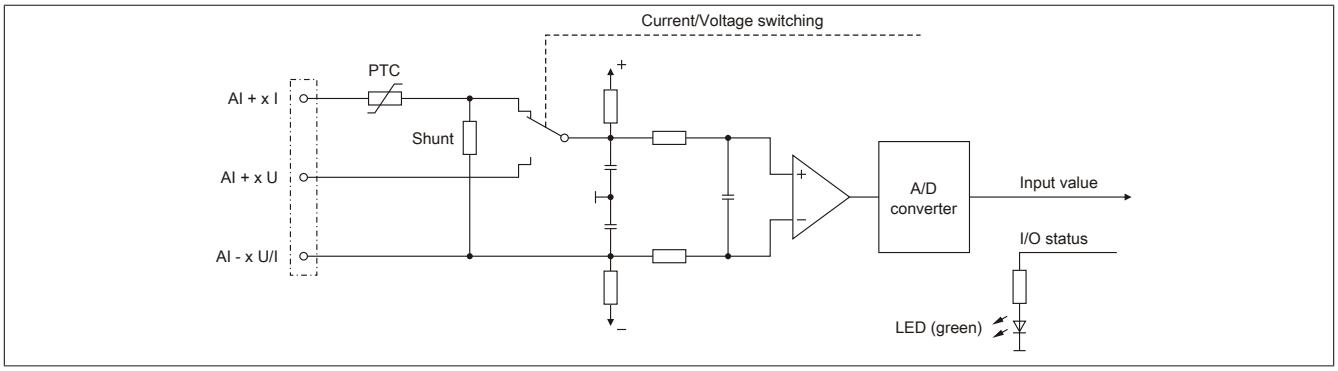
1.16.2.4 Connection example

To prevent disturbances, the following modules must be separated by at least one module:

- Bus receiver X20BR9300
- Supply module X20PS3300/X20PS3310
- Supply module X20PS9400/X20PS9402
- Power supply module X20PS9600/X20PS9602
- Controller



1.16.2.5 Input circuit diagram

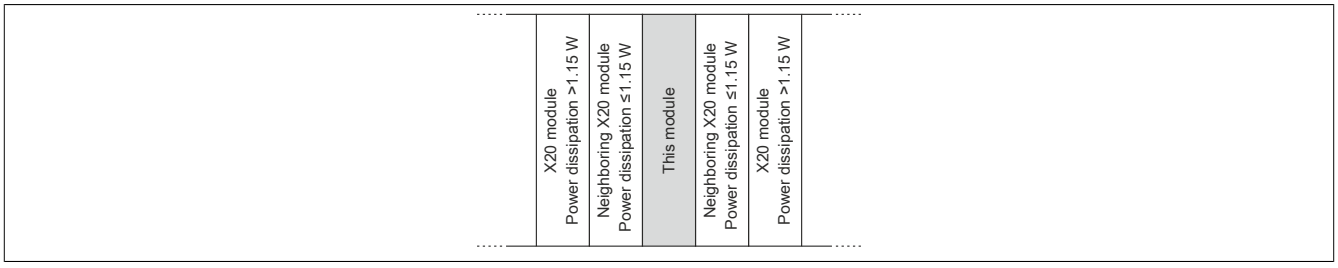


1.16.2.6 Derating

There is no derating when operated below 55°C.

When operated above 55°C, the modules to the left and right of this module are permitted to have a maximum power dissipation of 1.15 W!

For an example of calculating the power dissipation of I/O modules, see section "Mechanical and electrical configuration - Power dissipation of I/O modules" in the X20 user's manual.



1.16.3 Function description

1.16.3.1 Analog inputs

The module is equipped with analog inputs with connected 16-bit A/D converters. Each of the inputs can be configured separately for either voltage or current input for the following ranges:

- Permissible voltage: ±11 V at 20 Ω
- Permissible current: 22 mA (maximum 40 mA) (<400 Ω)

Configuration must take place in addition to using suitable terminals.

Information:

The register is described in "Channel configuration" on page 389.

1.16.3.1.1 Scaling

The A/D converter data can optionally be scaled by the user. The following additional registers are available for this:

- Gain = ku
- Offset = du

Scaling calculation:

Scaled value = k * A/C value + d

Gain k = $k_{Calibration}$ * ku

Offset d = $d_{Calibration}$ + du

The value must be limited since it can exceed the 16-bit constraints. If the application requires a restriction of the range of values, the user can define custom limit values. These are also used for the module's error statistics.

Information:

Within the module, 32-bit numbers are used for the limit values. A limit value violation can therefore also be detected if the permissible range of values of -32768 to 32767 has been defined.

Information:

The registers are described in "User-defined scaling" on page 390.

1.16.3.1.2 Filtering

If filtering has been enabled, the basic data of the A/D converters is filtered per channel. The filter order and respective cutoff frequency of the low-pass filter can be configured for this.

Internal filter orders greater than 1 are implemented as cascaded first-order filters.

Calculating the cutoff frequency of an nth-order filter:

Cutoff frequency = Cutoff frequency$_{n}$ / ((2 ^ (1 / n) - 1) ^ 0.5)

Approximate calculation

yn = a * xn + b * y(n-1)

a = Sampling time$_{Sec}$ / (Sampling time$_{Sec}$ + 1 / (2 Pi * Cutoff frequency$_{Hz}$))

b = 1 - a

Information:

Since low-pass filtering takes place using an approximation procedure with fixed-point arithmetic, there are discrepancies to the effective cutoff frequency that depend on the sampling cycle and filter sequence.

Information:

The registers are described in "Filtering" on page 390.

1.16.3.2 Error monitoring

There are various counter registers in the module that can be used to record the occurrence of certain errors.

The counters in these registers follow the rules of the event error counter, i.e. each occurrence or reset of an error increases the counter value. The last bit of the counter indicates the error state:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

The following errors are monitored:

- **Synchronization error**
  This error shows how often the conversion task was triggered more than 5 µs after the previous X2X cycle.
- **Invalid sampling cycles**
  This error indicates a cycle time violation. The error occurs if the conversion task triggers a sampling task before the last sampling cycle has been completed.
- **Workspace overshoots**
  This indicates errors outside the maximum possible measurement range of the module.
- **Range undershoots**
  This indicates range undershoots below the value set as "Minimum limit value".
- **Range overshoots**
  This indicates range overshoots above the value set as "Maximum limit value".

Overshoots and undershoots

These counters are only operated if the static error counters are enabled in the channel configuration.

Information:

The registers are described in "Error monitoring and counters" on page 392.

1.16.3.3 Analysis functions

In addition to sampling the analog input signal, this module can also be used to perform additional analysis of the values obtained.

1.16.3.3.1 Limit value analysis

Limit value analysis must be enabled for the desired channel. The sampled value of the channel is then compared with the minimum and maximum values stored internally within the module. If a new measurement period is triggered, the values from the last measuring period can be read out from the registers provided for this purpose.

If limit value analysis has been enabled for a channel, the sampled minimum and maximum values are latched within the module. A measurement period can be triggered via the control byte. If the corresponding configured edge is generated by the application, the limit values of the last measurement period are displayed and the internal latch registers are reset.

Information:

The registers are described in "Limit values" on page 395.

1.16.3.3.2 Recording the sampled values

If the recording of sampled values has been enabled for a channel, the sampled values are also recorded in a module-internal FIFO memory. When the configured event occurs, the contents of the FIFO memory are transmitted to the application.

Information:

Recording of sampled values can only be used if the module is operated on an X2X master that is a type SG4 controller.

The analog signal is sampled in 2 steps.

- **Conversion task**

  The A/D converter digitalizes the inputs signals for the enabled inputs once per conversion cycle. Then the results are available internally in the module. To ensure that this process is executed without delays, the corresponding task will be handled with very high priority.

  The timespan needed for conversion results from the set sampling time.
- **Processing task**

  The converted A/D converter values are further processed according to the user settings (filtering, scaling, limit values, error statistics, min/max analysis, hysteresis comparison). The task for this process has low priority. The timespan needed for further processing depends on the configured functions and is the second portion of the sampling time.

Cycle time violation

In normal operation, further processing is triggered after each conversion. The conversion and sampling tasks run synchronous to one another. If the predefined sampling time is not sufficient to convert all enabled channels and complete the configured functions, a cycle time violation occurs.

Information:

The register is described in "Sampling time" on page 389.

1.16.3.3.3 Trace

If the module is operated on a type SG4 controller, the digitized input values can be recorded by the module. Module monitoring must be enabled to use measured value recording.

Recording must be enabled for the desired channel. The enable bits can then control the recording at runtime. The sampled values are recorded in the module's internal FIFO memory.

If the previously defined state occurs on the channel, the contents of the FIFO memory are transmitted to the application. Whether the FIFO memory continued to be filled depends on how recording is configured.

Information:

The trace mechanism cannot be used if the module is operated behind a bus controller, but only when it is directly connected to the controller.

Information:

The registers are described in "Trace" on page 396.

Library "AsIOTrc" is used to read out the trace data.

Register "TraceChannelEnable" on page 396 determines the structure of the trace buffer.

Example of the structure of the trace buffer:

3 channels of the module are used in this example. All 3 channels are sampled per trigger and stored one after the other in the trace buffer.

Channel sequence
1
2
3
1
2
3
:

The length of the trace buffer is determined with registers "TraceTriggerStart" on page 400 and "TraceTriggerStop" on page 400.

Parameter "Number of trace buffers" must be defined in Automation Studio in order to configure the trace function block.

1.16.3.3.3.1 Comparator for trigger conditions

In order to adapt the trace as closely as possible to the requirements of the application, the trace function can also be controlled using the comparator. Threshold values (hysteresis) can be defined within the permitted range of values to do so. 2 status bits are then generated for each enabled channel:

- **InRange bit**
  The InRange status is "1" if the measured value falls within the defined limits.
  The InRange status is "0" if the measured value falls outside the defined limits.
- **Threshold value bit**
  The threshold value bit is "1" if the measured value exceeds the upper threshold value.
  The threshold value bit is "0" if the measured value falls below the lower threshold value.

The InRange and threshold bits of all channels are combined in the least significant byte of register CompState-Collection. In addition, the states of the previous sampling are stored in the high-order byte.

The 4 status messages of each channel can be linked via a link mask using AND or OR operators according to the following logic and used as triggers for recordings.

```
delta = (Current_HysteresisStatus ^ NominalValues)// Difference between current status and preset
cond = delta & Selected_HysteresisStatusBits// Eliminate irrelevant status messages
cond = Selected_HysteresisStatusBits (Current_HysteresisStatus ^ NominalValues)
if((0==(cond & ~LogicalOperators)) &&
(0!=(~cond & LogicalOperators))) {=> Generate trigger event}
```

	Corresponds to register:
Selected_HysteresisStatusBits	cfgComp_EnableMask
Current_HysteresisStatus	CompStateCollection
Nominal values	cfgComp_NominalState
Logical operators	cfgComp_ConditionTypeMask

Information:

The registers are described in "Comparator for trigger conditions" on page 398.

1.16.3.3.3.2 Recording measured values

The module has 16 kB available for the trace. The limitation of the FIFO memory means that a maximum of 8192 analog values can be recorded. The memory is divided evenly between the enabled channels. The actual maximum number of possible recordings therefore depends on the number of channels registered for the trace:

1 channel enabled: Maximum 8192 recordings
2 channels enabled: Maximum 4096 recordings per channel
3 channels enabled: Maximum 2730 recordings per channel
4 channels enabled: Maximum 2048 recordings per channel

Time-shifted recording

If the recording should be defined with a time offset to the trigger, additional conditions can be defined for shifting the start and stop time.

Information:

The registers are described in "Time-offset trace" on page 400.

1.16.4 Commissioning

1.16.4.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

1.16.4.1.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

1.16.5 Register description

1.16.5.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 System user's manual.

1.16.5.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration - Frame size						
-	AsynSize	-				
Configuration						
257 289 321 353	ConfigOutput01 (channel configuration) ConfigOutput06 ConfigOutput11 ConfigOutput16	USINT				•
	Sampling time					
390	ConfigOutput24 (sampling time)	UINT				•
	Filtering					
259 291 323 355	ConfigOutput26 (order for low-pass filter) ConfigOutput28 ConfigOutput30 ConfigOutput32	USINT				•
262 294 326 358	ConfigOutput27 (cutoff frequency of low-pass filter) ConfigOutput29 ConfigOutput31 ConfigOutput33	UINT				•
	Scaling					
276 308 340 372	ConfigOutput04 (user-defined gain) ConfigOutput09 ConfigOutput14 ConfigOutput19	DINT				•
284 316 348 380	ConfigOutput05 (user-defined offset) ConfigOutput10 ConfigOutput15 ConfigOutput20	DINT				•
	User-defined limit values					
266 298 330 362	ConfigOutput02 (minimum limit value) ConfigOutput07 ConfigOutput12 ConfigOutput17	UINT				•
270 302 334 366	ConfigOutput03 (maximum limit value) ConfigOutput08 ConfigOutput13 ConfigOutput18	UINT				•
Communication						
0 + (N-1) * 4	AnalogInput0N (index N = 1 to 4)	INT	•			
650	SampleCycleCounter	UINT		•		
	Error monitoring and counters					
641	Channel status	USINT	•			
	Channel01OK	Bit 0				
	...	...				
	Channel04OK	Bit 3				
	SyncStatus	Bit 6				
	ConvertionCycle	Bit 7				
654	SampleCycleViolationErrorCounter	UINT		•		
658	Counter for synchronization errors	UINT		•		
2097	Range undershoot and overshoot	USINT	•			
	Channel01underflow	Bit 0				
	...					
	Channel04underflow	Bit 3				
	Channel01overflow	Bit 4				
	...	...				
	Channel04overflow	Bit 7				
2099	Workspace overshoot	USINT	•			
	Channel01outofrange	Bit 0				
	...	...				
	Channel04outofrange	Bit 3				
518 + (N-1) * 32	Ch0NOverflow (index N = 1 to 4)	UINT		•		
522 + (N-1) * 32	Ch0NUnderflow (index N = 1 to 4)	UINT		•		

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
526 + (N-1) * 32	Ch0NOutOfRange (index N = 1 to 4)	UINT		•		
Additional analysis functions						
133	ConfigOutput21 (trigger reaction on falling edge)	USINT				•
135	ConfigOutput22 (trigger reaction on rising edge)	USINT				•
129	Analysis control byte	USINT			•	
	TraceTrigger01	Bit 0				
	MinMaxStart01	Bit 4				
	...	...				
	MinMaxStart04	Bit 7				
129	Analysis status byte	USINT	•			
	MinMaxStart01Readback	Bit 4				
	...	...				
	MinMaxStart04Readback	Bit 7				
	Limit values					
530 + (N-1) * 32	MinInput0N (index N = 1 to 4)	INT	•			
534 + (N-1) * 32	MaxInput0N (index N = 1 to 4)	INT	•			
538 + (N-1) * 32	Ch0NMinMaxLatchCounter (index N = 1 to 4)	UINT		•		
	Trace configuration					
1026	TraceChannelEnable	USINT				•
1030	TraceSampleDepth	UINT				•
4157	ConfigOutput25 (trace priority)	USINT				•
1037	Enabling the trace function	USINT			•	
	TraceEnable01	Bit 0				
1089	Trace status	USINT	•			
	TraceEnabled	Bit 0				
	TraceWriteActive	Bit 2				
	TraceReadActive	Bit 3				
	ReadyForTrigger	Bit 4				
	TriggerActive	Bit 5				
	TraceOK	Bit 6				
	TraceError	Bit 7				
1094	FreeBufferSize	UINT	•			
1098	TriggerCount	UINT	•			
1102	TriggerFailCount	UINT	•			
	Comparator					
450 + (N-1) * 8	cfgComp_LowLimitCh0N (index N = 1 to 4)	INT			(•)	•
454 + (N-1) * 8	cfgComp_HighLimitCh0N (index N = 1 to 4)	INT			(•)	•
662	CompStateCollection	UINT	•			
490	cfgComp_NominalState	UINT				•
482	cfgComp_EnableMask	UINT				•
486	cfgComp_ConditionTypeMask	UINT				•
	Time-offset trace					
1042	TraceTriggerStart	INT				•
1046	TraceTriggerStop	UINT				•

1.16.5.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration - Frame size							
-	-	AsynSize	-				
Configuration							
257 289 321 353	-	ConfigOutput01 (channel configuration) ConfigOutput06 ConfigOutput11 ConfigOutput16	USINT				•
	Sampling time						
390	-	ConfigOutput24 (sampling time)	UINT				•
	Filtering						
259 291 323 355	-	ConfigOutput26 (order for low-pass filter) ConfigOutput28 ConfigOutput30 ConfigOutput32	USINT				•
262 294 326 358	-	ConfigOutput27 (cutoff frequency of low-pass filter) ConfigOutput29 ConfigOutput31 ConfigOutput33	UINT				•
	Scaling						
276 308 340 372	-	ConfigOutput04 (user-defined gain) ConfigOutput09 ConfigOutput14 ConfigOutput19	DINT				•
284 316 348 380	-	ConfigOutput05 (user-defined offset) ConfigOutput10 ConfigOutput15 ConfigOutput20	DINT				•
	User-defined limit values						
266 298 330 362	-	ConfigOutput02 (minimum limit value) ConfigOutput07 ConfigOutput12 ConfigOutput17	UINT				•
270 302 334 366	-	ConfigOutput03 (maximum limit value) ConfigOutput08 ConfigOutput13 ConfigOutput18	UINT				•
Communication							
0 + (N-1) * 4	0 + (N-1) * 2	AnalogInput0N (index N = 1 to 4)	INT	•			
650	-	SampleCycleCounter	UINT		•		
	Error monitoring and counters						
641	-	Channel status	USINT		•		
		Channel01OK	Bit 0				
		...	...				
		Channel04OK	Bit 3				
		SyncStatus	Bit 6				
		ConvertionCycle	Bit 7				
654	-	SampleCycleViolationErrorCounter	UINT		•		
658	-	Counter for synchronization errors	UINT		•		
2097	-	Range undershoot and overshoot	USINT		•		
		Channel01underflow	Bit 0				
		...					
		Channel01underflow	Bit 3				
		Channel01overflow	Bit 4				
		...	...				
		Channel04overflow	Bit 7				
2099	-	Workspace overshoot	USINT		•		
		Channel01outofrange	Bit 0				
		...	...				
		Channel04outofrange	Bit 3				
518 + (N-1) * 32	-	Ch0NOverflow (index N = 1 to 4)	UINT		•		
522 + (N-1) * 32	-	Ch0NUnderflow (index N = 1 to 4)	UINT		•		
526 + (N-1) * 32	-	Ch0NOutOfRange (index N = 1 to 4)	UINT		•		
Additional analysis functions							
133	-	ConfigOutput21 (trigger reaction on falling edge)	USINT				•
135	-	ConfigOutput22 (trigger reaction on rising edge)	USINT				•
129	-	Analysis control byte	USINT				•
		MinMaxStart01	Bit 4				
		...	...				
		MinMaxStart04	Bit 7				

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
129	-	Analysis status byte	USINT		•		
		MinMaxStart01Readback	Bit 4				
		...	...				
		MinMaxStart04Readback	Bit 7				
	Limit values						
530 + (N-1) * 32	-	MinInput0N (index N = 1 to 4)	INT		•		
534 + (N-1) * 32	-	MaxInput0N (index N = 1 to 4)	INT		•		
538 + (N-1) * 32	-	Ch0NMinMaxLatchCounter (index N = 1 to 4)	UINT		•		

1) The offset specifies the position of the register within the CAN object.

1.16.5.4 Configuration

- Permitted voltage: ±11 V at 20 Ω
- Permitted current: 22 mA (maximum 40 mA) (<400 Ω)

1.16.5.4.1 Channel configuration

Name:
ConfigOutput01 for channel 1
ConfigOutput06 for channel 2
ConfigOutput11 for channel 3
ConfigOutput16 for channel 4

The individual inputs for processing the current or voltage signal are configured in these registers. This configuration must be made in addition to using suitable terminals.

Filtering, analysis and error monitoring (bits 4 to 6) can only be used if the channel is enabled (bit 7 = 0).

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	Terminal selector	0	Voltage terminal for ±11 VDC (bus controller default setting)
		1	Current terminal for 0 to 22 mA
1	Gain selector	0	Voltage ±11 VDC (bus controller default setting)
		1	Current 0 to 22 mA
2 - 3	Reserved	-	
4	Filtering active (only if bit 7 = 0)	0	Inactive (bus controller default setting)
		1	Active
5	Minimum/Maximum analysis active (only if bit 7 = 0)	0	Inactive (bus controller default setting)
		1	Active
6	Error monitoring active (only if bit 7 = 0)	0	Inactive (bus controller default setting)
		1	Active
7	Enables channel	0	Channel enabled (bus controller default setting)
		1	Channel disabled

1.16.5.4.2 Sampling time

Name:
ConfigOutput24

The sampling time is set to µs in this register. This makes it possible to improve the sampling cycle (resolution = 1 µs). The lowest configurable cycle time is 50 µs.

Data type	Value	Information
UINT	50 to 10,000	Bus controller default setting: 100

Information:

Values that are too low for the cycle time will result in cycle time violations.

1.16.5.4.3 Filtering

1.16.5.4.3.1 Filter order

Name:
ConfigOutput26 for channel 1
ConfigOutput28 for channel 2
ConfigOutput30 for channel 3
ConfigOutput32 for channel 4

The filter order is specified in this register. The "Filter cutoff frequency" on page 390 register is used to configure the respective cutoff frequency of the filter.

Data type	Value	Information
USINT	1 to 4	Bus controller default setting: 0

1.16.5.4.3.2 Filter cutoff frequency

Name:
ConfigOutput27 for channel 1
ConfigOutput29 for channel 2
ConfigOutput31 for channel 3
ConfigOutput33 for channel 4

The cutoff frequency of the respective filter is configured in these registers.

Data type	Value	Information
UINT	1 to 65,535	Cutoff frequency in hertz. Bus controller default setting: 0

Information:

The highest cutoff frequency is limited by the Nyquist Shannon sampling theorem (based on the sampling cycle time). The system does not check for violations of this sampling theorem.

1.16.5.4.4 User-defined scaling

1.16.5.4.4.1 User-defined gain

Name:
ConfigOutput04 for channel 1
ConfigOutput09 for channel 2
ConfigOutput14 for channel 3
ConfigOutput19 for channel 4

The user-defined gain for the A/D converter data of the respective physical channel can be specified in these registers.

The value 65536 (0x10000) corresponds to a gain of 1.

Data type	Values	Information
DINT	-2,147,483,648 to 2,147,483,647	Bus controller default setting: 65536

1.16.5.4.4.2 User-defined offset

Name:
ConfigOutput05 for channel 1
ConfigOutput10 for channel 2
ConfigOutput15 for channel 3
ConfigOutput20 for channel 4

The user-defined offset for the A/D converter data of the respective physical channel can be specified in this register.

The value 65536 (0x10000) corresponds to an offset of 1.

Data type	Values	Information
DINT	-2,147,483,648 to 2,147,483,647	Bus controller default setting: 0

1.16.5.4.5 User-defined limit values

1.16.5.4.5.1 Minimum limit value

Name:
ConfigOutput02 for channel 1
ConfigOutput07 for channel 2
ConfigOutput12 for channel 3
ConfigOutput17 for channel 4

The minimum limit value is configured in this register. This limit value is also used for the underflow error statistics (see register "Ch0xUnderflow" on page 394).

Data type	Values	Information
INT	-32768 to 32767	Bus controller default setting: -32768

1.16.5.4.5.2 Maximum limit value

Name:
ConfigOutput03 for channel 1
ConfigOutput08 for channel 2
ConfigOutput13 for channel 3
ConfigOutput18 for channel 4

The maximum limit value is configured in this register. This limit value is also used for the overflow error statistics (see register "Ch0xOverflow" on page 394).

Data type	Values	Information
INT	-32767 to 32767	Bus controller default setting: 32767

1.16.5.5 Communication - General

The analog inputs of the module convert the current or voltage values with a resolution of 16 bits. The information can be used by the application via the registers described here.

1.16.5.5.1 Analog inputs

Name:
AnalogInput01 to AnalogInput04

The analog input value is mapped in this register depending on the configured operating mode.

Data type	Value	Input signal
INT	-32,768 to 32,767	Voltage signal ±11 VDC
	0 to 32,767	Current signal 0 to 22 mA

1.16.5.5.2 Sampling cycle counter

Name:
SampleCycleCounter

The number of times the input signal has been sampled is provided in this register.

Data type	Values
UINT	0 to 65535

1.16.5.6 Error monitoring and counters

1.16.5.6.1 Channel status

Name:
Channel01OK to Channel04OK
SyncStatus
ConvertionCycle

This register collects error messages synchronously with the network cycle. Temporary error states that were registered in a conversion cycle remain active for at least 2 network cycles. In order to receive detailed error information, the corresponding error counters and X2X network events should also be observed.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01OK	0	OK
		1	Errors • Range overshot • Range undershot • Workspace overshoot
...		...	
3	Channel04OK	0	OK
		1	Errors See description for bit 0.
4 - 5	Reserved	-	
6	SyncStatus[1)]	0	OK
		1	Not synchronized
7	ConvertionCycle[2)]	0	OK
		1	Errors

1) Identical to bit 0 of the registers "SynchronizationViolationErrorCounter" on page 393.
2) Identical to bit 0 of the registers "SampleCycleViolationErrorCounter" on page 393.

1.16.5.6.2 Workspace overshoot

Name:
Channel01outofrange to Channel04outofrange

This register indicates whether the input value overshoots the module's maximum measurement range. The individual bits in this register are identical to the value of the lowest bit of register "Ch0xOutOfRange" on page 393.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01outofrange	0	No error
		1	Working range violation (pos.) of channel 1
...		...	
3	Channel04outofrange	0	No error
		1	Working range violation (pos.) of channel 4
4 - 7	Reserved	-	

1.16.5.6.3 Range undershoot and overshoot

Name:
Channel01underflow to Channel04underflow
Channel01overflow to Channel04overflow

This register indicates whether the limit values defined by registers "Minimum limit value" on page 391 and "Maximum limit value" on page 391 have been overshot or undershot. The individual bits in this register are identical to the value of the lowest bit of registers "Ch0xUnderflow" on page 394 and "Ch0xOverflow" on page 394.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01underflow	0	No error
		1	Range exceeded (.neg) on channel 1
...		...	
3	Channel04underflow	0	No error
		1	Range exceeded (.neg) on channel 4
4	Channel01overflow	0	No error
		1	Range exceeded (.pos) on channel 1
...		...	
7	Channel04overflow	0	No error
		1	Range exceeded (.pos) on channel 4

1.16.5.6.4 Counter for synchronization errors

Name:
SynchronizationViolationErrorCounter

This register counts how often the conversion task was triggered more than 5 µs after the next-coming X2X cycle. In this case, the module is considered being no longer synchronized with X2X Link.

Data type	Value	Information[1)]
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

1) For details, see "Error monitoring" on page 381.

1.16.5.6.5 Counter for faulty sampling cycles

Name:
SampleCycleViolationErrorCounter

This register is used to indicate the number of cycle time violations that have occurred thus far. A cycle time violation occurs if the conversion tasks initiates a sampling task before the last sampling cycle has finished. See "Recording the sampled values" on page 382.

Data type	Value	Information[1)]
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

1) For details, see "Error monitoring" on page 381.

1.16.5.6.6 Counter for workspace overshoots

Name:
Ch01OutOfRange to Ch04OutOfRange

This register indicates errors outside the maximum possible measurement range of the module. These errors result in a final deflection of the A/D converter.

Data type	Value	Information[1)]
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

1) For details, see "Error monitoring" on page 381.

1.16.5.6.7 Counter for range exceeded violations (neg.)

Name:
Ch01Underflow to Ch04Underflow

This register indicates the range undershoots below the value set in register "Minimum limit value" on page 391.

Data type	Value	Information[1)]
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

1) For details, see "Error monitoring" on page 381.

1.16.5.6.8 Counter for range exceeded violations (pos.)

Name:
Ch01Overflow to Ch04Overflow

This register indicates the range overshoots above the value set in register "Maximum limit value" on page 391.

Data type	Value	Information[1)]
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

1) For details, see "Error monitoring" on page 381.

1.16.5.7 Analysis functions

In addition to sampling the analog input signal, this module can also be used to perform additional analysis of the values obtained.

1.16.5.7.1 Trigger condition on falling edge

Name:
ConfigOutput21

This register can be used to configure whether the falling edge is used to trigger the trace and determine the input value in register "Analysis control byte" on page 395.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	No trigger (bus controller default setting)
		1	Falling edge active as trigger
1 - 3	Reserved	-	
4	MinMaxStart01	0	No determination (bus controller default setting)
		1	Falling edge determines input value of channel 1
...	...	...	
7	MinMaxStart04	0	No determination (bus controller default setting)
		1	Falling edge determines input value of channel 4

1.16.5.7.2 Trigger condition on rising edge

Name:
ConfigOutput22

This register can be used to configure whether the rising edge is used to trigger the trace and determine the input value in register "Analysis control byte" on page 395.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	Trigger not initiated on positive edge (bus controller default setting)
		1	Rising edge active as trigger
1 - 3	Reserved	-	
4	MinMaxStart01	0	No determination (bus controller default setting)
		1	Rising edge determines input value of channel 1
...	...	...	
7	MinMaxStart04	0	No determination (bus controller default setting)
		1	A positive edge determines the input value of channel 4.

1.16.5.7.3 Analysis control byte

Name:
TraceTrigger01
MinMaxStart01 to MinMaxStart04

The trace function and determination of the minimum/maximum input values can be started in this register. Whether the rising and/or falling edge is used to trigger the functions can be configured using the registers "Trigger condition on falling edge" on page 394 and "Trigger condition on rising edge" on page 394.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	Trigger/Trace not triggered (bus controller default setting)
		1	Initiates trigger/trace
1 - 3	Reserved	-	
4	MinMaxStart01	0	Determination not triggered (bus controller default setting)
		1	Determination of the input value of channel 1 is triggered.
...	...	...	
7	MinMaxStart04	0	Determination not triggered (bus controller default setting)
		1	Determination of the input value of channel 4 is triggered.

Information:

To reduce the cyclic data transfer, this register combines the trace and limit value determination functions.

1.16.5.7.4 Analysis status byte

Name:
MinMaxStart01Readback to MinMaxStart04Readback

The currently requested module-internal analyses can be checked in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Reserved	-	
4	MinMaxStart01Readback	0 or 1	Current state of the trigger bits for determining the limit values on channel 1
...	...	...	
7	MinMaxStart04Readback	0 or 1	Current state of the trigger bits for determining the limit values on channel 4

1.16.5.8 Limit values

1.16.5.8.1 Minimum input values

Name:
MinInput01 to MinInput04

The minimum value of the preceding trigger period is saved in this register based on the filtered, scaled and user-defined limit values. The register value is 0 if the channel is inactive.

Data type	Value
INT	-32,768 to 32,767

1.16.5.8.2 Maximum input values

Name:
MaxInput01 to MaxInput04

The maximum value of the preceding trigger period is saved in this register based on the filtered, scaled and user-defined limit values. The register value is 0 if the channel is inactive.

Data type	Value
INT	-32,768 to 32,767

1.16.5.8.3 Limit value trigger counter

Name:
Ch01MinMaxLatchCounter to Ch04MinMaxLatchCounter

The number of valid events that trigger a new measurement period for the limit value analysis is counted in this register.

Data type	Value
UINT	0 to 65535

1.16.5.9 Trace

1.16.5.9.1 Enabling channels

Name:
TraceChannelEnable

The respective channel is enabled for the trace with this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Channel disabled
		1	Channel enabled
...	...	...	
3	Channel 4	0	Channel disabled
		1	Channel enabled
4 - 7	Reserved	-	

1.16.5.9.2 Trace FIFO configuration

Name:
TraceSampleDepth

The module has 16 kB available for the trace. The limitation of the FIFO memory means that a maximum of 8192 analog values can be recorded. The memory is divided evenly between the enabled channels. The actual maximum number of possible recordings therefore depends on the number of channels registered for the trace.

Data type	Value
UINT	2 to 8192

1.16.5.9.3 Trace priority

Name:
ConfigOutput25

The priority of the trace can be increased with this register.

Data type	Value	Function
USINT	3	Standard
	6	Trace priority higher than X2X Link communication

1.16.5.9.4 Enabling the trace function

Name:

TraceEnable01

This register can be used to enable recording according to the edge control or comparator specifications.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	TraceEnable01	0	Disables the trace function
		1	Enables the trace function
1 - 7	Reserved	-	

1.16.5.9.5 Trace status

Name:
TraceEnabled
TraceWriteActive
TraceReadActive
ReadyForTrigger
TriggerActive
TraceOk
TraceError

The status of the trace is represented in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	TraceEnabled	0	Trace inactive
		1	Trace active
1	Reserved	-	
2	TraceWriteActive	0	Data not recorded
		1	Data recorded
3	TraceReadActive	0	Data not output/read
		1	Data output/read
4	ReadyForTrigger	0	Not ready for triggering
		1	Ready for triggering
5	TriggerActive	0	No trigger active or already executed
		1	Trigger active
6	TraceOk	0	Overflow or inactive
		1	No overflow
7	TraceError	0	No error or inactive
		1	Trace buffer full

1.16.5.9.6 Free trace buffer

Name:
FreeBufferSize

Specifies the free FIFO memory area for the trace in bytes.

Data type	Values
UINT	0 to 65535

1.16.5.9.7 Counter for trigger events

Name:
TriggerCount

This register indicates the number of trigger events that have occurred since the start of the trace.

Data type	Values
UINT	0 to 65535

1.16.5.9.8 Counter for invalid trigger events

Name:
TriggerFailCount

Counts the trigger events for which the trace could not be carried out.

Data type	Values
UINT	0 to 65535

1.16.5.9.9 Comparator for trigger conditions

1.16.5.9.9.1 Lower limit value for hysteresis

Name:
cfgComp_LowLimitCh01 to cfgComp_LowLimitCh04

The lower limit value for hysteresis is configured in this register.

Data type	Values
INT	-32768 to 32767

1.16.5.9.9.2 Upper limit value for hysteresis

Name:
cfgComp_HighLimitCh01 to cfgComp_HighLimitCh04

The upper limit value for hysteresis is configured in this register.

Data type	Values
INT	-32768 to 32767

1.16.5.9.9.3 Hysteresis status of the channels

Name:
CompStateCollection

The hysteresis status of the input channels for the current and last cycle are represented in this register.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
1	Channel01 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
...	...	...	
6	Channel04 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
7	Channel04 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
8	Channel01 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
9	Channel01 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
...	...	...	
14	Channel04 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
15	Channel04 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.

1.16.5.9.9.4 Comparison state of the channels

Name:
cfgComp_NominalState

The desired comparison state for the hysteresis status is indicated in this register.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
1	Channel01 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
...	...	...	
6	Channel04 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
7	Channel04 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
8	Channel01 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
9	Channel01 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.
...	...	...	
14	Channel04 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
15	Channel04 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value is between the lower and upper limit value.

Information:

This is a positive list. This means that recording starts as soon as the current status message assumes the state specified here.

Whether one match is sufficient or whether several matches are required depends on the selection of the relevant hysteresis status bits and logical operators.

1.16.5.9.9.5 Selecting the relevant hysteresis status bits

Name:
cfgComp_EnableMask

This register can be used to select which status bits of the hysteresis comparison should be used to generate the trigger.

For information about using this register, see "Comparator for trigger conditions" on page 384.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Do not use
		1	Use for generation
1	Channel01 InRange status in the current cycle	0	Do not use
		1	Use for generation
...	...	...	
6	Channel04 hysteresis status in the current cycle	0	Do not use
		1	Use for generation
7	Channel04 InRange status in the current cycle	0	Do not use
		1	Use for generation
8	Channel01 hysteresis status in the last cycle	0	Do not use
		1	Use for generation
9	Channel01 InRange status in the last cycle	0	Do not use
		1	Use for generation
...	...	...	
14	Channel04 hysteresis status in the last cycle	0	Do not use
		1	Use for generation
15	Channel04 InRange status in the last cycle	0	Do not use
		1	Use for generation

1.16.5.9.9.6 Logical connective operators for hysteresis status bits

Name:
cfgComp_ConditionTypeMask

This register is used to select the desired operators of the states with which the status bits are linked with one another to generate a trigger.

At least one OR operation must be configured, but it does not necessarily have to be located on a channel configured with "1" in the "cfgComp_EnableMask" on page 399 register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Use AND operation
		1	Use OR operation
1	Channel01 InRange status in the current cycle	0	Use AND operation
		1	Use OR operation
...	...	...	
6	Channel04 hysteresis status in the current cycle	0	Use AND operation
		1	Use OR operation
7	Channel04 InRange status in the current cycle	0	Use AND operation
		1	Use OR operation
8	Channel01 hysteresis status in the last cycle	0	Use AND operation
		1	Use OR operation
9	Channel01 InRange status in the last cycle	0	Use AND operation
		1	Use OR operation
...	...	...	
14	Channel04 hysteresis status in the last cycle	0	Use AND operation
		1	Use OR operation
15	Channel04 InRange status in the last cycle	0	Use AND operation
		1	Use OR operation

1.16.5.9.10 Time-offset trace

1.16.5.9.10.1 Starting the trace

Name:
TraceTriggerStart

The relative start position in relation to the configured trigger condition (pos./neg. edge) is defined in this register. Positive values mean that recording begins x samplings after the trigger condition. Negative values mean that the recording starts x samplings before the trigger condition.

With value -32768, recording is started immediately when the trace is enabled.

Data type	Value	Information
INT	-32767 to 32767	
	-32768	Continuous trace without a stopping point

1.16.5.9.10.2 Stopping the trace

Name:
TraceTriggerStop

The relative unsigned stop position in relation to the configured trigger condition is defined in this register.

- When configuring an early recording start, this value refers to the trigger event.
- When configuring a delayed start of recording, the value refers to the start of recording.

Data type	Values
UINT	0 to 65535

1.16.5.10 Acyclic frame size

Name:
AsynSize

When using the stream, the data is exchanged internally between the module and controller. A defined number of acyclic bytes is reserved for this slot for this purpose.
Increasing the acyclic frame size results in increased data throughput on this slot.

Information:

This configuration involves a driver setting that cannot be changed during runtime!

Data type	Values	Information
-	8 to 28	Acyclic frame size in bytes. Default = 24

1.16.5.11 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Standard priority	200 µs
High priority with trace function	300 µs

1.16.5.12 Minimum I/O update time

There is no limitation or dependency on the bus cycle time.

The I/O update time is defined using the "Sampling time" register. The fastest possible sampling time depends on the number of channels to be converted and the configuration.

1.17 X20AI4636

1.17.1 General information

1.17.1.1 Other applicable documents

For additional and supplementary information, see the following documents.

Other applicable documents

Document name	Title
MAX20	X20 System user's manual
MAEMV	Installation / EMC guide

1.17.1.2 Order data

Order number	Short description	Figure
	Analog inputs	
X20AI4636	X20 analog input module, 4 inputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, configurable input filter, oversampling functions	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 61: X20AI4636 - Order data

1.17.1.3 Module description

The module is equipped with 4 inputs with 16-bit digital converter resolution. It is possible to select between the current and voltage signal using different terminals. With the oversampling function, up to 16 analog values per channel can be recorded.

Functions:

- Physical values
- Logical values
- Oversampling
- Monitoring the inputs

Physical values

The conversion results of the analog inputs are scaled and filtered before being transferred to the higher-level system.

Logical values

The physical values can be further processed using mathematical functions and comparators. Another logical channel can also be used as a starting point for further processing for a logical function.

Oversampling

The input values of the enabled channels are stored in the module in a configurable interval independently of the X2X cycle. The memory depth is 16 analog values per physical and logical channel.

Monitoring the input signal

The input signal of the analog inputs is monitored for out-of-range, for upper and lower limit values and for filter errors.

1.17.2 Technical description

1.17.2.1 Technical data

Order number	X20AI4636
Short description	
I/O module	4 analog inputs ±10 V or 0 to 20 mA
General information	
B&R ID code	0xB3A8
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using LED status indicator and software
Inputs	Yes, using LED status indicator and software
Channel type	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	1.5 W [1)]
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
UKCA	Yes
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
DNV	Temperature: **B** (0 to 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
LR	ENV1
KR	Yes
ABS	Yes
BV	**EC33B** Temperature: 5 - 55°C Vibration: 4 g EMC: Bridge and open deck
EAC	Yes
KC	Yes
Analog inputs	
Input	±10 V or 0 to 20 mA, via different terminal connections
Input type	Differential input
Digital converter resolution	
Voltage	±15-bit
Current	15-bit
Conversion time	40 µs for all inputs
Output format	INT
Output format	
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0001 = 305.176 µV
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 610.352 nA
Input impedance in signal range	
Voltage	20 MΩ
Current	-
Load	
Voltage	-
Current	<400 Ω
Input protection	Protection against wiring with supply voltage
Permissible input signal	
Voltage	Max. ±30 V
Current	Max. ±50 mA
Output of digital value during overload	
Undershoot	
Voltage	0x8001
Current	0x0000
Overshoot	
Voltage	0x7FFF
Current	0x7FFF
Conversion procedure	SAR
Input filter	Hardware - Third-order low-pass filter / cutoff frequency 10 kHz

Table 62: X20AI4636 - Technical data

Order number	X20AI4636
Max. error	
Voltage	
Gain	0.08% 2)
Offset	0.01% 3)
Current	
Gain	0.08% 2)
Offset	0.02% 4)
Max. gain drift	
Voltage	0.01%/°C 2)
Current	0.01%/°C 2)
Max. offset drift	
Voltage	0.001%/°C 3)
Current	0.002%/°C 4)
Common-mode rejection	
DC	70 dB
50 Hz	70 dB
Common-mode range	±12 V
Crosstalk between channels	<-70 dB
Nonlinearity	
Voltage	<0.01% 3)
Current	<0.015% 4)
Insulation voltage between channel and bus	500 V_{eff}
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	See section "Derating".
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x terminal block X20TB12 separately. Order 1x bus module X20BM11 separately.
Pitch	$12.5^{+0.2}$ mm

Table 62: X20AI4636 - Technical data

1) To reduce power dissipation, B&R recommends bridging unused inputs on the terminal.
2) Based on the current measured value.
3) Based on the 20 V measurement range.
4) Based on the 20 mA measurement range.

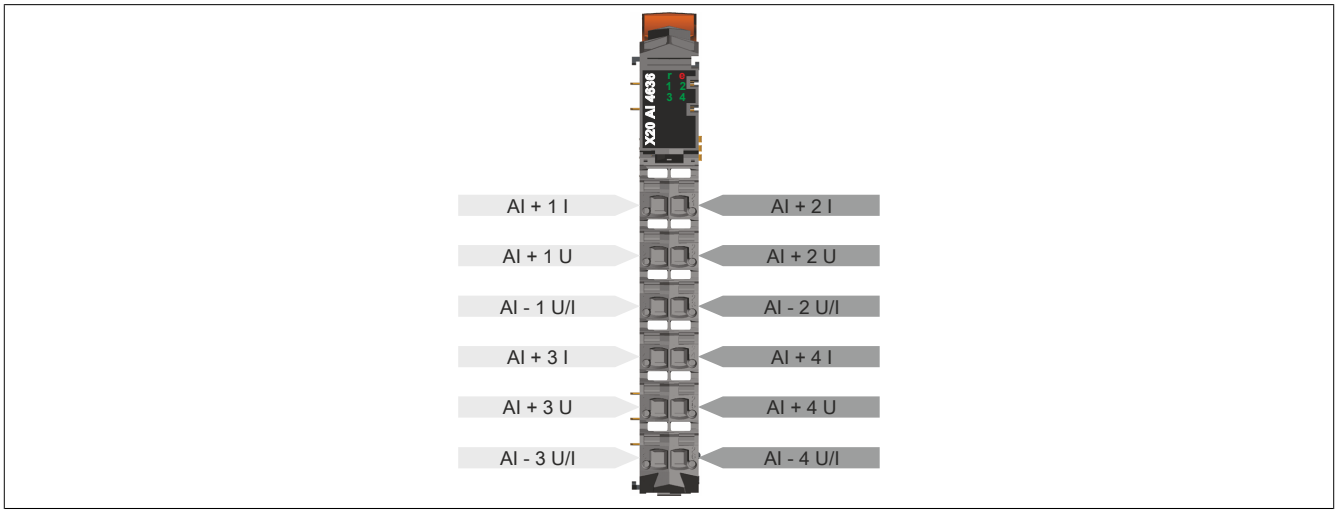
1.17.2.2 Status LEDs

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 System user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Double flash	System error: • Violation of the sampling cycle time • Synchronization error
		Green	Off	Open line[2] or sensor is disconnected
			Blinking	Channel error: Underflow, overflow or broken connection
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.
2) Open line detection only possible when measuring voltage.

1.17.2.3 Pinout

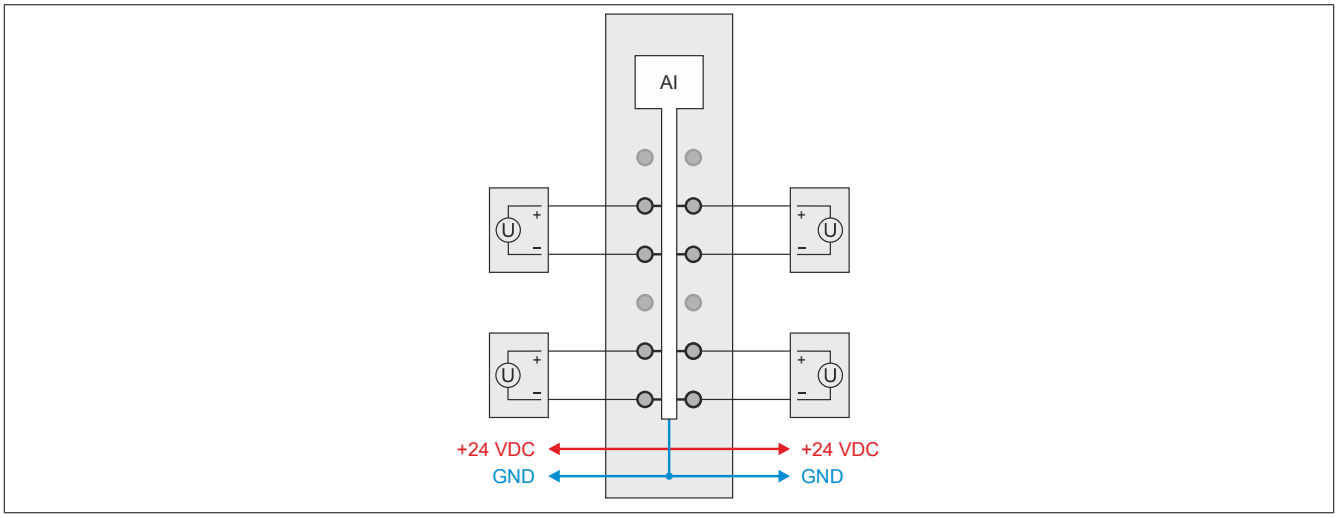


1.17.2.4 Connection example

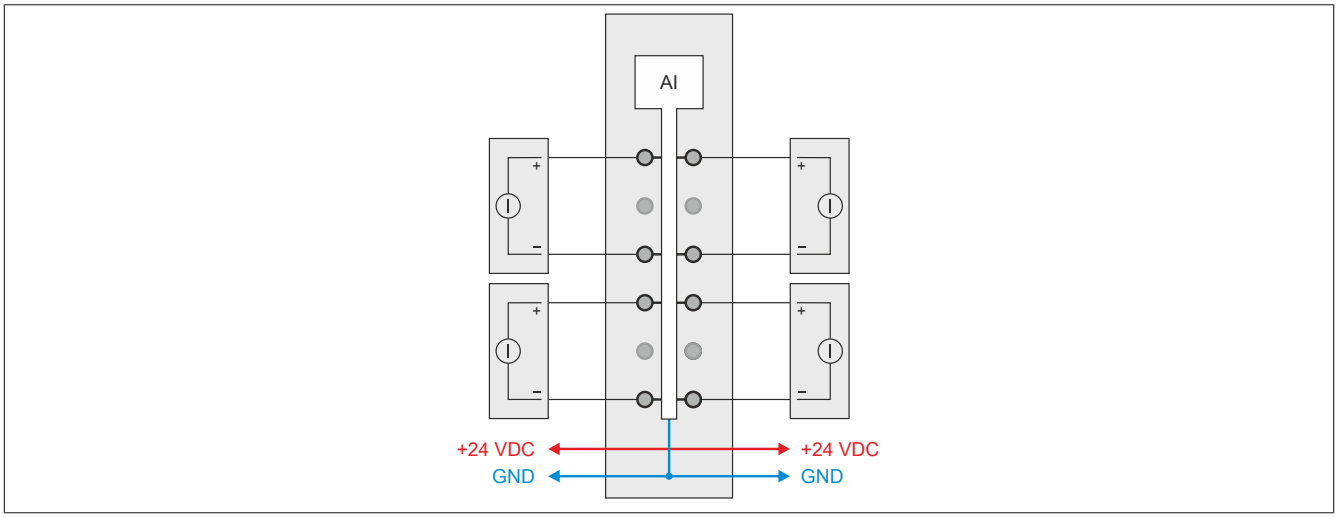
To prevent disturbances, the following modules must be separated by at least one module:

- Bus receiver X20BR9300
- Supply module X20PS3300/X20PS3310
- Supply module X20PS9400/X20PS9402
- Power supply module X20PS9600/X20PS9602
- Controller

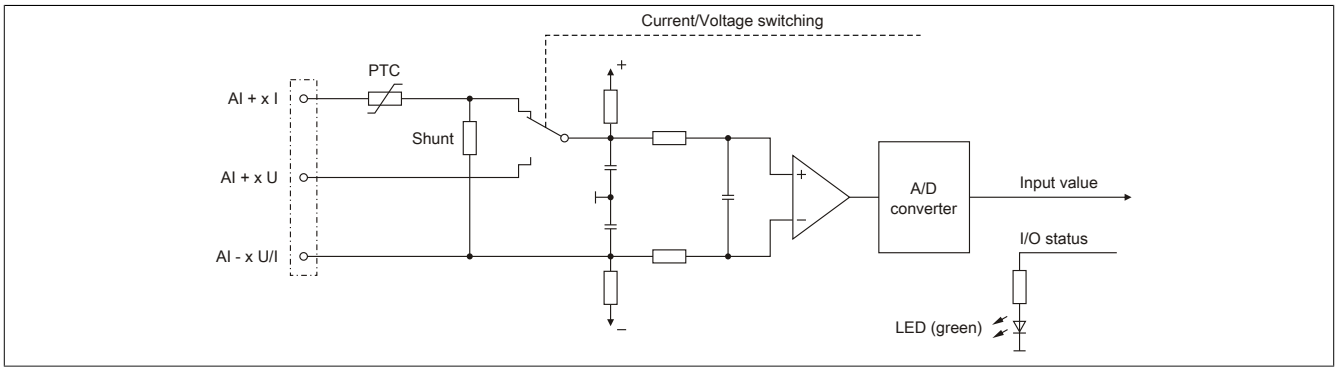
Voltage measurement



Current measurement



1.17.2.5 Input circuit diagram

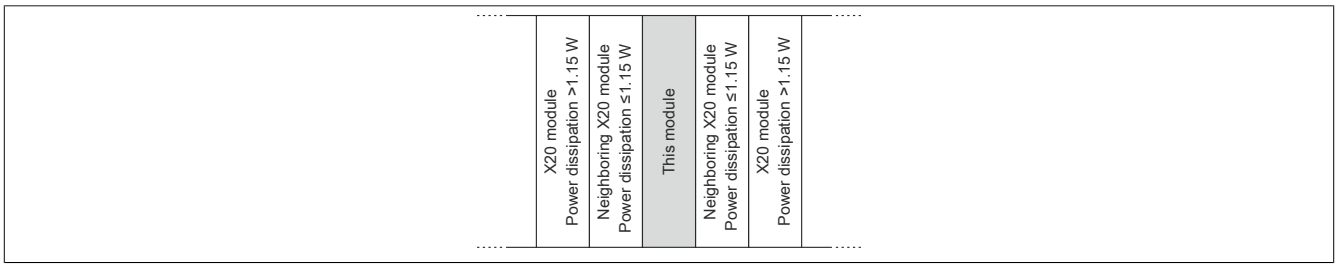


1.17.2.6 Derating

There is no derating when operated below 55°C.

When operated above 55°C, the modules to the left and right of this module are permitted to have a maximum power dissipation of 1.15 W!

For an example of calculating the power dissipation of I/O modules, see section "Mechanical and electrical configuration - Power dissipation of I/O modules" in the X20 user's manual.



1.17.3 Function description

1.17.3.1 Operating modes

1.17.3.1.1 Standard - Oversampling

The input values are recorded with a configurable sampling cycle time and saved with timestamp to the internal physical data buffer. This data range can then be read out in the cyclic data transfer using a configurable data length.

The recording and transmission system for the logical channels is identical to that for the physical channels. The functions of the logical channels are also executed in the configured sampling cycle time and saved with timestamp to the logical data buffer. The values can also be read out from here using configurable cyclic data points.

The defined sampling cycle time may not be sufficient for the sum of all physical and logical functions if using fast X2X Link cycle times, however. If influencing the physical sampling is not permitted, then a prescaler can be used to slow down the logical processing.

> **Information:**
>
> **The ability to adjust the sampling cycle time as needed on the module means there is basically no synchronization with X2X Link, regardless of whether standard inputs or an oversampling function is configured.**
>
> **If synchronization is required, then the configured sampling cycle time must be a multiple of the X2X Link cycle time!**

1.17.3.1.2 Bus controller

The module is operated as a normal analog input module in this mode. The input values are measured with a configurable sampling cycle time and saved in the internal physical data buffer with timestamp. Only the latest value is transferred in the next possible bus cycle.

It is possible to assign a logical function directly to each input channel, however. The analog data on the bus controller is mapped using the calculation options of the logical channels and configured automatically, see "Operation in the standard function model" on page 417.

Function model "Bus controller" has the following limitations compared to function model Standard:

- No oversampling function since consistency is not possible due to the small data range when operating on CAN-based bus controllers
- The sampling cycle time is set to 100 µs.
- No timestamp function
- A selection of logical functions is available with which the physical values can already be processed on the module:
    - Physical value output (standard)
    - Addition of two channels with scaling
    - Integral addition of two channels with scaling
    - Multiplication of two channels with scaling
    - Integral multiplication of two channels with scaling

1.17.3.2 Oversampling

1.17.3.2.1 Analog oversampling

With analog oversampling, the enabled channels are stored in the module in a configurable interval independently of the X2X cycle. The memory depth is 16 analog values per physical and logical channel.

These samplings are numbered from 1 to 16 in the registers. The conversions or calculations of the individual channels with the same number (i.e. sample line 1 to 16, e.g. PhysCh01Sample**10**, PhysCh02Sample**10**) originate from the same sampling cycle or logical calculation cycle and therefore have the same timestamp.

The timestamp refers to the newest data value, i.e. always to sample line 1. If a timestamp for older data points is needed, it needs to be back-calculated in the application using the sampling cycle time configured on the module. The prescaler must also be taken into account for logical channels.

Calculation example

Sample line	Calculation	
1	Timestamp	**Newest value**
2	Timestamp - Sampling cycle time	
3	Timestamp - 2 * Sampling cycle time	
4	Timestamp - 3 * Sampling cycle time	
...	...	
10	Timestamp - 9 * Sampling cycle time	
...	...	
16	Timestamp - 15 * Sampling cycle time	**Oldest value**

How the buffer is organized can be seen from this. This is not a FIFO buffer but a static buffer that the values are pushed through. Sample line 1 always contains the newest values, the next line the second newest, all the way up to sample line 16, which contains the oldest values.

The sample counter is a circular counter, with the number of new sample lines derived from the value of the last transfer cycle.

Example

A difference of 3 to the last transfer cycle means:

The data in sample line 1 and all subsequent data from the previous transfer cycle is now shifted in the current cycle beginning with sample line 4. Sample lines 1 through 3 contain the new values for further processing by the application. Sample lines 14 through 16 from the last transfer cycle are no longer in the buffer.

1.17.3.2.2 Comparator oversampling

With comparator oversampling, the results of the enabled channels are stored in the module in a configurable interval independently of the X2X cycle. The memory depth is 16 bits per logical channel.

These samplings, i.e. the result bits, are numbered consecutively from 1 to 8 and 9 to 16 for the two registers. The results of the individual channels with the same number (i.e. sample line 1 to 16, e.g. LogicCh01Sample**16_9**, LogicCh01Sample**8_1** for channel 1) originate from the same sampling cycle or logical calculation cycle and therefore have the same timestamp.

The timestamp refers to the latest data value, so always to sample line 1, i.e. bit 0 in register "LogicCh01Sample8_1". If a timestamp for the older comparator results is needed, this must be recalculated in the application using the sampling cycle time set on the module. The prescaler setting must also be taken into account.

Calculation example

Sample line	(register name)	Calculation	
1	(LogicCh01Sample8_1 bit 0)	Timestamp	**Newest value**
2	(LogicCh01Sample8_1 bit 1)	Timestamp - Sampling cycle time	
3	(LogicCh01Sample8_1 bit 2)	Timestamp - 2 * Sampling cycle time	
4	(LogicCh01Sample8_1 bit 3)	Timestamp - 3 * Sampling cycle time	
...			
10	(LogicCh01Sample16_9 bit 1)	Timestamp - 9 * Sampling cycle time	
...			
16	(LogicCh01Sample16_9 bit 7)	Timestamp - 15 * Sampling cycle time	**Oldest value**

How the buffer is organized can be seen from this. This is not a FIFO buffer but a static buffer that the values are pushed through. Sample line 1 always contains the newest values, the next line the second newest, all the way up to sample line 16, which contains the oldest values.

The sample counter is a circular counter, with the number of new sample lines derived from the value of the last transfer cycle.

Example

A difference of 3 to the last transfer cycle means:

The comparator result in sample line 1 and all subsequent data from the previous transfer cycle is now shifted in the current cycle beginning with sample line 4. Sample lines 1 through 3 contain the new bit values for further processing by the application. Sample lines 14 through 16 from the last transfer cycle are no longer in the buffer.

1.17.3.2.3 Priorities and values

Priority of logical oversampling

- Low priority setting
  Preparation of the logical and physical buffer does not run in the same context. If the calculation time in logical oversampling is longer than the set sampling cycle time, this setting and a prescaler >1 can be used to split the logical processing over several sampling cycle times. The sample lines of the physical and logical oversampling therefore do not automatically have the same recording or calculation time. If the prescaler is configured incorrectly, logical oversampling cannot be processed successfully.
- High priority setting
  The logical and physical buffers are prepared in the same context. The sample lines of the physical and logical oversampling have the same recording or calculation time. All configured functions must be able to be executed in the set sampling cycle time; otherwise, a cycle time violation will occur and the configuration must be changed accordingly. The setting of the logical prescaler has no influence here; only the data volume in logical oversampling is limited.

Current or referenced values for logical or physical oversampling

In a busy system, jitter can occur in the sampling cycle on the module even with synchronous cycle time settings due to the necessary processing of the functions (X2X Link operation, logical and physical oversampling). This results in a different number of sample lines in the same time frames. For this reason, more samples should be configured in the cyclic image as well than is mathematically necessary.

- Current values setting
  The sample lines are transferred to the higher-level system as quickly as possible, with more or fewer new sample lines possibly occurring.
- Referenced values setting
  With this setting, jitter is minimized and a constant number of new sample lines per cycle is achieved with the optimal setting. With regard to response time, however, there may be delays of several sampling cycle times.

Information:

The register is described in "Logical oversampling and data acquisition" on page 428.

1.17.3.2.4 Data transfer

The analog conversion rate / sampling cycle time can be considerably faster than the X2X Link cycle. Saved analog or comparator data can be transferred to the higher-level system synchronously and consistently.

In terms of the application, it must be ensured that the ratio of cyclic data points, the sampling cycle time on the module and the transfer time is sufficient to read out all new data points in the higher-level system.

The sample counter can be used to check how many data values are actually new since the last transfer cycle. If the counter difference to the previous cycle is larger than the number of existing cyclic data points, then values have been overlooked and the system needs to be adjusted.

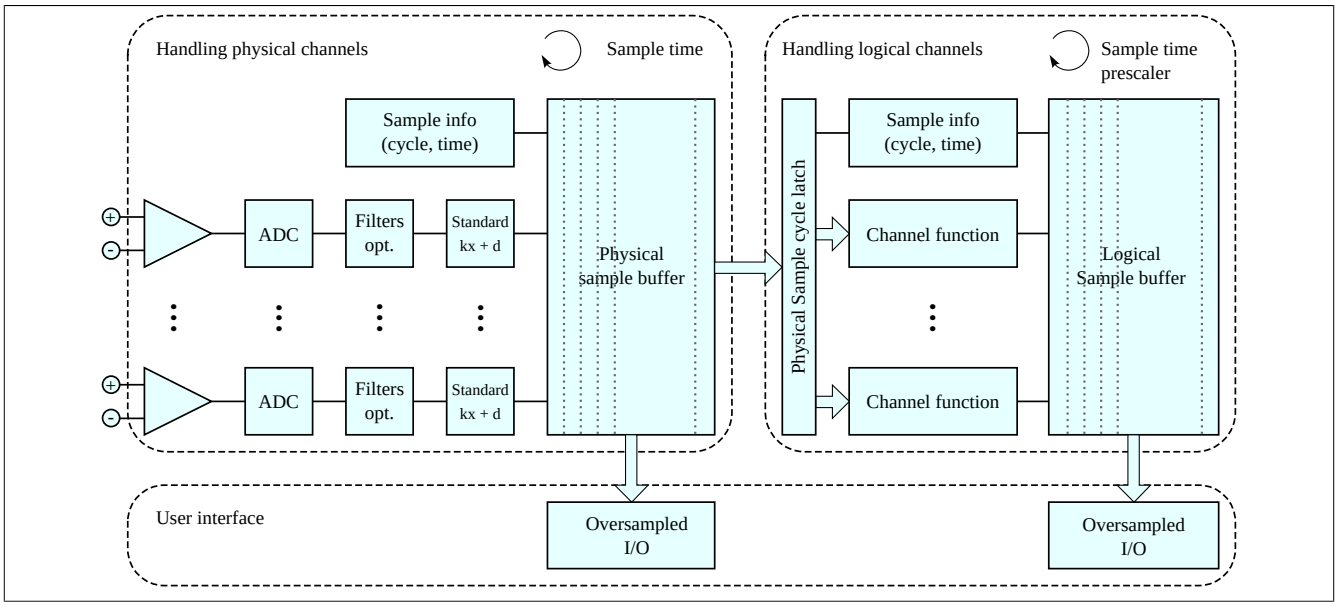
The general guideline is that a cyclic data point should be configured more than is actually required computing-wise.

Example with synchronous settings

- Sampling cycle time = 50 µs
- X2X Link cycle time = 500 µs

Samples 1 to 10 of a channel are possible to calculate in this example. Sample 11 should also be configured as a cyclic data point, however.
The reason for this is the possible jitter in the module caused by interruptions, e.g. from the X2X Link transfer. For the current cycle, this can mean that only 9 new values are available and that 11 values will have to be transferred in the next cycle.

For logical comparator functions, this problem doesn't exist since the maximum number is always transferred in the cycle data range.



1.17.3.3 Physical values

The conversion results are scaled and filtered before being transferred to the higher-level system. No further processing takes place.

Information:

The registers are described in "Physical configuration" on page 429.

1.17.3.3.1 Physical sampling

This module has a data buffer with 16 entries for each of the physical input channels. This buffer is processed according to the configured sampling cycle time.

A maximum of only 30 bytes is available for cyclic transfer on the X2X bus, however. Minus the status and sample counter, this allows only a selection of 14 samples (with a 16-bit data width) from the physical and logical buffer to be transferred.
Data loss can therefore occur with an imprecise selection and configuration.

Example

Displaying continuous sample lines.

- Sampling cycle time = 100 µs
- X2X cycle time = 500 µs

Sample line 1	PhysCh0xSample1
Sample line 2	PhysCh0xSample2
Sample line 3	PhysCh0xSample3
Sample line 4	PhysCh0xSample4
Sample line 5	PhysCh0xSample5
Sample line 6	PhysCh0xSample6
Difference SampleCount = 1	New value in sample line 1
Difference SampleCount = 2	New values in sample line 1 and sample line 2
...	
Difference SampleCount = 5	New values in sample line 1 to sample line 5

Information:

It is important to note that the sample counter refers to the update of the sample lines in the data buffer and not to the number of values transferred cyclically.

Display every second sample line to bridge a longer recording duration:

- Sampling cycle time = 100 µs
- X2X cycle time = 1000 µs

Sample line 1	PhysCh0xSample1
Sample line 3	PhysCh0xSample3
Sample line 5	PhysCh0xSample5
Sample line 7	PhysCh0xSample7
Sample line 9	PhysCh0xSample9
Sample line 11	PhysCh0xSample11
Difference SampleCount = 1	New value in sample line 1
Difference SampleCount = 3	New values in sample line 1 and sample line 3
...	
Difference SampleCount = 5	New values in sample line 1 to sample line 5
...	
Difference SampleCount = 9	New values in sample line 1 to sample line 9

1.17.3.3.2 Input filter

This module is equipped with an individually configurable input filter for each channel. The following filters can be selected:

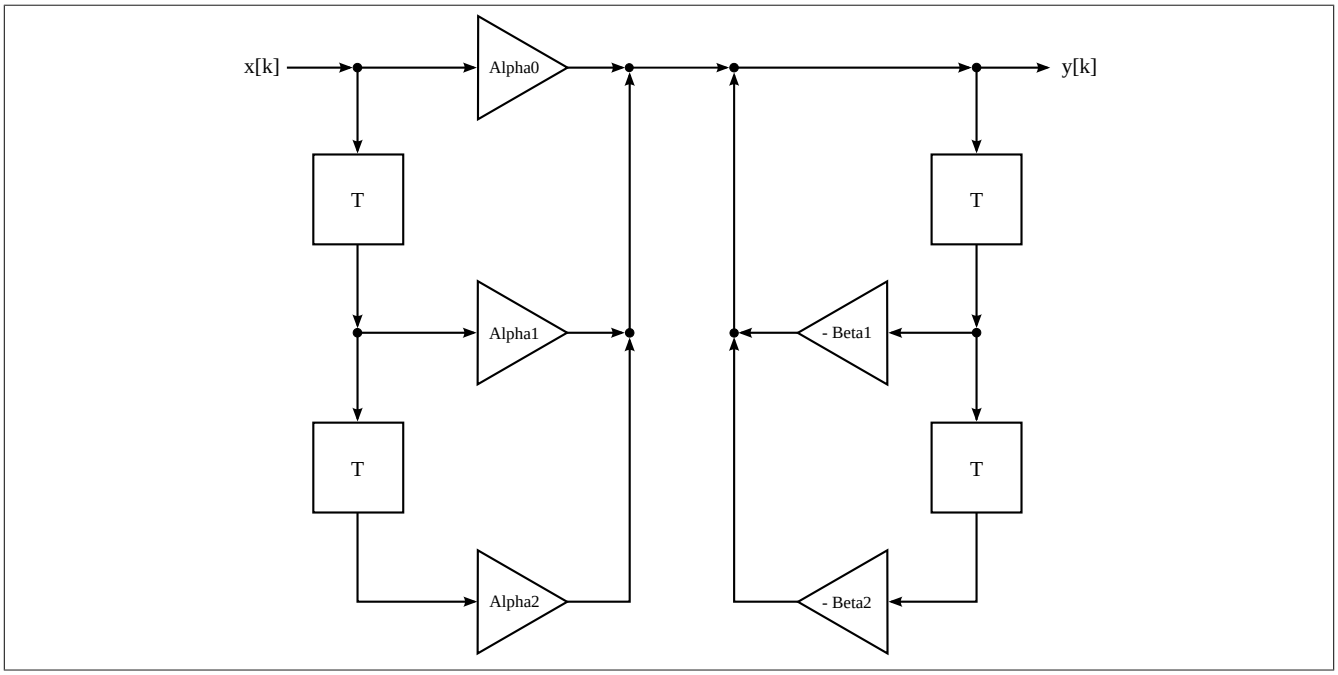
- 1st-order low pass
- 2nd-order low pass
- 2nd-order IIR

The cutoff frequency for the first-order and second-order low-pass filters is configurable. Coefficients Alpha0, Alpha1, Alpha2, Beta1 and Beta2 must be configured for the IIR filter.

Image as a z-transfer function

The second-order z-transfer function is specified in coefficient form (denominator polynomial Beta1, Beta2 and numerator polynomial Alpha0, Alpha1, Alpha2). The transfer method is calculated with the sampling cycle time.

$$S(Z) = \frac{a(Z)}{b(Z)} = \frac{Alpha0 + Alpha1 * Z^{-1} + Alpha2 * Z^{-2}}{1 + Beta1 * Z^{-1} + Beta2 * Z^{-2}}$$



Information:

The registers are described in "Filtering" on page 429.

1.17.3.3.3 Scaling

The analog input channels are calibrated and scaled when delivered (gain = k, offset = d).

User-defined scaling (gain = ku, offset = du) is also available. The calculation is optimized by combining the factors.

Normalization calculation:

nom = k * RawValue + d

k = k * ku

d = k * d + du

The values calculated here are limited to 16 bits.

Information:

The registers are described in "Scaling" on page 429.

1.17.3.4 Logical values

The physical values can be further processed using mathematical functions and comparators. Another logical channel can also be used as a starting point for further processing for a logical function.

Information:

The registers are described in "Logical configuration" on page 430.

1.17.3.4.1 Logical sampling

The module has a data buffer with 16 entries for each of the 6 logical channels. This buffer is processed according to the configured sampling cycle time. In addition, it's also possible to adjust the logical execution cycle using a prescaler for the sampling cycle time.

A maximum of only 30 bytes is available for cyclic transfer on the X2X bus, however. Minus the status and sample counter, this allows only a selection of 14 samples (with a 16-bit data width) from the physical and logical buffer to be transferred. For the logical channels, it is also possible to configure a 32-bit data width.
Data loss can therefore occur with an imprecise selection and configuration.

Example

Displaying continuous sample lines.

- Sampling cycle time = 100 µs
- X2X cycle time = 500 µs

Sample line 1	LogicCh0xSample1
Sample line 2	LogicCh0xSample2
Sample line 3	LogicCh0xSample3
Sample line 4	LogicCh0xSample4
Sample line 5	LogicCh0xSample5
Sample line 6	LogicCh0xSample6
Difference SampleCount = 1	New value in sample line 1
Difference SampleCount = 2	New values in sample line 1 and sample line 2
...	
Difference SampleCount = 5	New values in sample line 1 to sample line 5

Information:

It is important to note that the sample counter refers to the update of the sample lines in the data buffer and not to the number of values transferred cyclically.

Display every second sample line to bridge a longer recording duration:

- Sampling cycle time = 100 µs
- X2X cycle time = 1000 µs

Sample line 1	LogicCh0xSample1
Sample line 3	LogicCh0xSample3
Sample line 5	LogicCh0xSample5
Sample line 7	LogicCh0xSample7
Sample line 9	LogicCh0xSample9
Sample line 11	LogicCh0xSample11
Difference SampleCount = 1	New value in sample line 1
Difference SampleCount = 3	New values in sample line 1 and sample line 3
...	
Difference SampleCount = 5	New values in sample line 1 to sample line 5
...	
Difference SampleCount = 9	New values in sample line 1 to sample line 9

1.17.3.4.2 Operation in the standard function model

6 logical channels are available on the module. Each channel can be configured with one of the following functions:

- "Addition of two channels with scaling" on page 418
- "Integral addition of two channels with scaling" on page 419
- "Multiplication of two channels with scaling" on page 420
- "Integral multiplication of two channels with scaling" on page 421
- "Comparator function of two channels" on page 421
- "Hysteresis comparator of one channel " on page 421

The sources to be used for each logical channel are selected using register "CfO_LogCh0NSource0x". The additionally required function parameters are configured in the "CfO_LogCh0NFuncPar0x" registers. "N" stands for the logical channel to be used; "x" stands for the source or function 0 or 1.

The following links can be made:

- Addition: Result = (Source0 * FunctionParameter0) + (Source1 * FunctionParameter1)
- Integral of the addition: Result = Σ(Source0 * FunctionParameter0) + (Source1 * FunctionParameter1)
- Multiplication: Result = Source0 * Source1 * FunctionParameter0
- Integral of the multiplication: Result = Σ(Source0 * Source1 * FunctionParameter0)
- Channel comparator: Result = Comparison of Source0 with Source1
- Hysteresis comparator: Result = Comparison of Source0 with (Lower threshold value = FunctionParameter0) and (Upper threshold value = FunctionParameter1)
- Physical value display: Result = (Source0 * 1) + (Source1 * 0)

With logical oversampling, 32-bit data points are available in addition to the 16-bit data points due to the possible calculation results. Which ones are used can be selected via the Automation Studio I/O configuration or the data point mapping.

If there is no need for 32-bit data points or this would result in a large restriction in the number of data points, scaling can be used to limit the number range to 16 bits.

The buffer depth for the digital comparator is also able to handle 16 results. Since these are Boolean results, these 16 bits are compressed into 2-byte data points and transferred that way.

1.17.3.4.2.1 Addition

This function can be used to determine the sum or difference of two channels. Only negative scaling of a channel must be configured for calculating the difference.

Calculation

Sample line = (Channel 1 * Scaling 1) + (Channel 2 * Scaling 2)

The addition calculation is performed internally with 32 bits in 16.16 format; the data from the source channels is evaluated as integers (applied to the high word), with decimal places possible due to scaling. When displayed as a logical 32-bit result, these decimal places are visible. When displayed as a 16-bit value, only the integral high word is used.

Example

Channel 1 = 2000
Channel 2 = 1000
Both scalings = 1

Results

3000.x = (2000.x * 1.0) + (1000.x * 1.0)
32-bit representation = 196608000 = 0xBB80000
16-bit representation = 3000 = 0xBB8

Information:

The maximum value for channels 1 and 2 can only be 32767; otherwise, an additional overflow occurs. If values greater than 32767 are possible, the range of values must be limited with scaling.

1.17.3.4.2.2 Integral of addition

This function can be used in the application to establish the average value of the channels or to calculate the deviation/difference between two channels over n samples. In each cycle, addition of the channels is carried out first; the summed result is then saved with the previous value in the current sample line. Depending on the result data type used (16-bit or 32-bit), the calculation overflows sooner or later after n samples due to continuous integration. Due to the signed result value, it must be ensured by the application that number n of samples is chosen small enough so that the integral calculation is less than half the range of values. If this is done, determining the average value can be carried out despite an overflow.

Calculation

Sample line result = Integral ((Channel 1 * Scaling 1) + (Channel 2 * Scaling 2))

The addition calculation is performed internally with 32 bits in 16.16 format; the data from the source channels is evaluated as integers (applied to the high word), with decimal places possible due to scaling. When displayed as a logical 32-bit result, these decimal places are visible. When displayed as a 16-bit value, only the integral high word is used.

Example

Channel 1 = 2000
Channel 2 = 1000
Both scalings = 1

Results

3000.x = (2000.x * 1.0) + (1000.x * 1.0)
32-bit representation = 196608000 = 0xBB80000.
16-bit representation = 3000 = 0xBB8

The average value can now be calculated as follows:

n = Number of samples / sample line
$Value_x$ = Value from sample line x → Newer value
$Value_{(x-n)}$ = Value from sample line x-n → Older value, n samplings back

Average value = ($Value_x$ - $Value_{(x-n)}$) / n

Information:

The maximum value for channels 1 and 2 can only be 32767; otherwise, an additional overflow occurs. If values greater than 32767 are possible, the range of values must be limited with scaling.

1.17.3.4.2.3 Multiplication

This function can be used to calculate the current effective power P = U * I.

Calculation

Sample line = Channel 1 * Channel 2 * Scaling

Multiplication is calculated internally as a 32-bit value; the 16-bit data from the source channels is passed to the low word. When displayed as a logical 32-bit value, the entire result is visible (no multiplication overflow possible when scaling ≤1). When displayed as a 16-bit value, only the high word is used. Though there is a loss of precision, the 16-bit values allow more data points to be transferred.

Example

Channel 1 = 2000
Channel 2 = 1000
Scaling = 1

Results

2000000 = (2000 * 1000 * 1.0)
32-bit representation = 2000000 = 0x1E8480
16-bit representation = 30 = 0x1E

Information:

If higher accuracy is required for the 16-bit value, scaling can be used to shift the bit value in steps of 2^n (... *128, * 256, ...). It is important to ensure that the input values of the source channels are limited here as well; otherwise, there will be an overflow in the multiplication.

1.17.3.4.2.4 Integral of multiplication

This function can be used to calculate the average of the active power in the application. In each cycle, multiplication of the channels is carried out first; the summed result is then saved with the previous value in the current sample line. Depending on the result data type used (16-bit or 32-bit), the calculation overflows sooner or later after n samples due to continuous integration. Due to the signed result value, it must be ensured by the application that number n of samples is chosen small enough so that the integral calculation is less than half the range of values. If this is done, determining the average value can be carried out despite an overflow.

Calculation

Sample line = Integral (Channel 1 * Channel 2 * Scaling)

Multiplication is calculated internally as a 32-bit value; the 16-bit data from the source channels is passed to the low word. When displayed as a logical 32-bit value, the entire result is visible (no multiplication overflow possible when scaling ≤1). When displayed as a 16-bit value, only the high word is used. Though there is a loss of precision, the 16-bit values allow more data points to be transferred.

Example

Channel 1 = 2000
Channel 2 = 1000
Scaling = 1

Results

2000000 = (2000 * 1000 * 1.0)
32-bit representation = 2000000 = 0x1E8480
16-bit representation = 30 = 0x1E

The average value can now be calculated as follows:

n = Number of samples / sample line
$Value_x$ = Value from sample line x → Newer value
$Value_{(x-n)}$ = Value from sample line x-n → Older value, n samplings back

Average value = ($Value_x$ - $Value_{(x-n)}$) / n

Information:

If higher accuracy is required for the 16-bit value, scaling can be used to shift the bit value in steps of 2^n (... *128, * 256, ...). It is important to ensure that the input values of the source channels are limited here as well; otherwise, there will be an overflow in the multiplication.

1.17.3.4.2.5 Channel comparator

This function can be used to compare channel values. The following applies:

- Channel 1 > Channel 2 = 1
- Channel 1 < Channel 2 = 0
- Channel 1 = Channel 2 = State before values are the same

Calculation

Sample line (bit) = Comparison (channel value 1 with channel value 2)

1.17.3.4.2.6 Hysteresis comparator

This function can be used to monitor channel limit violations. The following applies:

- Channel > Upper threshold value = 1
- Channel < Lower threshold value = 0
- Channel within threshold = Value before occurrence

Calculation

Sample line (bit) = Comparison (channel value with lower threshold value) and (channel value with upper threshold value))

1.17.3.4.3 Operation in the bus controller function model

When used on the bus controller, there are 4 logical functions available for each of the analog input channels in addition to the physical value output. Each channel can be configured with one of the following functions:

- "Output of physical values" on page 422 (default setting)
- "Addition of two channels with scaling" on page 418
- "Integral addition of two channels with scaling" on page 419
- "Multiplication of two channels with scaling" on page 420
- "Integral multiplication of two channels with scaling" on page 421
- "Comparator function of two channels" on page 421
- "Hysteresis comparator of one channel " on page 421

In contrast to the standard function model, oversampling and the two digital comparators are not supported. As a result, there is only one newly generated value per channel in each update cycle. Another difference is that there are only 4 logical calculation channels instead of 6.

The logical functions addition, integral of addition, multiplication and integral of multiplication do not differ from the standard function model in their configuration and function when operating on the bus controller.

1.17.3.4.3.1 Value display in bus controller operating mode

The physical value display in the bus controller function model is initialized automatically and represents a special form of the logical function "Addition" with defined scaling factors.

Calculation

Result = Channel value
Formula used for addition: Result = (Channel value 1 * 1) + (Channel value 2 * 0)

Information:

In this function model, only the 4 physical input channels are available, and the scaling factors have fixed values.

1.17.3.5 Monitoring the inputs

The module's inputs are monitored. The standard and extended error messages must be enabled individually for each channel.

The following areas are monitored:

- **Out of range:** The analog input signal is outside the specified operating range.
- **Filter error:** The set filter theorem cannot be calculated (parameter error).
- **Underflow:** The input signal is less than the lower limit value.
- **Overflow:** The input signal is greater than the upper limit value.

Value	Information
0	No error occurred
1	Error occurred

The composite errors of the channels are derived from the individual extended error states, e.g. underflow, overflow of the input range on the analog value. The error state of the oversampling results from a cycle time violation of the set sampling cycle time. All configured physical and logical oversampling functions must be able to be carried out in the configured sampling cycle time; otherwise, an error message will be displayed.

Any error messages that occur must be acknowledged by setting the corresponding bits.

Information:

The registers are described in "Error monitoring" on page 434.

1.17.4 Commissioning

1.17.4.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

1.17.4.1.1 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

1.17.5 Register description

1.17.5.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 System user's manual.

1.17.5.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
System configuration						
513	CfO_BaseConfig	USINT				•
15364	CfO_CycleTime	UDINT				•
15370	CfO_SyncOffset	UINT				•
15374	CfO_Prescaler	UINT				•
Error messages - Configuration						
385	CfO_ErrorID0007	USINT				•
387	CfO_ErrorID080F	USINT				•
389	CfO_ErrorID1017	USINT				•
Physical channel configuration						
8194 + (N-1) * 256	CfO_ModeCh0N (index N = 1 to 4)	UINT				•
8204 + (N-1) * 256	CfO_UserGainCh0N (index N = 1 to 4)	DINT				•
8212 + (N-1) * 256	CfO_UserOffsetCh0N (index N = 1 to 4)	DINT				•
8220 + (N-1) * 256	CfO_Alpha0Ch0N (index N = 1 to 4)	DINT				•
8228 + (N-1) * 256	CfO_Alpha1Ch0N (index N = 1 to 4)	DINT				•
8236 + (N-1) * 256	CfO_Alpha2Ch0N (index N = 1 to 4)	DINT				•
8244 + (N-1) * 256	CfO_Beta1Ch0N (index N = 1 to 4)	DINT				•
8252 + (N-1) * 256	CfO_Beta2Ch0N (index N = 1 to 4)	DINT				•
8198 + (N-1) * 256	CfO_CutOffFrequCh0N (index N = 1 to 4)	UINT				•
Logical channel configuration						
10242 + (N-1) * 256	CfO_LogCh0NMode (index N = 1 to 6)	UINT				•
10245 + (N-1) * 256	CfO_LogCh0NSource00 (index N = 1 to 6)	USINT				•
10247 + (N-1) * 256	CfO_LogCh0NSource01 (index N = 1 to 6)	USINT				•
10260 + (N-1) * 256	CfO_LogCh0NFuncPar00 (index N = 1 to 6)	UDINT				•
10268 + (N-1) * 256	CfO_LogCh0NFuncPar01 (index N = 1 to 6)	UDINT				•
Analog inputs - Communication						
5062 + (N-1) * 8	AnalogInput0N (index N = 1 to 4)	INT	•			
Error messages - Communication						
261	Composite error	USINT	•			
	Channel01Error	Bit 0				
	...	...				
	Channel04Error	Bit 3				
	PhysicalError	Bit 4				
	LogicalError	Bit 5				
325	Acknowledging standard errors	USINT			•	
	AckChannel01Error	Bit 0				
	...	...				
	AckChannel04Error	Bit 3				
	AckPhysicalError	Bit 4				
	AckLogicalError	Bit 5				

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
257	Extended channel error messages	USINT	•			
	Channel01OutOfRange	Bit 0				
	Channel01FilterError	Bit 1				
	Channel01Underflow	Bit 2				
	Channel01Overflow	Bit 3				
	Channel02OutOfRange	Bit 4				
	Channel02FilterError	Bit 5				
	Channel02Underflow	Bit 6				
	Channel02Overflow	Bit 7				
321	Acknowledging extended channel error messages	USINT			•	
	AckChannel01OutOfRange	Bit 0				
	AckChannel01FilterError	Bit 1				
	AckChannel01Underflow	Bit 2				
	AckChannel01Overflow	Bit 3				
	AckChannel02OutOfRange	Bit 4				
	AckChannel02FilterError	Bit 5				
	AckChannel02Underflow	Bit 6				
	AckChannel02Overflow	Bit 7				
259	Extended channel error messages	USINT	•			
	Channel03OutOfRange	Bit 0				
	Channel03FilterError	Bit 1				
	Channel03underflow	Bit 2				
	Channel03Overflow	Bit 3				
	Channel04OutOfRange	Bit 4				
	Channel04FilterError	Bit 5				
	Channel04Underflow	Bit 6				
	Channel04Overflow	Bit 7				
323	Acknowledging extended channel error messages	USINT			•	
	AckChannel03OutOfRange	Bit 0				
	AckChannel03FilterError	Bit 1				
	AckChannel03Underflow	Bit 2				
	AckChannel03Overflow	Bit 3				
	AckChannel04OutOfRange	Bit 4				
	AckChannel04FilterError	Bit 5				
	AckChannel04Underflow	Bit 6				
	AckChannel04Overflow	Bit 7				
Physical analog sample display						
4102 + (16-N) * 64	PhysCh01SampleN (index N = 1 to 16)	INT	•			
4110 + (16-N) * 64	PhysCh02SampleN (index N = 1 to 16)	INT	•			
4118 + (16-N) * 64	PhysCh03SampleN (index N = 1 to 16)	INT	•			
4126 + (16-N) * 64	PhysCh04SampleN (index N = 1 to 16)	INT	•			
5106	PhysTimestamp	INT	•			
5108	PhysTimestamp	DINT	•			
5113	PhysSampleCount	SINT	•			
5114	PhysSampleCount	INT	•			
Logical analog and digital sample display						
6148 + (16-N) * 64	LogicCh01SampleN (index N = 1 to 16) (32-bit)	DINT	•			
6150 + (16-N) * 64	LogicCh01SampleN (index N = 1 to 16) (16-bit)	INT	•			
6156 + (16-N)*64	LogicCh02SampleN (index N = 1 to 16) (32-bit)	DINT	•			
6158 + (16-N)*64	LogicCh02SampleN (index N = 1 to 16) (16-bit)	INT	•			
6164 + (16-N)*64	LogicCh03SampleN (index N = 1 to 16) (32-bit)	DINT	•			
6166 + (16-N)*64	LogicCh03SampleN (index N = 1 to 16) (16-bit)	INT	•			
6172 + (16-N)*64	LogicCh04SampleN (index N = 1 to 16) (32-bit)	DINT	•			
6174 + (16-N)*64	LogicCh04SampleN (index N = 1 to 16) (16-bit)	INT	•			
6180 + (16-N)*64	LogicCh05SampleN (index N = 1 to 16) (32-bit)	DINT	•			
6182 + (N-16)*64	LogicCh05SampleN (index N = 1 to 16) (16-bit)	INT	•			
6188 + (16-N)*64	LogicCh06SampleN (index N = 1 to 16) (32-bit)	DINT	•			
6190 + (16-N)*64	LogicCh06SampleN (index N = 1 to 16) (16-bit)	INT	•			
7109 + (N-1) * 8	LogicCh0NSample16_9 (index N = 1 to 5)	USINT	•			

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
7151	LogicCh06Sample16_9	USINT	•			
7111 + (N-1) * 8	LogicCh0NSample8_1 (index N = 1 to 5)	USINT	•			
7149	LogicCh06Sample8_1	USINT	•			
7154	LogicTimestamp	INT	•			
7156	LogicTimestamp	DINT	•			
7161	LogicSampleCount	SINT	•			
7162	LogicSampleCount	INT	•			

1.17.5.3 Function model 254 - Bus controller

The "Bus controller" function model has the following limitations compared to the "Standard" function model:

- No oversampling function since consistency is not possible when operating CAN-based bus controllers due to the limited data range
- The sampling cycle time is set to 100 µs.
- No timestamp function
- A range of logical functions is available for processing the physical values right on the module:
  - Output of physical values (standard)
  - Addition of two channels with scaling
  - Integral addition of two channels with scaling
  - Multiplication of two channels with scaling
  - Integral multiplication of two channels with scaling

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
System configuration							
513	-	CfO_BaseConfig	USINT				•
15364	-	CfO_CycleTime	UDINT				•
15370	-	CfO_SyncOffset	UINT				•
15374	-	CfO_Prescaler	UINT				•
Error messages - Configuration							
385	-	CfO_ErrorID0007	USINT				•
387	-	CfO_ErrorID080F	USINT				•
389	-	CfO_ErrorID1017	USINT				•
Physical channel configuration							
8194 + (N-1) * 256	-	CfO_ModeCh0N (index N = 1 to 4)	UINT				•
8204 + (N-1) * 256	-	CfO_UserGainCh0N (index N = 1 to 4)	DINT				•
8212 + (N-1) * 256	-	CfO_UserOffsetCh0N (index N = 1 to 4)	DINT				•
8220 + (N-1) * 256	-	CfO_Alpha0Ch0N (index N = 1 to 4)	DINT				•
8236 + (N-1) * 256	-	CfO_Alpha2Ch0N (index N = 1 to 4)	DINT				•
8244 + (N-1) * 256	-	CfO_Beta1Ch0N (index N = 1 to 4)	DINT				•
8252 + (N-1) * 256	-	CfO_Beta2Ch0N (index N = 1 to 4)	DINT				•
8198 + (N-1) * 256	-	CfO_CutOffFrequCh0N (index N = 1 to 4)	UINT				•
Logical channel configuration							
10242 + (N-1) * 256	-	CfO_LogCh0NMode (index N = 1 to (index N = 1 to 6)	UINT				•
10245 + (N-1) * 256	-	CfO_LogCh0NSource00 (index N = 1 to 6)	USINT				•
10247 + (N-1) * 256	-	CfO_LogCh0NSource01 (index N = 1 to 6)	USINT				•
10260 + (N-1) * 256	-	CfO_LogCh0NFuncPar00 (index N = 1 to 6)	UDINT				•
10268 + (N-1) * 256	-	CfO_LogCh0NFuncPar01 (index N = 1 to 6)	UDINT				•
Analog inputs - Communication							
5062 + (N-1) * 8	(N-1) * 2	AnalogInput0N (index N = 1 to 4)	INT	•			

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Error messages - Communication							
261	-	Composite error	USINT		•		
		Channel01Error	Bit 0				
		...	...				
		Channel04Error	Bit 3				
		PhysicalError	Bit 4				
		LogicalError	Bit 5				
325	-	Acknowledging standard errors	USINT				•
		AckChannel01Error	Bit 0				
		...	...				
		AckChannel04Error	Bit 3				
		AckPhysicalError	Bit 4				
		AckLogicalError	Bit 5				
257	-	Extended channel error messages	USINT		•		
		Channel01OutOfRange	Bit 0				
		Channel01FilterError	Bit 1				
		Channel01Underflow	Bit 2				
		Channel01Overflow	Bit 3				
		Channel02OutOfRange	Bit 4				
		Channel02FilterError	Bit 5				
		Channel02Underflow	Bit 6				
		Channel02Overflow	Bit 7				
321	-	Acknowledging extended channel error messages	USINT				•
		AckChannel01OutOfRange	Bit 0				
		AckChannel01FilterError	Bit 1				
		AckChannel01Underflow	Bit 2				
		AckChannel01Overflow	Bit 3				
		AckChannel02OutOfRange	Bit 4				
		AckChannel02FilterError	Bit 5				
		AckChannel02Underflow	Bit 6				
		AckChannel02Overflow	Bit 7				
259	-	Extended channel error messages	USINT		•		
		Channel03OutOfRange	Bit 0				
		Channel03FilterError	Bit 1				
		Channel03underflow	Bit 2				
		Channel03Overflow	Bit 3				
		Channel04OutOfRange	Bit 4				
		Channel04FilterError	Bit 5				
		Channel04Underflow	Bit 6				
		Channel04Overflow	Bit 7				
323	-	Acknowledging extended channel error messages	USINT				•
		AckChannel03OutOfRange	Bit 0				
		AckChannel03FilterError	Bit 1				
		AckChannel03Underflow	Bit 2				
		AckChannel03Overflow	Bit 3				
		AckChannel04OutOfRange	Bit 4				
		AckChannel04FilterError	Bit 5				
		AckChannel04Underflow	Bit 6				
		AckChannel04Overflow	Bit 7				

1) The offset specifies the position of the register within the CAN object.

1.17.5.4 Configuration

Configuration must take place in addition to using suitable terminals.

1.17.5.4.1 System configuration

The following registers are used to configure the module's system settings.

1.17.5.4.1.1 Logical oversampling and data acquisition

Name:
CfO_BaseConfig

This register can be used to configure settings relating to handling logical oversampling and data acquisition. For details, see "Priorities and values" on page 412.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	49

Bit structure:

Bit	Description	Value	Information
0	"Display configuration for logical values active/inactive" in the Automation Studio I/O configuration	0	Inactive
		1	Active (bus controller default setting)
1	"Logical handling priority" in the Automation Studio I/O configuration	0	Low (bus controller default setting)
		1	High
2 - 3	Reserved	-	
4	"Physical input mode" in the Automation Studio I/O configuration	0	Newest value
		1	Referenced value (reference = prescaled system timer) (bus controller default setting)
5	"Logical input mode" in the Automation Studio I/O configuration	0	Newest value
		1	Referenced value (reference = prescaled system timer) (bus controller default setting)
6 - 7	Reserved	-	

1.17.5.4.1.2 Sampling cycle time

Name:
CfO_CycleTime
"Physical sample time" in the Automation Studio I/O configuration.

This register is used to set the sampling cycle time on the module. The format is a 16.16-bit unsigned 4-byte value, where the high word is the microseconds integer and the low word is the decimal places. The decimal places allow a more precise adjustment to the X2X cycle time. The absolute resolution is 1 µs.

Input value = Time in µs * 65536 data type

Data type	Value	Information
UDINT	2,621,440 to 2,147,483,647	40 µs to 32 ms sampling cycle time. Bus controller default setting: 6,553,600 = 100 µs

1.17.5.4.1.3 Prescaler of the logical channel processing time

Name:
CfO_Prescaler

This register contains the prescaler for configuring the logical channel processing time. The actual logical cycle time will be calculated from the multiple of the sampling cycle time that is defined here. If a very short sampling cycle time is required for physical samples, then the module load can be reduced using the second time base for the logical samples.

Data type	Value	Information
UINT	1 to 10	Multiples of the physical sampling cycle for logical processing Bus controller default setting: 2

1.17.5.4.1.4 Synchronization offset

Name:
CfO_SyncOffset
"Synchronization offset" in the Automation Studio I/O configuration.

The system cycle can be offset in 1 µs steps in this register.

Data type	Value	Information
UINT	-32,768 to 32,767	Synchronization offset in µs. Bus controller default setting: 0

1.17.5.4.2 Scaling

The analog input channels are calibrated and scaled when delivered. User-defined scaling is also available.

1.17.5.4.2.1 Gain

Name:
CfO_UserGainCh01 to CfO_UserGainCh04
"Configuration channel 0x / gain" in the Automation Studio I/O configuration

These registers are used to set the gain for the corresponding channel. The format is a 16.16-bit signed 4-byte value, where the high word is the integer and the low word is the decimal places.

Input value = Gain ku * 65536

Value 65535 corresponds to a gain of 1.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	Gain. Bus controller default setting: 65535

1.17.5.4.2.2 Offset

Name:
CfO_UserOffsetCh01 to CfO_UserOffsetCh04
"Configuration channel 0x / offset" in the Automation Studio I/O configuration

These registers are used to set the offset for the corresponding channel. The format is a 16.16-bit signed 4-byte value, where the high word is the integer and the low word is the decimal places.

Input value = Offset du * 65536

Value 65536 corresponds to an offset of 1.

Data type	Value	Information
DINT	-2,147,483,648 to 2,147,483,647	Offset. Bus controller default setting: 0

1.17.5.4.3 Filtering

The module is equipped with an individually configurable input filter for each individual channel.

1.17.5.4.3.1 Coefficients

Name:
CfO_CutOffFrequCh01 to CfO_CutOffFrequCh04

These registers are used to configure the limit frequency in hertz for a 1st- or 2nd-order low pass for the corresponding channel.

Data type	Value	Information
UINT	0 to 65535	Cutoff frequency for 1st- or 2nd-order low pass [Hz]. Bus controller default setting: 1000

1.17.5.4.3.2 Cutoff frequency

Name:
CfO_Alpha0Ch01 to CfO_Alpha0Ch04
CfO_Alpha1Ch01 to CfO_Alpha1Ch04
CfO_Alpha2Ch01 to CfO_Alpha2Ch04
CfO_Beta1Ch01 to CfO_Beta1Ch04
CfO_Beta1Ch01 to CfO_Beta1Ch04

These registers are used to set the coefficients for the IIR filter.

Data type	Values	
DINT	-2,147,483,648 to 2,147,483,647	IIR filter coefficient. Bus controller default setting: 0

1.17.5.4.4 Physical configuration

The conversion results are scaled and filtered before being transferred to the higher-level system. To do this, the operating mode must be set for each channel.

1.17.5.4.4.1 Operating mode

Name:
CfO_ModeCh01 to CfO_ModeCh04

The operating mode for each physical channel can be configured in this register.

Data type	Values	Bus controller default setting
UINT	See the bit structure.	256

Bit structure:

Bit	Description	Value	Information
0 - 2	Connection configuration **This value must be set the same for each register!**	000	Voltage signal (bus controller default setting)
		111	Current signal
3 - 7	Reserved	0	
8 - 10	Operating mode	000	Channel disabled
		001	No filtering (bus controller default setting)
		010	2nd-order IIR (configurable Alpha and Beta coefficients)
		011	1st-order low pass (configurable limit frequency)
		100	2nd-order low pass (configurable limit frequency)
		101 to 111	Reserved
11 - 15	Reserved	0	

1.17.5.4.5 Logical configuration

The physical values can be further processed using mathematical functions and comparators. Various settings must be made for this.

1.17.5.4.5.1 Operating mode

Name:
CfO_LogCh01Mode to CfO_LogCh06Mode
"Logical configuration channel 0x / Addition" in the Automation Studio I/O configuration.
"Logical configuration channel 0x / Integral of addition" in the Automation Studio I/O configuration.
"Logical configuration channel 0x / Multiplication" in the Automation Studio I/O configuration.
"Logical configuration channel 0x / Integral of multiplication" in the Automation Studio I/O configuration.
"Logical configuration channel 0x / Channel comparator" in the Automation Studio I/O configuration.
"Logical configuration channel 0x / Hysteresis comparator" in the Automation Studio I/O configuration.
"Logical configuration channel 0x / Physical value display" in the Automation Studio I/O configuration.

The operating mode for each logical channel can be configured in this register.

The sources to be used for each logical channel are selected using the "CfO_LogCh0NSource0x" on page 431 registers. The additionally required function parameters are configured in the "CfO_LogCh0NFuncPar0x" on page 431 registers. "N" stands for the logical channel to be used; "x" stands for the source or function 0 or 1.

Data type	Value	Information
UINT	0	Channel switched off. Bus controller default setting: Channel 5 to 6
	256	Addition or physical value display[1]. Bus controller default setting: Channel1 to 4
	257	Integral of addition
	512	Multiplication
	513	Integral of multiplication
	768	Channel comparator
	1024	Hysteresis comparator

1) Only registers CfO_LogCh01Mode to CfO_LogCh04Mode are used for physical value display.

1.17.5.4.5.2 Source registers

Name:
CfO_LogCh01Source00 to CfO_LogCh06Source00
CfO_LogCh01Source01 to CfO_LogCh06Source01

These registers can be used to select the source registers for the operating mode of the logical channel configured in the register "CfO_LogCh0NMode" on page 430.
In the name, "Source00" stands for source register 0; "Source01" stands for source register 1.

In Value display in bus controller operating mode mode, the same channel number is written to both source registers.

Data type	Value	Information
USINT	0	Physical channel 01. Bus controller default setting[1)]
	...	...
	3	Physical channel 04. Bus controller default setting[1)]
	8	Logical channel 01[1)]
	...	...
	13	Logical channel 06

1) **Values**

Channels 1 to 4: Channel number - 1
Channels 5 to 6: 0

2) Logical channels cannot be used in the bus controller function model.

1.17.5.4.5.3 Additional function parameters

Name:
CfO_LogCh01FuncPar00 to CfO_LogCh06FuncPar00
CfO_LogCh01FuncPar01 to CfO_LogCh06FuncPar01

These registers can be used to store additional function parameters for the operating modes of the logical channel set in register "CfO_LogCh0NMode" on page 430.

The meaning of the function parameter varies depending on the operating mode.

Operating mode	Parameter 1	Parameter 2
(Integral of) addition	Scaling factor	Scaling factor
(Integral of) multiplication	Scaling factor	-
Channel comparator	-	-
Hysteresis comparator	Upper threshold value	Lower threshold value
Output of physical values	Fixed scaling factor = 65536	Defined scaling factor = 0

Value 65536 corresponds to scaling or a threshold value of 1.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Scaling factor or threshold value. Bus controller default setting: Register "...FuncPar00" Channels 1 to 4 65536 Channels 5 to 6 0 Register "...FuncPar01" All 0

1.17.5.5 Communication - General

The analog inputs of the module convert the current or voltage values with a resolution of 16 bits.

1.17.5.5.1 Analog inputs

Name:
AnalogInput01 to AnalogInput04

This module can be configured and operated as a normal analog input module without logical auxiliary functions. The physical values from the last sampling cycle are used as input values in this case.

Analog input values are displayed as signed 16-bit values depending on the configured operating mode.

Data type	Value	Information
INT	-32,768 to 32,767	Voltage signal ±10 VDC
	0 to 32,767	Current signal 0 to 20 mA

Information:

It is important to note that the oversampling function is not available in the bus controller function model due to the amount of data and lack of consistency!

1.17.5.5.2 Physical sampling

The module has a data buffer with 16 entries for each of the physical input channels. This buffer is processed with the set sampling cycle time.

1.17.5.5.2.1 Physical data buffer

Name:
PhysCh01Sample1 to PhysCh01Sample16
...
PhysCh04Sample1 to PhysCh04Sample16

These registers are the physical buffer registers of the analog channels. 16 registers are available for each channel. Sample 1 is the newest value; sample 16 is the oldest.

Analog input values are displayed as signed 16-bit values.

Data type	Value	Information
INT	-32,768 to 32,767	Voltage signal ±10 VDC
	0 to 32,767	Current signal 0 to 20 mA

1.17.5.5.2.2 Physical sample counter

Name:
PhysSampleCount

This register is an integer counter that is increased as soon as the module has saved a new physical sample line. The number of new sample lines is calculated from the difference to the previous cycle.

Data type	Value
SINT	-128 to 127
INT	-32,768 to 32,767

1.17.5.5.2.3 Physical timestamp

Name:
PhysTimestamp

This register returns the timestamp of the values currently being determined as signed values in µs. This data point is the timestamp of the physical sample line 1.

Data type	Values
INT	-32768 to 32767
DINT	-2,147,483,648 to 2,147,483,647

1.17.5.5.3 Logical sampling

The physical values can be further processed using mathematical functions and comparators. The module has a data buffer with 16 entries for each of the 6 logical channels.

1.17.5.5.3.1 Logical data buffer

Name:
LogicCh01Sample1 to LogicCh01Sample16
...
LogicCh06Sample1 to LogicCh06Sample16

These registers are the buffer registers of the logical input channels. 16 registers are available for each channel. Sample 1 is the newest value; sample 16 is the oldest.

The calculated values are displayed as signed 16-bit or 32-bit values depending on the register used.

Data type	Values
INT	-32768 to 32767
DINT	-2,147,483,648 to 2,147,483,647

1.17.5.5.3.2 Results 1-8 of the comparator comparison

Name:
LogicCh01Sample8_1 to LogicCh06Sample8_1

These registers are used to represent the results of samples 1 to 8 of the logical digital comparator for the logical channels. Each of these bits corresponds to a sample line, with sample 1 the newest and Sample 8 the oldest comparator comparison. The results of samples 9 to 16 are represented in register "LogicSample16_9" on page 433.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Comparator result	x	Sample 1
...	...		
7	Comparator result	x	Sample 8

1.17.5.5.3.3 Results 9-16 of the comparator comparison

Name:
LogicCh01Sample16_9 to LogicCh06Sample16_9

The results of samples 9 to 16 of the logical digital comparator of the logical channels are contained in these registers. Each of these bits corresponds to a sample line, with sample 9 the newest and sample 16 the oldest comparator comparison. The results of samples 1 to 8 are contained in register "LogicCHSample8_1" on page 433.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Comparator result	x	Sample 9
...	...		
7	Comparator result	x	Sample 16

1.17.5.5.3.4 Logical sample counter

Name:
LogicSampleCount

This register is an integer counter that is increased as soon as the module has saved a new logical sample line. The number of new sample lines is calculated from the difference to the previous cycle.

Data type	Value
SINT	-128 to 127
INT	-32,768 to 32,767

1.17.5.5.3.5 Logical timestamp

Name:
LogicTimestamp

This register provides the timestamp of the currently determined values as a signed 2-byte or 4-byte value in microseconds. This data point is the timestamp of logical sample line 1.

Data type	Values
INT	-32768 to 32767
DINT	-2,147,483,648 to 2,147,483,647

1.17.5.6 Error monitoring

The registers for displaying and acknowledging errors are transferred either cyclically or acyclically depending on the function model.

1.17.5.6.1 Enabling standard error messages

Name:
CfO_ErrorID1017
Automatic enabling by the Automation Studio I/O configuration.

This register can be used to enable the standard error messages. The composite errors of the channels are derived from the individual extended error states, e.g. underflow, overflow of the input range on the analog value. The error status of the oversampling results from a cycle time violation of the set sampling cycle time.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	63

Bit structure:

Bit	Description	Value	Information
0	Composite errors on channel 01	0	Error generation disabled
		1	Error generation enabled (bus controller default setting)
...		...	
3	Composite errors on channel 04	0	Error generation disabled
		1	Error generation enabled (bus controller default setting)
4	Physical sample error status	0	Error generation disabled
		1	Error generation enabled (bus controller default setting)
5	Logical sample error status	0	Error generation disabled
		1	Error generation enabled (bus controller default setting)
6 - 7	Reserved	0	

1.17.5.6.2 Enabling extended error messages

Name:
CfO_ErrorID0007 (for channels 1 and 2)
CfO_ErrorID080F (for channels 3 and 4)
Automatic enabling in the Automation Studio I/O configuration by selecting "Extended error status information" and channel activation.

These registers can be used to enable the extended error messages for analog channels 1 and 2 or 3 and 4.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	Channel 1 or 3: Range exceeded violation (pos.)	0	Error generation disabled (bus controller default setting)
		1	Range exceeded violation (pos.) enabled
1	Channel 1 or 3: Filter error	0	Error generation disabled (bus controller default setting)
		1	Filter error enabled
2	Channel 1 or 3: Underflow	0	Error generation disabled (bus controller default setting)
		1	Underflow enabled
3	Channel 1 or 3: Overrun	0	Error generation disabled (bus controller default setting)
		1	Overflow enabled
4	Channel 2 or 4: Range exceeded violation (pos.)	0	Error generation disabled (bus controller default setting)
		1	Range exceeded violation (pos.) enabled
5	Channel 2 or 4: Filter error	0	Error generation disabled (bus controller default setting)
		1	Filter error enabled
6	Channel 2 or 4: Underflow	0	Error generation disabled (bus controller default setting)
		1	Underflow enabled
7	Channel 2 or 4: Overrun	0	Error generation disabled (bus controller default setting)
		1	Overflow enabled

1.17.5.6.3 Composite error

Name:
Channel01Error to Channel04Error
PhysicalError
LogicalError

Composite errors are mapped to this register.

All configured physical and logical oversampling functions must be able to be carried out in the configured sampling cycle time; otherwise, these error messages will be displayed. The system can be further adjusted with settings for the processing priority and the prescaler for logical oversampling.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01Error	0	No error
		1	Composite errors on channel 1
...		...	
3	Channel04Error	0	No error
		1	Composite errors on channel 4
4	PhysicalError	0	No error
		1	Physical sample error status, sampling cycle time too short
5	LogicalError	0	No error
		1	Logical sample error status, sampling cycle time too short or prescaler configured too low

1.17.5.6.4 Acknowledging standard errors

Name:
AckChannel01Error to AckChannel04Error
AckPhysicalError
AckLogicalError

In this register, error messages from register "Composite error" on page 435 can be acknowledged by setting the corresponding bits.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	AckChannel01Error	0	No change
		1	Acknowledge error
...		...	
3	AckChannel04Error	0	No change
		1	Acknowledge error
4	AckPhysicalError	0	No change
		1	Acknowledge error
5	AckLogicalError	0	No change
		1	Acknowledge error

1.17.5.6.5 Extended channel error messages

Name:
Channel01OutOfRange to Channel04OutOfRange
Channel01FilterError to Channel04FilterError
Channel01Underflow to Channel04Underflow
Channel01Overflow to Channel04Overflow

The error states of the input channels are represented in these registers. Input channels 1 and 2 as well as 3 and 4 are each grouped together in one register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01OutOfRange or Channel03OutOfRange	0	No error
		1	Range exceeded violation (pos.) occurred
1	Channel01FilterError or Channel03FilterError	0	No error
		1	Filter error occurred
2	Channel01Underflow or Channel03underflow	0	No error
		1	Underflow occurred
3	Channel01Overflow or Channel03Overflow	0	No error
		1	Overflow occurred
4	Channel02OutOfRange or Channel04OutOfRange	0	No error
		1	Range exceeded violation (pos.) occurred
5	Channel02FilterError or Channel04FilterError	0	No error
		1	Filter error occurred
6	Channel02Underflow or Channel04Underflow	0	No error
		1	Underflow occurred
7	Channel02Overflow or Channel04Overflow	0	No error
		1	Overflow occurred

1.17.5.6.6 Acknowledging extended channel error messages

Name:
AckChannel01OutOfRange to AckChannel04OutOfRange
AckChannel01FilterError to AckChannel04FilterError
AckChannel01Underflow to AckChannel04Underflow
AckChannel01Overflow to AckChannel04Overflow

These registers can be used to acknowledge the error messages from the "ExtendedChannelErrorMessages" on page 436 registers by setting the corresponding bit. The acknowledgment of input channels 1 and 2 as well as 3 and 4 are each grouped together in one register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	AckChannel01OutOfRange or AckChannel03OutOfRange	0	No change
		1	Acknowledge error
1	AckChannel01FilterError or AckChannel03FilterError	0	No change
		1	Acknowledge error
2	AckChannel01Underflow or AckChannel03Underflow	0	No change
		1	Acknowledge error
3	AckChannel01Overflow or AckChannel03Overflow	0	No change
		1	Acknowledge error
4	AckChannel02OutOfRange or AckChannel04OutOfRange	0	No change
		1	Acknowledge error
5	AckChannel02FilterError or AckChannel04FilterError	0	No change
		1	Acknowledge error
6	AckChannel02Underflow or AckChannel04Underflow	0	No change
		1	Acknowledge error
7	AckChannel02Overflow or AckChannel04Overflow	0	No change
		1	Acknowledge error

1.17.5.7 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

1.17.5.8 Minimum I/O update time

There is no limitation or dependency on the bus cycle time.

The I/O update time is defined using the "Sampling time" register. The fastest possible sampling time depends on the number of channels to be converted and the configuration.

1.18 X20AI8221

1.18.1 General information

The module is equipped with 8 inputs with 13-bit (including sign) digital converter resolution. It can be used to capture voltage signals in the range from ±10 V.

- 8 analog inputs ±10 V
- 13-bit digital converter resolution

1.18.2 Order data

Order number	Short description	Figure
	Analog inputs	
X20AI8221	X20 analog input module, 8 inputs, ±10 V, 13-bit converter resolution	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB1F	X20 terminal block, 16-pin, 24 VDC keyed	

Table 63: X20AI8221 - Order data

1.18.3 Technical data

Order number	X20AI8221
Short description	
I/O module	8 analog inputs ±10 V
General information	
B&R ID code	0xD82F
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1.04 W [1]
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
EAC	Yes
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
DNV GL	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
LR	ENV1
KR	Yes
Analog inputs	
Input	±10 V
Input type	Differential input
Digital converter resolution	±12-bit
Conversion time	1 ms for all inputs
Output format	
Data type	INT
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0008 = 2.441 mV
Input impedance in signal range	20 MΩ
Input protection	Protection against wiring with supply voltage
Open-circuit detection	Yes, using software
Reverse polarity protection	Yes
Permissible input signal	Max. ±30 V
Output of digital value during overload	Configurable
Conversion procedure	SAR
Input filter	3rd-order low pass / cutoff frequency 1 kHz
Max. error at 25°C	
Gain	0.08% [2]
Offset	0.015% [3]
Max. gain drift	0.006 %/°C [2]
Max. offset drift	0.002 %/°C [3]
Common-mode rejection	
DC	70 dB
50 Hz	70 dB
Common-mode range	±12 V
Crosstalk between channels	-70 dB
Nonlinearity	<0.025% [3]
Isolation voltage between channel and bus	500 VDC, 1 min
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20

Table 64: X20AI8221 - Technical data

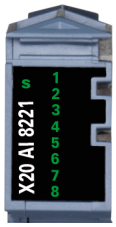
Order number	X20AI8221
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x X20TB1F terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5$^{+0.2}$ mm

Table 64: X20AI8221 - Technical data

1) To reduce power dissipation, B&R recommends bridging unused inputs on the terminals.
2) Based on the current measured value.
3) Based on the 20 V measurement range.

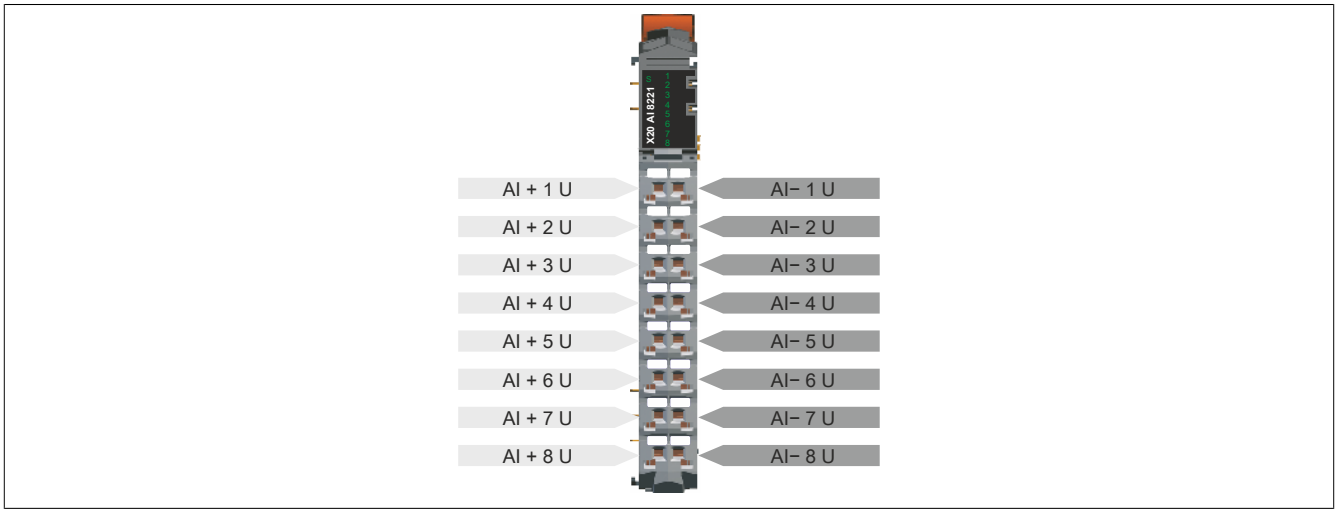
1.18.4 LED status indicators

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 system user's manual.

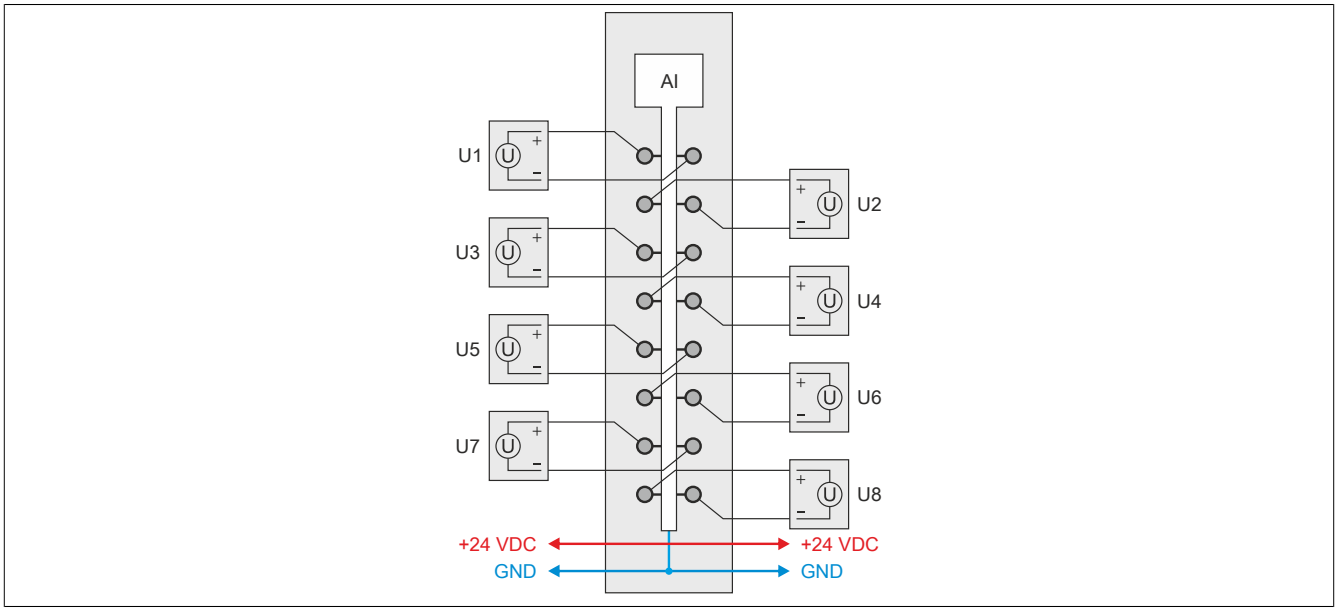
Figure	LED	Color	Status	Description
	S	Green	Off	No power to module
			Single flash	UNLINK mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking quickly	SYNC mode
			Blinking slowly	PREOPERATIONAL mode
			On	RUN mode
		Red	Off	No power to module or everything OK
			On	Error or reset status
	1 - 8	Green	Off	Indicates one of the following cases: • No power to module • Open line
			Single flash	Input signal overflow or underflow
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.

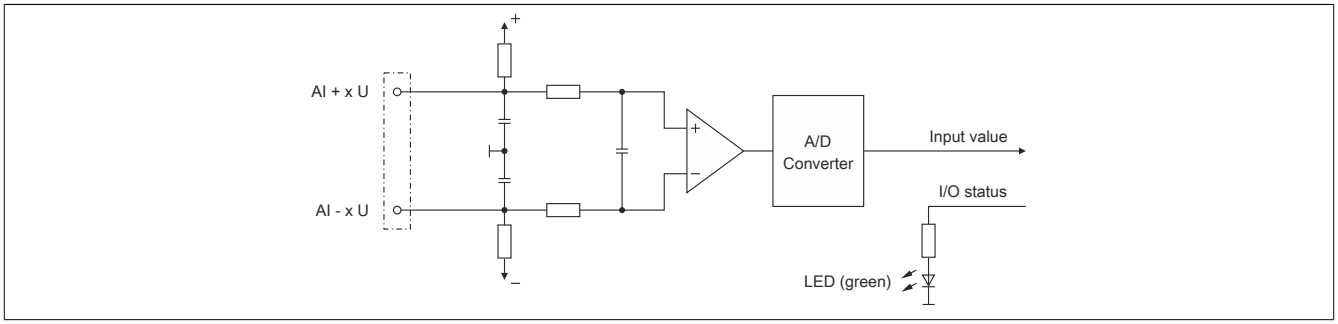
1.18.5 Pinout



1.18.6 Connection example



1.18.7 Input circuit diagram



1.18.8 Register description

1.18.8.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 system user's manual.

1.18.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration						
16	ConfigOutput01 (Input filter)	USINT				•
20	ConfigOutput03 (Lower limit value)	INT				•
22	ConfigOutput04 (Upper limit value)	INT				•
Analog signal - Communication						
Index * 2 - 2	AnalogInput0N (Index N = 1 to 8)	INT	•			
30	StatusInput01	USINT	•			
31	StatusInput02	USINT	•			

1.18.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration							
16	-	ConfigOutput01 (Input filter)	USINT				•
20	-	ConfigOutput03 (Lower limit value)	INT				•
22	-	ConfigOutput04 (Upper limit value)	INT				•
Analog signal - Communication							
Index * 2 - 2	Index * 2 - 2	AnalogInput0N (Index N = 1 to 8)	INT	•			
30	-	StatusInput01	USINT		•		
31	-	StatusInput02	USINT		•		

1) The offset specifies the position of the register within the CAN object.

1.18.8.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

1.18.8.3.2 CAN I/O bus controller

The module occupies 2 analog logical slots on CAN I/O.

1.18.8.4 Analog inputs

Input signals are converted asynchronously in a 1 ms interval.

1.18.8.5 Analog input values

Name:
AnalogInput01 to AnalogInput08

The analog input values are mapped to this register.

Data type	Value	Input signal:
INT	-32,768 to 32,767	Voltage signal -10 to 10 VDC

1.18.8.6 Input filter

This module is equipped with a configurable input filter.

Information:

The filter sampling time is fixed at 1 ms and is acyclic to the X2X cycle.

1.18.8.6.1 Input ramp limiting

Input ramp limiting can only be performed in conjunction with filtering. Input ramp limiting is performed before filtering.

The difference of the input value change is checked for exceeding the specified limit. In the event of overshoot, the tracked input value is equal to the old value ± the limit value.

Configurable limit values:

Value	Limit value
0	The input value is used without limitation.
1	0x3FFF = 16383
2	0x1FFF = 8191
3	0x0FFF = 4095
4	0x07FF = 2047
5	0x03FF = 1023
6	0x01FF = 511
7	0x00FF = 255

Input ramp limiting is well suited for suppressing disturbances (spikes). The following examples show the functionality of input ramp limiting based on an input step and a disturbance.

Example 1

The input value jumps from 8000 to 17000. The diagram shows the tracked input value with the following settings:

Input ramp limiting = 4 = 0x07FF = 2047

Filter level = 2

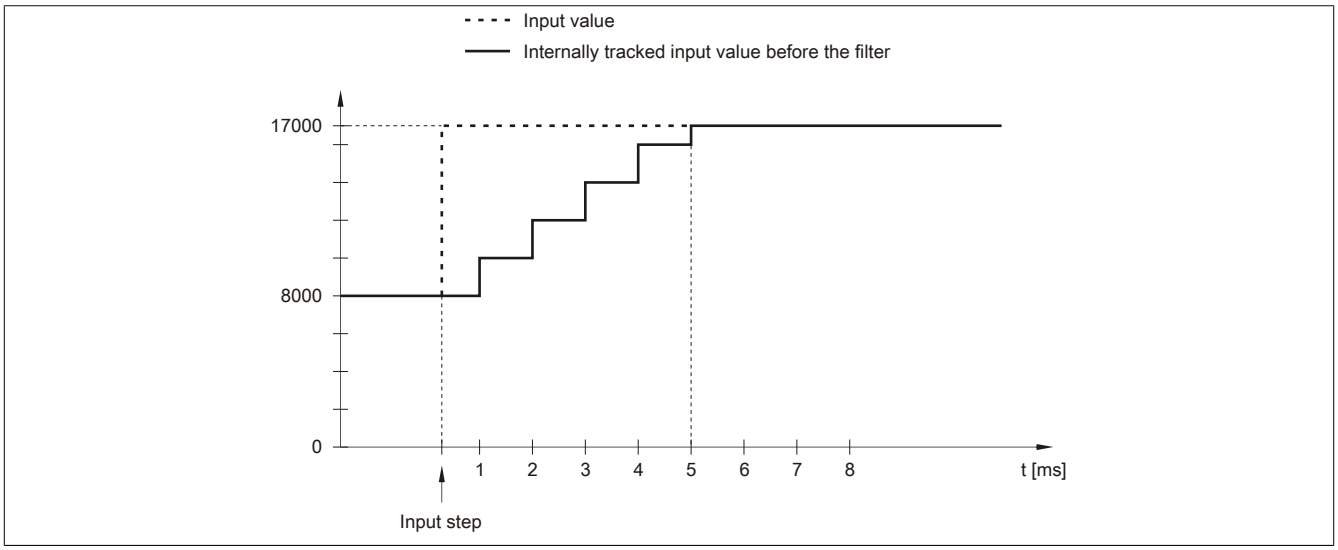


Figure 47: Tracked input value for input step

Example 2

A disturbance interferes with the input value. The diagram shows the tracked input value with the following settings:

Input ramp limiting = 4 = 0x07FF = 2047

Filter level = 2

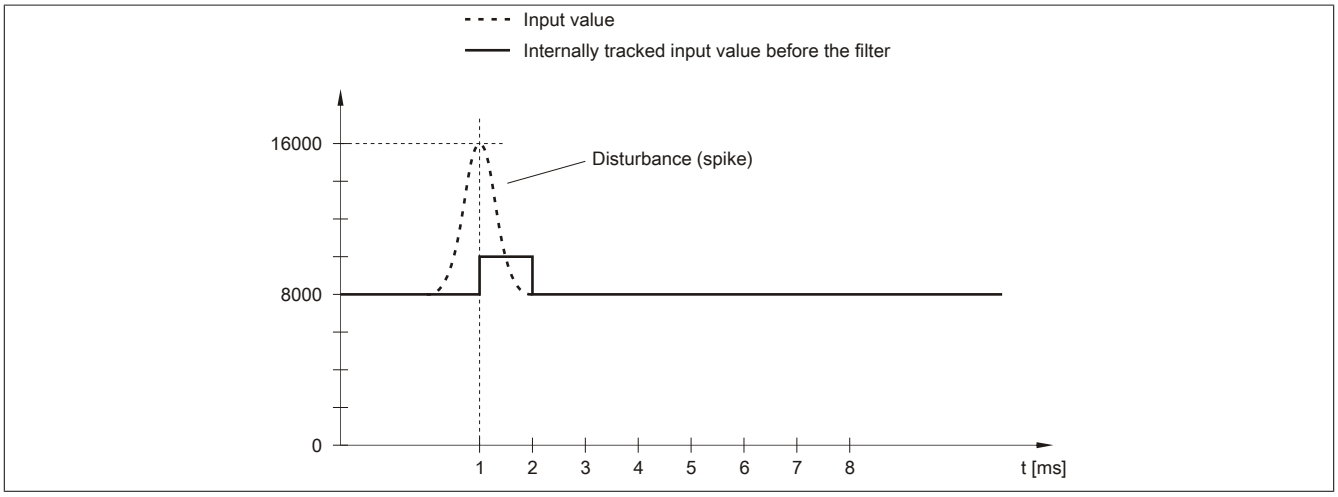


Figure 48: Tracked input value for disturbance

1.18.8.6.2 Filter level

A filter can be defined to prevent large input steps. This filter is used to bring the input value closer to the actual analog value over a period of several milliseconds.
Filtering takes place after any input ramp limiting has been carried out.

Formula for calculating the input value:

$$\text{Value}_{\text{New}} = \text{Value}_{\text{Old}} - \frac{\text{Value}_{\text{Old}}}{\text{Filter level}} + \frac{\text{Input value}}{\text{Filter level}}$$

Adjustable filter levels:

Value	Filter level
0	Filter switched off
1	Filter level 2
2	Filter level 4
3	Filter level 8
4	Filter level 16
5	Filter level 32
6	Filter level 64
7	Filter level 128

The following examples show the functionality of the filter based on an input step and a disturbance.

Example 1

The input value jumps from 8000 to 16000. The diagram shows the calculated value with the following settings:

Input ramp limiting = 0

Filter level = 2 or 4

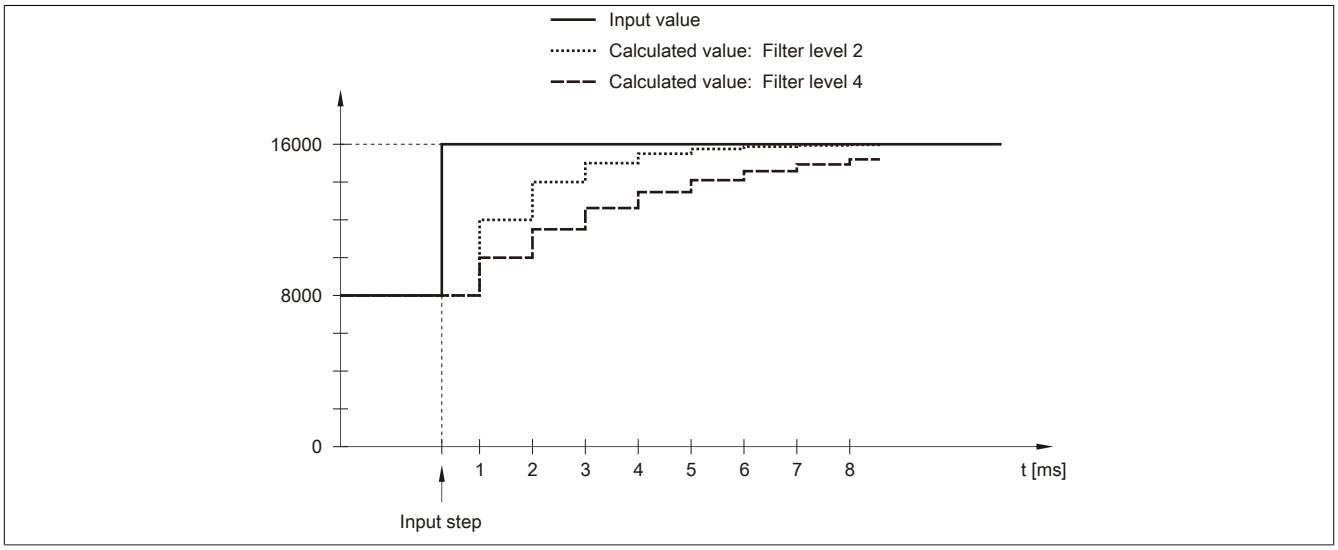


Figure 49: Calculated value during input step

Example 2

A disturbance interferes with the input value. The diagram shows the calculated value with the following settings:

Input ramp limiting = 0

Filter level = 2 or 4

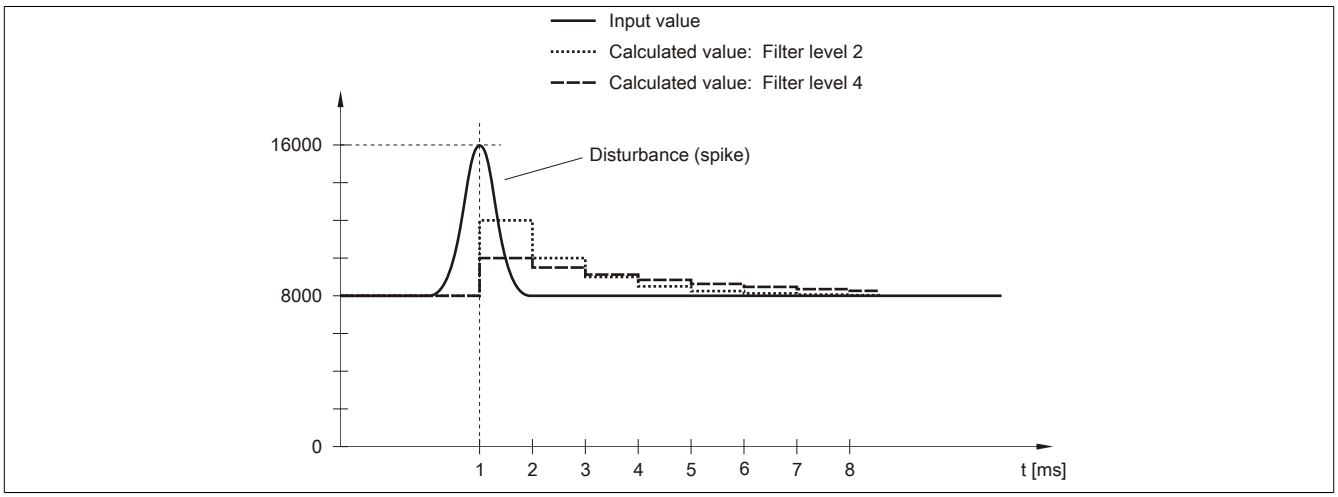


Figure 50: Calculated value during disturbance

1.18.8.7 Configuring the input filter

Name:
ConfigOutput01

This register is used to define the filter level and input ramp limitation of the input filter.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter disabled (bus controller default setting)
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines the input ramp limitation	000	The input value is applied without limitation (bus controller default setting)
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7 - 15	Reserved	0	

1.18.8.8 Lower limit value

Name:
ConfigOutput03

The lower limit value for analog values can be set in this register. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Values	Information
INT	-32767 to 32767	Bus controller default setting: -32767

Information:

The default value of -32767 corresponds to the minimum default value of -10 VDC.

It is important to note that this setting applies to all channels!

1.18.8.9 Upper limit value

Name:
ConfigOutput04

The upper limit value for analog values can be set in this register. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Values	Information
INT	-32767 to 32767	Bus controller default setting: 32767

Information:

Default value 32767 corresponds to the maximum default value at +10 VDC.

It is important to note that this setting applies to all channels!

1.18.8.10 Input status

Name:
StatusInput01 to StatusInput02

This register is used to monitor the module inputs. A change in the monitoring status generates an error message.

Data type	Values
USINT	See the bit structure.

Bit structure:

StatusInput01 monitors Channels 1 to 4
StatusInput02 monitors Channels 5 to 8

Bit	Description	Value	Information
0 - 1	Channel 1 or 5	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line
...		...	
6 - 7	Channel 4 or 8	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
		11	Open line

Limiting the analog value

In addition to the status information, the analog value is fixed to the values listed below by default in an error state. The analog value is limited to the new values if the limit values were changed.

Error state	Digital value on error (default values)
Open circuit	+32767 (0x7FFF)
Upper limit value overshot	+32767 (0x7FFF)
Lower limit value undershot	-32767 (0x8001)
Invalid value	-32768 (0x8000)

1.18.8.11 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
150 µs

1.18.8.12 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time
1 ms

1.19 X20AI8321

1.19.1 General information

The module is equipped with 8 inputs with 12-bit digital converter resolution. It is possible to select between the two current ranges 0 to 20 mA and 4 to 20 mA.

- 8 analog inputs, 0 to 20 mA or 4 to 20 mA
- 12-bit digital converter resolution

1.19.2 Order data

Order number	Short description	Figure
	Analog inputs	
X20AI8321	X20 analog input module, 8 inputs, 0 to 20 mA, 12-bit converter resolution	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB1F	X20 terminal block, 16-pin, 24 VDC keyed	

Table 65: X20AI8321 - Order data

1.19.3 Technical data

Order number	X20AI8321
Short description	
I/O module	8 analog inputs 0 to 20 mA / 4 to 20 mA
General information	
B&R ID code	0xD831
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Inputs	Yes, using status LED and software
Power consumption	
Bus	0.01 W
Internal I/O	1.37 W (Rev. ≥ D0), 1.24 W (Rev. < D0)
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
EAC	Yes
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
DNV GL	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
LR	ENV1
KR	Yes
Analog inputs	
Input	0 to 20 mA/4 to 20 mA
Input type	Differential input
Digital converter resolution	12-bit
Conversion time	1 ms for all inputs
Output format	
Data type	INT
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0008 = 4.883 µA
Load	<300 Ω
Input protection	Protection against wiring with supply voltage
Reverse polarity protection	Yes
Permissible input signal	Max. ±50 mA
Output of digital value during overload	Configurable
Conversion procedure	SAR
Input filter	3rd-order low pass / cutoff frequency 1 kHz
Max. error at 25°C	
Gain	0.08% [1)]
Offset	0.03% [2)]
Max. gain drift	0.009 %/°C [1)]
Max. offset drift	0.005 %/°C [2)]
Common-mode rejection	
DC	70 dB
50 Hz	70 dB
Common-mode range	±12 V
Crosstalk between channels	-70 dB
Nonlinearity	<0.05% [2)]
Isolation voltage between channel and bus	500 VDC, 1 min
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20

Table 66: X20AI8321 - Technical data

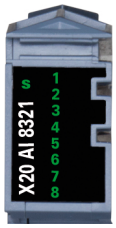
Order number	X20AI8321
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x X20TB1F terminal block separately Order 1x X20BM11 bus module separately
Spacing	12.5$^{+0.2}$ mm

Table 66: X20AI8321 - Technical data

1) Based on the current measured value.
2) Based on the 20 mA measurement range.

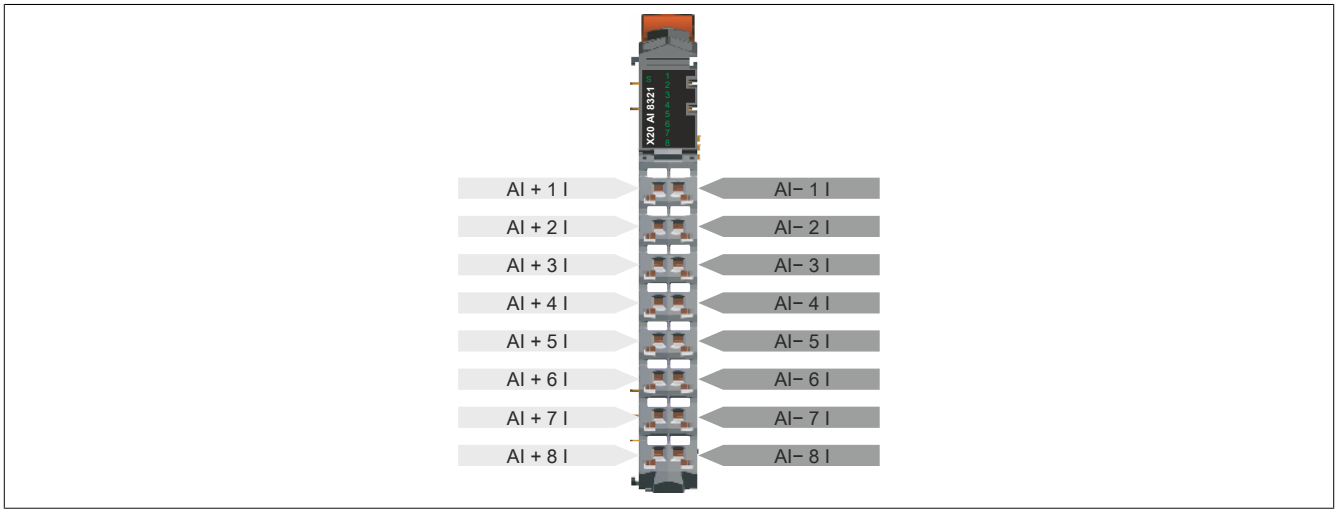
1.19.4 LED status indicators

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 system user's manual.

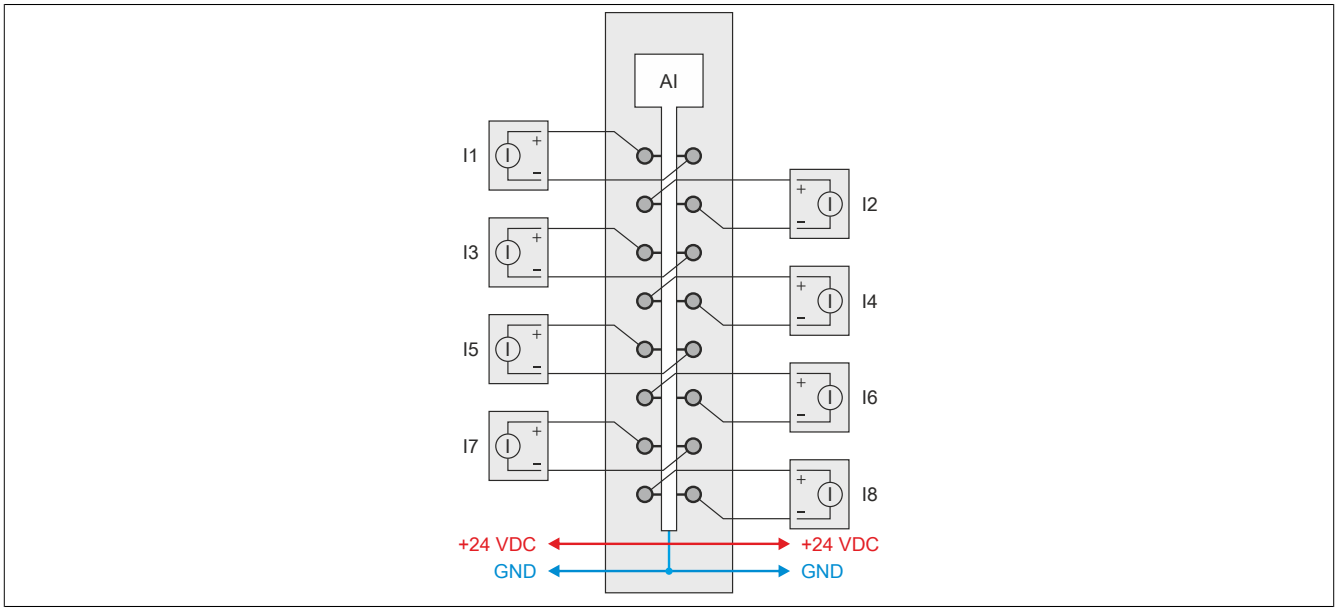
Figure	LED	Color	Status	Description
	S	Green	Off	No power to module
			Single flash	UNLINK mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking quickly	SYNC mode
			Blinking slowly	PREOPERATIONAL mode
			On	RUN mode
		Red	Off	No power to module or everything OK
			On	Error or reset status
	1 - 8	Green	Off	No power to module
			Single flash	Input signal overflow or underflow
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.

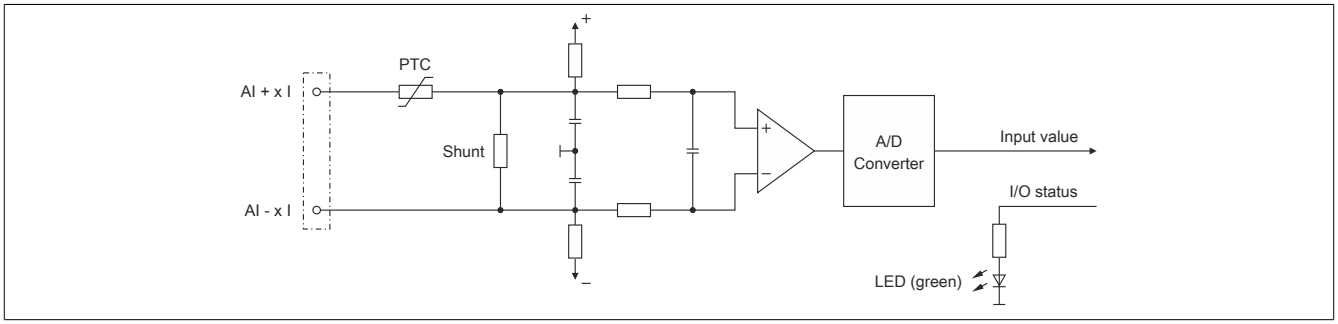
1.19.5 Pinout



1.19.6 Connection example



1.19.7 Input circuit diagram



1.19.8 Register description

1.19.8.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 system user's manual.

1.19.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration						
16	ConfigOutput01 (Input filter)	USINT				•
18	ConfigOutput02 (Channel type)	UINT				•
20	ConfigOutput03 (Lower limit value)	INT				•
22	ConfigOutput04 (Upper limit value)	INT				•
Analog signal - Communication						
Index * 2 - 2	AnalogInput0N (Index N = 1 to 8)	INT	•			
30	StatusInput01	USINT	•			
31	StatusInput02	USINT	•			

1.19.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration							
16	-	ConfigOutput01 (Input filter)	USINT				•
18	-	ConfigOutput02 (Channel type)	UINT				•
20	-	ConfigOutput03 (Lower limit value)	INT				•
22	-	ConfigOutput04 (Upper limit value)	INT				•
Analog signal - Communication							
Index * 2 - 2	Index * 2 - 2	AnalogInput0N (Index N = 1 to 8)	INT	•			
30	-	StatusInput01	USINT		•		
31	-	StatusInput02	USINT		•		

1) The offset specifies the position of the register within the CAN object.

1.19.8.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

1.19.8.3.2 CAN I/O bus controller

The module occupies 2 analog logical slots on CAN I/O.

1.19.8.4 Analog inputs

Input signals are converted asynchronously in a 1 ms interval.

1.19.8.5 Analog input values

Name:
AnalogInput01 to AnalogInput08

The analog input values are mapped to this register.

Data type	Value	Input signal:
INT	0 to 32767	Current signal 0 to 20 mA or 4 to 20 mA

1.19.8.6 Input filter

This module is equipped with a configurable input filter.

Information:

The filter sampling time is fixed at 1 ms and is acyclic to the X2X cycle.

1.19.8.6.1 Input ramp limiting

Input ramp limiting can only be performed in conjunction with filtering. Input ramp limiting is performed before filtering.

The difference of the input value change is checked for exceeding the specified limit. In the event of overshoot, the tracked input value is equal to the old value ± the limit value.

Configurable limit values:

Value	Limit value
0	The input value is used without limitation.
1	0x3FFF = 16383
2	0x1FFF = 8191
3	0x0FFF = 4095
4	0x07FF = 2047
5	0x03FF = 1023
6	0x01FF = 511
7	0x00FF = 255

Input ramp limiting is well suited for suppressing disturbances (spikes). The following examples show the functionality of input ramp limiting based on an input step and a disturbance.

Example 1

The input value jumps from 8000 to 17000. The diagram shows the tracked input value with the following settings:

Input ramp limiting = 4 = 0x07FF = 2047

Filter level = 2

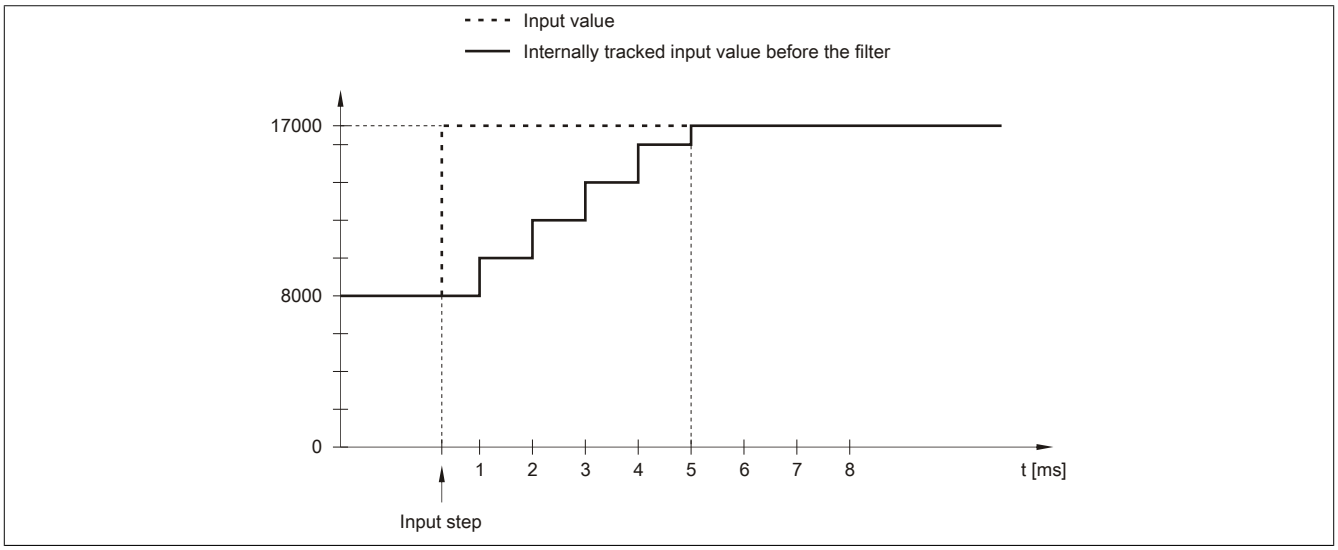


Figure 51: Tracked input value for input step

Example 2

A disturbance interferes with the input value. The diagram shows the tracked input value with the following settings:

Input ramp limiting = 4 = 0x07FF = 2047

Filter level = 2

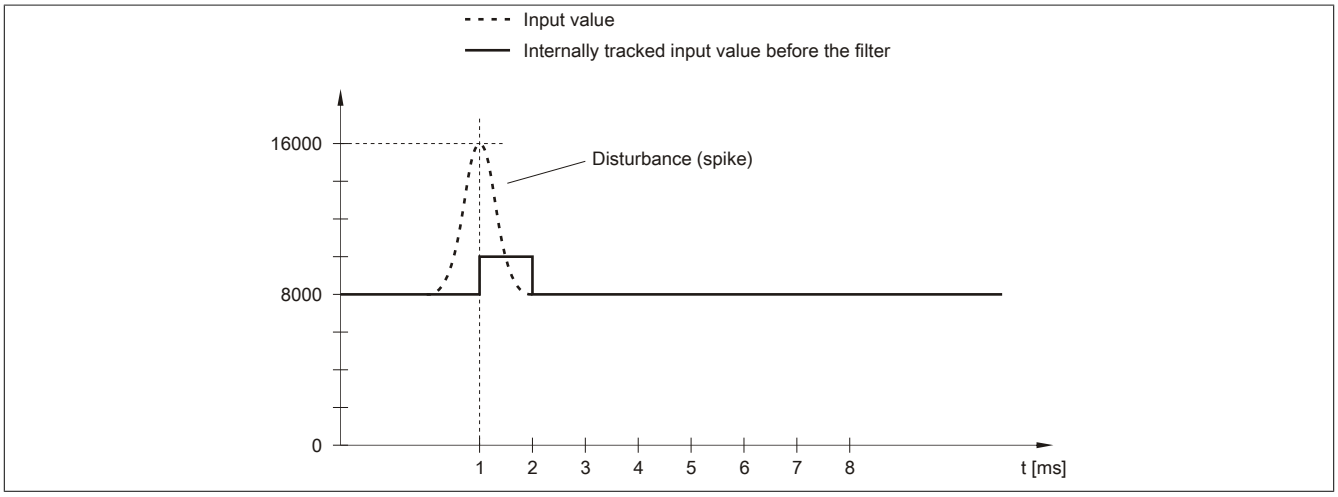


Figure 52: Tracked input value for disturbance

1.19.8.6.2 Filter level

A filter can be defined to prevent large input steps. This filter is used to bring the input value closer to the actual analog value over a period of several milliseconds.
Filtering takes place after any input ramp limiting has been carried out.

Formula for calculating the input value:

$$\text{Value}_{\text{New}} = \text{Value}_{\text{Old}} - \frac{\text{Value}_{\text{Old}}}{\text{Filter level}} + \frac{\text{Input value}}{\text{Filter level}}$$

Adjustable filter levels:

Value	Filter level
0	Filter switched off
1	Filter level 2
2	Filter level 4
3	Filter level 8
4	Filter level 16
5	Filter level 32
6	Filter level 64
7	Filter level 128

The following examples show the functionality of the filter based on an input step and a disturbance.

Example 1

The input value jumps from 8000 to 16000. The diagram shows the calculated value with the following settings:

Input ramp limiting = 0

Filter level = 2 or 4

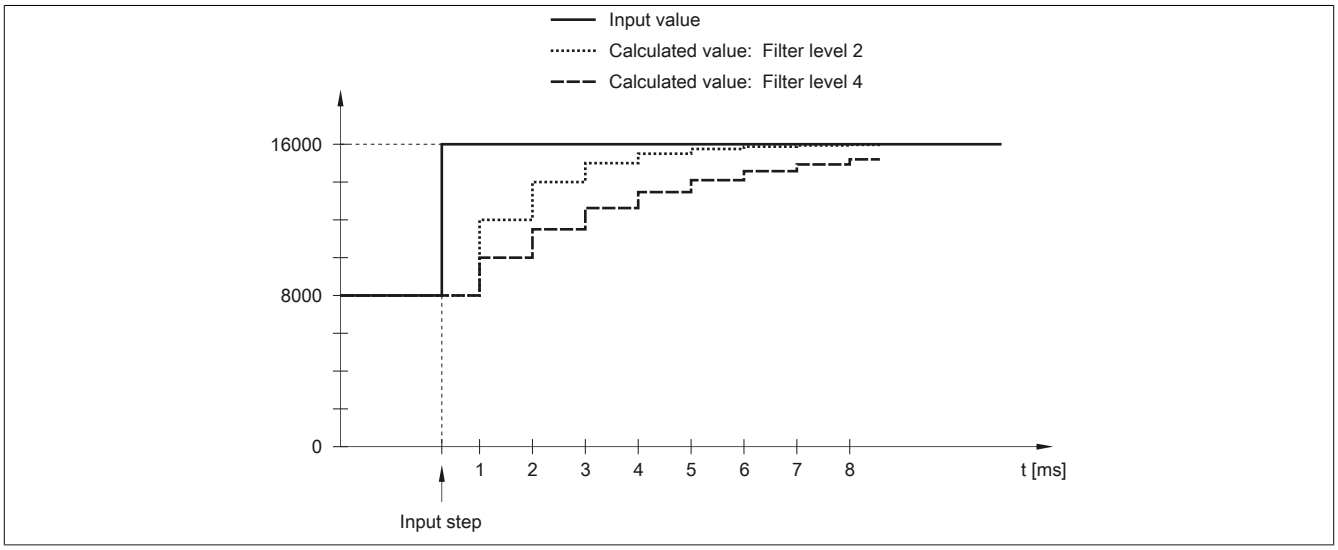


Figure 53: Calculated value during input step

Example 2

A disturbance interferes with the input value. The diagram shows the calculated value with the following settings:

Input ramp limiting = 0

Filter level = 2 or 4

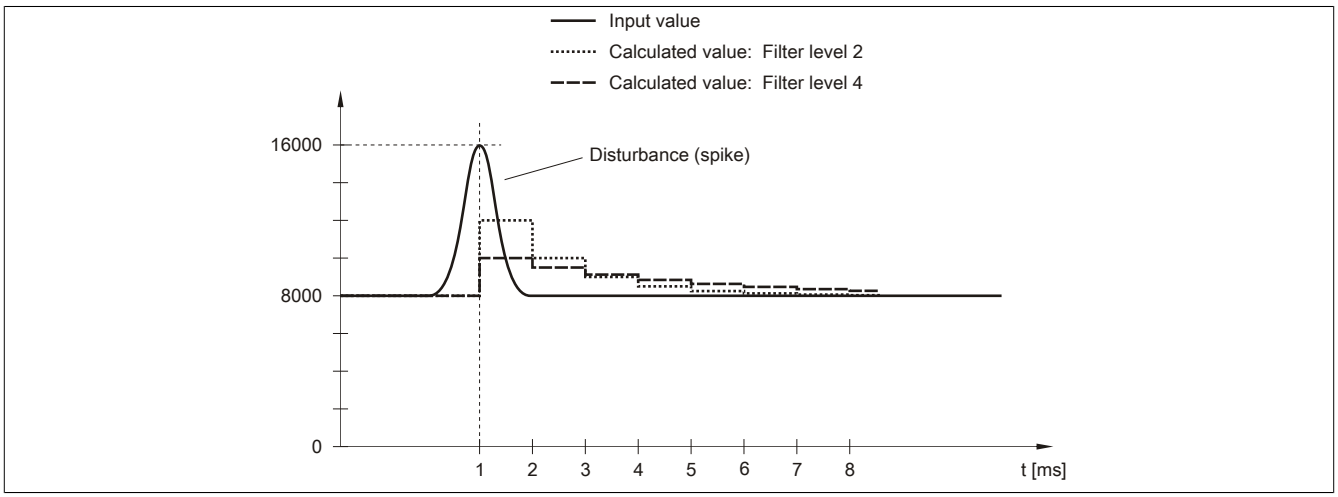


Figure 54: Calculated value during disturbance

1.19.8.7 Configuring the input filter

Name:
ConfigOutput01

This register is used to define the filter level and input ramp limitation of the input filter.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0 - 2	Defines the filter level	000	Filter disabled (bus controller default setting)
		001	Filter level 2
		010	Filter level 4
		011	Filter level 8
		100	Filter level 16
		101	Filter level 32
		110	Filter level 64
		111	Filter level 128
3	Reserved	0	
4 - 6	Defines the input ramp limitation	000	The input value is applied without limitation (bus controller default setting)
		001	Limit value = 0x3FFF (16383)
		010	Limit value = 0x1FFF (8191)
		011	Limit value = 0x0FFF (4095)
		100	Limit value = 0x07FF (2047)
		101	Limit value = 0x03FF (1023)
		110	Limit value = 0x01FF (511)
		111	Limit value = 0x00FF (255)
7 - 15	Reserved	0	

1.19.8.8 Channel type

Name:
ConfigOutput02

This register can be used to set the range of the current signal. This is determined by how they are configured. The following input signals can be set:

- 0 to 20 mA current signal
- 4 to 20 mA current signal

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	Channel 1: Current measurement range	0	0 to 20 mA current signal (bus controller default setting)
		1	4 to 20 mA current signal
...		...	
7	Channel 8: Current measurement range	0	0 to 20 mA current signal (bus controller default setting)
		1	4 to 20 mA current signal

1.19.8.9 Lower limit value

Name:
ConfigOutput03

This register can be used to configure the lower limit for analog values. If the analog value goes below the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Values	Information
INT	-32768 to 32767	Bus controller default setting: -32767

Information:

- **When configured as 0 to 20 mA, this value should be set to 0.**
- **When configured as 4 to 20 mA, this value can be set to -8192 (corresponds to 0 mA) in order to display values <4 mA.**

Keep in mind that this setting applies to all channels!

1.19.8.10 Upper limit value

Name:
ConfigOutput04

This register can be used to configure the upper limit for analog values. If the analog value goes above the limit value, it is frozen at this value and the corresponding error status bit is set.

Data type	Values	Information
INT	-32768 to 32767	Bus controller default setting: 32767

Information:

The default value of 32767 corresponds to the maximum default value at 20 mA.

Keep in mind that this setting applies to all channels!

1.19.8.11 Input status

Name:
StatusInput01 to StatusInput02

This register is used to monitor the module inputs. A change in the monitoring status generates an error message.

Data type	Values
USINT	See the bit structure.

Bit structure:

StatusInput01 monitors Channels 1 to 4
StatusInput02 monitors Channels 5 to 8

Bit	Description	Value	Information
0 - 1	Channel 1 or 5	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded
...		...	
6 - 7	Channel 4 or 8	00	No error
		01	Lower limit value exceeded
		10	Upper limit value exceeded

Limiting the analog value

In addition to the status information, the analog value is set to the values listed below by default when an error occurs. The analog value is limited to the new values if the limit values were changed.

Error status	Digital value for error (default values)	
	0 to 20 mA	4 to 20 mA
Upper limit value exceeded	+32767 (0x7FFF)	
Lower limit value exceeded	0	-8191 (0xE001)

1.19.8.12 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
150 µs

1.19.8.13 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time
1 ms

1.20 X20AIA744

1.20.1 General information

This module works with 4-wire strain gauge load cells. The concept applied by the module requires compensation in the measurement system. This compensation eliminates the absolute uncertainty in the measurement circuit, such as component tolerances, effective bridge voltage or zero offset. The measurement precision refers to the absolute (compensated) value, which will only change as a result of changes in the operating temperature.

- 2 full-bridge strain gauge inputs
- 5 kHz data output rate for both channels
- Independently configurable strain gauge factor and filter level for each of the 2 channels

1.20.1.1 Other applicable documents

For additional and supplementary information, see the following documents.

Other applicable documents

Document name	Title
MAX20	X20 System user's manual
MAEMV	Installation / EMC guide

1.20.2 Order data

Order number	Short description	Figure
	Analog inputs	
X20AIA744	X20 analog input module, 2 full-bridge strain inputs, 24-bit converter resolution, 2.5 kHz input filter	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB1F	X20 terminal block, 16-pin, 24 VDC keyed	

Table 67: X20AIA744 - Order data

1.20.3 Technical description

1.20.3.1 Technical data

Order number	X20AIA744
Short description	
I/O module	2 full-bridge strain gauge inputs
General information	
B&R ID code	0xE50C
Status indicators	Channel status, operating state, module status
Diagnostics	
Module run/error	Yes, using LED status indicator and software
Open circuit	Yes, using LED status indicator and software
Input	Yes, using LED status indicator and software
Power consumption	
Bus	0.01 W
Internal I/O	0.7 W
Additional power dissipation caused by actuators (resistive) [W]	+0.72 [1)]
Certifications	
CE	Yes
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
UL	cULus E115267 Industrial control equipment
EAC	Yes
Full-bridge strain gauge	
Strain gauge factor	2 to 256 mV/V, configurable using software
Connection	4-wire connections
Input type	Differential, used to evaluate a full-bridge strain gauge
Digital converter resolution	24-bit
Conversion time	200 µs
Data output rate	5000 samples per second and per channel (f_{DATA})
Input filter	
Cutoff frequency	2.5 kHz
Order	3
Slope	60 dB
ADC filter characteristics	Sigma-delta, see section "Filter"
Operating range / Measurement sensor	85 to 5000 Ω
Influence of cable length	Twisted and shielded conductors, cable length as short as possible, cable routing separate from load circuits, without intermediate terminal to sensor
Input protection	RC protection
Common-mode range	0.6 to 3.8 VDC Permissible input voltage range (with regard to the electric potential strain gauge GND) on inputs "Input +" and "Input -"
Insulation voltage between input and bus	500 V_{eff}
Conversion procedure	Sigma-delta
Output of digital value	
Broken bridge supply line	Value approaching 0
Broken sensor line	Value approaching ±end value (status bit "Open circuit" set in register "Module status")
Valid range of values	0xFF800001 to 0x007FFFFF (-8,388,607 to 8,388,607)
Strain gauge supply	
Voltage	5.5 VDC / Max. 65 mA per channel
Short-circuit and overload-proof	Yes
Quantization [2)]	
LSB value	
2 mV/V	1.31 nV
4 mV/V	2.62 nV
8 mV/V	5.25 nV
16 mV/V	10.49 nV
32 mV/V	20.98 nV
64 mV/V	41.96 nV
128 mV/V	83.92 nV
256 mV/V	167.85 nV
Max. gain drift	35 ppm/°C [3)]
Max. offset drift	15 ppm/°C [4)]
Nonlinearity	<10 ppm [4)]
Electrical properties	
Electrical isolation	Bus isolated from analog input and strain gauge supply voltage Channel not isolated from channel and I/O power supply

Table 68: X20AIA744 - Technical data

Order number	X20AIA744
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	See section "Hardware configuration"
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x terminal block X20TB1F separately. Order 1x bus module X20BM11 separately.
Pitch	12.5$^{+0.2}$ mm

Table 68: X20AIA744 - Technical data

1) Depends on the full-bridge strain gauge being used.
2) Quantization depends on the strain gauge factor.
3) Based on the current measured value.
4) Based on the entire measurement range.

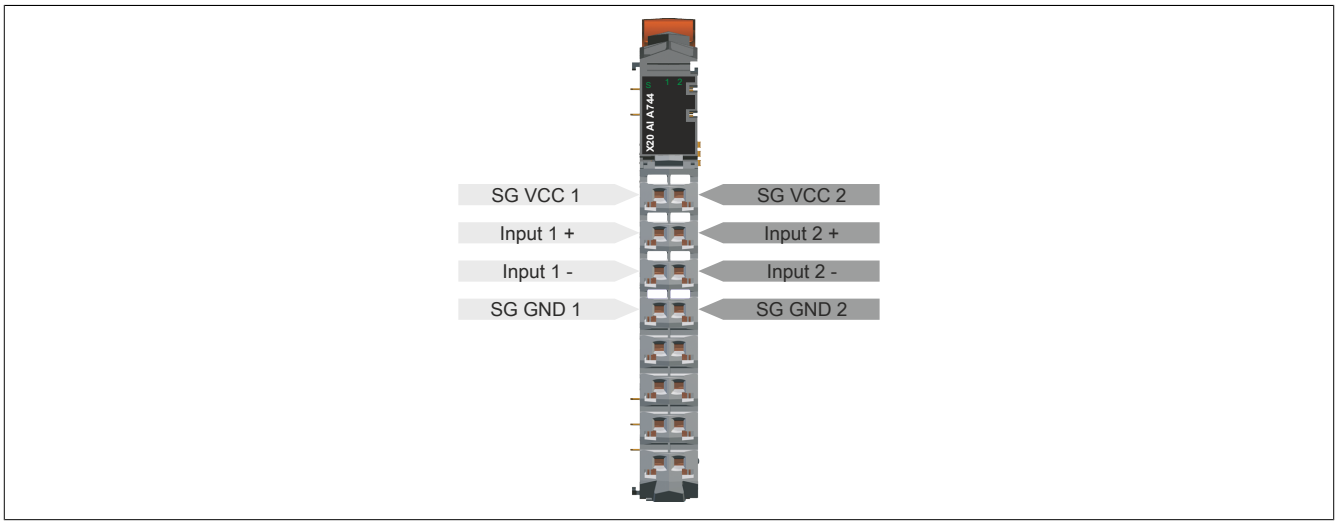
1.20.3.2 LED status indicators

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 System user's manual.

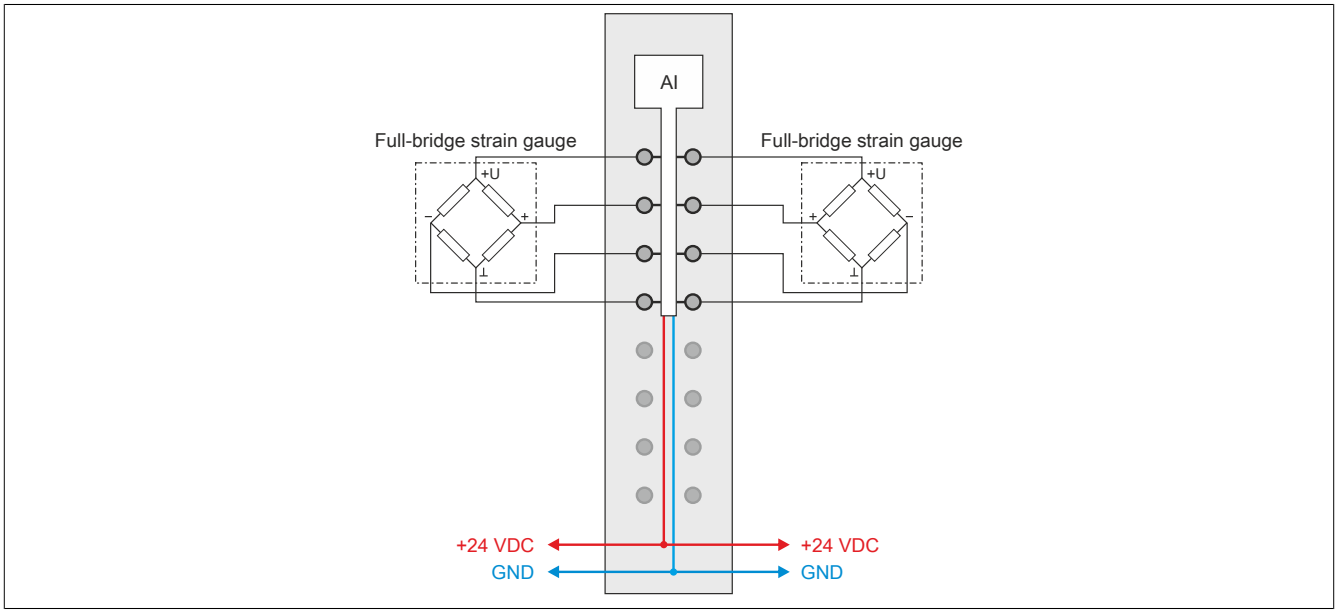
Figure	LED	Color	Status	Description
	S	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
		Red	Off	No power to module or everything OK
			Double flash	I/O supply outside limits
			On	Error or reset status
	1 - 2	Green	Off	Possible causes: • Supply error • Channel not yet configured
			Blinking	Possible causes: • Open line • Overvoltage • Undervoltage
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.

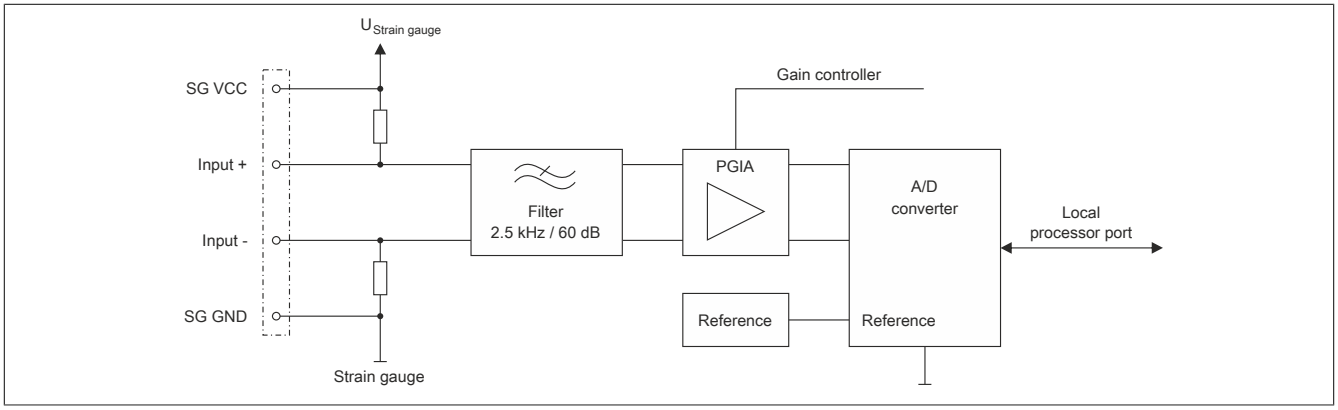
1.20.3.3 Pinout



1.20.3.4 Connection example



1.20.3.5 Input circuit diagram

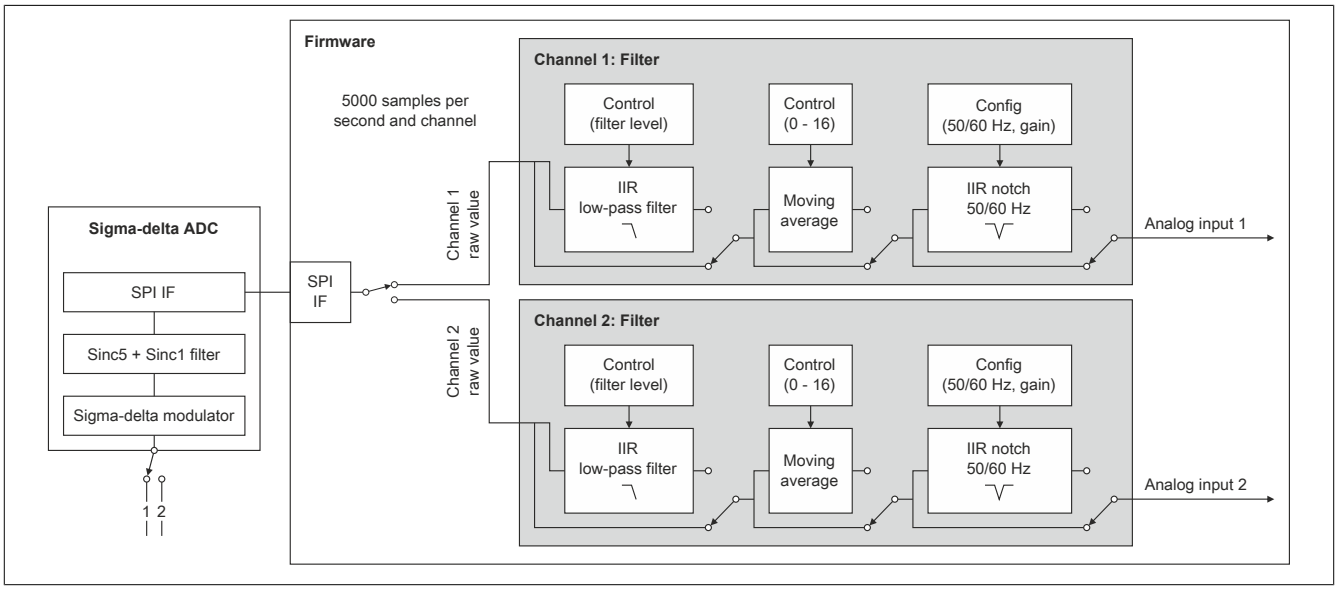


1.20.3.6 Software filters

An independent cascade of filters is available for each channel. They can be individually enabled and configured at runtime. By default, all filters are disabled when the device is switched on. Filters are controlled and configured using the "ControlPacked0N" on page 473 and "ConfigChannel0N" on page 474 (N = 1 to 2) registers.

In order to allow the filter behavior to be adapted to the measuring situation or machine cycle (high dynamics and low precision or low dynamics and high precision), the filter characteristics of both the IIR low-pass filter as well as the moving average filter can be changed synchronously at any time.

Filter diagram



1.20.3.6.1 IIR low-pass filter

1.20.3.6.1.1 General information

The IIR low-pass filter is used to generally smooth and increase the resolution of the analog value. The filter works according to the following formula:

$$y = y_{Old} + \frac{x - y_{Old}}{2^{Filter\ level}}$$

x ... current filter input value
y_{Old} ... old filter output value
y ... new filter output value

The "Filter level" parameter in the formula above is configured with the help of the "ControlPacked0N" on page 473 register. "Filter level" = 0 if the IIR low-pass filter is disabled.

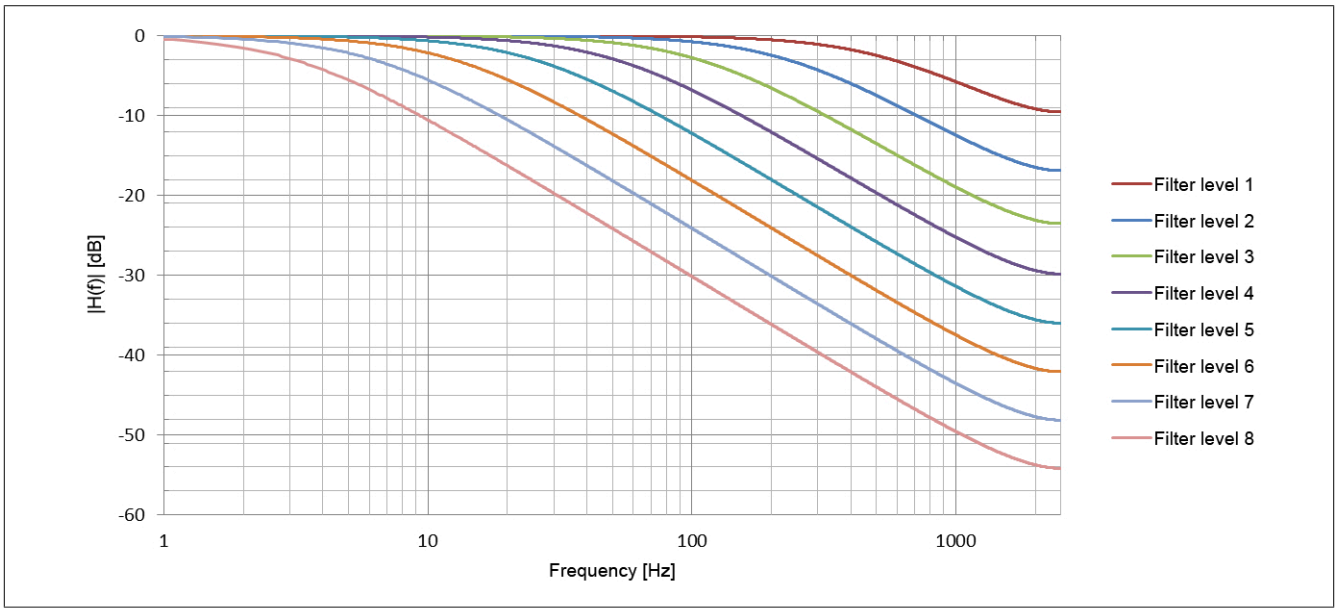
1.20.3.6.1.2 Filter characteristics of the 1st-order IIR low-pass filter

Limit frequency f_c

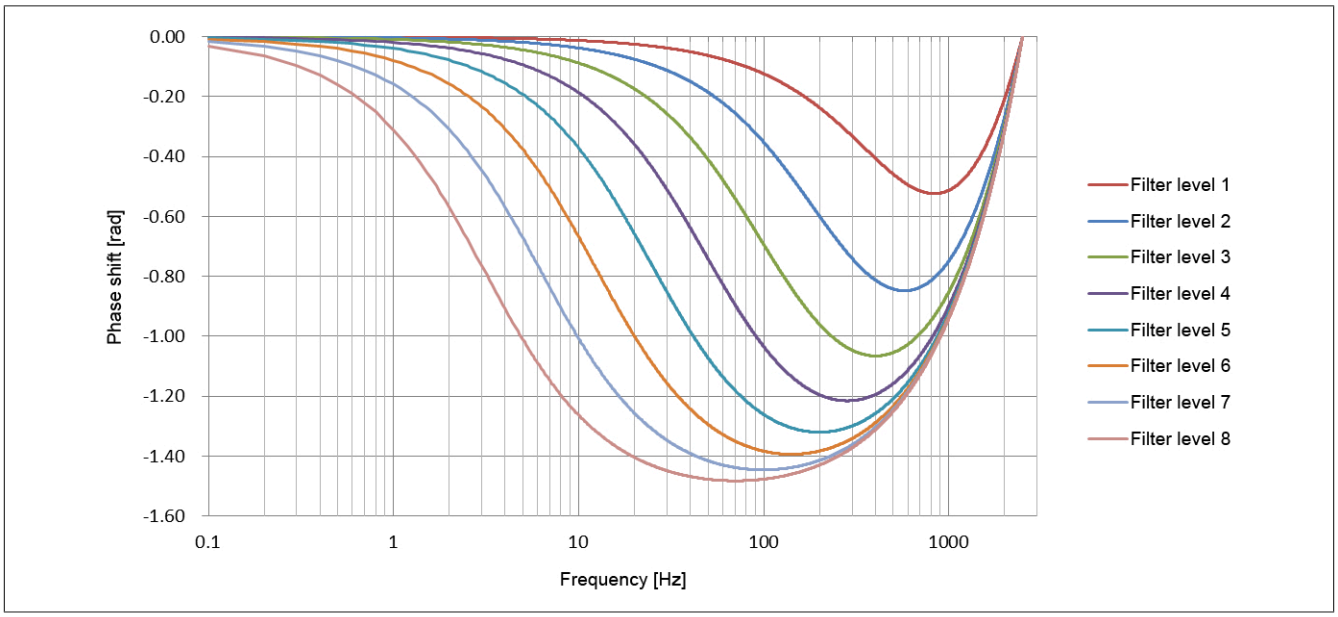
The following table provides an overview of the -3 dB limit frequency f_c depending on the configured filter level.

IIR low-pass filter level	f_c [Hz]
1	575
2	230
3	106
4	51
5	25
6	12.5
7	6.2
8	3.1

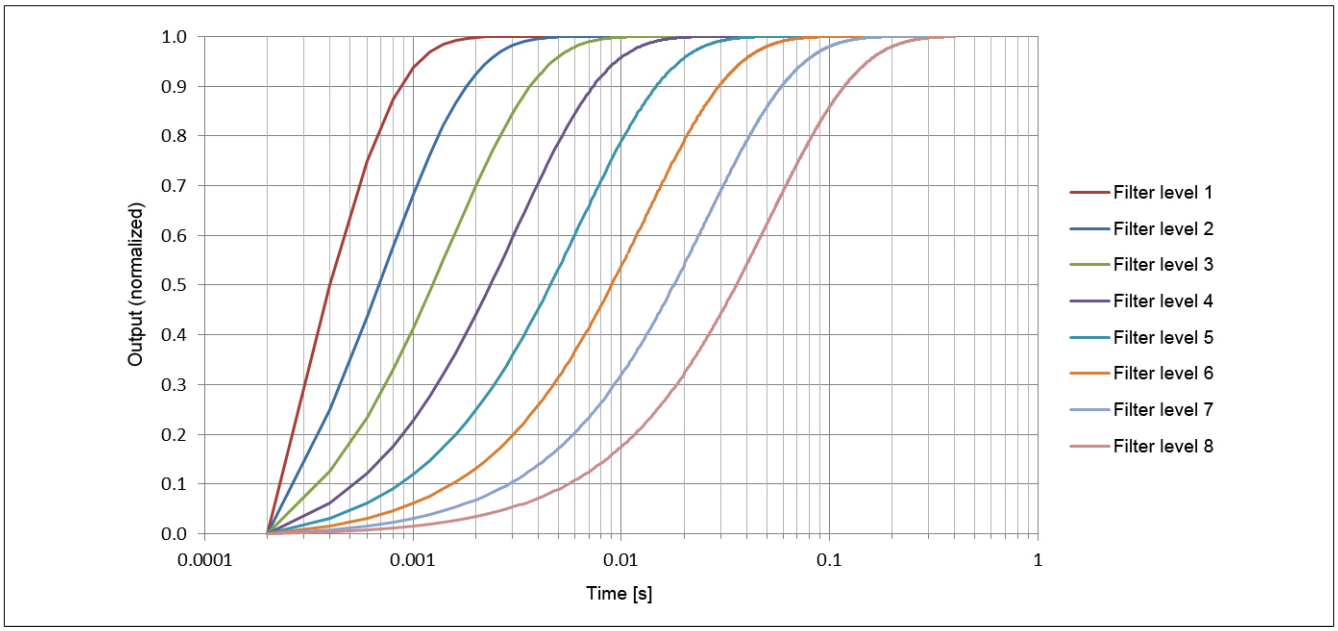
Gain of the IIR low-pass filter



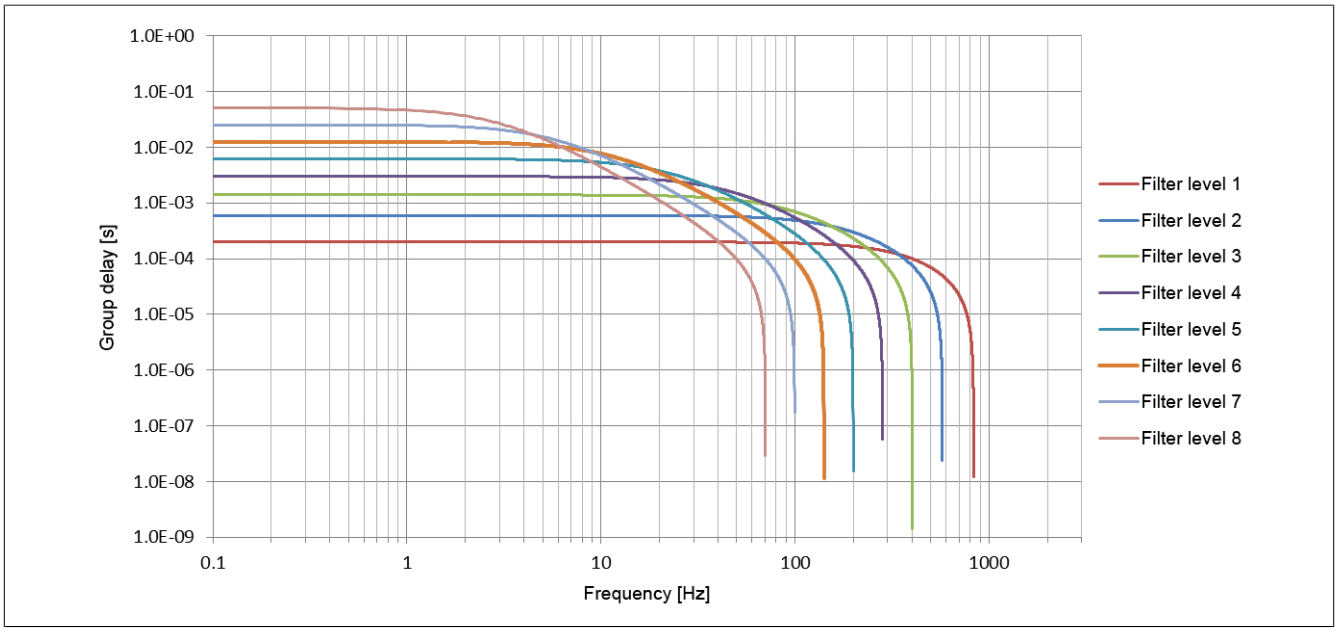
Phase shift of the IIR low-pass filter



Step response of the IIR low-pass filter



Group delay of the IIR low-pass filter



1.20.3.6.2 Sinc1 / Moving average filter

Like the low-pass filter, the moving average filter can also be used to smooth out the signal and increase its resolution. In addition, configuring the filter length accordingly makes it possible to target and efficiently filter out individual interference frequencies. The source of these interference frequencies may be mechanical or electromagnetic. Multiples of these are also filtered out (as long as they are a whole-number factor of the data output rate of 5000 samples per second and channel).

Example:
Data output rate = 5000 samples/s/channel, averaging over 4 values -> "Notch" at 1.25 kHz (and 2.5 kHz)

When reconfiguring the filter length from "n" to "m", it takes |m-n| * 200 µs until the desired filter length setpoint is reached again. As long as the filter length setpoint is not reached, this situation will be indicated by the bit 7 status bit in the "StatusPacked0N" on page 475 register.

1.20.3.6.2.1 Filter characteristics of the moving average filter

Filter configuration	Filter length	f_{Notch} [Hz] [1]	f_c [Hz] [2]
0	1		
1	2	2500	1244
2	4	1250	568
3	5	1000	450
4	10	500	222
5	20	250	111
6	25	200	88.4
7	50	100	44.0
8	83	60.24	26.5
9	100	50	21.9
10	125	40	17.5
11	167	29.94	13.0
12	200	25	10.9
13	250	20	8.6
14	300	16.67	7.1
15	500	10	4.3
16	1000	5	2.0

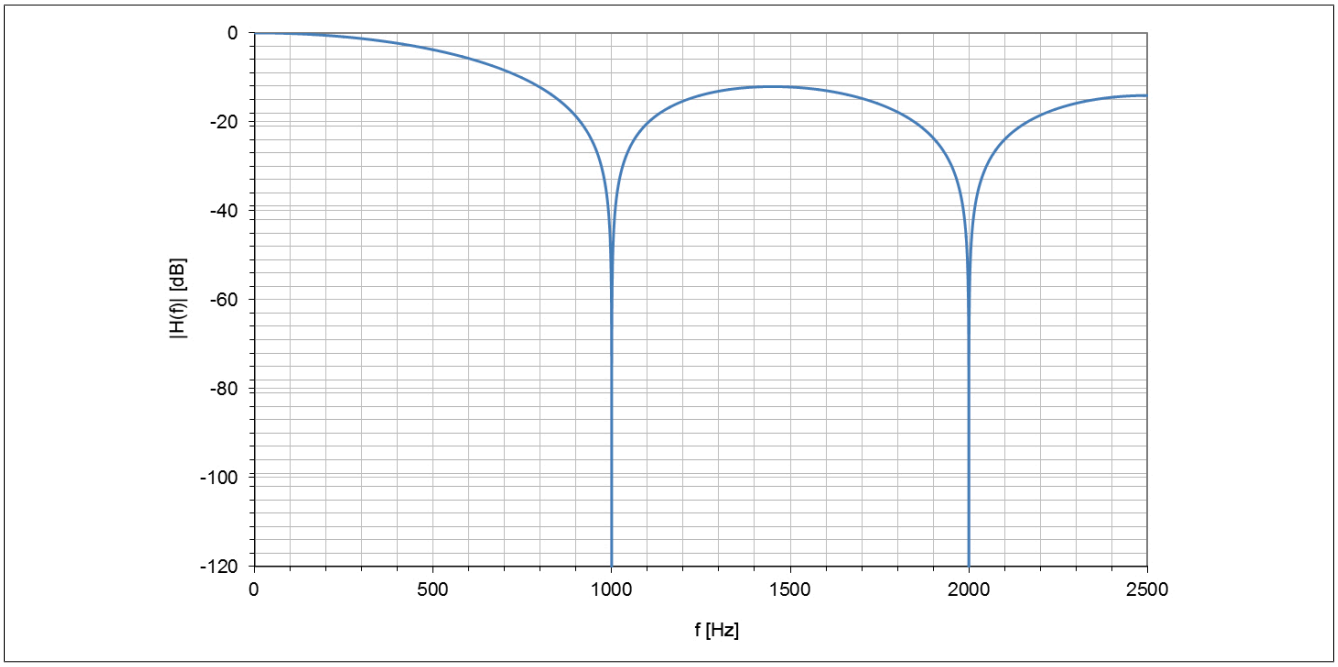
1) Mid-band frequency of the first attenuation maximum.
2) -3 dB limit frequency.

1.20.3.6.2.2 Examples for the gain of the moving average filter

Example 1

Filter setting = 3:

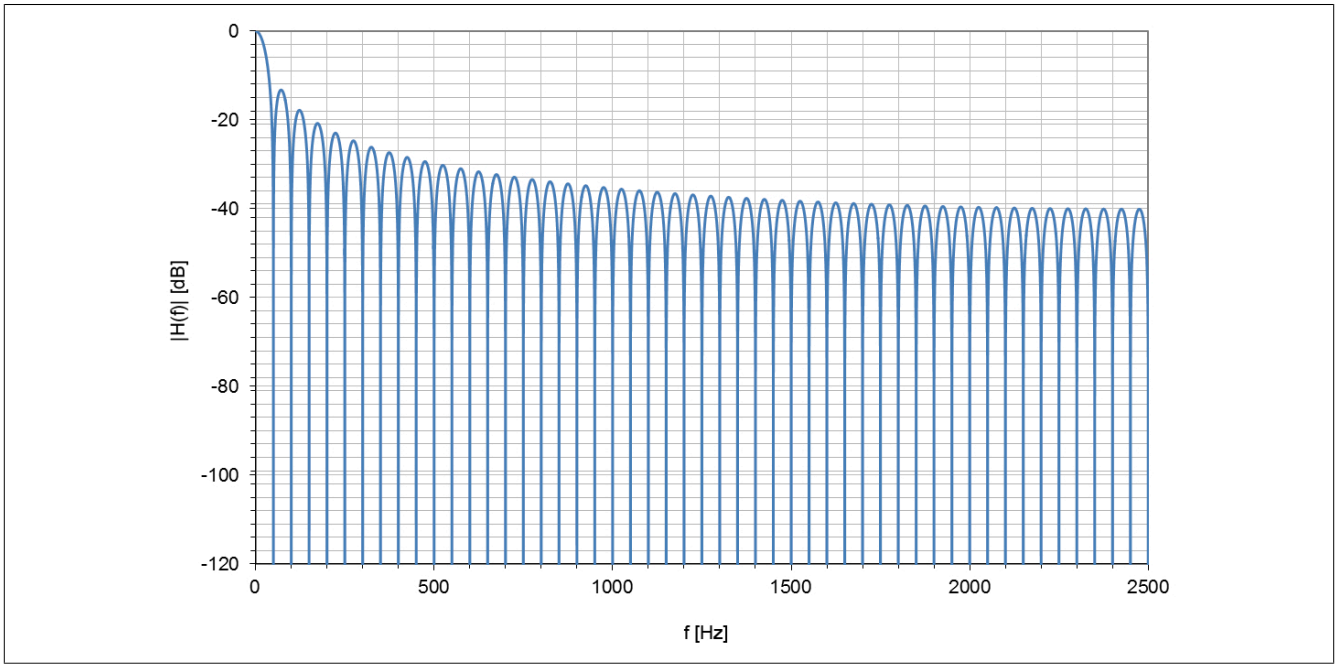
- f_{Notch} = 1000 Hz
- f_c = 449.6 Hz



Example 2

Filter setting = 9:

- f_{Notch} = 50 Hz
- f_c = 21.9 Hz



1.20.3.6.3 50/60 Hz IIR notch filter

The IIR notch filter is used for narrow-band suppression of interference caused by the mains frequency.

This is an 8th-order IIR notch filter implemented in the form of a cascade of 4 2nd-order IIR notch filters.

Information:

The IIR notch filter should only be enabled if there is actually interference being caused by the mains frequency. You should always check whether sufficiently low and sufficiently narrow band filtering at 50 Hz / 60 Hz can be implemented using a moving average filter (see "Filter characteristics of the moving average filter" on page 465).

This is because, like every higher-order IIR notch filter, this filter also has a tendency to respond to an input step with an attenuating vibration. The higher the dynamics of the expected measurement signal, the greater the potential interfering effect of this vibration tendency. In extreme cases, the vibration can temporarily be greater than the mains interference that is supposed to be filtered out.

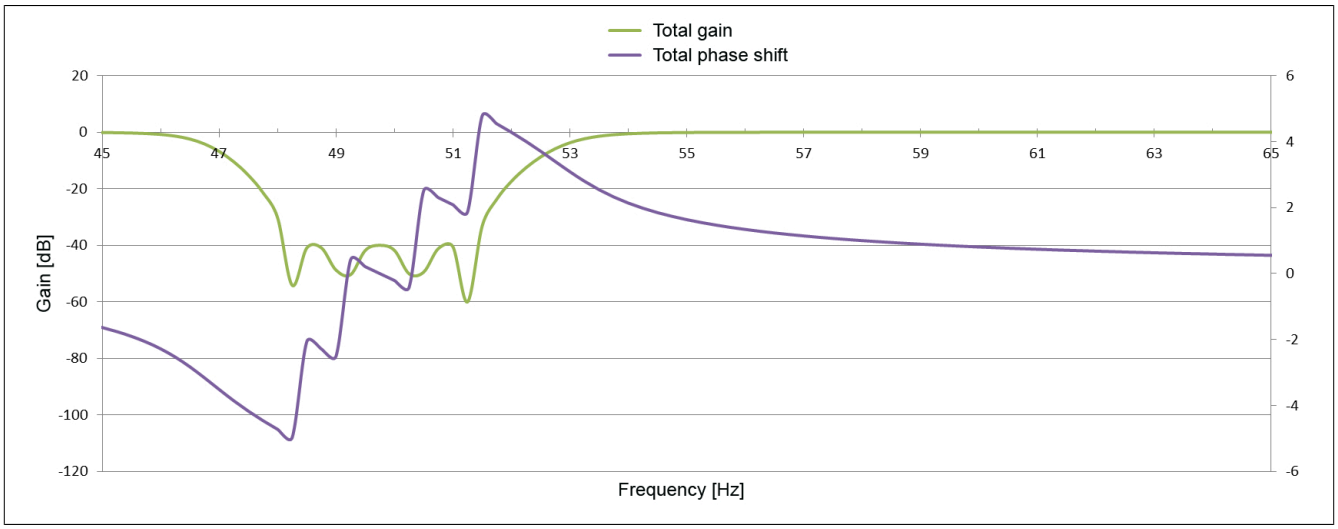
1.20.3.6.3.1 Filter characteristics of the IIR notch filter

There are 3 different filter characteristics that can be selected for both 50 Hz and 60 Hz (-40 dB, -60 dB and -80 dB). The higher the attenuation, the narrower the stopband.

Example 1

Filter characteristics for the following settings:

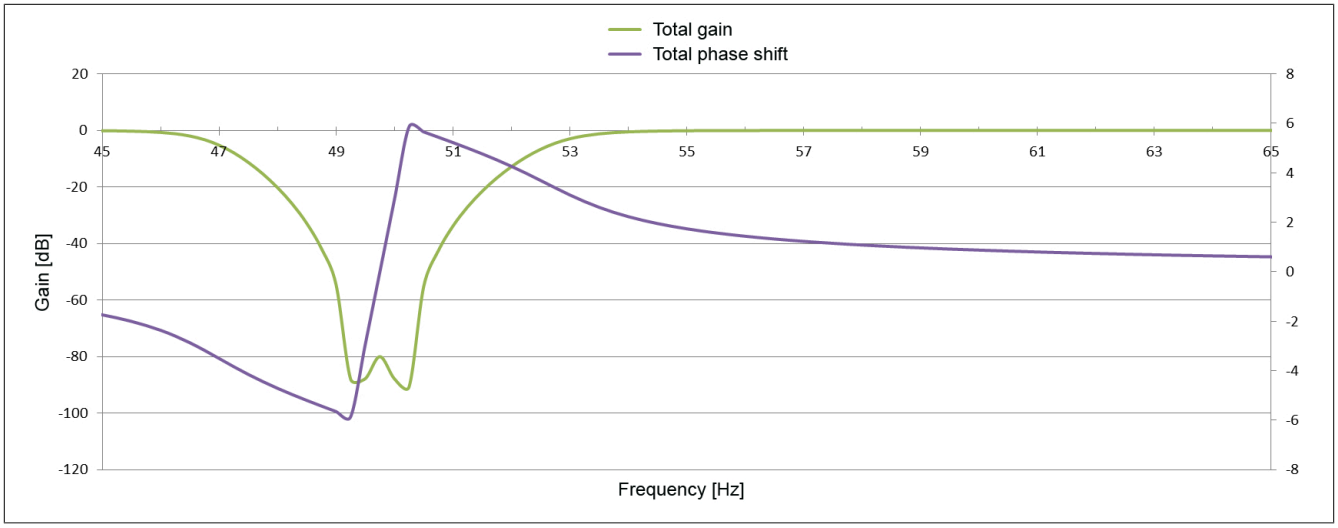
- Gain = -40 dB
- Frequency = 50 Hz
- Passband = 5 Hz
- Stopband = ±1 Hz



Example 2

Filter characteristics for the following settings:

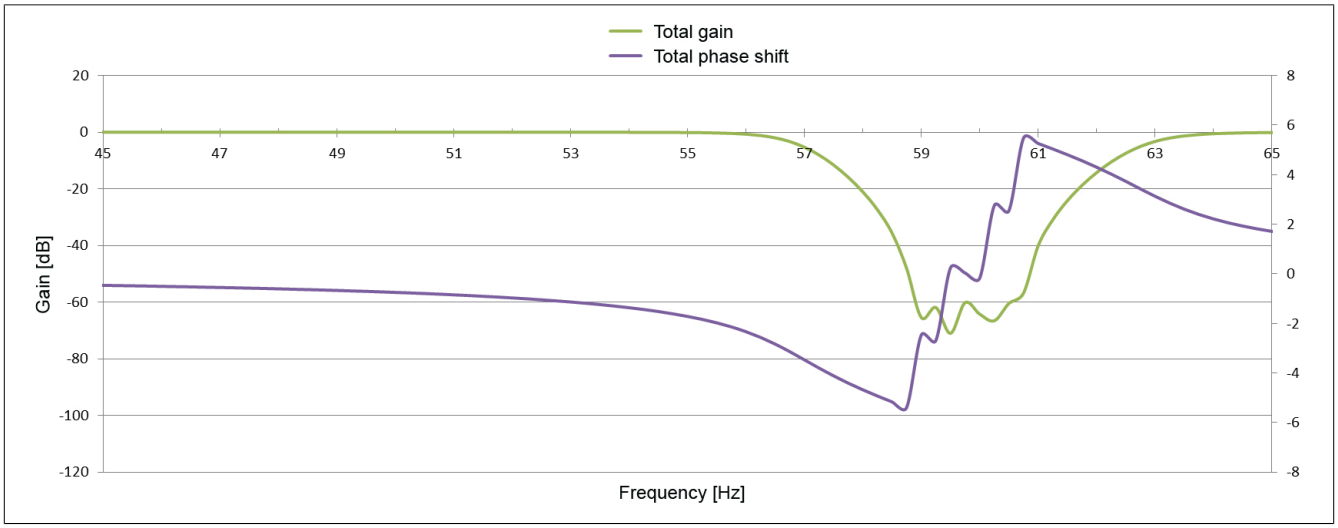
- Gain = -80 dB
- Frequency = 50 Hz
- Passband = 5 Hz
- Stopband = ±0.25 Hz



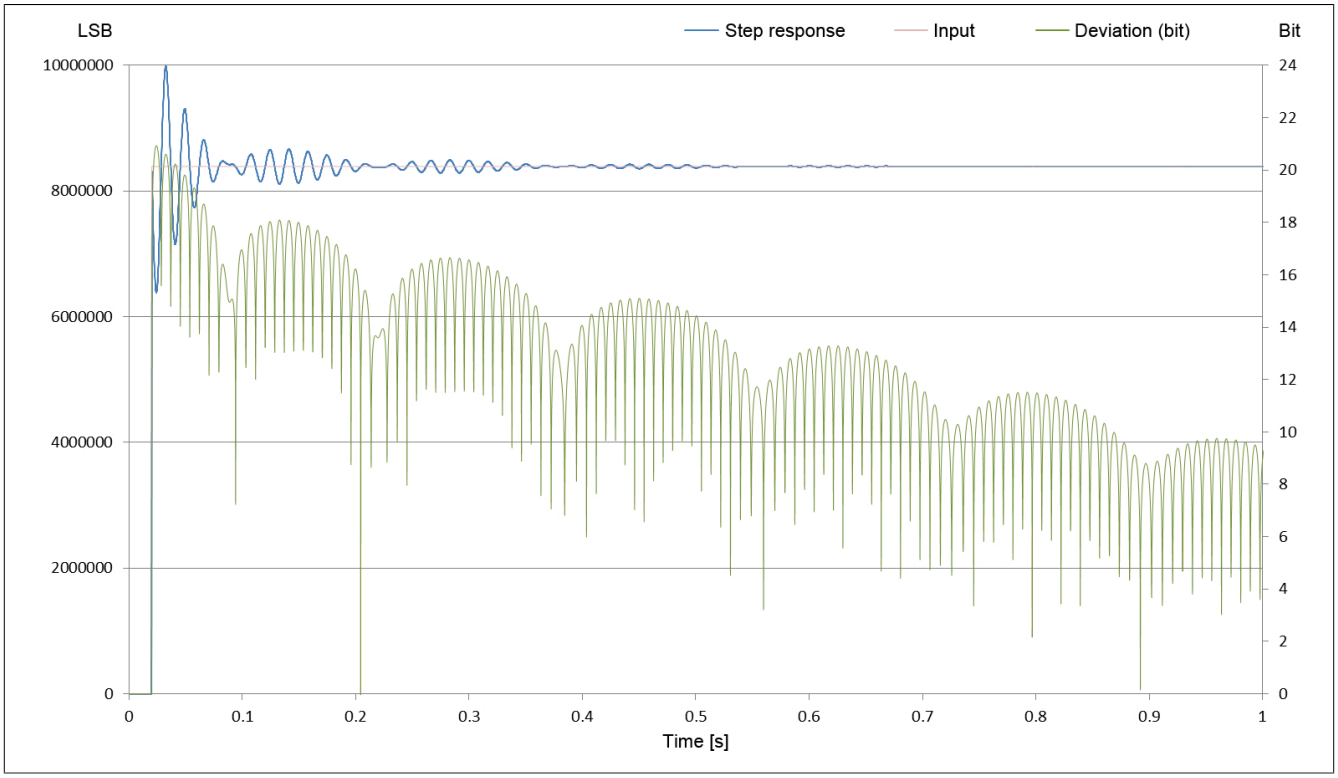
Example 3

Filter characteristics for the following settings:

- Gain = -60 dB
- Frequency = 60 Hz
- Passband = 5 Hz
- Stopband = ±0.5 Hz



Step response of an 8th-order IIR notch filter, including the deviation in bits:

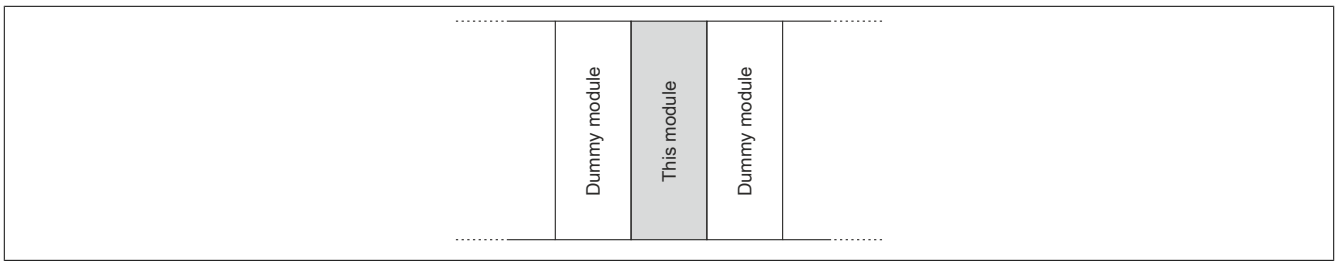


1.20.3.7 Hardware configuration

1.20.3.7.1 Hardware configuration for horizontal installation starting at 55°C ambient temperature

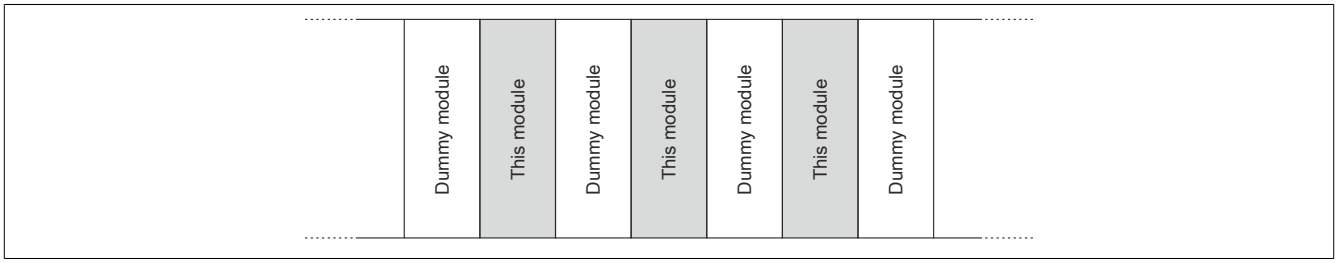
Operating a strain gauge module

Starting at an ambient temperature of 55°C, a dummy module must be connected to the left and right of the strain gauge module in a horizontal mounting orientation.



Operating multiple strain gauge modules side by side

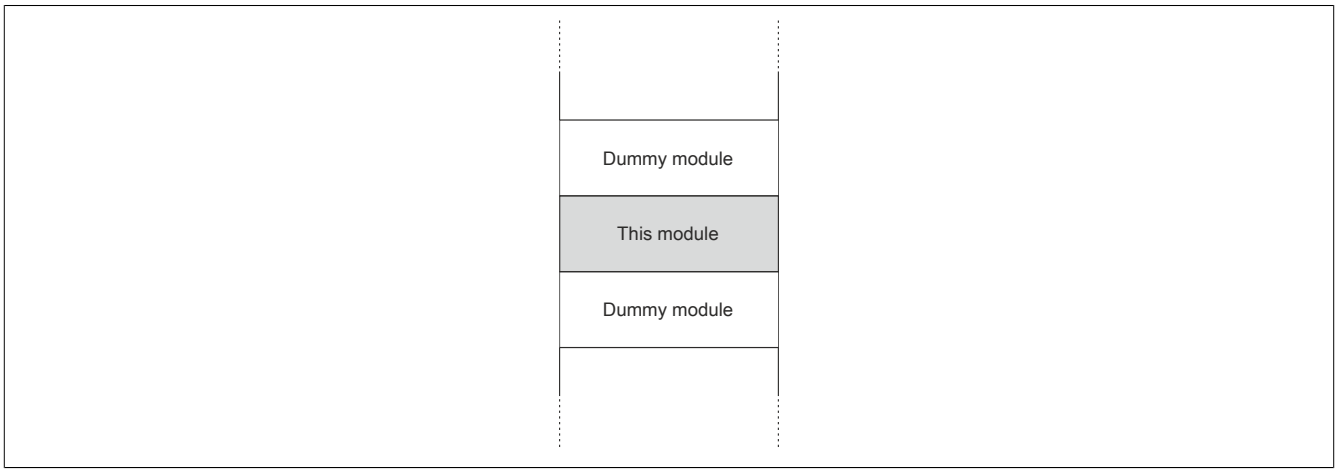
If 2 or more horizontal strain gauge modules are being operated in a cluster, the following arrangement of modules must be observed.



1.20.3.7.2 Hardware configuration for vertical installation starting at 45°C ambient temperature

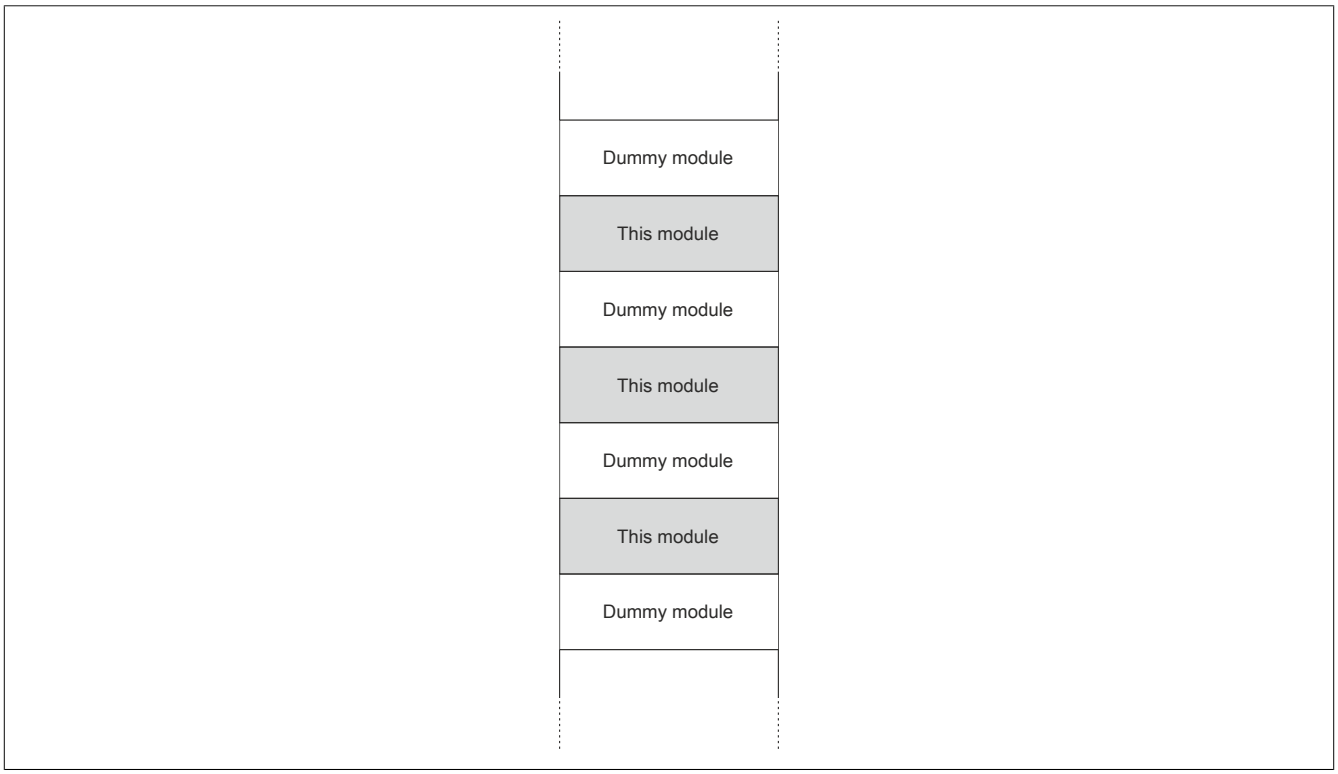
Operating a strain gauge module

Starting at an ambient temperature of 45°C, a dummy module must be connected to the left and right of the strain gauge module in a vertical mounting orientation.



Operating multiple strain gauge modules side by side

If 2 or more vertical strain gauge modules are being operated in a cluster, the following arrangement of modules must be observed.



1.20.4 Register description

1.20.4.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 system user's manual.

1.20.4.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration						
2	ControlPacked01 (configuration of strain gauge inputs)	UINT			•	
6	ControlPacked02 (configuration of strain gauge inputs)	UINT			•	
514	ConfigChannel01 (channel configuration)	UINT				•
578	ConfigChannel02 (channel configuration)	UINT				•
Analog signal - Communication						
4	AnalogInput01	DINT	•			
12	AnalogInput02	DINT	•			
33	StatusPacked01	USINT	•			
35	StatusPacked02	USINT	•			
257	AdcConvCtr01	SINT	•			
268	AdcConvTimeStamp01	DINT	•			

1.20.4.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration							
2	2	ControlPacked01 (configuration of strain gauge inputs)	UINT			•	
6	10	ControlPacked02 (configuration of strain gauge inputs)	UINT			•	
514	514	ConfigChannel01 (channel configuration)	UINT				•
578	578	ConfigChannel02 (channel configuration)	UINT				•
Analog signal - Communication							
4	4	AnalogInput01	DINT	•			
12	12	AnalogInput02	DINT	•			
33	0	StatusPacked01	USINT	•			
35	8	StatusPacked02	USINT	•			

1) The offset specifies the position of the register within the CAN object.

1.20.4.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

1.20.4.3.2 CAN I/O bus controller

The module occupies 4 analog logical slots on CAN I/O.

1.20.4.4 Configuration

1.20.4.4.1 Configuration of strain gauge inputs

Name:
ControlPacked01 and ControlPacked02

The strain gauge inputs are configured in these registers:

- Strain gauge factor of strain gauge load cell
- Enabling of filters

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information	
0 - 2	Strain gauge factor	000	Default: 256 mV/V	
		001	128 mV/V	
		010	64 mV/V	
		011	32 mV/V	
		100	16 mV/V	
		101	8 mV/V	
		110	4 mV/V	
		111	2 mV/V	
			Averaging	Notch frequency [Hz]
3 - 7	Moving average	00000	Default: Moving average disabled (bypass)	
		00001	2	2500
		00010	4	1250
		00011	5	1000
		00100	10	500
		00101	20	250
		00110	25	200
		00111	50	100
		01000	83	60
		01001	100	50
		01010	125	40
		01011	167	30
		01100	200	25
		01101	250	20
		01110	300	16.66
		01111	500	10
		10000	1000	5
		10001 to 11111	Reserved (firmware limited to 1000)	
8	Notch filter	0	Default: IIR notch filter disabled (bypass)	
		1	IIR notch filter enabled	
9	Reserved	0		
10 - 11	Low-pass filter mode	00	IIR low-pass filter disabled (bypass)	
		01	1st-order IIR low-pass filter (see "IIR low-pass filter" on page 462)	
		10 - 11	Reserved: No IIR low-pass filter active	
			Filter level	-3 db frequency [Hz]
12 - 14	Low-pass filter level	000	1	575
		001	2	230
		010	3	106
		011	4	51
		100	5	25
		101	6	12.5
		110	7	6.2
		111	8	3.1
15	Reserved	0		

1.20.4.4.2 Channel configuration

Name:
ConfigChannel01 and ConfigChannel02

The IIR notch filter is configured individually for each channel in these registers.

Data type	Values	Bus controller default setting
UINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0 - 11	Reserved	0	
12 - 13	Notch filter attenuation	00	Gain: -40 dB Pass: ±5 Hz Stop: ±1 Hz (Bus controller default setting)
		01	Gain: -60 dB Pass: ±5 Hz Stop: ±0.5 Hz
		10	Gain: -80 dB Pass: ±5 Hz Stop: ±0.25 Hz
		11	Reserved
14	Notch filter frequency	0	With 50 Hz (bus controller default setting)
		1	At 60 Hz
15	Reserved	0	

1.20.4.5 Communication

1.20.4.5.1 Analog input values

Name:
AnalogInput01 and AnalogInput02

The analog input value is mapped in this register.

Data type	Value	Input signal:
DINT	-8,388,608	Negative invalid value
	-8,388,607	Negative full-scale deflection / Underflow
	-8,388,606 to 8,388,606	Valid range
	8,388,607	Positive full-scale deflection / Overflow / Open line

1.20.4.5.2 Module status

Name:
StatusPacked01 and StatusPacked02

These registers contain the current state of the module.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	I/O power supply	0	No error
		1	Error in power supply
1	Bypass current	0	No error
		1	Overcurrent (sum from all sensors)
2 - 3	Reserved	0	
4	A/D converter configuration	0	Already configured
		1	Not yet configured
5	Analog values	0	Analog value valid
		1	Analog value invalid (analog value = -8,388,608 = 0xFF800000). Possible causes: • Internal transfer error (XOR checksum verification) • Error in strain gauge supply (bit 1) • Error in I/O voltage supply (bit 0) • A/D converter not (yet) configured
6	Analog value range overrun	0	Analog value valid
		1	Analog value invalid. Possible causes: • Overflow / Open circuit (analog value = 8,388,607 = 0x007FFFFF) • Underflow (analog value = -8,388,607 = 0xFF800001)
7	Moving average filter	0	Moving average filter engaged
		1	Moving average filter not engaged Possible causes: • After changing the filter length • Consequence of the filter being reset by another error

1.20.4.5.3 A/D conversion counter

Name:
AdcConvCtr01

Instead of being measured simultaneously, the strain gauge channels of the module are measured according to the multiplexing procedure. The "AdcConvTimestamp01" on page 475 register contains the timestamp of the encoded last channel converted in the "AdcConvCtr01" register. The timestamp of the other channels can then be calculated later using this information.

Data type	Value
SINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Index of the last converted channel	0	Analog input 1
		1	Analog input 2
		2	Reserved
		3	Reserved
2 - 7	Rotating cycle counter	x	Incremented at the end of a conversion cycle. All channels are converted in a conversion cycle.

1.20.4.5.4 ADC conversion timestamp

Name:
AdcConvTimestamp01

The timestamp of the last converted channel is stored in this register (see bits 0 and 1 in the "AdcConvCtr01" on page 475 register). This is always the point in time (in µs) at which the conversion of the latest A/D converter raw value is completed.

Data type	Value	Function
DINT	-2147483648 to 2147483647	Timestamp (in µs) of the last converted channel (see bits 0 and 1 in the A/D conversion counter)

The timestamp of the remaining channels can be determined in the application using the number and timestamp of the last converted channel according to the following table.

Channel	Age difference
2 - 1	47 µs
1 - 2	153 µs

Example 1:

- Latest channel (bit 0 - 1 in the AdcConvCtr01 register) = 01 (analog input 2):
- Timestamp: "AdcConvTimestamp01" register = 0 µs

Channel	Timestamp
2	0 µs
1	-47 µs

Example 2:

- Latest channel (bit 0 - 1 in the AdcConvCtr01 register) = 00 (analog input 1):
- Timestamp: "AdcConvTimestamp01" register = 0 µs

Channel	Timestamp
1	0 µs
2	-153 µs

1.20.4.6 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

1.20.4.7 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time
200 µs

1.21 X20AIB744

1.21.1 General information

This module works with 4-wire strain gauge load cells. The concept applied by the module requires compensation in the measurement system. This compensation eliminates the absolute uncertainty in the measurement circuit, such as component tolerances, effective bridge voltage or zero offset. The measurement precision refers to the absolute (compensated) value, which will only change as a result of changes in the operating temperature.

- 4 full-bridge strain gauge inputs
- 5 kHz data output rate for all 4 channels
- Independently configurable strain gauge factor and filter level for each of the 4 channels

1.21.2 Order data

Order number	Short description	Figure
	Analog inputs	
X20AIB744	X20 analog input module, 4 full-bridge strain inputs, 24-bit converter resolution, 2.5 kHz input filter	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB1F	X20 terminal block, 16-pin, 24 VDC keyed	

Table 69: X20AIB744 - Order data

1.21.3 Technical data

Order number	X20AIB744
Short description	
I/O module	4 full-bridge strain gauge inputs
General information	
B&R ID code	0xE286
Status indicators	Channel status, operating state, module status
Diagnostics	
Module run/error	Yes, using LED status indicator and software
Open circuit	Yes, using LED status indicator and software
Input	Yes, using LED status indicator and software
Power consumption	
Bus	0.01 W
Internal I/O	1 W
Additional power dissipation caused by actuators (resistive) [W]	+1.43 [1]
Certifications	
CE	Yes
EAC	Yes
UL	cULus E115267 Industrial control equipment
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
Full-bridge strain gauge	
Strain gauge factor	2 to 256 mV/V, configurable using software
Connection	4-wire connections
Input type	Differential, used to evaluate a full-bridge strain gauge
Digital converter resolution	24-bit
Conversion time	200 µs
Data output rate	5000 samples per second and per channel (f_{DATA})
Input filter	
Cutoff frequency	2.5 kHz
Order	3
Slope	60 dB
ADC filter characteristics	Sigma-delta, see section "Filter"
Operating range / Measurement sensor	85 to 5000 Ω
Influence of cable length	Twisted and shielded conductors, cable length as short as possible, cable routing separate from load circuits, without intermediate terminal to sensor
Input protection	RC protection
Common-mode range	0.6 to 3.8 VDC Permissible input voltage range (with regard to the potential strain gauge GND) on inputs "Input +" and "Input -"
Insulation voltage between input and bus	500 V_{eff}
Conversion procedure	Sigma-delta
Output of digital value	
Broken bridge supply line	Value approaching 0
Broken sensor line	Value approaching ±end value (status bit "Open circuit" set in register "Module status")
Valid range of values	0xFF800001 to 0x007FFFFF (-8,388,607 to 8,388,607)
Strain gauge supply	
Voltage	5.5 VDC / Max. 65 mA per channel
Short-circuit and overload resistant	Yes
Quantization [2]	
LSB value	
2 mV/V	1.31 nV
4 mV/V	2.62 nV
8 mV/V	5.25 nV
16 mV/V	10.49 nV
32 mV/V	20.98 nV
64 mV/V	41.96 nV
128 mV/V	83.92 nV
256 mV/V	167.85 nV
Max. gain drift	35 ppm/°C [3]
Max. offset drift	15 ppm/°C [4]
Nonlinearity	<10 ppm [4]
Electrical properties	
Electrical isolation	Bus isolated from analog input and strain gauge supply voltage Channel not isolated from channel and I/O power supply
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes

Table 70: X20AIB744 - Technical data

Order number	X20AIB744
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	See section "Hardware configuration"
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x terminal block X20TB1F separately. Order 1x bus module X20BM11 separately.
Pitch	12.5 $^{+0.2}$ mm

Table 70: X20AIB744 - Technical data

1) Depends on the full-bridge strain gauge being used.
2) Quantization depends on the strain gauge factor.
3) Based on the current measured value.
4) Based on the entire measurement range.

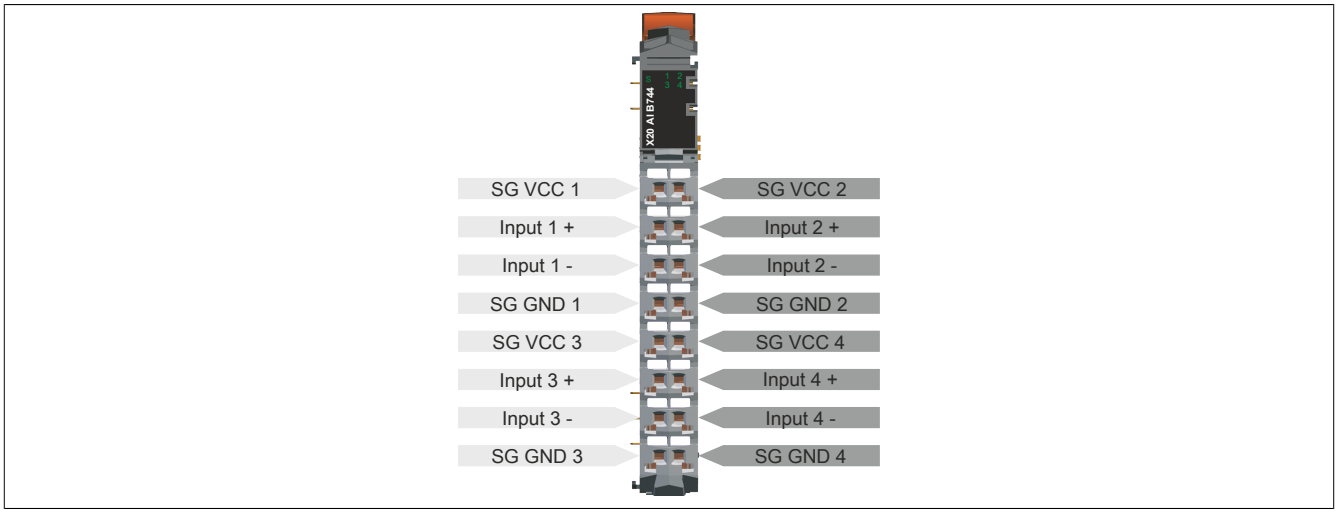
1.21.4 LED status indicators

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 system user's manual.

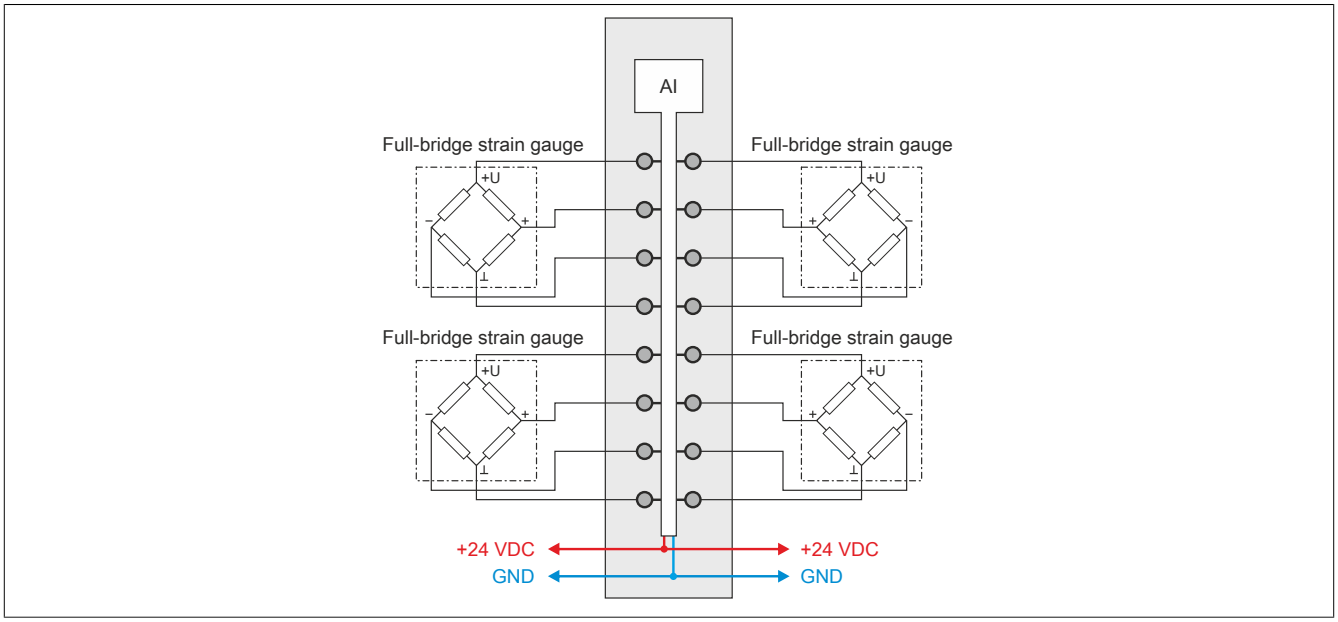
Figure	LED	Color	Status	Description
	S	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
		Red	Off	No power to module or everything OK
			Double flash	I/O power supply outside limits
			On	Error or reset status
	1 - 4	Green	Off	Possible causes: • Supply error • Channel not yet configured
			Blinking	Possible causes: • Open line • Overvoltage • Undervoltage
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.

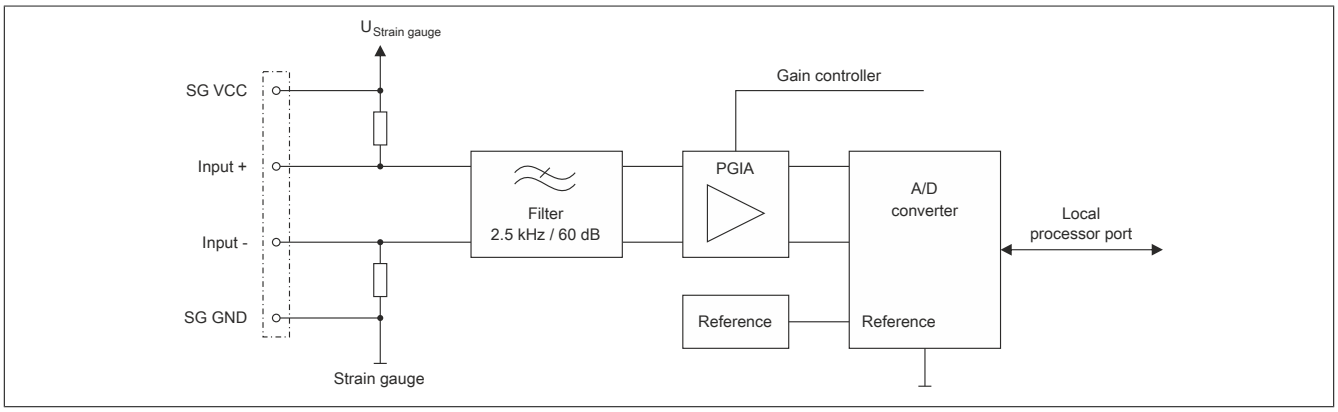
1.21.5 Pinout



1.21.6 Connection example



1.21.7 Input circuit diagram

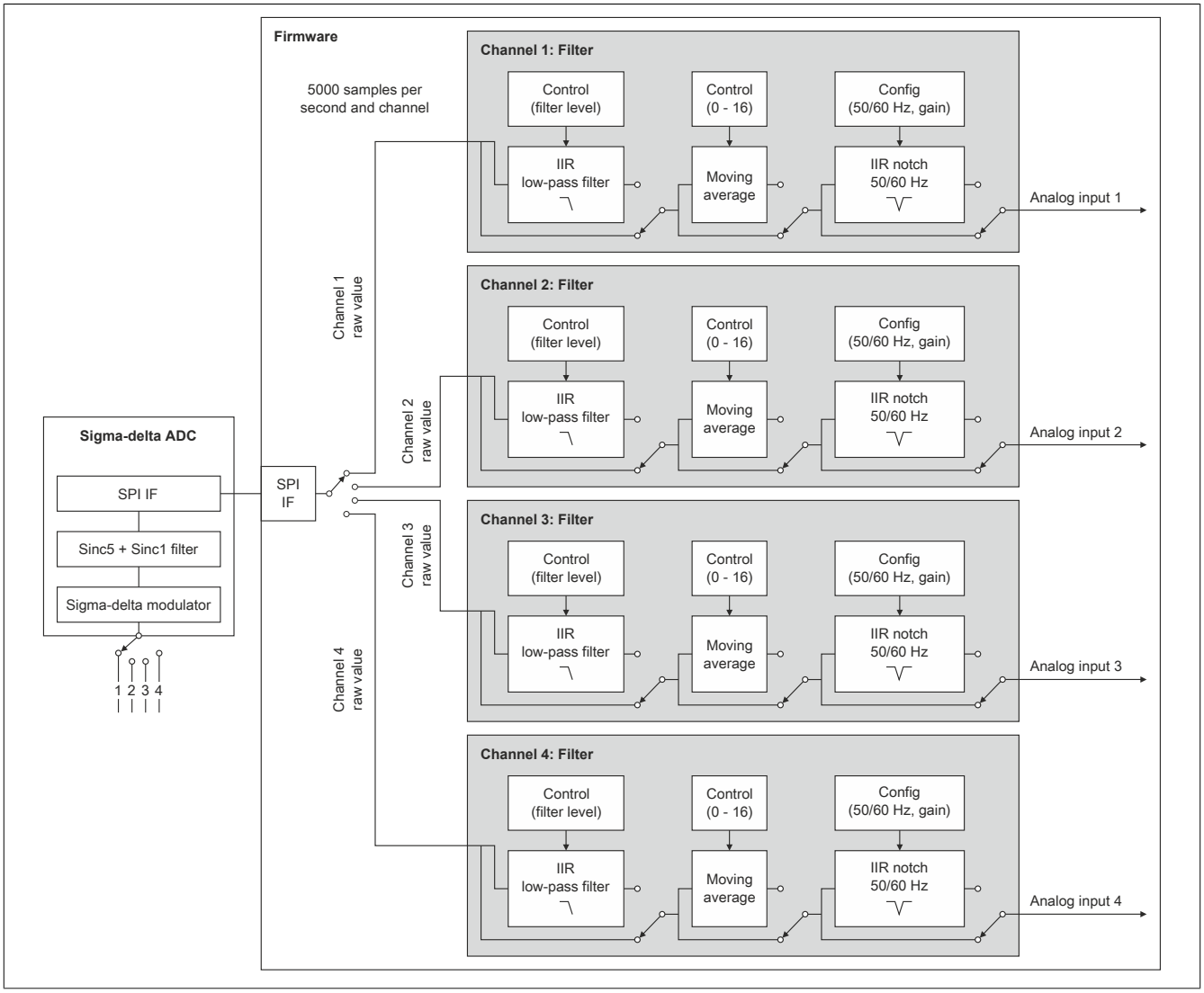


1.21.8 Software filters

An independent cascade of filters is available for each channel. They can be individually enabled and configured at runtime. By default, all filters are disabled when the device is switched on. Filters are controlled and configured using the "ControlPacked0N" on page 492 and "ConfigChannel0N" on page 493 (N = 1 to 4) registers.

In order to allow the filter behavior to be adapted to the measuring situation or machine cycle (high dynamics and low precision or low dynamics and high precision), the filter characteristics of both the IIR low-pass filter as well as the moving average filter can be changed synchronously at any time.

Filter diagram



1.21.8.1 IIR low-pass filter

1.21.8.1.1 General information

The IIR low-pass filter is used to generally smooth and increase the resolution of the analog value. The filter works according to the following formula:

$$y = y_{Old} + \frac{x - y_{Old}}{2^{Filter\ level}}$$

x ... current filter input value
y_{Old} ... old filter output value
y ... new filter output value

The "Filter level" parameter in the formula above is configured with the help of the "ControlPacked0N" on page 492 register. "Filter level" = 0 if the IIR low-pass filter is disabled.

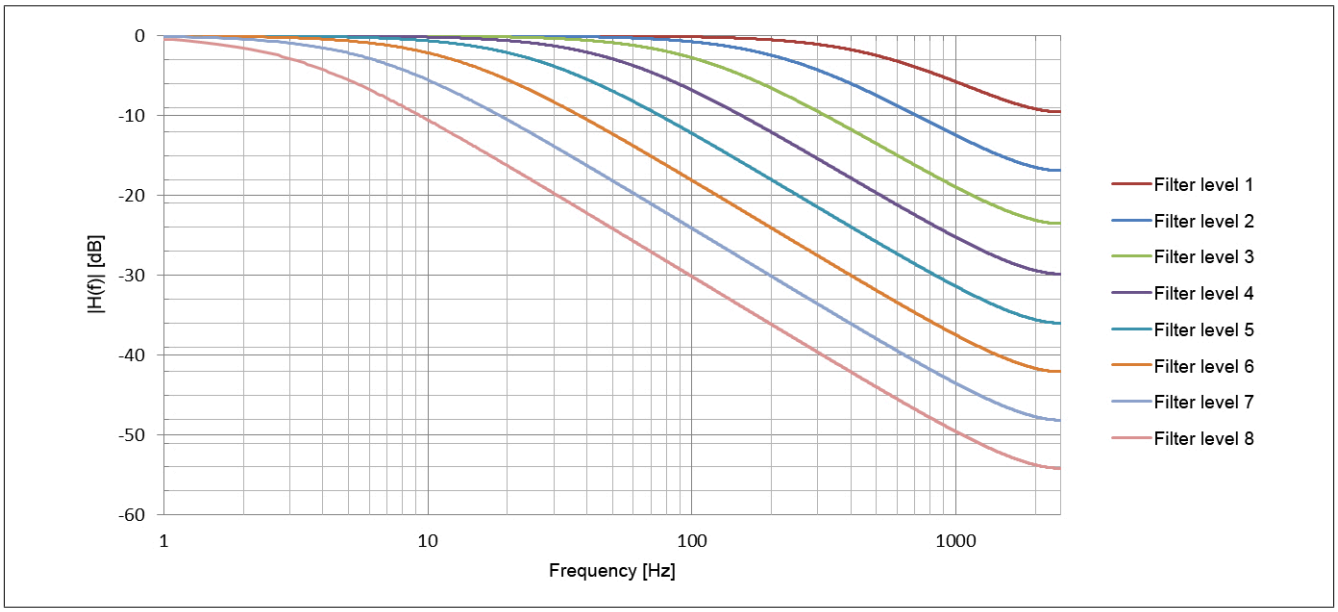
1.21.8.1.2 Filter characteristics of the 1st-order IIR low-pass filter

Limit frequency f_c

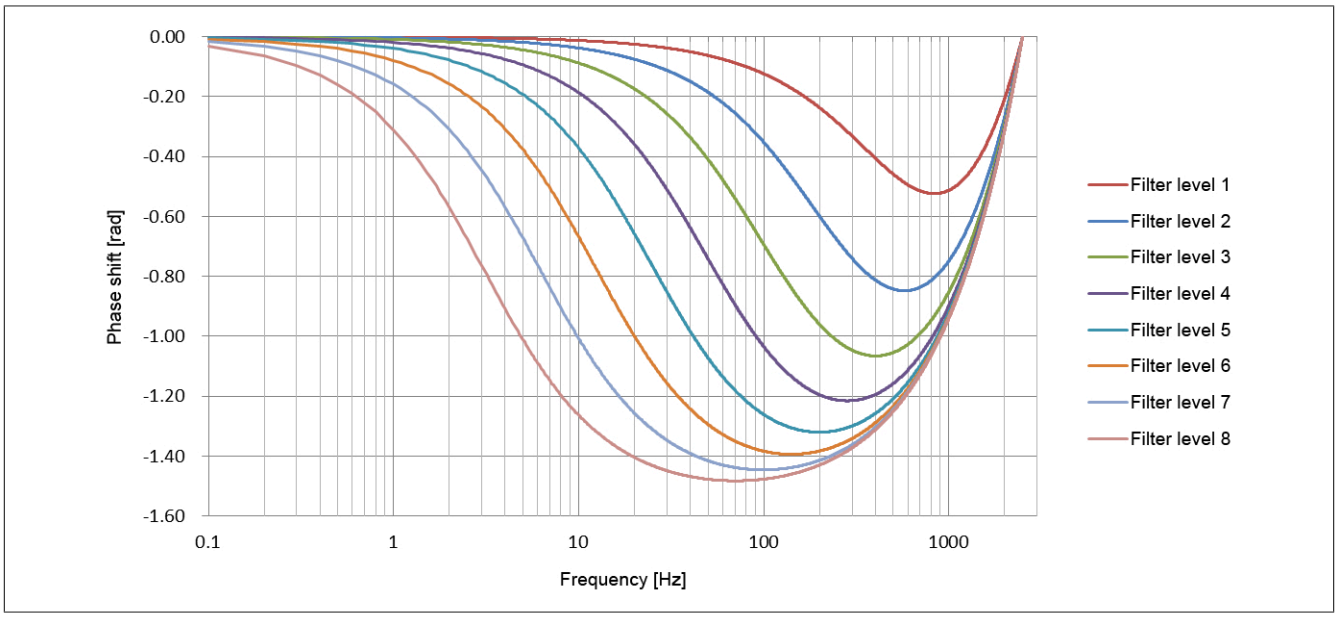
The following table provides an overview of the -3 dB limit frequency f_c depending on the configured filter level.

IIR low-pass filter level	f_c [Hz]
1	575
2	230
3	106
4	51
5	25
6	12.5
7	6.2
8	3.1

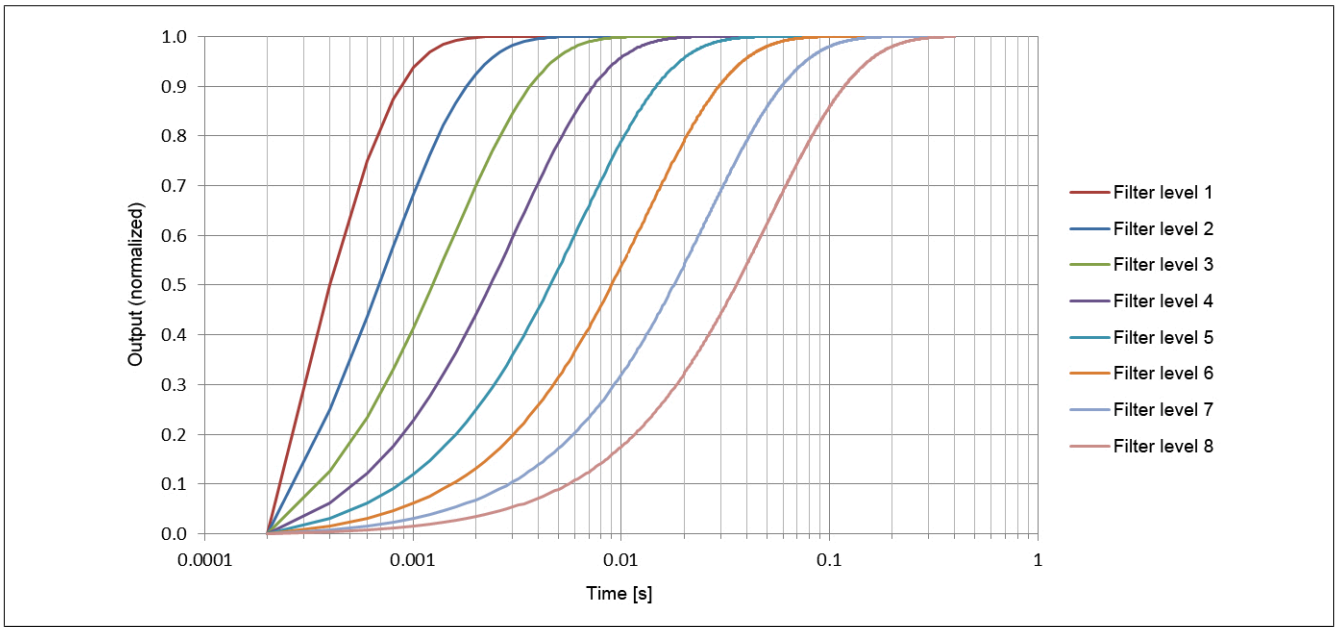
Gain of the IIR low-pass filter



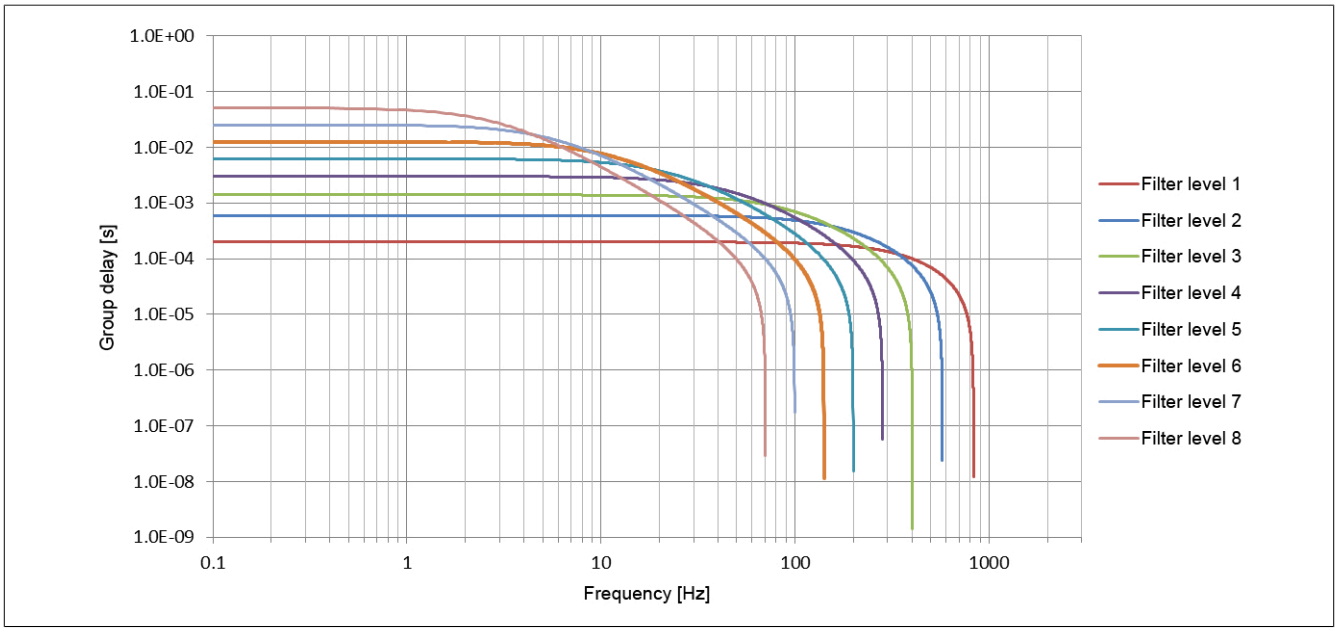
Phase shift of the IIR low-pass filter



Step response of the IIR low-pass filter



Group delay of the IIR low-pass filter



1.21.8.2 Sinc1 / Moving average filter

Like the low-pass filter, the moving average filter can also be used to smooth out the signal and increase its resolution. In addition, configuring the filter length accordingly makes it possible to target and efficiently filter out individual interference frequencies. The source of these interference frequencies may be mechanical or electromagnetic. Multiples of these are also filtered out (as long as they are a whole-number factor of the data output rate of 5000 samples per second and channel).

Example:
Data output rate = 5000 samples/s/channel, averaging over 4 values -> "Notch" at 1.25 kHz (and 2.5 kHz)

When reconfiguring the filter length from "n" to "m", it takes |m-n| * 200 µs until the desired filter length setpoint is reached again. As long as the filter length setpoint is not reached, this situation will be indicated by the bit 7 status bit in the "StatusPacked0N" on page 494 register.

1.21.8.2.1 Filter characteristics of the moving average filter

Filter configuration	Filter length	f_{Notch} [Hz] 1)	f_c [Hz] 2)
0	1		
1	2	2500	1244
2	4	1250	568
3	5	1000	450
4	10	500	222
5	20	250	111
6	25	200	88.4
7	50	100	44.0
8	83	60.24	26.5
9	100	50	21.9
10	125	40	17.5
11	167	29.94	13.0
12	200	25	10.9
13	250	20	8.6
14	300	16.67	7.1
15	500	10	4.3
16	1000	5	2.0

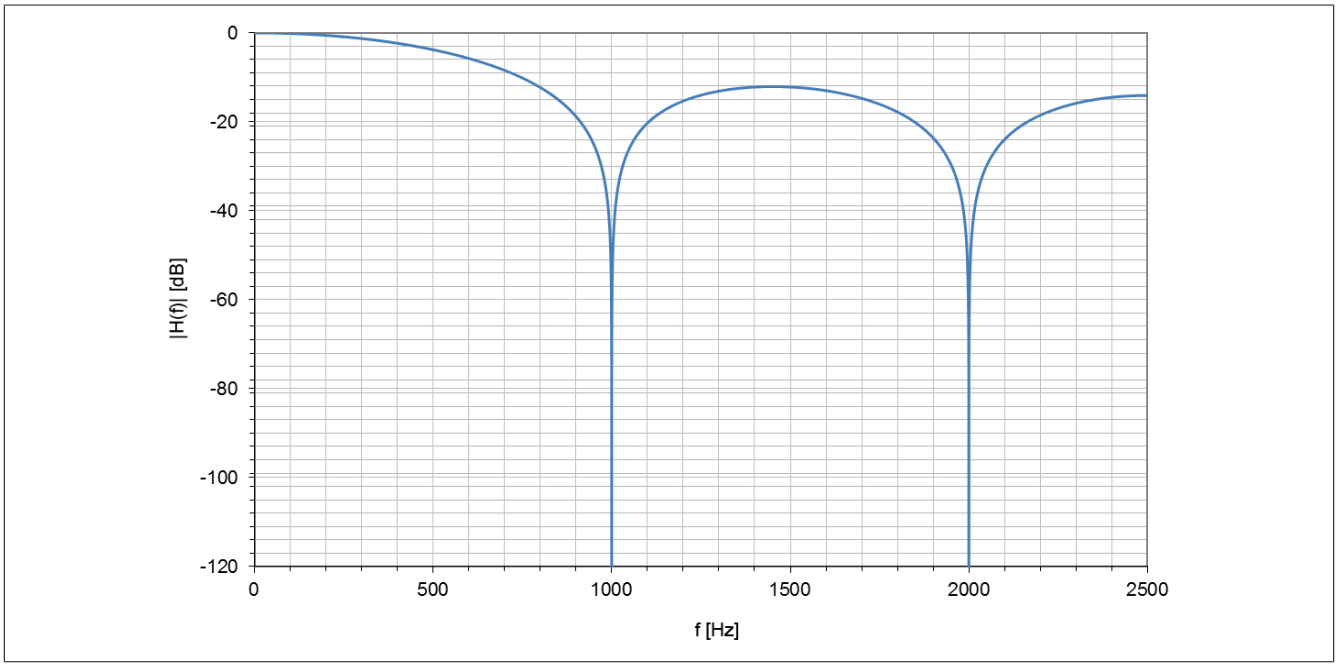
1) Mid-band frequency of the first attenuation maximum.
2) -3 dB limit frequency.

1.21.8.2.2 Examples for the gain of the moving average filter

Example 1

Filter setting = 3:

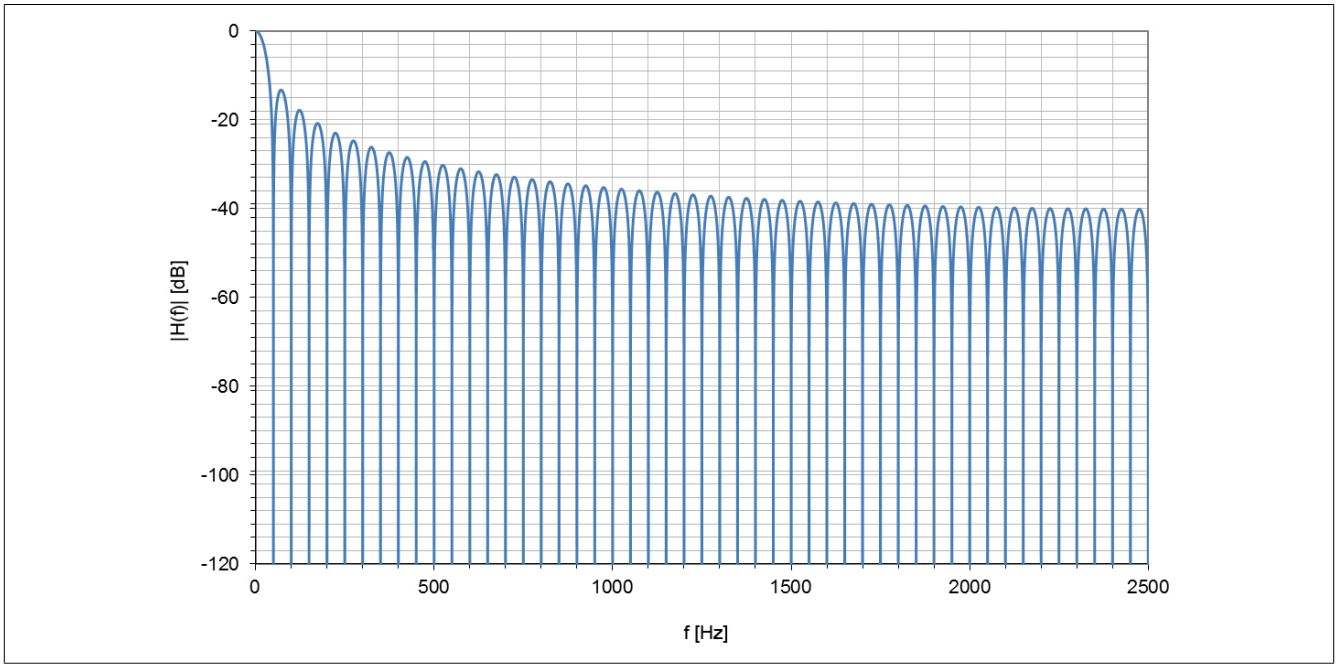
- f_{Notch} = 1000 Hz
- f_c = 449.6 Hz



Example 2

Filter setting = 9:

- f_{Notch} = 50 Hz
- f_c = 21.9 Hz



1.21.8.3 50/60 Hz IIR notch filter

The IIR notch filter is used for narrow-band suppression of interference caused by the mains frequency.

This is an 8th-order IIR notch filter implemented in the form of a cascade of 4 2nd-order IIR notch filters.

Information:

The IIR notch filter should only be enabled if there is actually interference being caused by the mains frequency. You should always check whether sufficiently low and sufficiently narrow band filtering at 50 Hz / 60 Hz can be implemented using a moving average filter (see "Filter characteristics of the moving average filter" on page 484).

This is because, like every higher-order IIR notch filter, this filter also has a tendency to respond to an input step with an attenuating vibration. The higher the dynamics of the expected measurement signal, the greater the potential interfering effect of this vibration tendency. In extreme cases, the vibration can temporarily be greater than the mains interference that is supposed to be filtered out.

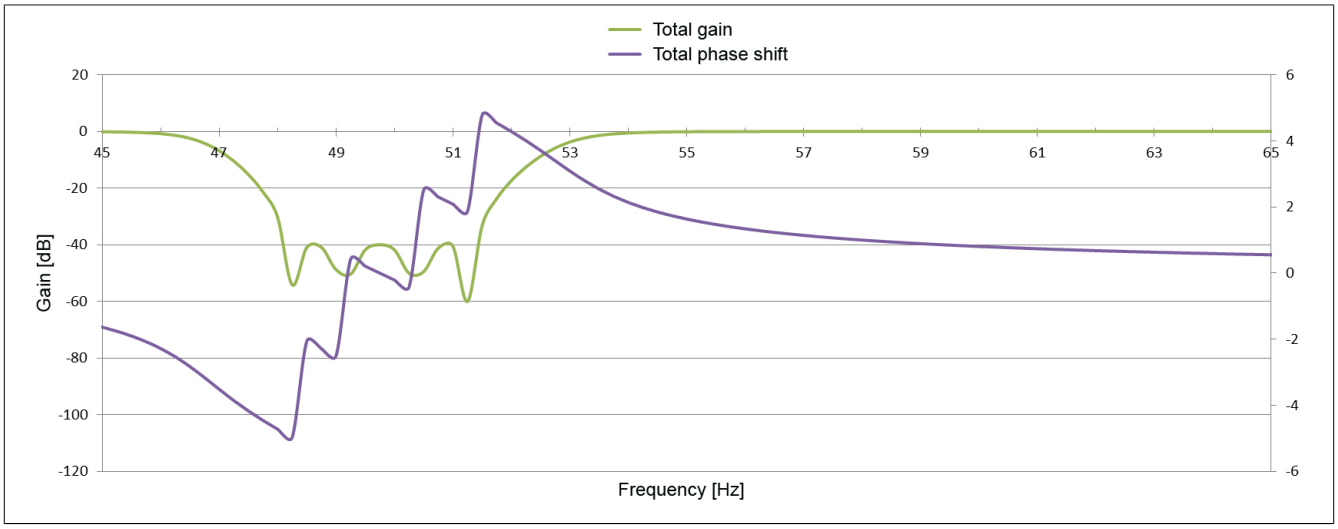
1.21.8.3.1 Filter characteristics of the IIR notch filter

There are 3 different filter characteristics that can be selected for both 50 Hz and 60 Hz (-40 dB, -60 dB and -80 dB). The higher the attenuation, the narrower the stopband.

Example 1

Filter characteristics for the following settings:

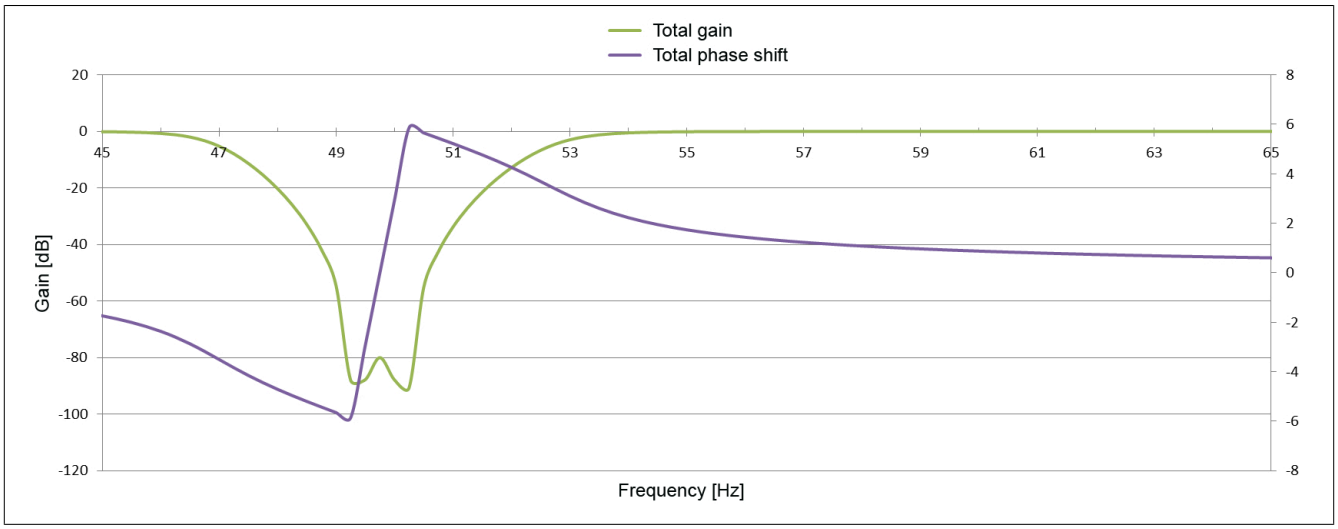
- Gain = -40 dB
- Frequency = 50 Hz
- Passband = 5 Hz
- Stopband = ±1 Hz



Example 2

Filter characteristics for the following settings:

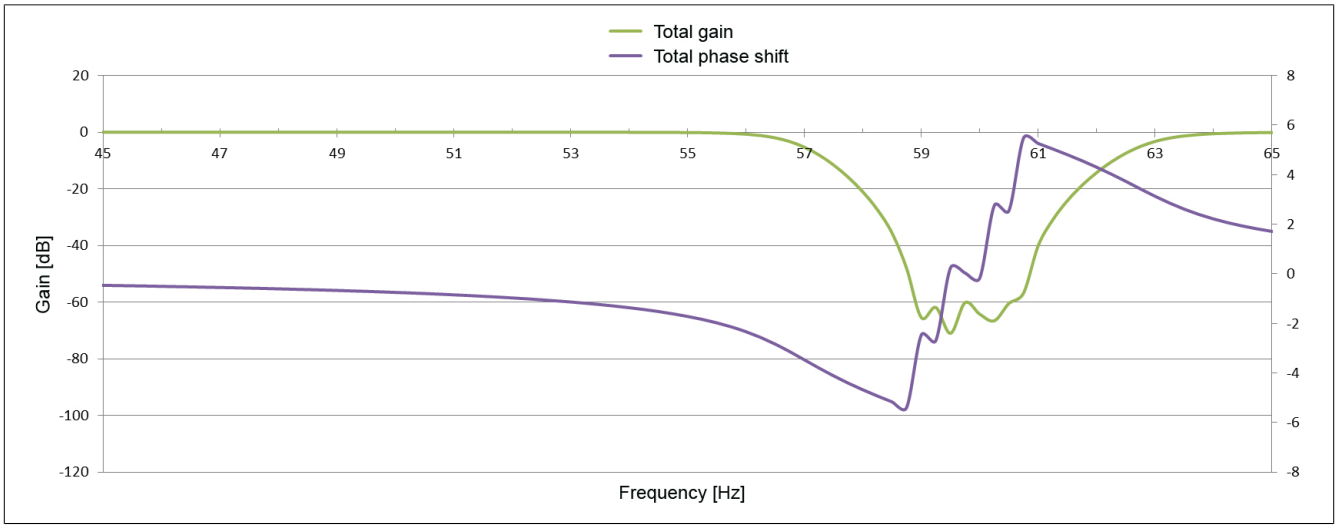
- Gain = -80 dB
- Frequency = 50 Hz
- Passband = 5 Hz
- Stopband = ±0.25 Hz



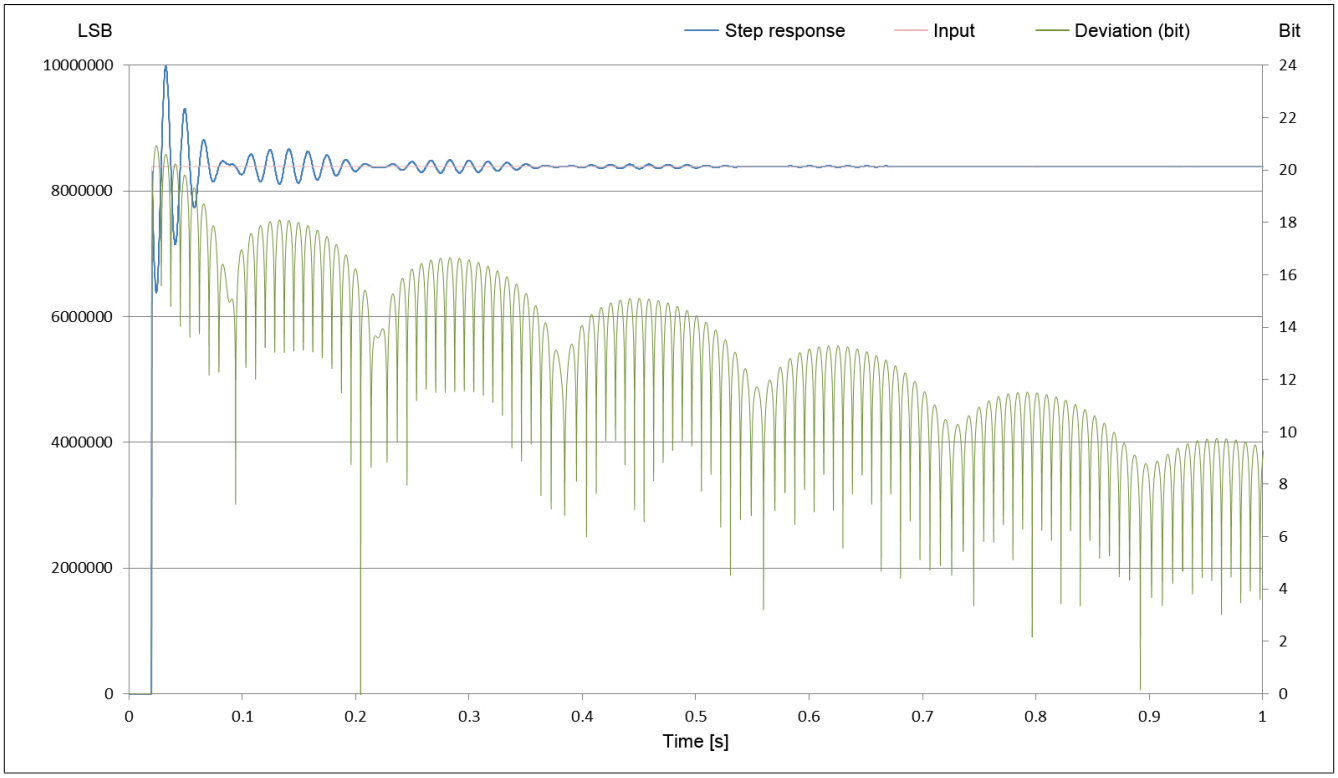
Example 3

Filter characteristics for the following settings:

- Gain = -60 dB
- Frequency = 60 Hz
- Passband = 5 Hz
- Stopband = ±0.5 Hz



Step response of an 8th-order IIR notch filter, including the deviation in bits:

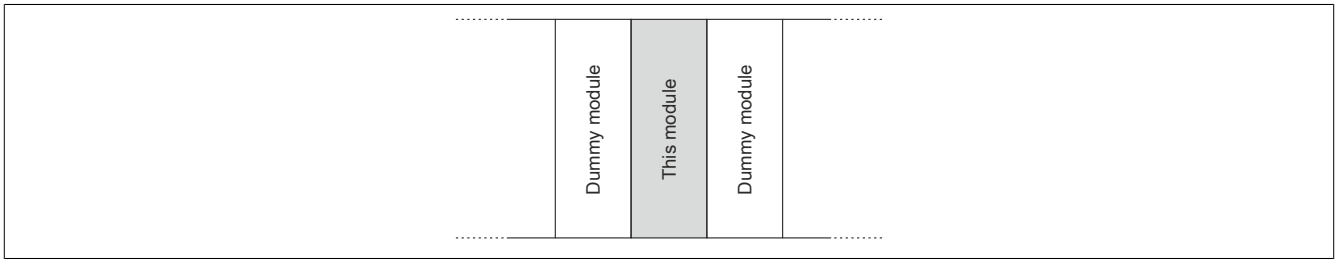


1.21.9 Hardware configuration

1.21.9.1 Hardware configuration for horizontal installation starting at 55°C ambient temperature

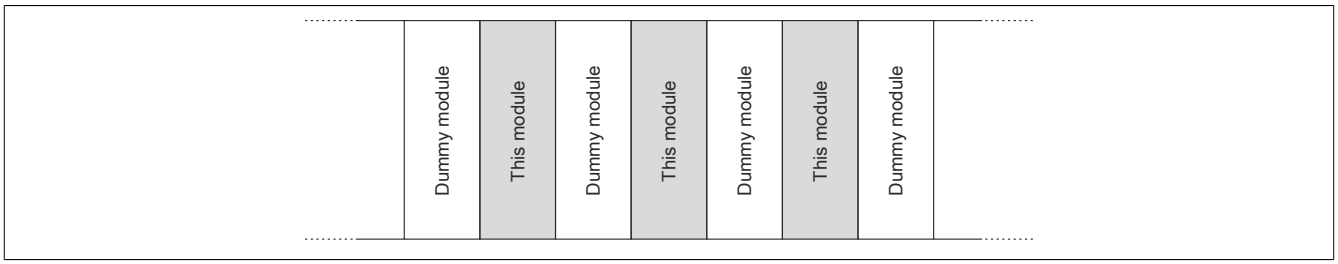
Operating a strain gauge module

Starting at an ambient temperature of 55°C, a dummy module must be connected to the left and right of the strain gauge module in a horizontal mounting orientation.



Operating multiple strain gauge modules side by side

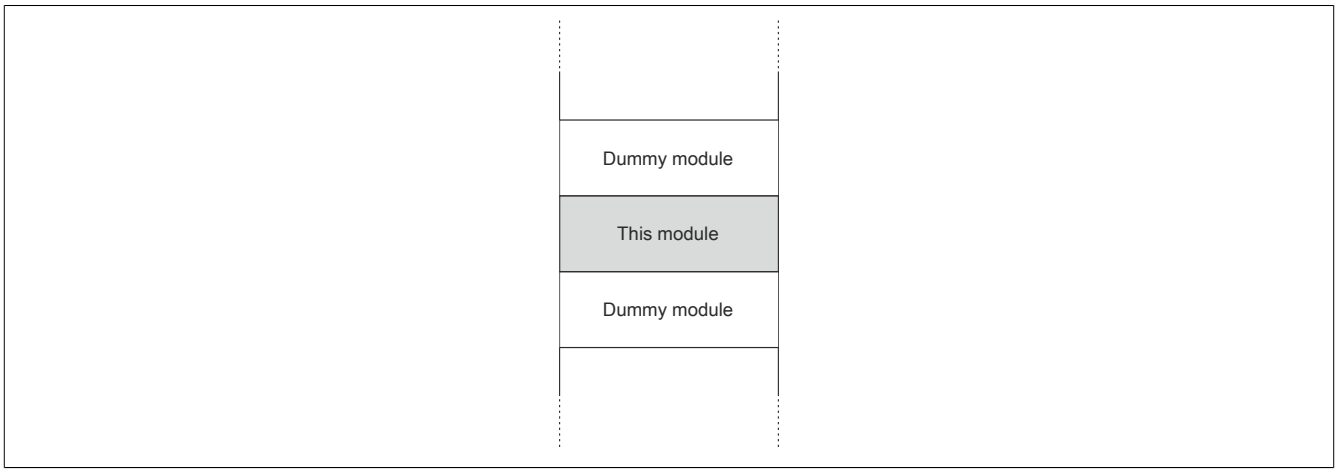
If 2 or more horizontal strain gauge modules are being operated in a cluster, the following arrangement of modules must be observed.



1.21.9.2 Hardware configuration for vertical installation starting at 45°C ambient temperature

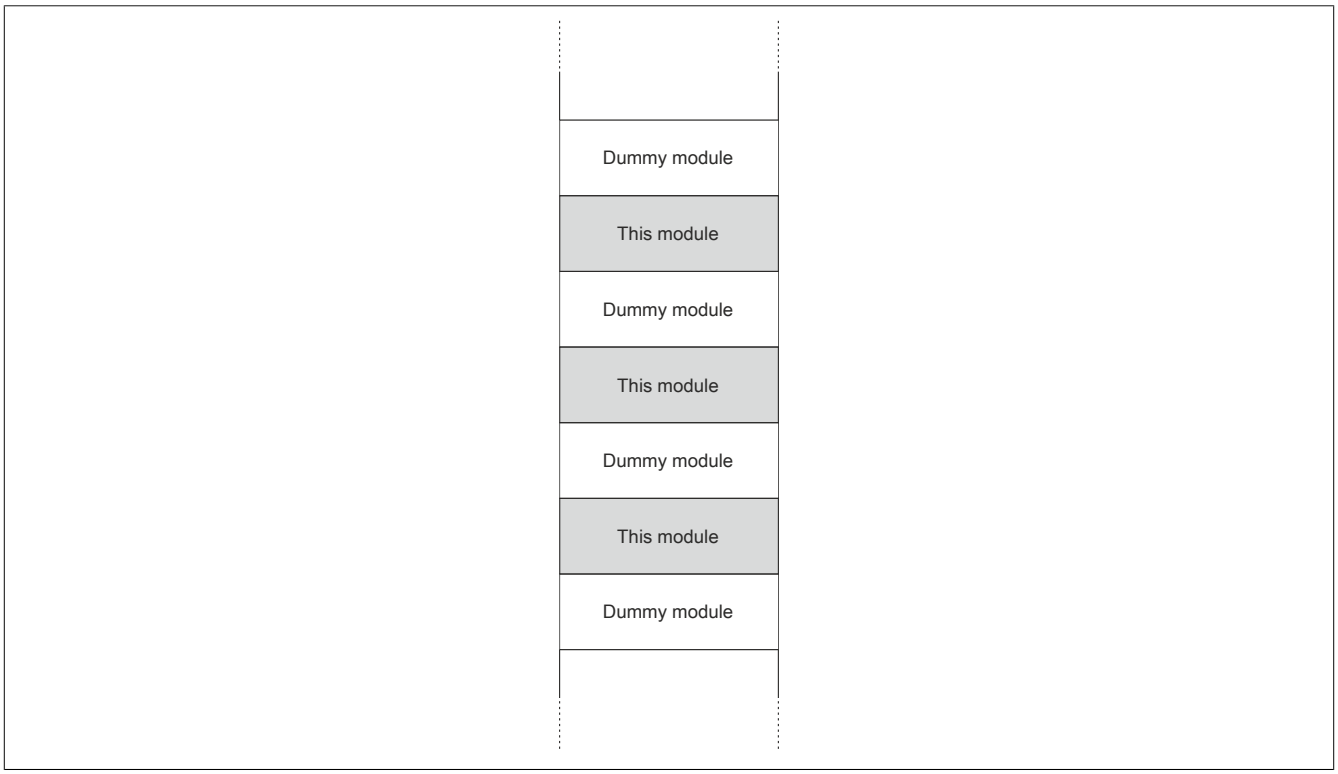
Operating a strain gauge module

Starting at an ambient temperature of 45°C, a dummy module must be connected to the left and right of the strain gauge module in a vertical mounting orientation.



Operating multiple strain gauge modules side by side

If 2 or more vertical strain gauge modules are being operated in a cluster, the following arrangement of modules must be observed.



1.21.10 Register description

1.21.10.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 system user's manual.

1.21.10.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration						
2	ControlPacked01 (configuration of strain gauge inputs)	UINT			•	
6	ControlPacked02 (configuration of strain gauge inputs)	UINT			•	
10	ControlPacked03 (configuration of strain gauge inputs)	UINT			•	
14	ControlPacked04 (configuration of strain gauge inputs)	UINT			•	
514	ConfigChannel01 (channel configuration)	UINT				•
578	ConfigChannel02 (channel configuration)	UINT				•
642	ConfigChannel03 (channel configuration)	UINT				•
706	ConfigChannel04 (channel configuration)	UINT				•
Analog signal - Communication						
4	AnalogInput01	DINT	•			
12	AnalogInput02	DINT	•			
20	AnalogInput03	DINT	•			
28	AnalogInput04	DINT	•			
33	StatusPacked01	USINT	•			
35	StatusPacked02	USINT	•			
37	StatusPacked03	USINT	•			
39	StatusPacked04	USINT	•			
257	AdcConvCtr01	SINT	•			
268	AdcConvTimeStamp01	DINT	•			

1.21.10.3 Function model 254 - Bus controller

Register	Offset [1]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration							
2	2	ControlPacked01 (configuration of strain gauge inputs)	UINT			•	
6	10	ControlPacked02 (configuration of strain gauge inputs)	UINT			•	
10	18	ControlPacked03 (configuration of strain gauge inputs)	UINT			•	
14	26	ControlPacked04 (configuration of strain gauge inputs)	UINT			•	
514	514	ConfigChannel01 (channel configuration)	UINT				•
578	578	ConfigChannel02 (channel configuration)	UINT				•
642	642	ConfigChannel03 (channel configuration)	UINT				•
706	706	ConfigChannel04 (channel configuration)	UINT				•
Analog signal - Communication							
4	4	AnalogInput01	DINT	•			
12	12	AnalogInput02	DINT	•			
20	20	AnalogInput03	DINT	•			
28	28	AnalogInput04	DINT	•			
33	0	StatusPacked01	USINT	•			
35	8	StatusPacked02	USINT	•			
37	16	StatusPacked03	USINT	•			
39	24	StatusPacked04	USINT	•			

1) The offset specifies the position of the register within the CAN object.

1.21.10.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

1.21.10.3.2 CAN I/O bus controller

The module occupies 4 analog logical slots on CAN I/O.

1.21.10.4 Configuration

1.21.10.4.1 Configuration of strain gauge inputs

Name:
ControlPacked01 to ControlPacked04

The strain gauge inputs are configured in these registers:

- Strain gauge factor of strain gauge load cell
- Enabling of filters

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information	
0 - 2	Strain gauge factor	000	Default: 256 mV/V	
		001	128 mV/V	
		010	64 mV/V	
		011	32 mV/V	
		100	16 mV/V	
		101	8 mV/V	
		110	4 mV/V	
		111	2 mV/V	
			Averaging	1. Notch frequency [Hz]
3 - 7	Moving average	00000	Default: Moving average disabled (bypass)	
		00001	2	2500
		00010	4	1250
		00011	5	1000
		00100	10	500
		00101	20	250
		00110	25	200
		00111	50	100
		01000	83	60
		01001	100	50
		01010	125	40
		01011	167	30
		01100	200	25
		01101	250	20
		01110	300	16.66
		01111	500	10
		10000	1000	5
		10001 to 11111	Reserved (firmware limited to 1000)	
8	Notch filter	0	Default: IIR notch filter disabled (bypass)	
		1	IIR notch filter enabled	
9	Reserved	0		
10 - 11	Low-pass filter mode	00	IIR low-pass filter disabled (bypass)	
		01	1st-order IIR low-pass filter (see "IIR low-pass filter" on page 481)	
		10 - 11	Reserved: No IIR low-pass filter active	
			Filter level	-3 db frequency [Hz]
12 - 14	Low-pass filter level	000	1	575
		001	2	230
		010	3	106
		011	4	51
		100	5	25
		101	6	12.5
		110	7	6.2
		111	8	3.1
15	Reserved	0		

1.21.10.4.2 Channel configuration

Name:
ConfigChannel01 to ConfigChannel04

The IIR notch filter is configured individually for each channel in these registers.

Data type	Values	Bus controller default setting
UINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0 - 11	Reserved	0	
12 - 13	Notch filter attenuation	00	Gain: -40 dB Pass: ±5 Hz Stop: ±1 Hz (Bus controller default setting)
		01	Gain: -60 dB Pass: ±5 Hz Stop: ±0.5 Hz
		10	Gain: -80 dB Pass: ±5 Hz Stop: ±0.25 Hz
		11	Reserved
14	Notch filter frequency	0	With 50 Hz (bus controller default setting)
		1	At 60 Hz
15	Reserved	0	

1.21.10.5 Communication

1.21.10.5.1 Analog input values

Name:
AnalogInput01 to AnalogInput04

The analog input value is mapped in this register.

Data type	Value	Input signal:
DINT	-8,388,608	Negative invalid value
	-8,388,607	Negative full-scale deflection / Underflow
	-8,388,606 to 8,388,606	Valid range
	8,388,607	Positive full-scale deflection / Overflow / Open line

1.21.10.5.2 Module status

Name:
StatusPacked01 to StatusPacked04

These registers contain the current state of the module.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	I/O power supply	0	No error
		1	Error in power supply
1	Bypass current	0	No error
		1	Overcurrent (sum from all sensors)
2 - 3	Reserved	0	
4	A/D converter configuration	0	Already configured
		1	Not yet configured
5	Analog values	0	Analog value valid
		1	Analog value invalid (analog value = -8,388,608 = 0xFF800000). Possible causes: • Internal transfer error (XOR checksum verification) • Error in strain gauge supply (bit 1) • Error in I/O voltage supply (bit 0) • A/D converter not (yet) configured
6	Analog value range overrun	0	Analog value valid
		1	Analog value invalid. Possible causes: • Overflow / Open circuit (analog value = 8,388,607 = 0x007FFFFF) • Underflow (analog value = -8,388,607 = 0xFF800001)
7	Moving average filter	0	Moving average filter engaged
		1	Moving average filter not engaged Possible causes: • After changing the filter length • Consequence of the filter being reset by another error

1.21.10.5.3 A/D conversion counter

Name:
AdcConvCtr01

Instead of being measured simultaneously, the strain gauge channels of the module are measured according to the multiplexing procedure. The "AdcConvTimestamp01" on page 494 register contains the timestamp of the encoded last channel converted in the "AdcConvCtr01" register. The timestamp of the other channels can then be calculated later using this information.

Data type	Value
SINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 1	Index of the last converted channel	0	Analog input 1
		1	Analog input 2
		2	Analog input 3
		3	Analog input 4
2 - 7	Rotating cycle counter	x	Incremented at the end of a conversion cycle. All channels are converted in a conversion cycle.

1.21.10.5.4 A/D conversion timestamp

Name:
AdcConvTimestamp01

The timestamp of the last converted channel is stored in this register (see bits 0 and 1 in the "AdcConvCtr01" on page 494 register). This is always the point in time (in µs) at which the conversion of the latest A/D converter raw value is completed.

Data type	Value	Function
DINT	-2147483648 to 2147483647	Timestamp (in µs) of the last converted channel (see bits 0 and 1 in the A/D conversion counter)

The timestamp of the remaining channels can be determined in the application using the number and timestamp of the last converted channel according to the following table.

Channel	Age difference
4 - 3	47 µs
3 - 2	47 µs
2 - 1	47 µs
1 - 4	59 µs

Example:

- Latest channel (bit 0 - 1 in the AdcConvCtr01 register) = 01 (analog input 2):
- Timestamp: "AdcConvTimestamp01" register = 0 µs

Channel	Timestamp
2	0 µs
1	-47 µs
4	-47-59 = -106 µs
3	-47-59-47 = -153 µs

1.21.10.6 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

1.21.10.7 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time
200 µs

1.22 X20(c)AP31xx

1.22.1 General information

Power monitoring

These modules measure active, reactive and apparent power individually for each of the 3 phases as well as all of them collectively. The power consumption of each phase is also recorded individually and in total. In addition, the modules provide the RMS values for voltage and current on the 3 phases. When measuring the current, the value of the current through the neutral conductor can also be detected and monitored. Measurement of the mains frequency and the phase angle of the 3 phases (current and voltage) complete the power measurement data.

Energy management

The integrated functions on the modules map the immediate power requirements of the machine in detail as well as record its total power consumption. For the user, all relevant data is prepared and made available in the process image.

The ability to measure currents and voltages up to the 31st harmonic enables higher precision recording of RMS values than is generally possible. This allows the modules to easily cope with irregular sine curves and makes them well-suited to renewable energy applications. In these types of applications, for example, being able to accurately measure the frequency at a resolution of 0.01 Hz between 45 and 65 Hz is a great advantage. In general, the modules are suitable for use with 1-phase, 2-phase or 3-phase networks.

Characteristics

- Calculates RMS values from currents and voltages
- Calculates active, reactive and apparent power
- Phasing detection
- Measures individual phases and calculates cumulative values
- Optional measurement of current through the neutral conductor
- Calculates frequency and harmonics with high precision
- NetTime timestamp: Moment when measured value groups are read

NetTime timestamp of readout moments

Not only is the measured value important for many applications, but also the exact time when measured values are read out. The module is equipped with a NetTime timestamp function for this that supplies a timestamp for the recorded measurements with microsecond accuracy.

The timestamp function is based on synchronized timers. If a timestamp event occurs, the module immediately saves the current NetTime. After the respective data is transferred to the controller, including this precise moment, the controller can then evaluate the data using its own NetTime (or system time), if necessary.

1.22.1.1 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, method 4, exposure 21 days

1.22.1.1.1 Starting temperature

The starting temperature describes the minimum permissible ambient temperature in a voltage-free state at the time the coated module is switched on. This is permitted to be as low as -40°C. During operation, the conditions as specified in the technical data continue to apply.

Information:

It is important to absolutely ensure that there is no forced cooling by air currents in the closed control cabinet, e.g. due to the use of a fan or ventilation slots.

1.22.1.2 Other applicable documents

For additional and supplementary information, see the following documents.

Other applicable documents

Document name	Title
MAX20	X20 System user's manual
MAEMV	Installation / EMC guide

1.22.2 Order data

Order number	Short description	Figure
	Analog inputs	
X20AP3111	X20 energy metering module, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 20 mA AC, calculates effective, reactive and apparent power/energy, calculates RMS values, 240 V keyed, NetTime function	
X20AP3121	X20 energy metering module, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 1 A AC, calculates effective, reactive and apparent power/energy, calculates RMS values, 240 V keyed, NetTime function	
X20AP3131	X20 energy metering module, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 5 A AC, calculates effective, reactive and apparent power/energy, calculates RMS values, 240 V keyed, NetTime function	
X20AP3161	X20 energy metering module, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 333 mV AC, calculates effective, reactive and apparent power/energy, calculates RMS values, 240 V keyed, NetTime function	
X20AP3171	X20 energy metering module, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, Rogowski adjustable (µV/A), max. 52 mV, calculates effective, reactive and apparent power/energy, calculates RMS values, 240 V keyed, NetTime function	
X20AP3122	X20 energy metering module, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 1 A AC, groundable, calculates effective, reactive and apparent power/energy, calculates RMS values, 240 V keyed, NetTime function	
X20AP3132	X20 energy metering module, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 5 A AC, groundable, calculates effective, reactive and apparent power/energy, calculates RMS values, 240 V keyed, NetTime function	
X20cAP3121	X20 energy metering module, coated, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 1 A AC, calculates effective, reactive and apparent power/energy, calculates RMS values, 240 V keyed, NetTime function	
X20cAP3131	X20 energy metering module, coated, 3 analog inputs, 480 VAC, 50/60 Hz, 4 analog inputs, 5 A AC, calculates effective, reactive and apparent power/energy, calculates RMS values, 240 V keyed, NetTime function	
	Required accessories	
	Bus modules	
X20BM32	X20 bus module, for double-width modules, 240 VAC keyed, internal I/O power supply connected through	
X20cBM32	X20 bus module, coated, for double-width modules, 240 VAC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB32	X20 terminal block, 12-pin, 240 VAC keyed	

Table 71: X20AP3111, X20AP3121, X20AP3131, X20AP3161, X20AP3171, X20AP3122, X20AP3132, X20cAP3121, X20cAP3131 - Order data

1.22.3 Technical description

1.22.3.1 Technical data

1.22.3.1.1 X20AP3111, X20(c)AP3121 and X20(c)AP3131

Order number	X20AP3111	X20AP3121	X20cAP3121	X20AP3131	X20cAP3131
Short description					
I/O module	3-phase power and energy metering module for current transformers				
General information					
B&R ID code	0xC9DA	0xC9DB	0xE214	0xC9DC	0xEB55
Status indicators	I/O function per channel, operating state, module status				
Diagnostics					
Module run/error	Yes, using LED status indicator and software				
Inputs	Yes, using LED status indicator and software				
Power consumption					
Bus	0.85 W (Rev. <D0) 0.50 W (Rev. =D0) 0.45 W (Rev. >D0)		0.85 W (Rev. <C0) 0.50 W (Rev. =C0) 0.45 W (Rev. >C0)	0.85 W (Rev. <E0) 0.50 W (Rev. =E0) 0.45 W (Rev. >E0)	
Internal I/O	-				
Additional module power dissipation [W]	40 mW [1]	2 W [1]			
Insulation voltages					
Inputs - Bus / I/O power supply	Tested at 5500 VDC, 1 min				
Inputs - Ground	Tested at 5500 VDC, 1 min				
Bus / I/O power supply - Ground	Tested at 510 VAC, 1 min				
Certifications					
CE	Yes				
UKCA	Yes				
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X				
UL	cULus E115267 Industrial control equipment				
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5		-	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5	
DNV	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)				
LR	ENV1				
KR	Yes				
ABS	Yes				
EAC	Yes		-	Yes	-
Voltage inputs					
Number of phases	3				
Input impedance	1.68 MΩ				
Nominal voltage U_N					
Between phases	Max. 480 VAC [2]				
Phase to N	Max. 277 VAC				
Max. display value	655 VAC				
Resolution	10 mV, with voltage connected directly				
Rated frequency	50 and 60 Hz				
Measurable frequency					
Measurement range	45 to 65 Hz				
Resolution	0.01 Hz				
Current inputs					
Quantity	4 AC inputs				
Nominal current I_N					
Secondary	20 mA	1 A		5 A	
Primary	65 A directly configurable, larger values through conversion in the application [3]				
Max. overload current	20 x I_N for 0.5 s	8 x I_N for 0.5 s			
Max. measurement current	20 mA	1 A		5 A	
Resolution	1 mA, based on the primary current [3]				
Load	25 Ω	500 mΩ		20 mΩ	
Measurement accuracy [4]					
U_{RMS} and I_{RMS}	<0.5%				-
U_{RMS}	±0.65% [5]				
I_{RMS}	±0.65% [6]	±0.65% [7]		±1.65% (Rev. <E0) ±0.70% (Rev. ≥E0) [8]	±0.70% [8]
Effective, reactive and apparent power	±0.80% [9]	±0.80% [10]		±1.80% (Rev. <E0) ±0.85% (Rev. ≥E0) [11]	±0.85% [11]

Table 72: X20AP3111, X20AP3121, X20cAP3121, X20AP3131, X20cAP3131 - Technical data

Order number	X20AP3111	X20AP3121	X20cAP3121	X20AP3131	X20cAP3131
Frequency, power factor and phase angle	±0.50% [12]				
Calibration accuracy	<0.15%				-
Active energy per phase and total [13]	±0.40% [9]	±0.40% [10]		±1.40% (Rev. <E0) ±0.45% (Rev. ≥E0) [11]	±0.45% [11]
Active energy per phase and total					
Power factor = 1.0	0.1%				-
Power factor = 0.5 L	0.1%				-
Power factor = 0.8 C	0.1%				-
Active energy of fundamental frequency per phase and total [13]	±0.50% [9]	±0.50% [10]		±1.50% (Rev. <E0) ±0.55% (Rev. ≥E0) [11]	±0.55% [11]
Active energy of fundamental frequency per phase and total					
Power factor = 1.0	0.2%				-
Power factor = 0.5 L	0.2%				-
Power factor = 0.8 C	0.2%				-
Active energy of harmonics per phase and total [13]	±0.80% [9]	±0.80% [10]		±1.80% (Rev. <E0) ±0.85% (Rev. ≥E0) [11]	±0.85% [11]
Active energy of harmonics per phase and total					
sin ϕ = 1.0	0.5%				-
sin ϕ = 0.5 L	0.5%				-
sin ϕ = 0.8 C	0.5%				-
Reactive energy per phase and total [14]	±0.50% [9]	±0.50% [10]		±1.50% (Rev. <E0) ±0.55% (Rev. ≥E0) [11]	±0.55% [11]
Reactive energy per phase and total					
sin ϕ = 1.0	0.2%				-
sin ϕ = 0.5 L	0.2%				-
sin ϕ = 0.8 C	0.2%				-
Apparent energy					
Per phase and arithmetic total	±0.50% [9]	±0.50% [10]		±1.50% (Rev. <E0) ±0.55% (Rev. ≥E0) [11]	±0.55% [11]
Vector sum	±0.80% [9]	±0.80% [10]		±1.80% (Rev. <E0) ±0.85% (Rev. ≥E0) [11]	±0.85% [11]
Electrical properties					
Electrical isolation	Channel isolated from bus Channel not isolated from channel				
Operating conditions					
Mounting orientation					
Horizontal	Yes				
Vertical	Yes				
Installation elevation above sea level					
0 to 2000 m	No limitation				
>2000 m	Not permitted				
Degree of protection per EN 60529	IP20				
Ambient conditions					
Temperature					
Operation					
Horizontal mounting orientation	-25 to 60°C				
Vertical mounting orientation	-25 to 50°C				
Derating	-	See section "Derating".			
Storage	-40 to 85°C				
Transport	-40 to 85°C				
Relative humidity					
Operation	5 to 95%, non-condensing		Up to 100%, condensing	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing				
Transport	5 to 95%, non-condensing				
Mechanical properties					
Note	Order 1x terminal block X20TB32 separately. Order 1x bus module X20BM32 separately.		Order 1x terminal block X20TB32 separately. Order 1x bus module X20cBM32 separately.	Order 1x terminal block X20TB32 separately. Order 1x bus module X20BM32 separately.	Order 1x terminal block X20TB32 separately. Order 1x bus module X20cBM32 separately.
Pitch	$25^{+0.2}$ mm				

Table 72: X20AP3111, X20AP3121, X20cAP3121, X20AP3131, X20cAP3131 - Technical data

1) Power dissipation of current measurement shunts
2) The design of the module allows 480 VAC to be applied to the terminal block.
3) For measuring higher current values, see section "Current transformer - Pinout".
4) Based on the current measured value.
   The actual error value percentage may be larger due to the digital display.
5) With drift of 25 ppm/K
6) With drift of 50 ppm/K
7) With drift of 35 ppm/K
8) With drift of 225 ppm/K (Rev. < E0) or 100 ppm/K (Rev. ≥ E0)

9) With drift of 75 ppm/K
10) With drift of 60 ppm/K
11) With drift of 250 ppm/K (Rev. < E0) or 125 ppm/K (Rev. ≥ E0)
12) In power systems with approximately sinusoidal voltage starting at 10 VAC.
13) At power factor cos ϕ = 1, 0.5L and 0.8C
14) At reactive power factor sin ϕ = 1, 0.5L and 0.8C

1.22.3.1.2 X20AP3122 and X20AP3132

Order number	X20AP3122	X20AP3132
Short description		
I/O module	3-phase power and energy metering module for current transformers, groundable on one side	
General information		
B&R ID code	0xE7BF	0xE7C0
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using LED status indicator and software	
Inputs	Yes, using LED status indicator and software	
Power consumption		
Bus	0.85 W (Rev. <C0) 0.50 W (Rev. =C0) 0.45 W (Rev. >C0)	
Internal I/O	-	
Additional module power dissipation [W]	2 W [1]	
Insulation voltages		
Voltage inputs - Current inputs	Tested at 1300 VAC, 1 min	
Inputs - Bus / I/O power supply	Tested at 5500 VDC, 1 min	
Inputs - Ground	Tested at 5500 VDC, 1 min	
Bus / I/O power supply - Ground	Tested at 510 VAC, 1 min	
Certifications		
CE	Yes	
UKCA	Yes	
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X	
UL	cULus E115267 Industrial control equipment	
EAC	Yes	
Voltage inputs		
Number of phases	3	
Input impedance	1.68 MΩ	
Measurement category	CAT II	
Nominal voltage U_N		
Between phases	Max. 480 VAC [2]	
Phase to N	Max. 277 VAC	
Max. display value	655 VAC	
Resolution	10 mV, with voltage connected directly	
Rated frequency	50 and 60 Hz	
Measurable frequency		
Measurement range	45 to 65 Hz	
Resolution	0.01 Hz	
Current inputs		
Quantity	4 AC inputs	
Measurement category	CAT II	
Nominal current I_N		
Secondary	1 A	5 A
Primary	65 A directly configurable, larger values through conversion in the application [3]	
Max. overload current	8 x I_N for 0.5 s	
Max. measurement current	1 A	5 A
Resolution	1 mA, based on the primary current [3]	
Load	250 mΩ	20 mΩ
Measurement accuracy [4]		
U_{RMS}	±0.65% [5]	
I_{RMS}	±0.65% [6]	±0.65% [5]
Effective, reactive and apparent power	±0.80% [7]	±0.80% [8]
Frequency, power factor and phase angle	±0.50% [9]	
Active energy per phase and total [10]	±0.40% [7]	±0.40% [8]
Active energy of fundamental frequency per phase and total [10]	±0.50% [7]	±0.50% [8]
Active energy of harmonics per phase and total [10]	±0.80% [11]	±0.80% [8]
Reactive energy per phase and total [12]	±0.50% [7]	±0.50% [8]
Apparent energy		
Per phase and arithmetic total	±0.50% [7]	±0.50% [8]
Vector sum	±0.80% [7]	±0.80% [8]
Electrical properties		
Electrical isolation	Channel isolated from bus Channel not isolated from channel	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	

Table 73: X20AP3122, X20AP3132 - Technical data

Order number	X20AP3122	X20AP3132
Installation elevation above sea level		
0 to 2000 m	No limitation	
>2000 m	Not permitted	
Degree of protection per EN 60529	IP20	
Ambient conditions		
Temperature		
Operation		
Horizontal mounting orientation	-25 to 60°C	
Vertical mounting orientation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical properties		
Note	Order 1x terminal block X20TB32 separately. Order 1x bus module X20BM32 separately.	
Pitch	$25^{+0.2}$ mm	

Table 73: X20AP3122, X20AP3132 - Technical data

1) Power dissipation of current measurement shunts
2) The design of the module allows 480 VAC to be applied to the terminal block.
3) For measuring higher current values, see section "Current transformer - Pinout".
4) Based on the current measured value.
   The actual error value percentage may be larger due to the digital display.
5) With drift of 25 ppm/K
6) With drift of 100 ppm/K
7) With drift of 125 ppm/K
8) With drift of 50 ppm/K
9) In power systems with approximately sinusoidal voltage starting at 10 VAC.
10) At power factor cos ϕ = 1, 0.5L and 0.8C
11) With drift of 125 ppm/K (Rev. < D0) or 40 ppm/K (Rev. ≥ D0)
12) At reactive power factor sin ϕ = 1, 0.5L and 0.8C

1.22.3.1.3 X20AP3161 and X20AP3171

Order number	X20AP3161	X20AP3171
Short description		
I/O module	3-phase power and energy metering module for current/voltage transformers	3-phase power and energy metering module for Rogowski current transformers
General information		
B&R ID code	0xE17B	0xE7C1
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using LED status indicator and software	
Inputs	Yes, using LED status indicator and software	
Power consumption		
Bus	0.85 W (Rev. <D0) 0.50 W (Rev. =D0) 0.45 W (Rev. >D0)	0.85 W (Rev. <C0) 0.50 W (Rev. =C0) 0.45 W (Rev. >C0)
Internal I/O	-	
Additional module power dissipation [W]	- [1)]	
Insulation voltages		
Current inputs / Neutral conductor - Ground	-	Tested at 2300 VAC, 1 min
Voltage inputs / Neutral conductor - Ground	-	Tested at 3700 VAC, 1 min
Current inputs / Neutral conductor - Bus / I/O power supply	-	Tested at 2300 VAC, 1 min
Voltage inputs / Neutral conductor - Bus / I/O power supply	-	Tested at 3700 VAC, 1 min
Inputs - Bus / I/O power supply	Tested at 5500 VDC, 1 min	
Inputs - Ground	Tested at 5500 VDC, 1 min	
Bus / I/O power supply - Ground	Tested at 510 VAC, 1 min	
Certifications		
CE	Yes	
UKCA	Yes	
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X	
UL	cULus E115267 Industrial control equipment	
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5	-
DNV	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)	-
LR	ENV1	-
KR	Yes	-
ABS	Yes	-
EAC	Yes	
Voltage inputs		
Number of phases	3	
Input impedance	1.68 MΩ	
Measurement category	-	CAT II
Nominal voltage U_N		
Between phases	Max. 480 VAC [2)]	
Phase to N	Max. 277 VAC	
Max. display value	655 VAC	
Resolution	10 mV, with voltage connected directly	
Rated frequency	50 and 60 Hz	
Measurable frequency		
Measurement range	45 to 65 Hz	
Resolution	0.01 Hz	
Current inputs		
Quantity	4 AC inputs	
Measurement category	-	CAT II
Nominal voltage (secondary)	333 mV	Configurable in µV/A
Nominal current (primary)	65 A directly configurable, larger values through conversion in the application [3)]	
Max. overload current	-	
Max. measurement voltage	333 mV	52 mV
Resolution	1 mA, based on the primary current [3)]	
Load	-	
Measurement accuracy [4)]		
U_{RMS} and I_{RMS}	<0.5%	-
U_{RMS}	±0.65% [5)]	
I_{RMS}	±0.65%	±0.85% [6)]
Effective, reactive and apparent power	±0.80% [5)]	±1.00%

Table 74: X20AP3161, X20AP3171 - Technical data

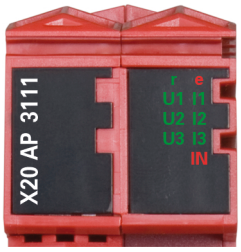
Order number	X20AP3161	X20AP3171
Frequency, power factor and phase angle	±0.50% 7)	
Calibration accuracy	<0.15%	-
Active energy per phase and total 8)	±0.40% 5)	±0.60% 5)
Active energy per phase and total		
Power factor = 1.0	0.1%	-
Power factor = 0.5 L	0.1%	-
Power factor = 0.8 C	0.1%	-
Active energy of fundamental frequency per phase and total 8)	±0.50% 5)	±0.70% 5)
Active energy of fundamental frequency per phase and total		
Power factor = 1.0	0.2%	-
Power factor = 0.5 L	0.2%	-
Power factor = 0.8 C	0.2%	-
Active energy of harmonics per phase and total 8)	±0.80% 5)	±1.00% 5)
Active energy of harmonics per phase and total		
sin ϕ = 1.0	0.5%	-
sin ϕ = 0.5 L	0.5%	-
sin ϕ = 0.8 C	0.5%	-
Reactive energy per phase and total 9)	±0.50% 5)	±0.70% 5)
Reactive energy per phase and total		
sin ϕ = 1.0	0.2%	-
sin ϕ = 0.5 L	0.2%	-
sin ϕ = 0.8 C	0.2%	-
Apparent energy		
Per phase and arithmetic total	±0.50% 5)	±0.70% 5)
Vector sum	±0.80% 5)	±1.00% 5)
Electrical properties		
Electrical isolation	Channel isolated from bus Channel not isolated from channel	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation elevation above sea level		
0 to 2000 m	No limitation	
>2000 m	Not permitted	
Degree of protection per EN 60529	IP20	
Ambient conditions		
Temperature		
Operation		
Horizontal mounting orientation	-25 to 60°C	
Vertical mounting orientation	-25 to 50°C	
Derating	-	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical properties		
Note	Order 1x terminal block X20TB32 separately. Order 1x bus module X20BM32 separately.	Order 1x terminal block X20TB32 separately. Order 1x bus module X20BM32 separately.
Pitch	$25^{+0.2}$ mm	

Table 74: X20AP3161, X20AP3171 - Technical data

1) Shunts are external in the current transformer.
2) The design of the module allows 480 VAC to be applied to the terminal block.
3) For measuring higher current values, see section "Current transformer - Pinout".
4) Based on the current measured value.
The actual error value percentage may be larger due to the digital display.
5) With drift of 25 ppm/K
6) At URogowski > 1 mVRMS
7) In power systems with approximately sinusoidal voltage starting at 10 VAC.
8) At power factor cos ϕ = 1, 0.5L and 0.8C
9) At reactive power factor sin ϕ = 1, 0.5L and 0.8C

1.22.3.2 LED status indicators

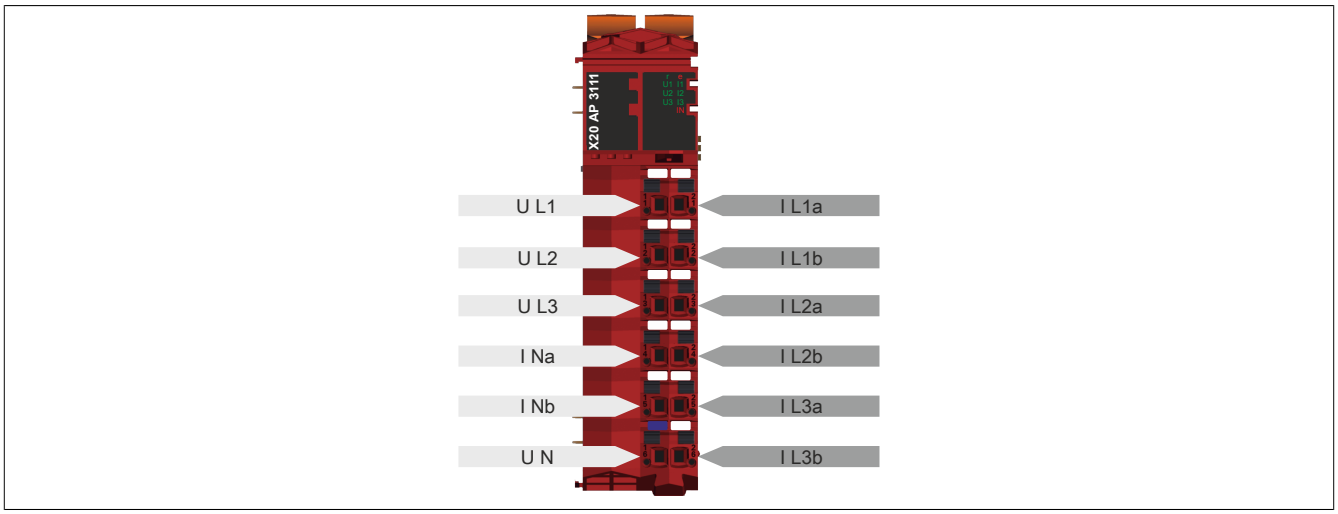
For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 System user's manual.

Figure	LED	Color	Status	Description
	**Operating state**			
	r	Green	Off	No power to module
			Single flash	UNLINK mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking quickly	SYNC mode
			Blinking slowly	PREOPERATIONAL mode
			On	RUN mode
	Module status			
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	Analog input voltage			
	U1 - U3	Green/Yellow	Off	Display disabled or U_{Eff} < threshold value "Failure"
		Green	Blinking	Phase sequence is correct and U_{Eff} < threshold value "Warning"
			On	Phase sequence is correct and U_{Eff} > threshold value "Warning"
		Yellow	Blinking	Phase sequence is incorrect and U_{Eff} < threshold value "Warning"
			On	Phase sequence is incorrect and U_{Eff} > threshold value "Warning"
	Analog input current			
	I1 - I3	Green/Yellow	Off	Display disabled or I_{Eff} < threshold value "Display"
		Green	On	Active power positive
		Yellow	On	Active power negative
	Analog input neutral current			
	IN		Off	Neutral current < Threshold value
		Green	On	Neutral current > Threshold value "Failure", within the tolerance of the calculated total current
		Red	On	Neutral current > Threshold value "Failure", outside the tolerance of the calculated total current

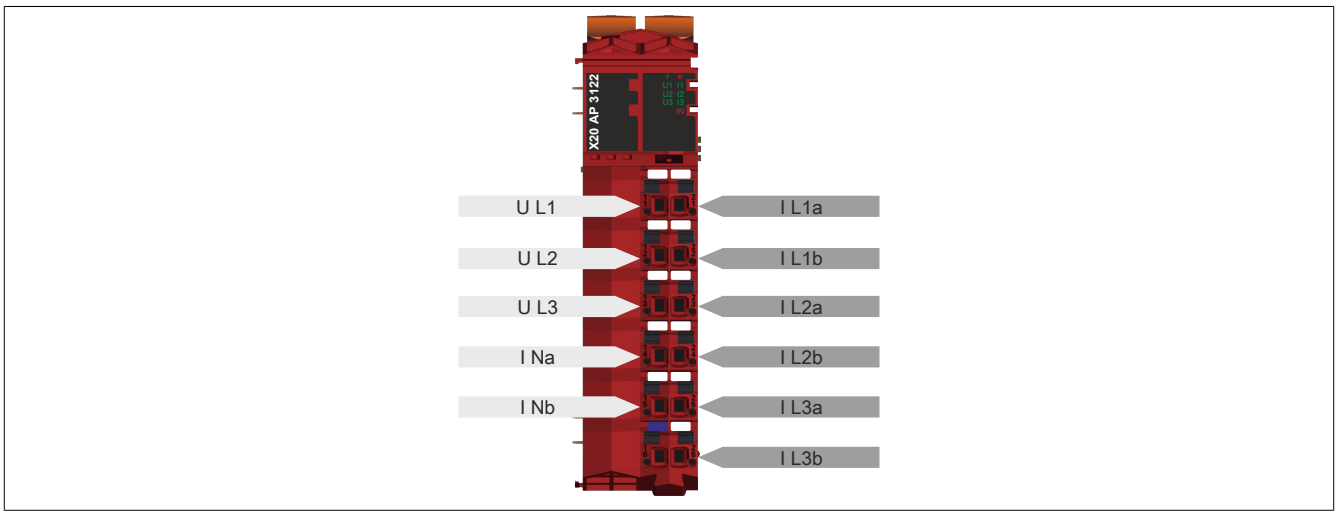
1) Depending on the configuration, a firmware update can take up to several minutes.

1.22.3.3 Pinout

X20AP31x1



X20AP31x2



Danger!

Risk of electric shock!

The terminal block is only permitted to conduct voltage when it is connected. It is not permitted to be disconnected or connected while voltage is applied or have voltage applied to it while it is removed under any circumstances!

This module is not permitted to be the last module connected on the X2X Link network. At least one subsequent X20ZF dummy module must provide protection against contact.

Shielding

Shielded cables must be used for the current channels of module X20AP3171 in order to maintain the specified accuracy. Cabling can either take place using one cable per channel or a multiple twisted pair cable for multiple channels.

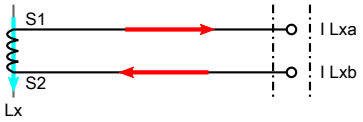
Information:

Shielded cables must be grounded on both sides.

1.22.3.3.1 Connecting current transformers

In order to be able to properly calculate values, it is important for the current transformer phases to be connected correctly (i.e. direction of the current flow).

- Output on the transformer (S1) to the respective ILxa input on the module.
- Input on the transformer (S2) to the respective ILxb output on the module.



1.22.3.4 Safety guidelines

General

Information:

If the maximum voltage value of 655 V is displayed, it is necessary to check whether the input measurement range has been exceeded.

Caution!

The insulation for all current inputs must be double or reinforced.

X20AP31x2

X20AP31x2 modules with current transformers that are groundable meet the requirement from the median voltage guideline that states that a current transformer connection must always be grounded in systems that exceed a certain system voltage.

Caution!

Only a connection labeled "ILxb" is permitted to be grounded.

Caution!

The use of modules with current transformers that groundable is only permitted in systems with grounded median voltage. Operating these modules without connected grounding is not permitted.

Information:

Because these modules do not feature a neutral conductor connection, the ground potential on the current transformer connections forms the central reference point. (See "Input circuit diagram" on page 510.)

Danger!

In the event of a fault (e.g. a break in insulation), further insulating measures have to be taken in addition to the basic insulation between voltage and current inputs on the module.
To avoid electric shocks, the wiring to the module must have adequate insulation. The dielectric strength of the cable insulation MUST be designed for the level of phase-to-phase nominal voltage.

1.22.3.5 Current transformers

Since the current inputs are not floating, a current transformer is required for each current channel used. The current transformer is a transducer that delivers a secondary signal proportional to the primary current. This secondary signal is measured by the module. The maximum directly configurable primary current is 65 A. Values greater than 65 A can also be measured by implementing a conversion in the software application (see explanation and example provided below).

The maximum secondary signal depends on the module:

Module	Secondary current/voltage
X20AP3111	20 mA
X20AP3121	1 A
X20AP3122	1 A
X20AP3131	5 A
X20AP3132	5 A
X20AP3161	333 mV
X20AP3171	Configurable, maximum 52 mV

The rated transformation ratio is calculated using the following formula:

X20AP3111 - X20AP3121 - X20AP3131 - X20AP3122 - X20AP3132	Rated transformation ratio $K_n = \frac{\text{Primary nominal current}}{\text{Secondary nominal current}}$
X20AP3161	No transformation; the maximum primary current corresponds to the 333 mV.
X20AP3171	Direct input of µV/A

A smaller transformation ratio should be defined for measuring higher primary currents. The values calculated by the module must be converted in the application according to the real rated transformation ratio that must be defined.

Examples

Information:

The same factor must be used for all power ratings and energy values when making the conversion.

All AP modules except for AP3171

Currents of up to 100 A flow on the primary side. A current transformer with a rated transformation ratio of 100 to 1 A or a measurement range of 100 A is used. A rated transformation ratio of 50 to 1 A or a measurement range of 50 A is defined in the module to match the current transformer. If the primary current calculated by the module is 40 A, then the actual value will be calculated as follows:

Actual primary current = 40 A * 100 / 50 = 80 A
Actual resolution = 1 mA * 100 / 50 = 2 mA

Because the primary current can be up to 300 A, a Rogowski coil with a primary current range of up to 500 A is used. This exhibits a transformation ratio of 100 µV/A.
Since the module can only supply values up to 65000, however, only a maximum of 65 A could be displayed or measured with it. The transformation ratio of the phases must therefore additionally be set.

The unit of the phase is 0.1 µV/A; the transformation ratio must therefore be converted. For example, the value 5000 * 0.1 µV corresponds to 500 µV/A.

Example
The transformation ratio of the Rogowski coil is 100 µV/A.
The transformation ratio of the phase is set to value 5000.
The module returns a value of 8155 mA.

The calculation is made according to this formula:

$$\text{Value} = \frac{\text{Transformation ratio}_{\text{Phase}} * \text{Unit}_{\text{Phase}}}{\text{Transformation ratio}_{\text{Rogowski}}} * \text{Measured value}$$

This results in this value for our example:

$$\frac{5000 * 0.1\mu V/A}{100\mu V/A} * 8155 = 40.775\ A$$

Maximum primary current that can be measured by the module:

$$\text{Primary current}_{\text{Maximum}} = \frac{8000_{\text{Phase}} * \text{Unit}_{\text{Phase}}}{\text{Transformation ratio}_{\text{Rogowski}}} * 65000$$

Caution!

To avoid damage to the module, ensure that the current inputs are floating. A current transformer must therefore be connected to each current input used.

Any other devices connected to this secondary circuit must be galvanically isolated.

X20AP31x1:

The current inputs on the module are not galvanically isolated, so the secondary circuit between the transformer and the module is not permitted to be grounded. Grounding or making other conductive connections between the transformers distorts the measurement and results in current values that are too low!

X20AP31x2:

Since the "ILxb" connections on the current inputs are all at the same electric potential, the transformers on the "Lxb" side must be grounded for these modules.

1.22.3.6 Voltage transformer

Voltage transformers are not provided in the configuration by default (e.g. by setting the transformation ratio).

However, voltage transformers can be used if higher voltages need to be measured than are specified under nominal voltages in the technical data.

In addition, as with current value correction, the rated transformation between primary and secondary current must be calculated and applied (see "Current transformers" on page 508)

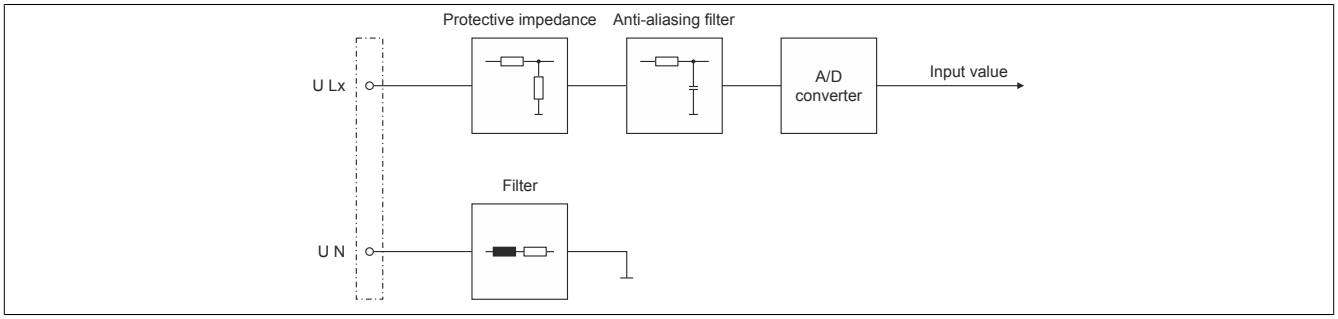
Information:

The same factor must be used for all voltage values, power ratings and energy values when making the transformation.

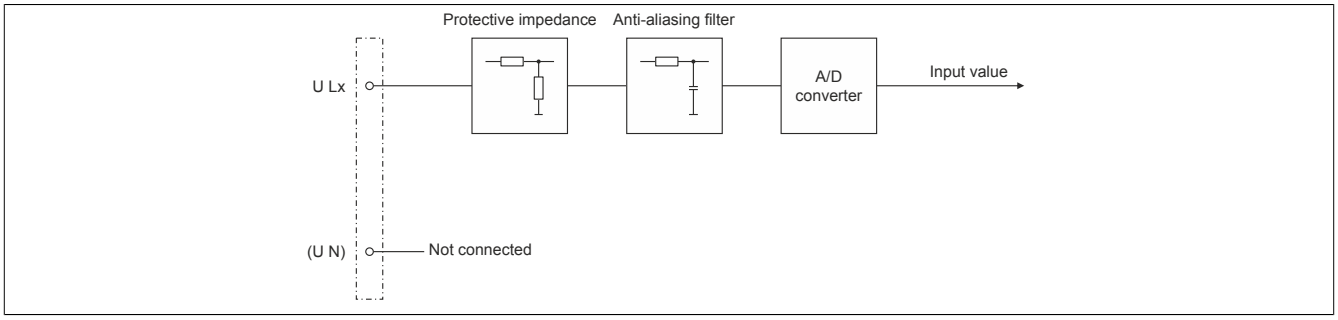
1.22.3.7 Input circuit diagram

AC voltage inputs

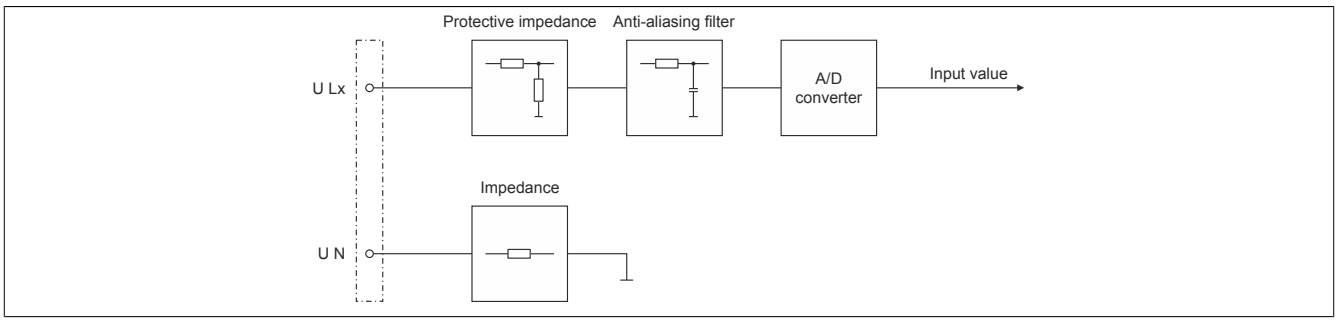
AP3111, AP3121, AP3131, AP3161



AP3122, AP3132

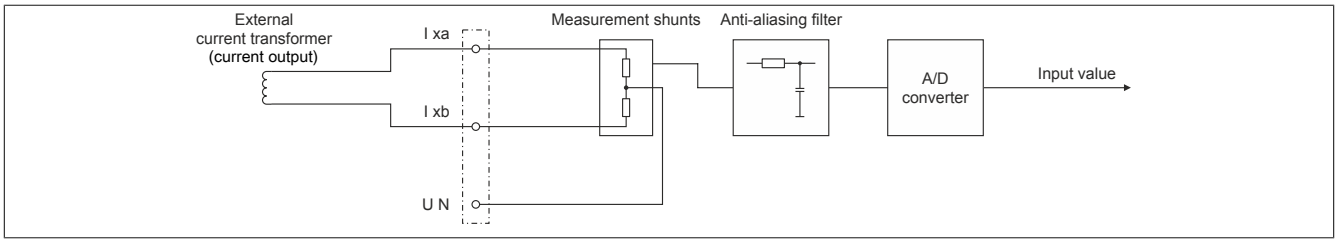


AP3171

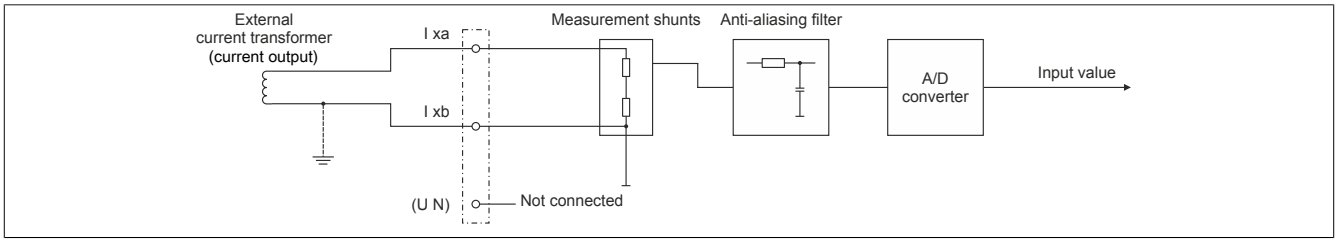


AC current inputs

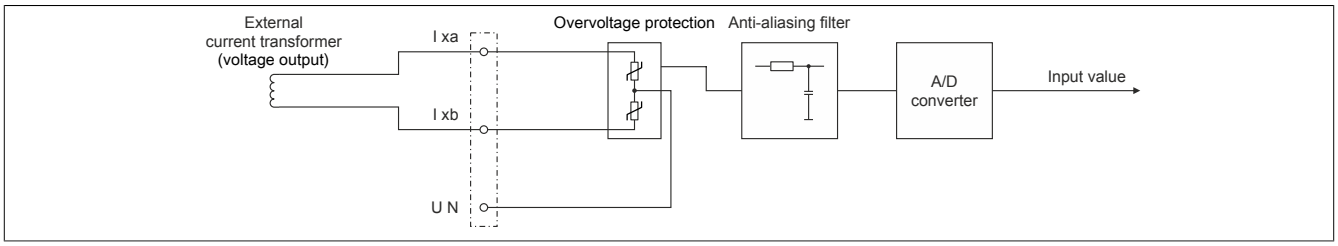
AP3111, AP3121, AP3131: (Current measurement)



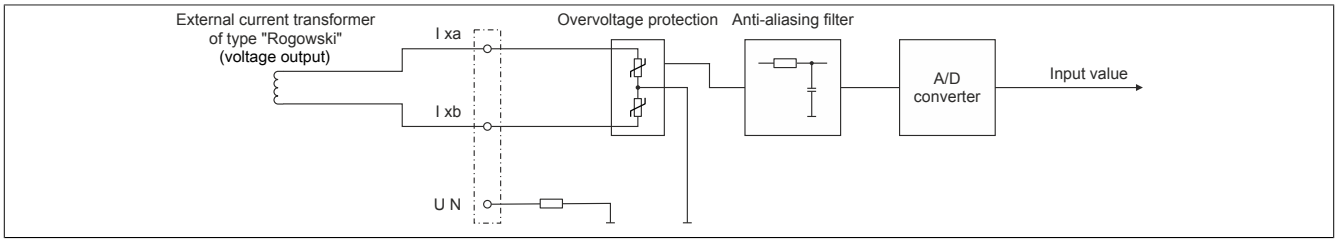
AP31x2: (Current measurement)



AP3161: (Voltage measurement)



AP3171: (Voltage measurement)



1.22.3.8 Typical connection examples for different network configurations

General information

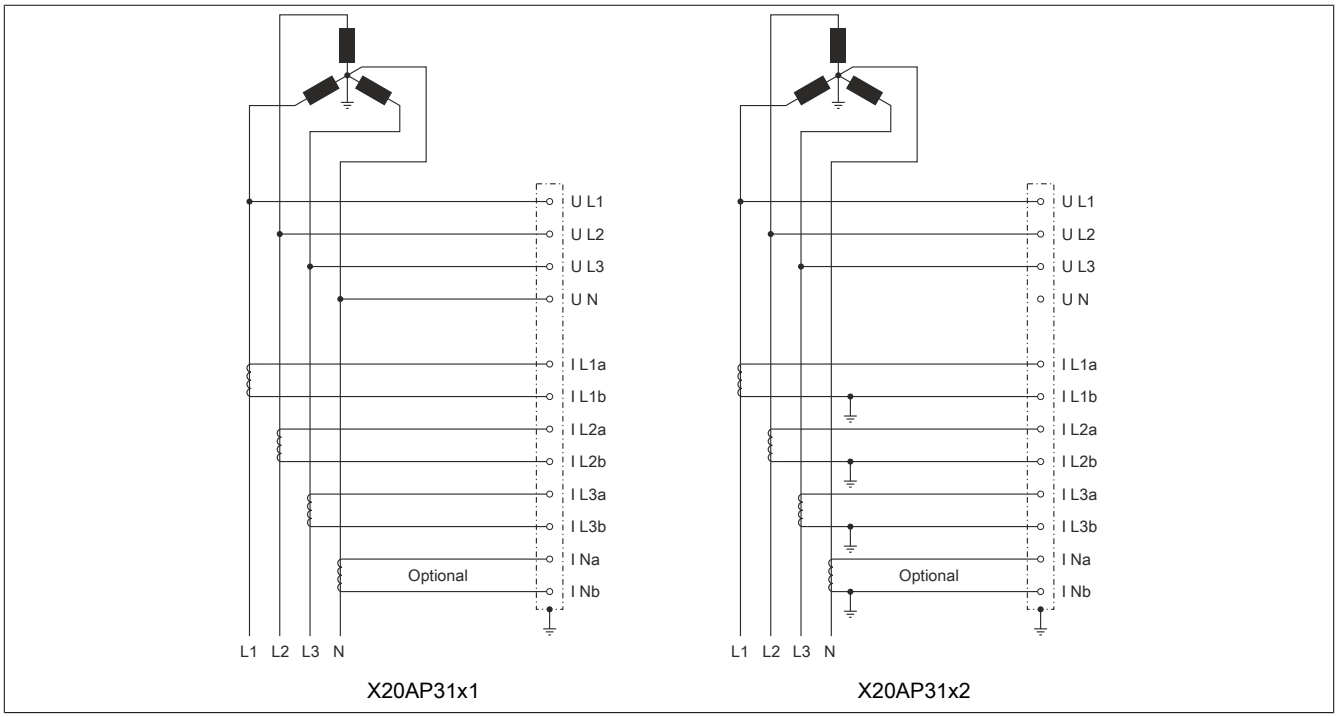
There are many different network configurations around the world. This section will present a few typical connection examples.

Notice!

The X20AP31x2 modules may not be used with network configurations B, D and F due to a lack of grounding.

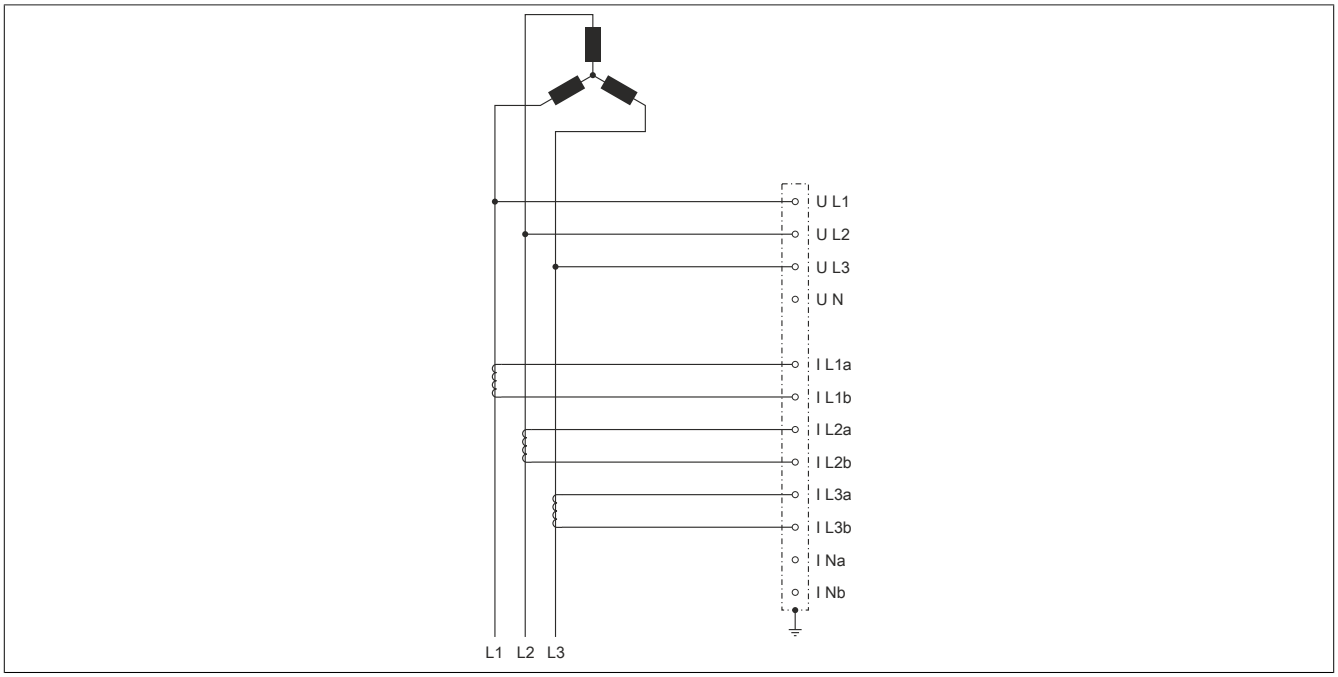
Connection example 1 - Network A

This example involves a 3-element, 3-phase, 4-line star measurement with grounded neutral conductor and optional fault current detection.



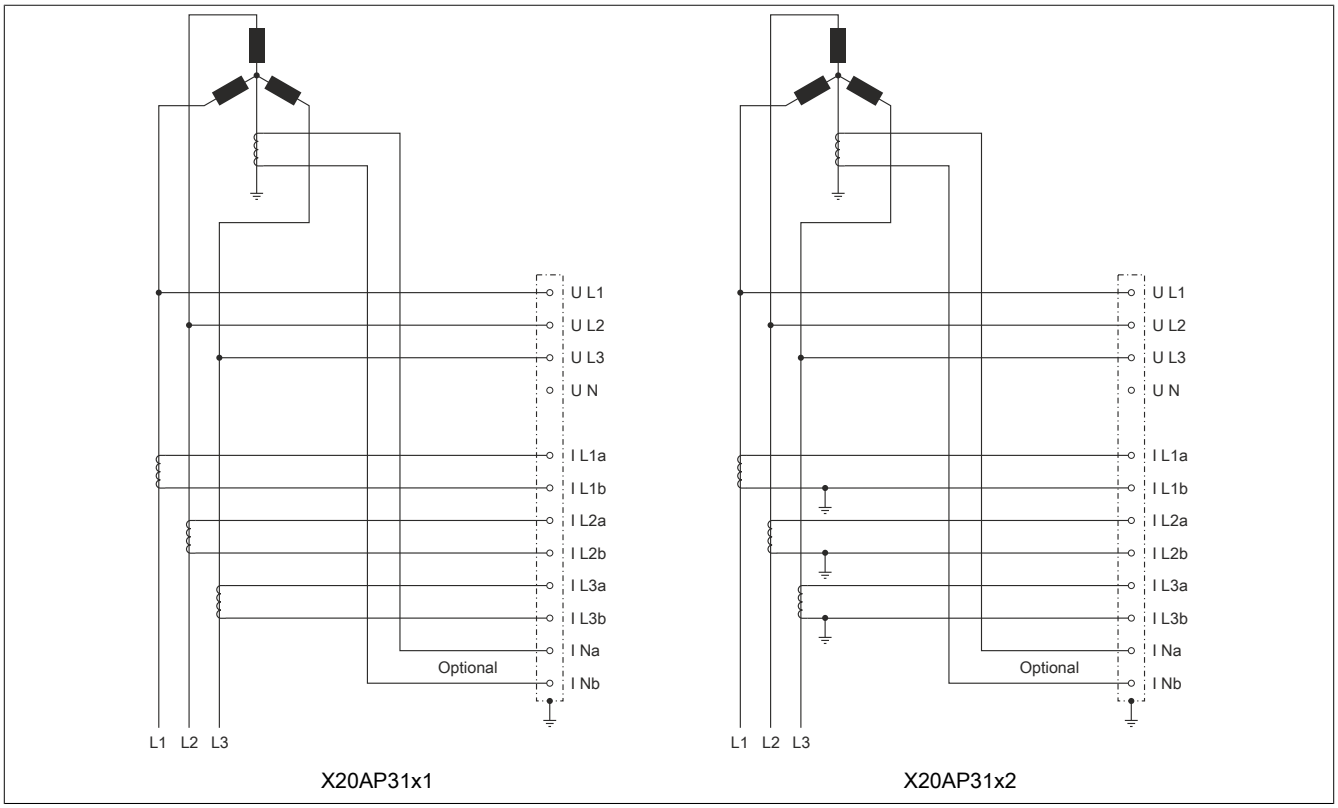
Connection example 2 - Network B

This example involves a 3-element, 3-phase, 3-line star measurement.



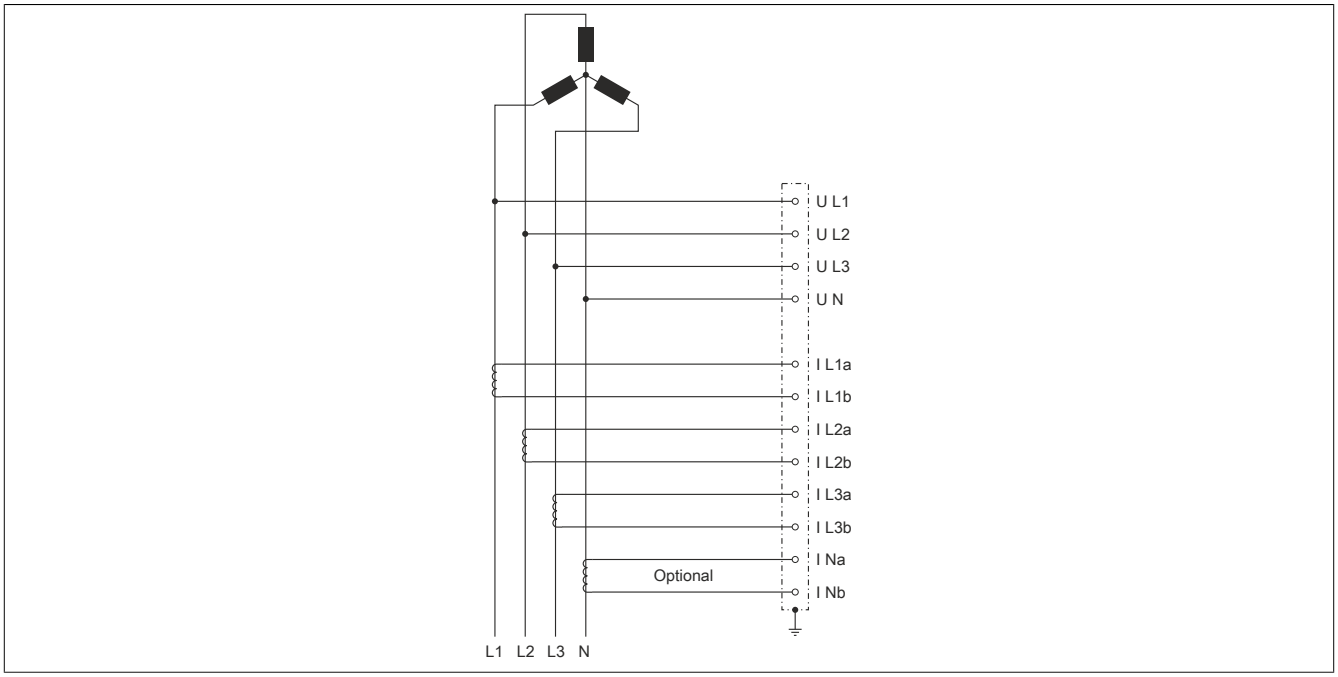
Connection example 3 - Network C

This example involves a 3-element, 3-phase, 3-line star measurement with grounded neutral conductor and optional fault current detection.



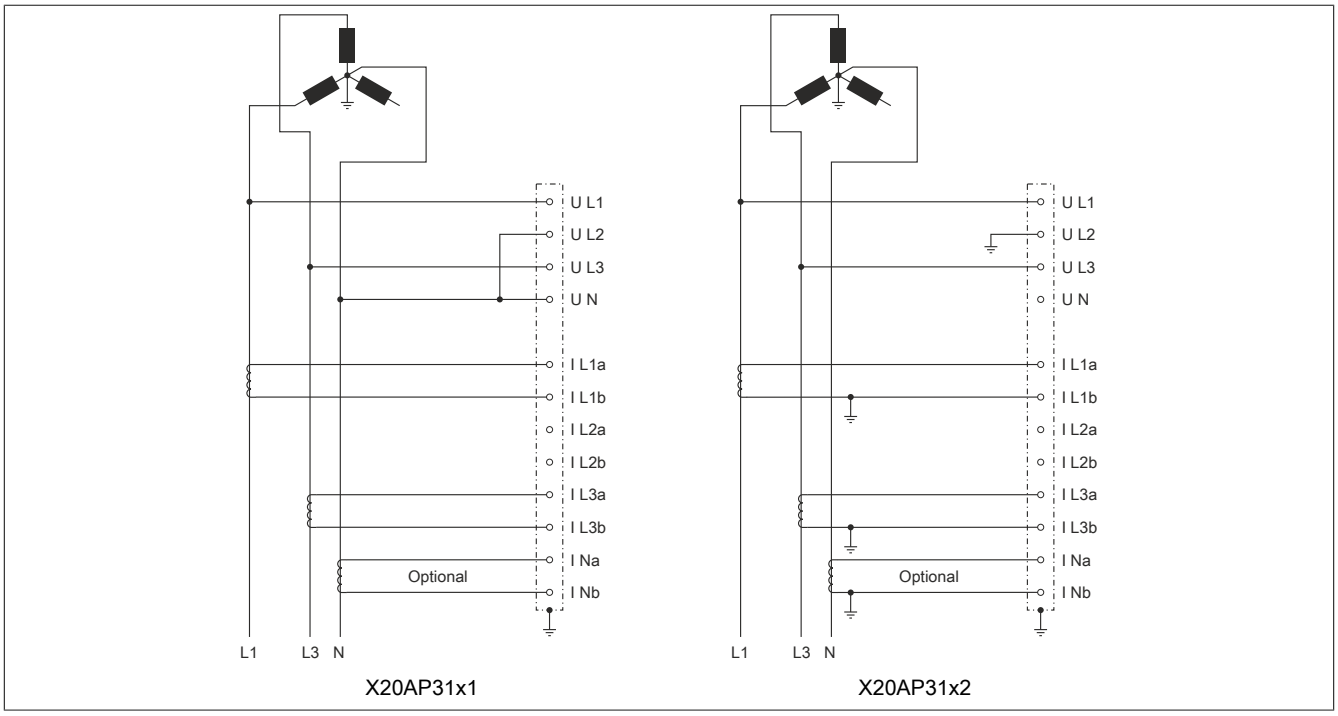
Connection example 4 - Network D

This example involves a 3-element, 3-phase, 4-line star measurement with optional fault current detection.



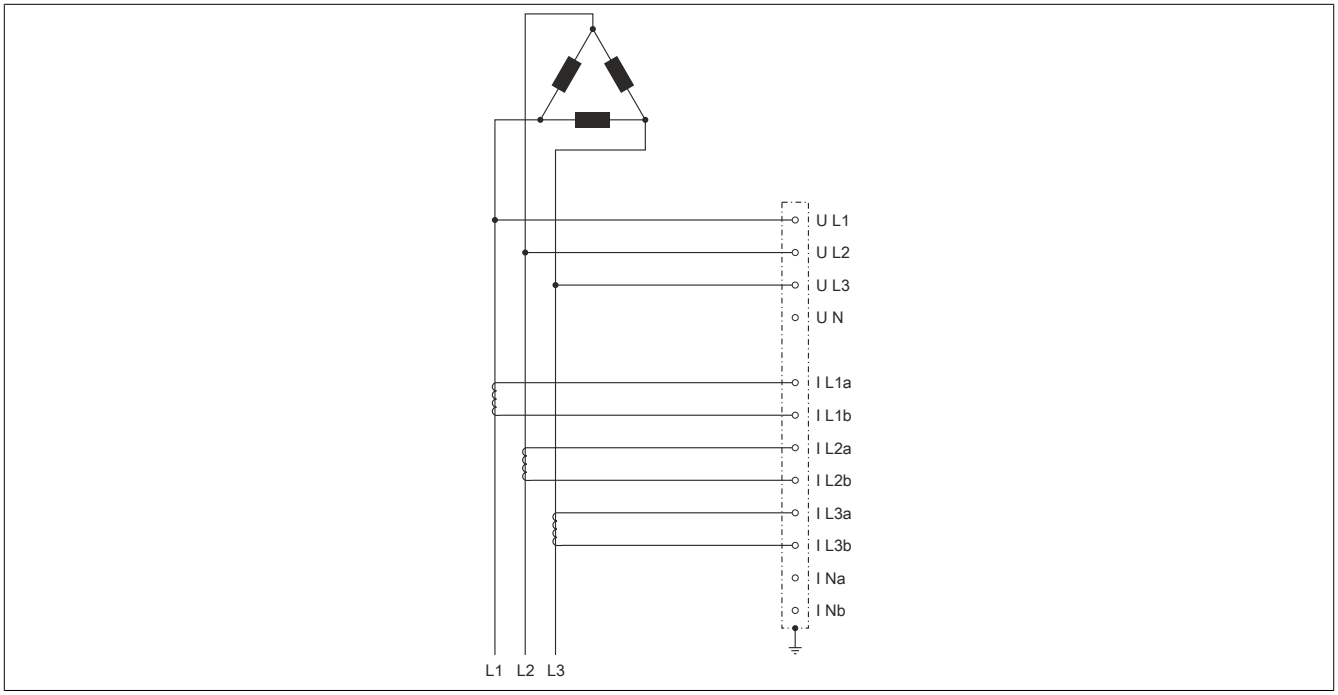
Connection example 5 - Network E

This example involves a 2-element, 2-phase, 3-line star measurement with grounded neutral conductor.



Connection example 6 - Network F

This example involves a 3-element, 3-phase, 3-line delta measurement.

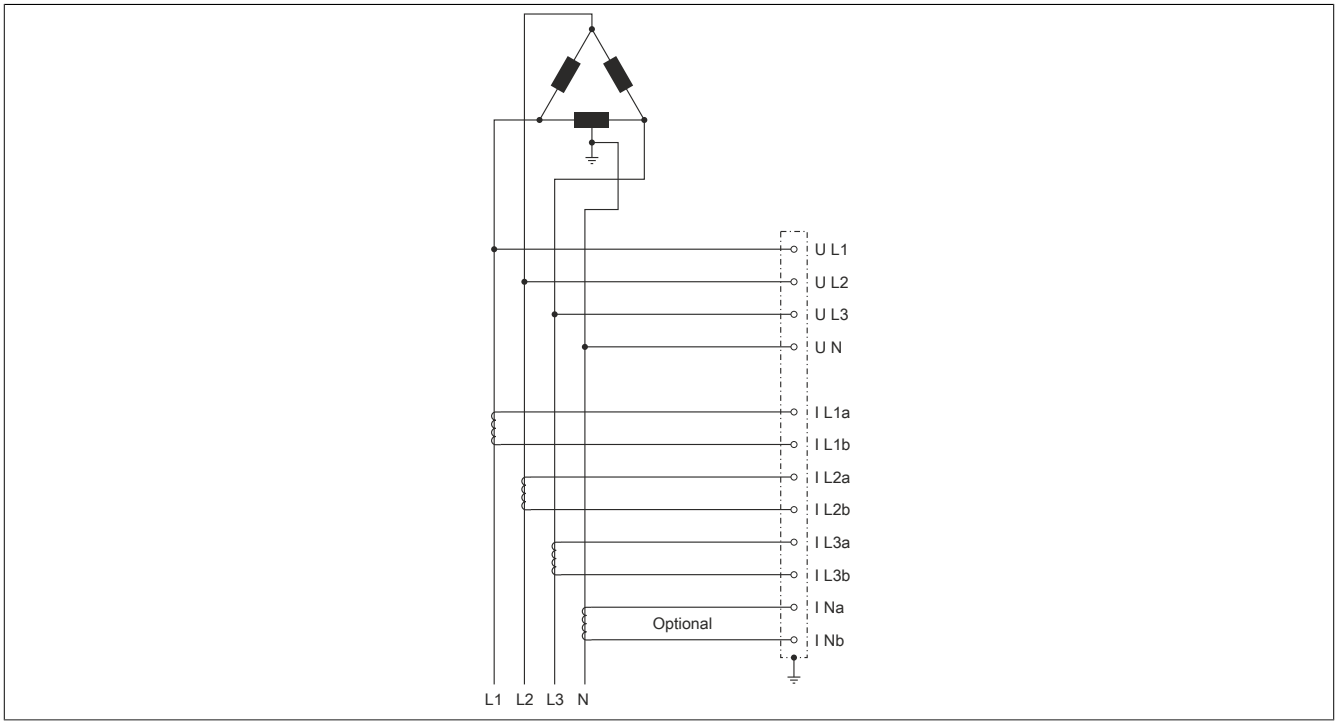


Connection example 7 - Network G

This example involves a 3-element, 3-phase, 4-line, delta measurement with grounded star point.

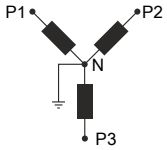
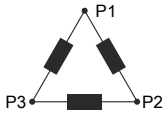
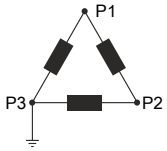
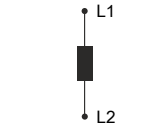
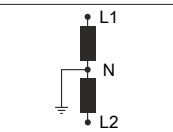
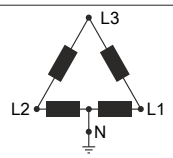
Information:

Exceeding the maximum voltage value specified in the data sheet is not permitted!



1.22.3.9 Permitted line-to-line nominal voltages (rated voltages)

The following table provides an overview of the maximum permitted line-to-line nominal voltage (rated voltage) depending on the used mains type and module.

Network configuration	Network type		Modules	Permissible rated voltage
1	3 phases 4 lines Grounded neutral conductor		All AP modules	480 V
2	3 phases 3 lines Not grounded		X20AP31x1	480 V
			X20AP31x2	Not permitted
3	3 phases 4 lines Grounded phase		X20AP31x1	480 V
			X20AP21x2	Not permitted
4	1 phase 2 lines Not grounded		X20AP31x1	480 V
			X20AP31x2	Not permitted
5	1 phase divided 3 lines Grounded neutral conductor		All AP modules	480 V
6	3 phases 4 lines Divided phase and grounded neutral conductor		All AP modules	240 V

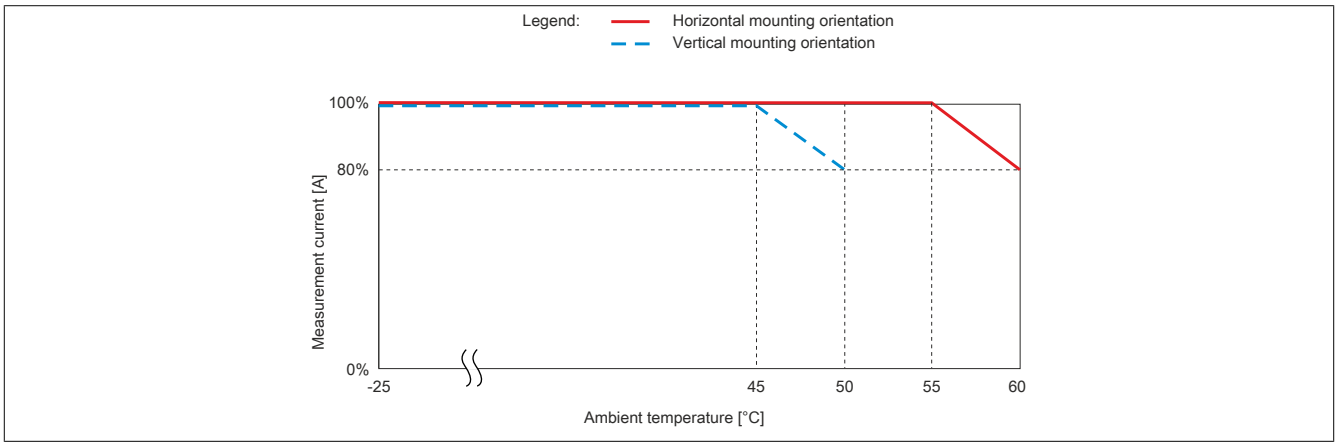
1.22.3.10 Derating

X20AP(c)3121, X20AP3131:

At high temperatures, the averaged measurement current is not permitted to exceed the percentage values of the diagram.

100% corresponds to 3x the nominal current of a channel. Averaging the measurement current is done in a time period of 10 minutes.

The derating listed below must be applied for the current:



1.22.3.11 Usage after the X20IF1091-1

If this module is operated after X2X Link module X20IF1091-1, delays may occur during the Flatstream transfer. For detailed information, see section "Data transfer on the Flatstream" in X20IF1091-1.

1.22.4 UL certificate information

To install the module(s) according to the UL standard, the following rules must be observed.

Information:

- **Use copper conductors only. Minimum temperature rating of the cable to be connected to the field wiring terminals: 76°C, xxx - xxx AWG.**
- **All models are intended to be used in a final safety enclosure that must conform with requirements for protection against the spread of fire and have adequate rigidity per UL 61010-1 and UL 61010-2-201.**
- **Repairs can only be made by B&R.**

Information:

- **Remark regarding UL61010 certification: For use with UL-Listed Energy-Monitoring Current Transformers only.**
- **The current transformers are not permitted to be installed in equipment where they exceed 75 percent of the wiring space of any cross-sectional area within the equipment**
- **Restrict installation of current transformer in an area where it would block ventilation openings.**
- **Restrict installation of current transformer in an area of breaker arc venting.**
- **Not suitable for Class 2 wiring methods.**
- **Not intended for connection to Class 2 equipment.**
- **Secure current transformer and route conductors so that they do not directly contact live terminals or bus.**
- **For use with listed energy-monitoring current transformers.**
- **Associated leads of the current transformers must be maintained within the same overall enclosure.**
- **Unless the current transformers and its leads have been evaluated for REINFORCED INSULATION, a statement to segregate or insulate the leads from different circuits must be provided.**
- **The current transformers are intended for installation within the same enclosure as the equipment. These are not permitted to be installed within switchgear and panel boards.**

Danger!

- **To reduce the risk of electric shock, always open or disconnect circuit from the power distribution system (or service) of the building before installing or servicing current-sensing transformers.**

1.22.5 Register description

1.22.5.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 System user's manual.

1.22.5.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Status register						
130	StatusInput	UINT	•			
	CntPulseActive	Bit 0				
	CntPulseApparent	Bit 1				
	CntPulseActiveFund	Bit 2				
	CntPulseActiveHarm	Bit 3				
	ZeroCrossA	Bit 4				
	ZeroCrossB	Bit 5				
	ZeroCrossC	Bit 6				
	RBTrigDFT	Bit 8				
	RBUpdateEnergy	Bit 9				
	RBClearEnergy	Bit 10				
	RBForceEnergy	Bit 11				
194	ControlOutput	UINT			•	
	TrigDFT	Bit 0				
	EnabEnergy	Bit 1				
	ClearEnergy	Bit 2				
	ForceEnergy	Bit 3				
266	SysStatus1	UINT	•			
270	SysStatus2	UINT	•			
274	SysStatus3	UINT	•			
278	SysStatus4	UINT	•			
265	SystemStatusSel01	USINT	•			
	SumStatusPhaseLoss	Bit 2				
	SumStatusPhaseWarning	Bit 3				
	ErrOrderPhasecurrent	Bit 6				
	ErrOrderPhaseVoltage	Bit 7				
271	SystemStatusSel02	USINT	•			
	SumStatusWarningTHDCurrent	Bit 2				
	SumStatusWarningTHDVoltage	Bit 3				
	ErrIrmsNCalc	Bit 6				
	ErrIrmsNMeas	Bit 7				
278	PhaseStatus	UINT	•			
	LossPhaseC	Bit 0				
	LossPhaseB	Bit 1				
	LossPhaseA	Bit 2				
	WarningPhaseC	Bit 4				
	WarningPhaseB	Bit 5				
	WarningPhaseA	Bit 6				
Analog RMS value registers						
290	IrmsN (measured)	UINT	•			
294	UrmsA	UINT	•			
298	UrmsB	UINT	•			
302	UrmsC	UINT	•			
306	IrmsNcalc (calculated)	UINT	•			
310	IrmsA	UINT	•			
314	IrmsB	UINT	•			
318	IrmsC	UINT	•			
Analog THD and angle registers						
538	Freq	UINT	•			
542	PAngleA	INT	•			
546	PAngleB	INT	•			
550	PAngleC	INT	•			
554	Temperature	INT	•			
558	UAngleA	INT	•			
562	UAngleB	INT	•			
564	UAngleC	INT	•			
Analog power registers						
778	PmeanT	INT	•			
782	PmeanA	INT	•			

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
786	PmeanB	INT	•			
790	PmeanC	INT	•			
794	QmeanT	INT	•			
798	QmeanA	INT	•			
802	QmeanB	INT	•			
806	QmeanC	INT	•			
810	SmeanT	INT	•			
814	SmeanA	INT	•			
818	SmeanB	INT	•			
822	SmeanC	INT	•			
826	PFmeanT	INT	•			
830	PFmeanA	INT	•			
834	PFmeanB	INT	•			
838	PFmeanC	INT	•			
Analog energy registers						
4108	APenergyT	UDINT	•			
4116	APenergyA	UDINT	•			
4124	APenergyB	UDINT	•			
4132	APenergyC	UDINT	•			
4140	ANenergyT	UDINT	•			
4148	ANenergyA	UDINT	•			
4156	ANenergyB	UDINT	•			
4164	ANenergyC	UDINT	•			
4172	RPenergyT	UDINT	•			
4180	RPenergyA	UDINT	•			
4188	RPenergyB	UDINT	•			
4196	RPenergyC	UDINT	•			
4204	RNenergyT	UDINT	•			
4212	RNenergyA	UDINT	•			
4220	RNenergyB	UDINT	•			
4228	RNenergyC	UDINT	•			
4236	SAenergyT	UDINT	•			
4244	SenergyA	UDINT	•			
4252	SenergyB	UDINT	•			
4260	SenergyC	UDINT	•			
4268	SVenergyT	UDINT	•			
4404	AEnergyT	DINT	•			
4412	REnergyT	DINT	•			
Module configuration						
1026	ChanControl	UINT				•
1030	IDispTh	UINT				•
1034	I_RatioA	UINT				•
1038	I_RatioB	UINT				•
1042	I_RatioC	UINT				•
1046	I_RatioN	UINT				•
Update request						
1050	CfgUpdate	UINT				•
1054	Cs0Update	UINT				•
1058	Cs1Update	UINT				•
1066	Cs3Update	UINT				•
1570	Cs1UpdateFB	UINT		•		
1578	Cs3UpdateFB	UINT		•		
A/D converter status configuration						
1090	ZXConfig	UINT				•
1094	SagTh	UINT				•
1098	PhaseLoseTh	UINT				•
1102	INWarnTh0	UINT				•
1106	INWarnTh1	UINT				•
1110	THDNUTh	UINT				•
1114	THDNITh	UINT				•
A/D converter measurement configuration checksum 0						
1154	PLconstH	UINT				•
1158	PLconstL	UINT				•
1162	MeteringMode	UINT				•
A/D converter power calibration checksum 1						
1246	PhiA_W	UINT				•
1254	PhiB_W	UINT				•
1262	PhiC_W	UINT				•
A/D converter RMS value synchronization checksum 3						
1346	UGainA_W	UINT				•
1350	IGainA_W	UINT				•
1354	UoffsetA_W	INT				•
1358	IoffsetA_W	INT				•

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
1362	UGainB_W	UINT				•
1366	IGainB_W	UINT				•
1370	UoffsetB_W	INT				•
1374	IoffsetB_W	INT				•
1378	UGainC_W	UINT				•
1382	IGainC_W	UINT				•
1386	UoffsetC_W	INT				•
1390	IoffsetC_W	INT				•
1394	IGainN_W	UINT				•
1398	IoffsetN_W	INT				•
A/D converter power calibration – read						
1758	PhiA_R	UINT		•		
1766	PhiB_R	UINT		•		
1774	PhiC_R	UINT		•		
A/D converter RMS value synchronization – read						
1858	UGainA_R	UINT		•		
1862	IGainA_R	UINT		•		
1866	UoffsetA_R	INT		•		
1870	IoffsetA_R	INT		•		
1874	UGainB_R	UINT		•		
1878	IGainB_R	UINT		•		
1882	UoffsetB_R	INT		•		
1886	IoffsetB_R	INT		•		
1890	UGainC_R	UINT		•		
1894	IGainC_R	UINT		•		
1898	UoffsetC_R	INT		•		
1902	IoffsetC_R	INT		•		
1906	IGainN_R	UINT		•		
1910	IoffsetN_R	INT		•		
Flatstream interface						
2049	OutputMTU	USINT				•
2051	InputMTU	USINT				•
2055	FlatstreamMode	USINT				•
2057	Forward	USINT				•
2059	ForwardDelay	USINT				•
2113	InputSequence	USINT	•			
2113 + 2*N	RxByteN (index N = 1 to 27)	USINT	•			
2177	OutputSequence	USINT			•	
2177 + 2*N	TxByteN (index N = 1 to 15)	USINT			•	
Force analog energy registers						
2316	Frc_APenergyT	UDINT				•
2324	Frc_APenergyA	UDINT				•
2332	Frc_APenergyB	UDINT				•
2340	Frc_APenergyC	UDINT				•
2348	Frc_ANenergyT	UDINT				•
2356	Frc_ANenergyA	UDINT				•
2364	Frc_ANenergyB	UDINT				•
2372	Frc_ANenergyC	UDINT				•
2380	Frc_RPenergyT	UDINT				•
2388	Frc_RPenergyA	UDINT				•
2396	Frc_RPenergyB	UDINT				•
2404	Frc_RPenergyC	UDINT				•
2412	Frc_RNenergyT	UDINT				•
2420	Frc_RNenergyA	UDINT				•
2428	Frc_RNenergyB	UDINT				•
2436	Frc_RNenergyC	UDINT				•
2444	Frc_SAenergyT	UDINT				•
2452	Frc_SenergyA	UDINT				•
2460	Frc_SenergyB	UDINT				•
2468	Frc_SenergyC	UDINT				•
2476	Frc_SVenergyT	UDINT				•
2484	Frc_APenergyTF	UDINT				•
2492	Frc_APenergyAF	UDINT				•
2500	Frc_APenergyBF	UDINT				•
2508	Frc_APenergyCF	UDINT				•
2516	Frc_ANenergyTF	UDINT				•
2524	Frc_ANenergyAF	UDINT				•
2532	Frc_ANenergyBF	UDINT				•
2540	Frc_ANenergyCF	UDINT				•
2548	Frc_APenergyTH	UDINT				•
2556	Frc_APenergyAH	UDINT				•
2564	Frc_APenergyBH	UDINT				•
2572	Frc_APenergyCH	UDINT				•

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
2580	Frc_ANenergyTH	UDINT				•
2588	Frc_ANenergyAH	UDINT				•
2596	Frc_ANenergyBH	UDINT				•
2604	Frc_ANenergyCH	UDINT				•
Oversampling buffer						
6146 + ((16-N)*40)	IactN_SampleN (Index N = 1 to 16)	INT	•			
6150 + ((16-N)*40)	IactA_SampleN (Index N = 1 to 16)	INT	•			
6154 + ((16-N)*40)	UactA_SampleN (Index N = 1 to 16)	INT	•			
6158 + ((16-N)*40)	IactB_SampleN (Index N = 1 to 16)	INT	•			
6162 + ((16-N)*40)	UactB_SampleN (Index N = 1 to 16)	INT	•			
6166 + ((16-N)*40)	IactC_SampleN (Index N = 1 to 16)	INT	•			
6170 + ((16-N)*40)	UactC_SampleN (Index N = 1 to 16)	INT	•			
6773	SampleCountN	SINT	•			
6774		INT				
6778	Timestamp	INT	•			
6780		DINT				
Environment variables						
15108	OnTime	UDINT		•		
15116	UpCounter	UDINT		•		
15122	MinTemp	INT		•		
15126	MaxTemp	INT		•		

1.22.5.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Status register							
130	0	StatusInput	UINT	•			
		CntPulseActive	Bit 0				
		CntPulseApparent	Bit 1				
		CntPulseActiveFund	Bit 2				
		CntPulseActiveHarm	Bit 3				
		ZeroCrossA	Bit 4				
		ZeroCrossB	Bit 5				
		ZeroCrossC	Bit 6				
		RBTrigDFT	Bit 8				
		RBUpdateEnergy	Bit 9				
		RBClearEnergy	Bit 10				
		RBForceEnergy	Bit 11				
194	0	ControlOutput	UINT			•	
		TrigDFT	Bit 0				
		EnabEnergy	Bit 1				
		ClearEnergy	Bit 2				
		ForceEnergy	Bit 3				
266	-	SysStatus1	UINT		•		
270	-	SysStatus2	UINT		•		
274	-	SysStatus3	UINT		•		
278	-	SysStatus4	UINT		•		
265	-	SystemStatusSel01	USINT		•		
		SumStatusPhaseLoss	Bit 2				
		SumStatusPhaseWarning	Bit 3				
		ErrOrderPhasecurrent	Bit 6				
		ErrOrderPhaseVoltage	Bit 7				
271	-	SystemStatusSel02	USINT		•		
		SumStatusWarningTHDCurrent	Bit 2				
		SumStatusWarningTHDVoltage	Bit 3				
		ErrIrmsNCalc	Bit 6				
		ErrIrmsNMeas	Bit 7				
278	-	PhaseStatus	UINT		•		
		LossPhaseC	Bit 0				
		LossPhaseB	Bit 1				
		LossPhaseA	Bit 2				
		WarningPhaseC	Bit 4				
		WarningPhaseB	Bit 5				
		WarningPhaseA	Bit 6				
Analog RMS value registers							
290	-	IrmsN (measured)	UINT		•		
294	-	UrmsA	UINT		•		
298	-	UrmsB	UINT		•		
302	-	UrmsC	UINT		•		
306	-	IrmsNcalc (calculated)	UINT		•		
310	-	IrmsA	UINT		•		
314	-	IrmsB	UINT		•		
318	-	IrmsC	UINT		•		
Analog THD and angle registers							
538	-	Freq	UINT		•		
542	-	PAngleA	INT		•		
546	-	PAngleB	INT		•		
550	-	PAngleC	INT		•		
554	-	Temperature	INT		•		
558	-	UAngleA	INT		•		
562	-	UAngleB	INT		•		
564	-	UAngleC	INT		•		
Analog power registers							
778	2	PmeanT	INT	•			
782	-	PmeanA	INT		•		
786	-	PmeanB	INT		•		
790	-	PmeanC	INT		•		
794	4	QmeanT	INT	•			
798	-	QmeanA	INT		•		
802	-	QmeanB	INT		•		
806	-	QmeanC	INT		•		
810	6	SmeanT	INT	•			
814	-	SmeanA	INT		•		
818	-	SmeanB	INT		•		
822	-	SmeanC	INT		•		
826	-	PFmeanT	INT		•		

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
830	-	PFmeanA	INT		•		
834	-	PFmeanB	INT		•		
838	-	PFmeanC	INT		•		
Analog energy registers							
4108	-	APenergyT	UDINT		•		
4116	-	APenergyA	UDINT		•		
4124	-	APenergyB	UDINT		•		
4132	-	APenergyC	UDINT		•		
4140	-	ANenergyT	UDINT		•		
4148	-	ANenergyA	UDINT		•		
4156	-	ANenergyB	UDINT		•		
4164	-	ANenergyC	UDINT		•		
4172	-	RPenergyT	UDINT		•		
4180	-	RPenergyA	UDINT		•		
4188	-	RPenergyB	UDINT		•		
4196	-	RPenergyC	UDINT		•		
4204	-	RNenergyT	UDINT		•		
4212	-	RNenergyA	UDINT		•		
4220	-	RNenergyB	UDINT		•		
4228	-	RNenergyC	UDINT		•		
4236	-	SAenergyT	UDINT		•		
4244	-	SenergyA	UDINT		•		
4252	-	SenergyB	UDINT		•		
4260	-	SenergyC	UDINT		•		
4268	-	SVenergyT	UDINT		•		
4404	8	AEnergyT	DINT	•			
4412	12	REnergyT	DINT	•			
Module configuration							
1026	-	ChanControl	UINT				•
1030	-	IDispTh	UINT				•
1034	-	I_RatioA	UINT				•
1038	-	I_RatioB	UINT				•
1042	-	I_RatioC	UINT				•
1046	-	I_RatioN	UINT				•
Update request							
1050	-	CfgUpdate	UINT				•
1054	-	Cs0Update	UINT				•
1058	-	Cs1Update	UINT				•
1066	-	Cs3Update	UINT				•
1570	-	Cs1UpdateFB	UINT		•		
1578	-	Cs3UpdateFB	UINT		•		
A/D converter status configuration							
1090	-	ZXConfig	UINT				•
1094	-	SagTh	UINT				•
1098	-	PhaseLoseTh	UINT				•
1102	-	INWarnTh0	UINT				•
1106	-	INWarnTh1	UINT				•
1110	-	THDNUTh	UINT				•
1114	-	THDNITh	UINT				•
A/D converter measurement configuration checksum 0							
1154	-	PLconstH	UINT				•
1158	-	PLconstL	UINT				•
1162	-	MeteringMode	UINT				•
A/D converter power calibration checksum 1							
1246	-	PhiA_W	UINT				•
1254	-	PhiB_W	UINT				•
1262	-	PhiC_W	UINT				•
A/D converter RMS value synchronization checksum 3							
1346	-	UGainA_W	UINT				•
1350	-	IGainA_W	UINT				•
1354	-	UoffsetA_W	INT				•
1358	-	IoffsetA_W	INT				•
1362	-	UGainB_W	UINT				•
1366	-	IGainB_W	UINT				•
1370	-	UoffsetB_W	INT				•
1374	-	IoffsetB_W	INT				•
1378	-	UGainC_W	UINT				•
1382	-	IGainC_W	UINT				•
1386	-	UoffsetC_W	INT				•
1390	-	IoffsetC_W	INT				•
1394	-	IGainN_W	UINT				•
1398	-	IoffsetN_W	INT				•

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
A/D converter power calibration – read							
1758	-	PhiA_R	UINT		•		
1766	-	PhiB_R	UINT		•		
1774	-	PhiC_R	UINT		•		
A/D converter RMS value synchronization – read							
1858	-	UGainA_R	UINT		•		
1862	-	IGainA_R	UINT		•		
1866	-	UoffsetA_R	INT		•		
1870	-	IoffsetA_R	INT		•		
1874	-	UGainB_R	UINT		•		
1878	-	IGainB_R	UINT		•		
1882	-	UoffsetB_R	INT		•		
1886	-	IoffsetB_R	INT		•		
1890	-	UGainC_R	UINT		•		
1894	-	IGainC_R	UINT		•		
1898	-	UoffsetC_R	INT		•		
1902	-	IoffsetC_R	INT		•		
1906	-	IGainN_R	UINT		•		
1910	-	IoffsetN_R	INT		•		
Flatstream interface							
2049	-	OutputMTU	USINT				•
2051	-	InputMTU	USINT				•
2055	-	FlatstreamMode	USINT				•
2057	-	Forward	USINT				•
2059	-	ForwardDelay	USINT				•
2113	16	InputSequence	USINT	•			
2113 + 2*N	16 + N	RxByteN (index N = 1 to 7)	USINT	•			
2177	16	OutputSequence	USINT			•	
2177 + 2*N	16 + N	TxByteN (index N = 1 to 7)	USINT			•	
Force analog energy registers							
2316	-	Frc_APenergyT	UDINT				•
2324	-	Frc_APenergyA	UDINT				•
2332	-	Frc_APenergyB	UDINT				•
2340	-	Frc_APenergyC	UDINT				•
2348	-	Frc_ANenergyT	UDINT				•
2356	-	Frc_ANenergyA	UDINT				•
2364	-	Frc_ANenergyB	UDINT				•
2372	-	Frc_ANenergyC	UDINT				•
2380	-	Frc_RPenergyT	UDINT				•
2388	-	Frc_RPenergyA	UDINT				•
2396	-	Frc_RPenergyB	UDINT				•
2404	-	Frc_RPenergyC	UDINT				•
2412	-	Frc_RNenergyT	UDINT				•
2420	-	Frc_RNenergyA	UDINT				•
2428	-	Frc_RNenergyB	UDINT				•
2436	-	Frc_RNenergyC	UDINT				•
2444	-	Frc_SAenergyT	UDINT				•
2452	-	Frc_SenergyA	UDINT				•
2460	-	Frc_SenergyB	UDINT				•
2468	-	Frc_SenergyC	UDINT				•
2476	-	Frc_SVenergyT	UDINT				•
2484	-	Frc_APenergyTF	UDINT				•
2492	-	Frc_APenergyAF	UDINT				•
2500	-	Frc_APenergyBF	UDINT				•
2508	-	Frc_APenergyCF	UDINT				•
2516	-	Frc_ANenergyTF	UDINT				•
2524	-	Frc_ANenergyAF	UDINT				•
2532	-	Frc_ANenergyBF	UDINT				•
2540	-	Frc_ANenergyCF	UDINT				•
2548	-	Frc_APenergyTH	UDINT				•
2556	-	Frc_APenergyAH	UDINT				•
2564	-	Frc_APenergyBH	UDINT				•
2572	-	Frc_APenergyCH	UDINT				•
2580	-	Frc_ANenergyTH	UDINT				•
2588	-	Frc_ANenergyAH	UDINT				•
2596	-	Frc_ANenergyBH	UDINT				•
2604	-	Frc_ANenergyCH	UDINT				•
Environment variables							
15108	-	OnTime	UDINT		•		
15116	-	UpCounter	UDINT		•		
15122	-	MinTemp	INT		•		
15126	-	MaxTemp	INT		•		

1) The offset specifies the position of the register within the CAN object.

1.22.5.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

1.22.5.3.2 CAN I/O bus controller

The module occupies 3 analog logical slots with CAN I/O.

1.22.5.4 General information

The modules are used for power monitoring and for a machine's energy management. Examples of where this would be used:

- Multi-phase energy measurement for class 0.5S or class 1 for
  - 3-phase, 4-line applications with neutral conductor (with/without grounding)
  - 3-phase, 3-line applications (with/without grounding)
  - 2-phase networks with grounded phase B connection
- Single-phase measurement by disabling inputs that are not needed
- Mains analysis according to harmonic content
- Signal trace by 8 kHz recording of the 3 voltage channels and 4 current channels with FIFO

1.22.5.4.1 Measured value preparation

The modules provide the following possibilities for measured value preparation:

- Temperature coefficient of internal reference of 6 ppm/°C
- Energy registers for active, reactive and apparent energy, separated for forward and backward, fundamental waves and harmonics
- Threshold register for status signal generation and activation of power and energy measurement
- Determining the THD harmonic component
- Discrete Fourier Transformation (DFT) up to 31st harmonic component per phase for voltage and current
- Status signals for voltage dip, loss of voltage, phase sequence, energy flow, neutral current monitor, harmonic component monitor

1.22.5.4.2 Additional information

Information	Description
Measurement range limiting	Due to the majority of registers consisting of 16-bit values (exception: energy registers, which are interpolated to 32-bit by the firmware), the measurement ranges are subject to limitations, e.g. voltage 650.00 Vrms and current 65,000 Arms (after accounting for the transfer factor of the current transformer).
Extended measurement ranges	Extended measurement ranges can be achieved with the software application by upscaling the measured values.
Frozen values	Sample time register: If the group of measured values is read from the power meter, it is assigned a NetTime. Using this NetTime, a freezing of the values can be determined.
Environment variables	The values for duty cycle, boot counter, and minimum / maximum transformer temperature are recorded.

1.22.5.4.3 Measurement function

The values measured for RMS, power, active power factor, phase angle and frequency are mean values over 16 full waves, the update rate is ~3 Hz.

The following represents the measurement time over 16 full waves at the corresponding frequency:

50 Hz → 320 ms
60 Hz → 267 ms

1.22.5.4.3.1 Energy measurement

The power measurement (energy measurement) is based on the integration of the measured values with a sampling rate of 1 MHz.

The gathered energy values are provided according to the set unit (1 Ws, 10 Ws, etc.) in the energy registers.

Automatic reading of the energy meter from the transformer must be enabled because valid values are only available after the transformer has been configured. It is possible to clear the energy registers or to configure them with a block of the register written in the software application.

Information:

When 1 Wh and 1 kWh are set, the energy pulses on the register "StatusInput" on page 534 may not be used.

1.22.5.4.3.2 Power measurement

The phase power ratings are calculated by the module and stored in the corresponding registers.

The total power ratings are equal to the sum of the phase power ratings. To prevent the number range from being exceeded, the value in the registers is equal to a fourth of the actual power. This value must be multiplied by 4 by the application.

The vector-based total apparent power (complex total apparent power) is calculated according to IEEE1459.

1.22.5.4.3.3 Power factor

The phase power factor is calculated by dividing the phase active power by the phase apparent power.

The total power factor is calculated by dividing the total active power by the total apparent power.

1.22.5.4.3.4 Neutral current

The neutral current can be measured or calculated. Both values are available.

The user can configure which one to use for displaying the status.

1.22.5.4.3.5 Phase angle

The phase angle is calculated based on the zero-crossing detection.

1.22.5.4.3.6 Frequency

Frequency measurement is based on Phase A. If A fails, then Phase C is used. If both A and C fail, then Phase B is used.

1.22.5.4.3.7 Temperature

The Chip-Junction temperature is measured approximately every 100 ms using the sensor integrated in the transformer.

1.22.5.4.3.8 THD+N - Sum of interference power of the harmonic (THD) + interference power of the noise (N)

The THD+N measurement is used to monitor the percentage of harmonics in the network.

If this percentage falls below 10%, then an accuracy of 0.01% can no longer be guaranteed.

This is calculated as follows: (SQR (RMS value$_{Total}$^2 - RMS value$_{FundamentalWave}$^2)) / RMS value$_{FundamentalWave}$

1.22.5.4.3.9 Fourier analysis

The harmonic component from the 2nd to the 31st harmonic is calculated for voltage and current and the THD (Total Harmonic Distortion) of each phase.

The DFT period (DFT = discrete Fourier Transformation) is 0.5 s. This corresponds to a resolution of 2 Hz. The input samples are recorded at a sampling rate of 8 kHz and can be optionally multiplied with a "Hann window" before being evaluated. This is initiated when requested by the application.

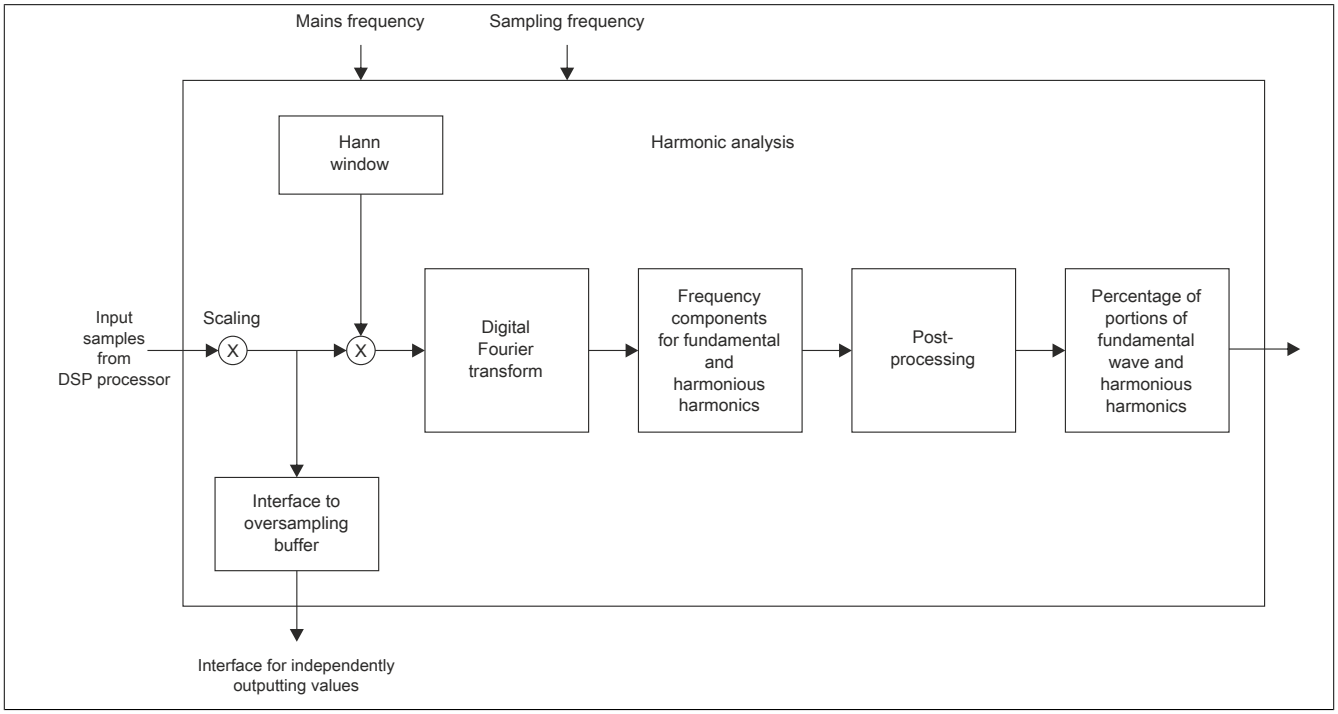


Figure 55: Diagram of Fourier analysis

1.22.5.4.4 Event generation

1.22.5.4.4.1 Zero-crossing detection

Zero-crossing detection can be configured for each phase for current or voltage and edge and forms the basis for frequency and angle measurements and subsequently also for active and reactive power calculations.

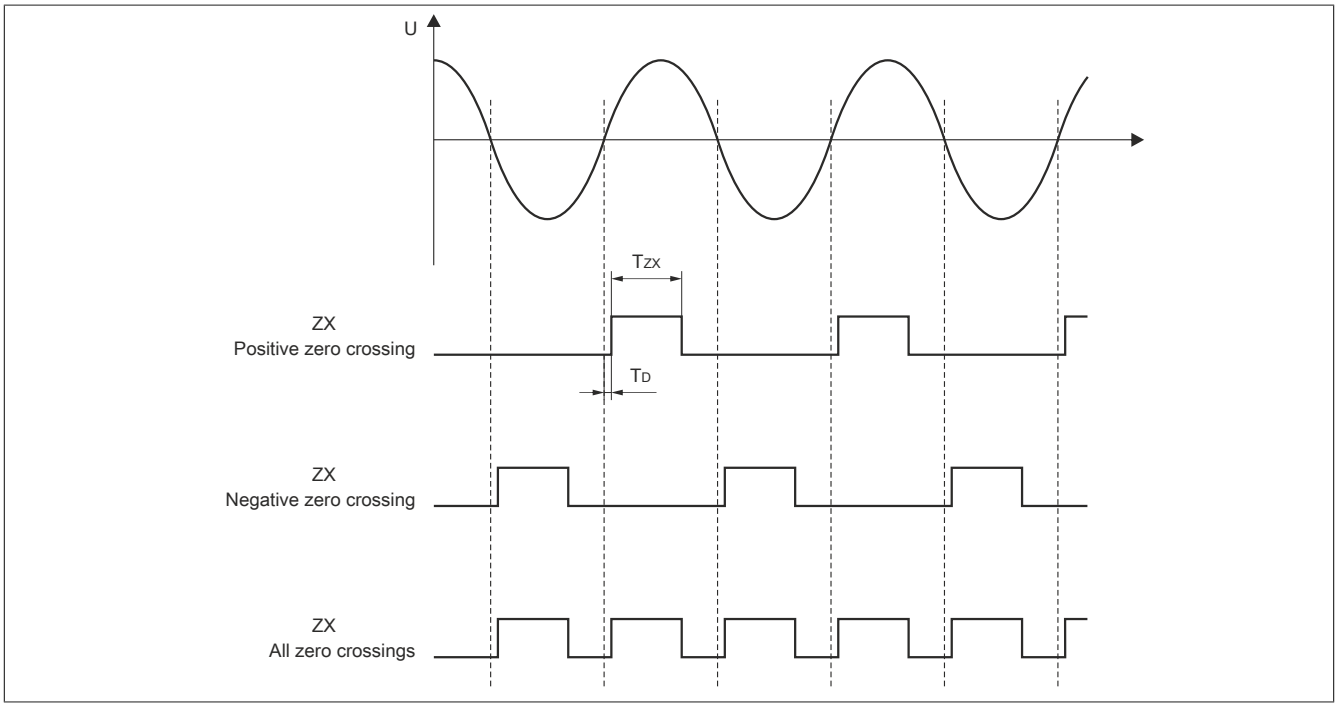


Figure 56: Timing diagram of zero-crossing detection per phase

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{ZX}	Length of high signal		5		ms
T_D	Delay time		0.2	0.5	ms

1.22.5.4.4.2 Voltage dip or power failure detection

Event	Description
Voltage dip	The threshold for the voltage dip is typically set to 78% of the standard voltage (approx. 170 Vrms). The status flag is set if more than 3 8 kHz samples are below the threshold within 2 consecutive 11 ms windows.
Power failure	The threshold for the power failure is typically set to 10% of the standard voltage (approx. 22 Vrms). The status flag is set if more than 3 8 kHz samples are below the threshold within 2 consecutive 11 ms windows. If a power failure is detected, zero crossing detection for voltage and current is disabled for this phase.

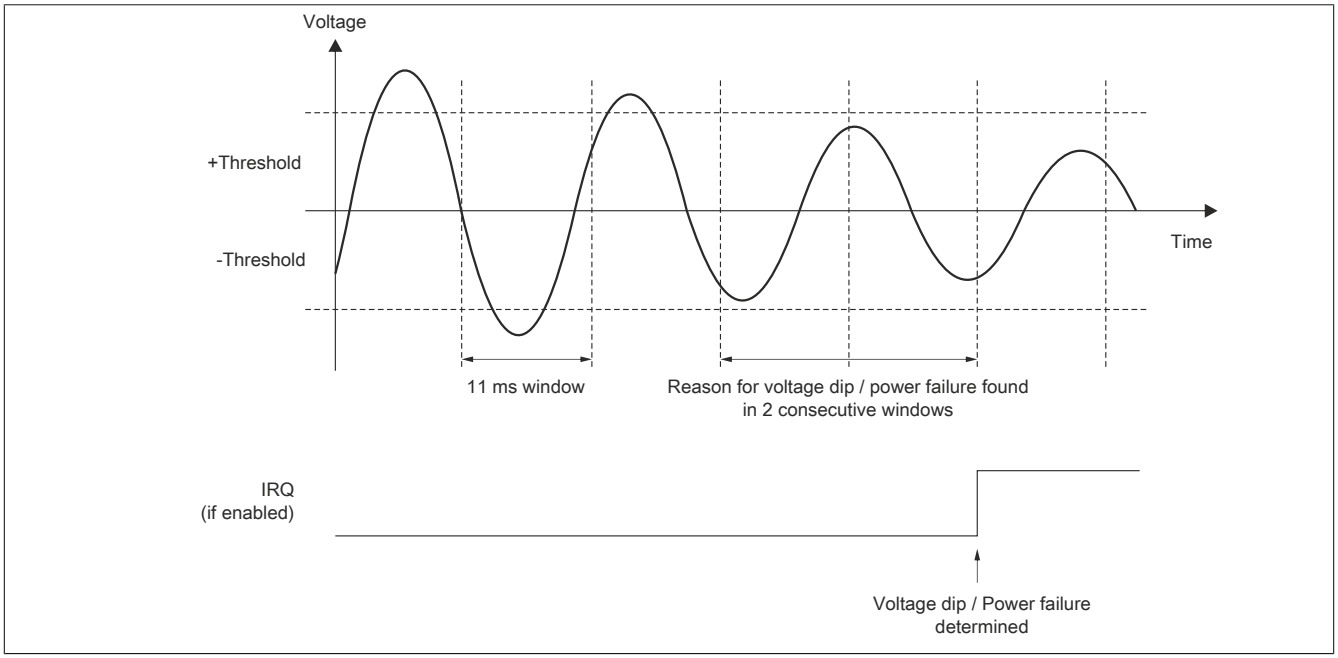


Figure 57: Timing diagram for detection of a voltage dip or power failure

1.22.5.4.4.3 Neutral current monitoring

Neutral current monitoring of the measured and the calculated value is done with separate threshold value registers and status flags.

1.22.5.4.4.4 Phase sequence monitoring

3 phase and 2 phase applications are handled differently:

Application	Description
3 phases	Zero cross-overs of voltage and current must follow the sequence Phase A before Phase B before Phase C
2 phases	Zero cross-overs of voltage and current must follow the sequence Phase A at least 180° before Phase C

1.22.5.4.5 Configuration registers

The configuration and calibration registers are each composed of blocks and employ a checksum feature to highlight undesired changes. In order to apply this register to the transformer, the respective transfer register must be changed after the data is transferred to the module (incrementing, bit toggling, etc.). The start value of the transfer register is 0 after startup.

1.22.5.4.6 Oversampling

The input values are measured with a configurable sampling cycle time and saved in the internal physical data buffer with timestamp. This data area can now be read out by means of configurable data length in cyclic data transfer.

The recording and transfer system of logical channels is identical to that of the physical channels. The functions of the logical channels are also executed in the configured sampling cycle time and saved in the logical data buffer with timestamp. From here, the values can also be read out via configurable cyclic data points.

With fast cycle times, however, it can happen that the set sampling cycle time is not sufficient for the sum of all physical and logical functions. If the physical sampling should remain unaffected, logical processing can be slowed down via a prescaler setting.

Information:

Due to the free configurability of the sampling cycle time on the module, there is no synchronicity to the X2X Link network, regardless of configuration as standard inputs or with the oversampling function.

If synchronicity is desired or required, then the configured sampling cycle time must be a multiple of the X2X Link cycle time!

1.22.5.5 Interface for transferring process variable mapping

Due to the amount of potential cyclic input data and the limitation to 30 byte cyclic X2X data, the extended Flat-stream Interface (DPS = Data Point Stream) has been defined as the mechanism for transferring the process variables. DPS is based on the Flat Streaming Interface for serial interface modules. The Flat Streaming Interface was expanded to include the block number as the first byte of the user data frame and implements the termination of a frame (data image of the channel) with a zero segment.

The data blocks are re-transferred if a read request is triggered after a transfer has been completed. A block number can be sent via the DPS to set a different block or transfer the entire image (default: block number 0).

It should be possible to adapt the DPS interface to the available buffer size. However, the higher-level fieldbus must be taken into account when doing so (e.g. CAN 8 byte object, InputMTU size 7). The block number is added to the front of the actual payload data as a means to differentiate the blocks.

```
#define ADC_BLK_ALL        0   // struct ADC_REG
#define ADC_BLK_STATUS     1   // long NetTimeReg + struct ADC_REG_STATUS
#define ADC_BLK_RMS        2   // struct ADC_REG_RMS
#define ADC_BLK_POWER      3   // struct ADC_REG_POWER
#define ADC_BLK_THD_ANGLE  4   // struct THD_ANGLE
#define ADC_BLK_ENERGY     5   // long NetTimeEnergy + struct ADC_REG_ENERGY
#define ADC_BLK_DFT        6   // long NetTimeDft + struct ADC_REG_DFT
#define ADC_BLK_CFGACT     7   // struct ADC_REG_CFGACT
#define ADC_BLK_ENVREG     8   // struct ENV_STATUS
```

Information:

- **Consistency of the data is only provided for the individual variables because the data is transferred from the A/D converter asynchronously to the conversion.**
- **Make sure that the byte sequence of the register is in accordance with the Little Endian model (Intel format).**

The NetTime timestamps are always updated after the blocks have been generated when a new alternating buffer is provided.

1.22.5.5.1 Data block structures

1.22.5.5.1.1 ADC_REG

```
typedef struct ADC_REG     ADC_REG;
struct ADC_REG
{
 long              NetTimeReg;  // Time of Section copy to Buffer
 ADC_REG_STATUS    Status;      // Status registers
 ADC_REG_RMS       Rms;         // RMS Registers
 ADC_REG_POWER     Power;       // Power Registers
 ADC_REG_THD_ANGLE ThdAngle;    // THD + Angle Registers

// Regular Energy Registers
 long            NetTimeEnergy; // Time of Section copy to Buffer
 ADC_REG_ENERGY  Energy;        // Energy Registers

 long            NetTimeDft;    // Time of Section copy to Buffer
 ADC_REG_DFT     Dft;           // DFT Registers
// Read Back selected CFG Registers
  ADC_REG_CFGACT  CfgAct;       // Config read back
// Read Back Environment Registers
  ENV_STATUS      EnvReg;
};
```

1.22.5.5.1.2 ADC_REG_STATUS

```
typedef struct ADC_REG_STATUS  ADC_REG_STATUS;
struct ADC_REG_STATUS
{
  unsigned short SysStatus0;   // SysStatus 0
  unsigned short SysStatus1;   // SysStatus 1
  unsigned short EnStatus0;    // SysStatus 2
  unsigned short EnStatus1;    // SysStatus 3
};
```

1.22.5.5.1.3 ADC_REG_RMS

```
typedef struct ADC_REG_RMS  ADC_REG_RMS;
struct ADC_REG_RMS
{
  unsigned short IrmsN1;   // N Line Sampled current RMS
  unsigned short UrmsA;    // phase A voltage RMS
  unsigned short UrmsB;    // phase B voltage RMS
  unsigned short UrmsC;    // phase C voltage RMS
  unsigned short IrmsN0;   // N Line calculated current RMS
  unsigned short IrmsA;    // phase A current RMS
  unsigned short IrmsB;    // phase B current RMS
  unsigned short IrmsC;    // phase C current RMS
};
```

1.22.5.5.1.4 ADC_REG_POWER

```
typedef struct ADC_REG_POWER  ADC_REG_POWER;
struct ADC_REG_POWER
{
  unsigned short SVmeanTLSB;  // LSB of (Vector Sum) Total Apparent Power
  unsigned short SVmeanT;     // (Vector Sum) Total Apparent Power

  // Power and Power Factor Register
  signed short PmeanT;   // Total Active Power
  signed short PmeanA;   // Phase A Active Power
  signed short PmeanB;   // Phase B Active Power
  signed short PmeanC;   // Phase C Active Power
  signed short QmeanT;   // Total Reactive Power
  signed short QmeanA;   // Phase A Reactive Power
  signed short QmeanB;   // Phase B Reactive Power
  signed short QmeanC;   // Phase C Reactive Power
  signed short SmeanT;   // (Arithmetic Sum) Total apparent power
  signed short SmeanA;   // phase A apparent power
  signed short SmeanB;   // phase B apparent power
  signed short SmeanC;   // phase C apparent power
  signed short PFmeanT;  // Total power factor
  signed short PFmeanA;  // phase A power factor
  signed short PFmeanB;  // phase A power factor
  signed short PFmeanC;  // phase A power factor

  // Fundamental/ Harmonic Power and Voltage/ Current RMS Registers
  signed short PmeanTF;  // Total active fundamental power
  signed short PmeanAF;  // phase A active fundamental power
  signed short PmeanBF;  // phase B active fundamental power
  signed short PmeanCF;  // phase C active fundamental power
  signed short PmeanTH;  // Total active harmonic power
  signed short PmeanAH;  // phase A active harmonic power
  signed short PmeanBH;  // phase B active harmonic power
  signed short PmeanCH;  // phase C active harmonic power
};
```

1.22.5.5.1.5 ADC_REG_THD_ANGLE

```
typedef struct ADC_REG_THD_ANGLE  ADC_REG_THD_ANGLE;
struct ADC_REG_THD_ANGLE
{
  // THD+N, Frequency, Angle and Temperature Registers
  unsigned short THDNUA;    // phase A voltage THD+N
  unsigned short THDNUB;    // phase B voltage THD+N
  unsigned short THDNUC;    // phase C voltage THD+N
  unsigned short THDNIA;    // phase A current THD+N
  unsigned short THDNIB;    // phase B current THD+N
  unsigned short THDNIC;    // phase C current THD+N
  unsigned short Freq;      // Frequency
  signed short     PAngleA;   // phase A mean phase angle
  signed short     PAngleB;   // phase B mean phase angle
  signed short     PAngleC;   // phase C mean phase angle
  signed short     Temp;      // Measured temperature
  signed short     UangleA;   // phase A voltage phase angle
  signed short     UangleB;   // phase B voltage phase angle
  signed short     UangleC;   // phase C voltage phase angle
};
```

1.22.5.5.1.6 ADC_REG_ENERGY

```
typedef struct ADC_REG_ENERGY  ADC_REG_ENERGY;
struct ADC_REG_ENERGY
{
  unsigned long APenergyT;   // Total Forward Active Energy
  unsigned long APenergyA;   // Phase A Forward Active Energy
  unsigned long APenergyB;   // Phase B Forward Active Energy
  unsigned long APenergyC;   // Phase C Forward Active Energy
  unsigned long ANenergyT;   // Total Reverse Active Energy
  unsigned long ANenergyA;   // Phase A Reverse Active Energy
  unsigned long ANenergyB;   // Phase B Reverse Active Energy
  unsigned long ANenergyC;   // Phase C Reverse Active Energy
  unsigned long RPenergyT;   // Total Forward Reactive Energy
  unsigned long RPenergyA;   // Phase A Forward Reactive Energy
  unsigned long RPenergyB;   // Phase B Forward Reactive Energy
  unsigned long RPenergyC;   // Phase C Forward Reactive Energy
  unsigned long RNenergyT;   // Total Reverse Reactive Energy
  unsigned long RNenergyA;   // Phase A Reverse Reactive Energy
  unsigned long RNenergyB;   // Phase B Reverse Reactive Energy
  unsigned long RNenergyC;   // Phase C Reverse Reactive Energy
  unsigned long SAenergyT;   // (Arithmetic Sum) Total Apparent Energy
  unsigned long SenergyA;    // Phase A Apparent Energy
  unsigned long SenergyB;    // Phase B Apparent Energy
  unsigned long SenergyC;    // Phase C Apparent Energy
  unsigned long SVenergyT;   // (Vector Sum) Total Apparent Energy

  // Fundamental / Harmonic Energy Register
  unsigned long APenergyTF;  // Total Forward Active Fundamental Energy
  unsigned long APenergyAF;  // Phase A Forward Active Fundamental Energy
  unsigned long APenergyBF;  // Phase B Forward Active Fundamental Energy
  unsigned long APenergyCF;  // Phase C Forward Active Fundamental Energy
  unsigned long ANenergyTF;  // Total Reverse Active Fundamental Energy
  unsigned long ANenergyAF;  // Phase A Reverse Active Fundamental Energy
  unsigned long ANenergyBF;  // Phase B Reverse Active Fundamental Energy
  unsigned long ANenergyCF;  // Phase C Reverse Active Fundamental Energy
  unsigned long APenergyTH;  // Total Forward Active Harmonic Energy
  unsigned long APenergyAH;  // Phase A Forward Active Harmonic Energy
  unsigned long APenergyBH;  // Phase B Forward Active Harmonic Energy
  unsigned long APenergyCH;  // Phase C Forward Active Harmonic Energy
  unsigned long ANenergyTH;  // Total Reverse Active Harmonic Energy
  unsigned long ANenergyAH;  // Phase A Reverse Active Harmonic Energy
  unsigned long ANenergyBH;  // Phase B Reverse Active Harmonic Energy
  unsigned long ANenergyCH;  // Phase C Reverse Active Harmonic Energy

  signed long AEnergyT;   // Total Active Energy
  signed long REnergyT;   // Total Reactive Energy
};
```

1.22.5.5.1.7 ADC_REG_DFT

```
typedef struct ADC_REG_DFT  ADC_REG_DFT;
struct ADC_REG_DFT
{
  // Arithmetic ratio, 2 bits integer and 14 bits fractional;
  // That is: Harmonic Ratio (%) = Register Value / 163.84
  unsigned short DftAI[32]; // phase A, Current, Harmonic Ratio for 2nd to 32nd
                            // order componentand Total Harmonic DistortionRatio
  unsigned short DftBI[32]; // phase B, Current, Harmonic Ratio for 2nd to 32nd
                            // order componentand Total Harmonic DistortionRatio
  unsigned short DftCI[32]; // phase C, Current, Harmonic Ratio for 2nd to 32nd
                            // order componentand Total Harmonic DistortionRatio
  unsigned short DftAV[32]; // phase A, Voltage, Harmonic Ratio for 2nd to 32nd
                            // order componentand Total Harmonic DistortionRatio
  unsigned short DftBV[32]; // phase B, Voltage, Harmonic Ratio for 2nd to 32nd
                            // order componentand Total Harmonic DistortionRatio
  unsigned short DftCV[32]; // phase C, Voltage, Harmonic Ratio for 2nd to 32nd
                            // order componentand Total Harmonic DistortionRatio

  unsigned short DftAI_Fund;
  unsigned short DftAV_Fund;
  unsigned short DftBI_Fund;
  unsigned short DftBV_Fund;
  unsigned short DftCI_Fund;
  unsigned short DftCV_Fund;
};
```

1.22.5.5.1.8 ADC_REG_CFACT

```
// Except of configuration registers used by APROL, readable only by FS-IF
// and with register numbers of registers with the same names.

typedef struct ADC_REG_CFGACTADC_REG_CFGACT;
struct ADC_REG_CFGACT
{
  unsigned short ChanControl;
  unsigned short IDispTh;
  unsigned short I_RatioA;
  unsigned short I_RatioB;
  unsigned short I_RatioC;
  unsigned short I_RatioN;
  unsigned short ZXConfig;
  unsigned short SagTh;
  unsigned short PhaseLoseTh;
  unsigned short INWarnTh0;
  unsigned short INWarnTh1;
  unsigned short THDNUTh;
  unsigned short THDNITh;
  unsigned short MeteringMode;
  unsigned short PLconstL;
  unsigned short PLconstH;
};
```

1.22.5.5.1.9 ENV_STATUS

```
// Environment Variables

typedef struct ENV_STATUSENV_STATUS;
struct ENV_STATUS
{
  unsigned long  ulUpTime;
  unsigned long  ulUpCnt;
  signed short   ssMinTemp;
  signed short   ssMaxTemp;
  unsigned long  ulRes[13];      // reserved
};
```

1.22.5.6 Status register

1.22.5.6.1 Status signals and responses

Name:
StatusInput

The signals are recorded in 200 µs intervals. The energy pulse values in this register are not valid when 1 kWh and 1 Wh are set.

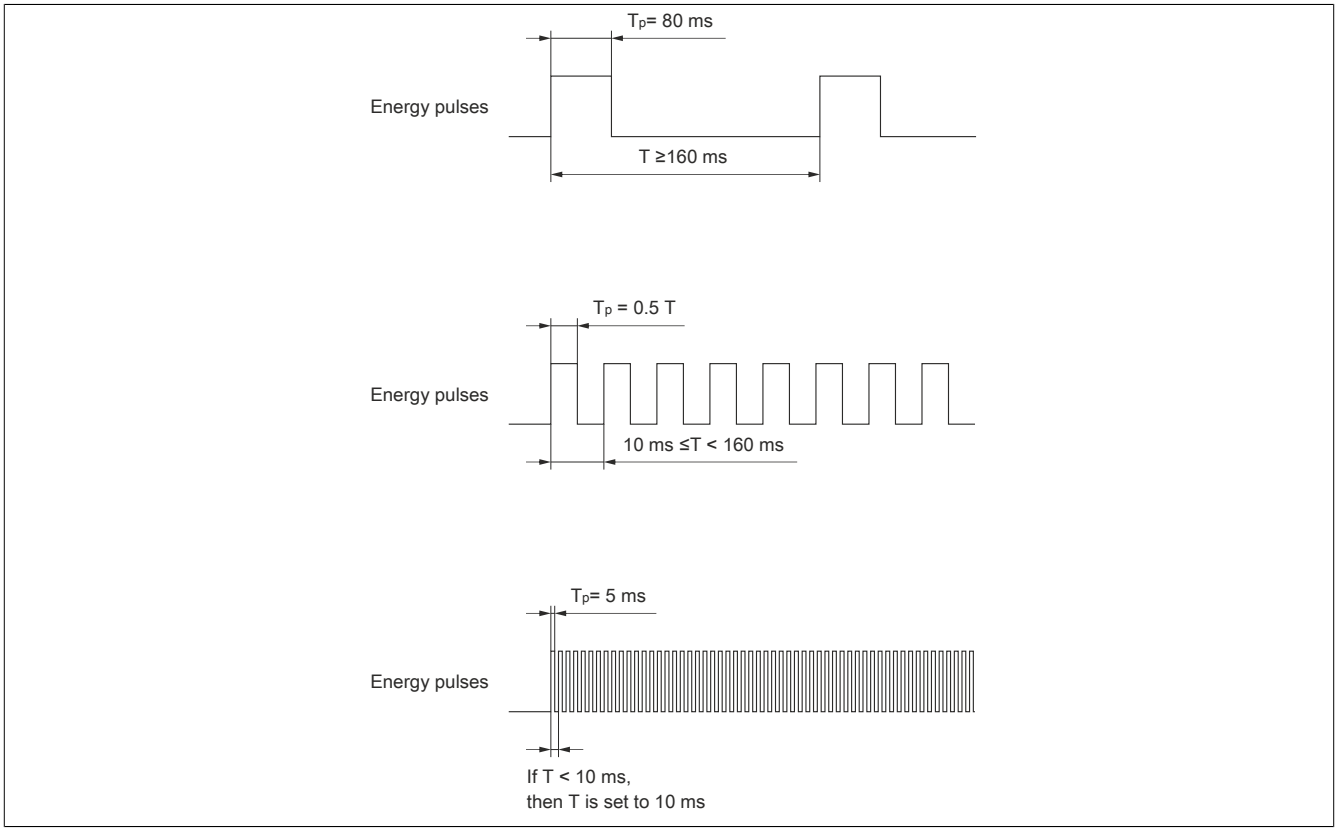
Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	Energy pulse total active energy	0	Energy increase too low
		1	Energy threshold reached
1	Energy pulse total apparent energy Default: Arithmetic or vector sum (see register "MeteringMode" on page 561, bit 6)	0	Energy increase too low
		1	Energy threshold reached
2	Energy pulse total active energy, fundamental wave	0	Energy increase too low
		1	Energy threshold reached
3	Energy pulse total active energy, harmonics	0	Energy increase too low
		1	Energy threshold reached
4	ZX1 zero cross signal (ZCS) – Phase A	0	Zero crossing not detected
		1	Default: Pulse at rising edge of the zero cross signal of the voltage input, can be reconfigured via register "ZXConfig" on page 558
5	ZX2 zero cross signal (ZCS) – Phase B	0	Zero crossing not detected
		1	Default: Pulse at rising edge of the zero cross signal of the voltage input, can be reconfigured via register "ZXConfig" on page 558
6	ZX3 zero cross signal (ZCS) – Phase C	0	Zero crossing not detected
		1	Default: Pulse at rising edge of the zero cross signal of the voltage input, can be reconfigured via register "ZXConfig" on page 558
7	Reserved	0	
8	DFT response sent	x	If the state in the register "ControlOutput" on page 535 corresponds with the response, then the action is complete
9	Energy value update response sent	0	No update
		1	Update complete
10	Energy value response deleted	x	If the state in the register "ControlOutput" on page 535 corresponds with the response, then the action is complete
11	Energy value response set	x	If the state in the register "ControlOutput" on page 535 corresponds with the response, then the action is complete
12 - 15	Reserved	0	

Energy measurement

The length of the energy pulses can vary according to the resulting output rate.



1.22.5.6.2 Control signals

Name:
ControlOutput

Control signals are evaluated in a ~5 ms interval.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	DFT analysis	0	Don't start
		1	Start[1)]
1	Automatically read energy values	0	Do not automatically read
		1	Automatically read
2	Clear energy values	0	Don't delete
		1	Clear[1)]
3	Set energy values	0	Don't start
		1	Start[1)]
4 - 15	Reserved	0	

1) If the state in the register "ControlOutput" on page 535 corresponds with the response, then the action is complete.

1.22.5.6.3 Read timestamp for I/O register (+0x0022 = 16-bit)

Name:
SampleTime01_32bit

NetTime timestamp for the readout time of the status, effective value and power registers.

For additional information about NetTime and timestamps, see "NetTime Technology" on page 598.

Data type	Value	Information
DINT	-2,147,483,647 to 2,147,483,647	NetTime timestamp in µs

1.22.5.6.4 A/D converter system status 1

Name:
SysStatus1

The register is read by the converter in a ~5 ms interval.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 1	Reserved	0	
2	SumStatusPhaseLoss Voltage of one or more phases < failure threshold in the register "PhaseLoseTh" on page 559	0	Voltage within permitted range
		1	Voltage lower than the failure threshold
3	SumStatusPhaseWarning Voltage of one or more phases < warning threshold in the register "SagTh" on page 559	0	Voltage within permitted range
		1	Voltage lower than the warning threshold
4 - 5	Reserved	0	
6	ErrOrderPhasecurrent Error in the order of phase currents	0	No error
		1	Errors
7	ErrOrderPhaseVoltage Error in the order of phase voltages	0	No error
		1	Errors
8	CS3Err Checksum error in configuration block 3	0	No error
		1	Errors
9	Reserved	0	
10	CS2Err Checksum error in configuration block 2	0	No error
		1	Errors
11	Reserved	0	
12	CS1Err Checksum error in configuration block 1	0	No error
		1	Errors
13	Reserved	0	
14	CS0Err Checksum error in configuration block 0	0	No error
		1	Errors
15	Reserved	0	

1.22.5.6.5 A/D converter system status 2

Name:
SysStatus2

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	RevPchgC Direction of the active energy for phase C has changed	0	No change of direction
		1	Direction has changed
1	RevPchgB Direction of the active energy for phase B has changed	0	No change of direction
		1	Direction has changed
2	RevPchgA Direction of the active energy for phase A has changed	0	No change of direction
		1	Direction has changed
3	RevPchgT Direction of the active energy for the sum has changed	0	No change of direction
		1	Direction has changed
4	RevQchgC Direction of the reactive energy for phase C has changed	0	No change of direction
		1	Direction has changed
5	RevQchgB Direction of the reactive energy for phase B has changed	0	No change of direction
		1	Direction has changed
6	RevQchgA Direction of the reactive energy for phase A has changed	0	No change of direction
		1	Direction has changed
7	RevQchgT Direction of the reactive energy for the total has changed	0	No change of direction
		1	Direction has changed
8	Reserved	0	
9	DFTDone DFT analysis complete (temporary bit)	0	DFT analysis not complete
		1	DFT analysis complete
10	SumStatusWarningTHDCurrent THDIx value of one or more phases > warning threshold in register "THDNITh" on page 559	0	THDIx value within permitted range
		1	THDIx value higher than warning threshold
11	SumStatusWarningTHDVoltage THDUx value of one or more phases > warning threshold in register "THDNUTh" on page 559	0	THDUx value within permitted range
		1	THDUx value higher than warning threshold
12 - 13	Reserved	0	
14	ErrIrmsNCalc Calculated value of the neutral conductor > warning threshold in register "INWarnTh0" on page 559	0	Calculated value within permitted range
		1	Calculated value higher than warning threshold
15	ErrIrmsNMeas Measured value of the neutral conductor > warning threshold in register "INWarnTh1" on page 559	0	Measured value within permitted range
		1	Measured value higher than warning threshold

1.22.5.6.6 A/D converter system status 3

Name:
SysStatus3

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	CF1RevFlag Direction of energy pulses	0	Forward[1)]
		1	Back[2)]
1	CF2RevFlag Direction of energy pulses	0	Forward[1)]
		1	Back[2)]
2	CF3RevFlag Direction of energy pulses	0	Forward[1)]
		1	Back[2)]
3	CF4RevFlag Direction of energy pulses	0	Forward[1)]
		1	Back[2)]
4 - 11	Reserved	0	
12	TVSNoload Vector based total apparent power of all phases in "No load" state	0	Status with load
		1	State without load
13	TASNoload Total apparent power of all phases in "No load" state	0	Status with load
		1	State without load
14	TPNoload Total active power of all phases in "No load" state	0	Status with load
		1	State without load
15	TQNoload Total reactive power of all phases in "No load" state	0	Status with load
		1	State without load

1) Forward direction of energy pulses (positive sign of corresponding energy register)
2) Reverse direction of energy pulses (negative sign of corresponding energy register)

1.22.5.6.7 A/D converter system status 4

Name:
SysStatus4

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	LossPhaseC Voltage < failure threshold in the register "PhaseLoseTh" on page 559	0	Voltage within permitted range
		1	Voltage less than the failure threshold
1	LossPhaseB Voltage < failure threshold in the register "PhaseLoseTh" on page 559	0	Voltage within permitted range
		1	Voltage less than the failure threshold
2	LossPhaseA Voltage < failure threshold in the register "PhaseLoseTh" on page 559	0	Voltage within permitted range
		1	Voltage less than the failure threshold
3	Reserved	0	
4	WarningPhaseC Voltage < Warning threshold in register "SagTh" on page 559	0	Voltage within permitted range
		1	Voltage less than the warning threshold
5	WarningPhaseB Voltage < warning threshold in the register "SagTh" on page 559	0	Voltage within permitted range
		1	Voltage less than the warning threshold
6	WarningPhaseA Voltage < warning threshold in the register "SagTh" on page 559	0	Voltage within permitted range
		1	Voltage less than the warning threshold
7 - 15	Reserved	0	

1.22.5.6.8 Selection A/D converter system status 1

Name:
SystemStatusSel01

The most important bits of the "SysStatus1" on page 536 register are stored in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 1	Reserved	0	
2	SumStatusPhaseLoss Voltage of one or more phases < failure threshold in the register "PhaseLoseTh" on page 559	0	Voltage within permitted range
		1	Voltage lower than the failure threshold
3	SumStatusPhaseWarning Voltage of one or more phases < warning threshold in the register "SagTh" on page 559	0	Voltage within permitted range
		1	Voltage lower than the warning threshold
4 - 5	Reserved	0	
6	ErrOrderPhasecurrent Error in the order of phase currents	0	No error
		1	Errors
7	ErrOrderPhaseVoltage Error in the order of phase voltages	0	No error
		1	Errors

1.22.5.6.9 Selection A/D converter system status 2

Name:
SystemStatusSel02

The most important bits of the "SysStatus2" on page 537 register are stored in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 1	Reserved	0	
2	SumStatusWarningTHDCurrent THDIx value of one or more phases > warning threshold in register "THDNITh" on page 559	0	THDIx value within permitted range
		1	THDIx value higher than warning threshold
3	SumStatusWarningTHDVoltage THDUx value of one or more phases > warning threshold in register "THDNUTh" on page 559	0	THDUx value within permitted range
		1	THDUx value higher than warning threshold
4 - 5	Reserved	0	
6	ErrIrmsNCalc The calculated value of the neutral line > warning threshold in the register "INWarnTh0" on page 559	0	Calculated value within permitted range
		1	Calculated value higher than warning threshold
7	ErrIrmsNMeas Measured value of the neutral line > warning threshold in the register "INWarnTh1" on page 559	0	Measured value within permitted range
		1	Measured value higher than warning threshold

1.22.5.6.10 Phase status

Name:
PhaseStatus

This register corresponds to the "SysStatus4" on page 538 register. It contains the status of the 3 phases A, B and C.

Data type	Value
UINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	LossPhaseC Voltage < failure threshold in the register "PhaseLoseTh" on page 559	0	Voltage within permitted range
		1	Voltage less than the failure threshold
1	LossPhaseB Voltage < failure threshold in the register "PhaseLoseTh" on page 559	0	Voltage within permitted range
		1	Voltage less than the failure threshold
2	LossPhaseA Voltage < failure threshold in the register "PhaseLoseTh" on page 559	0	Voltage within permitted range
		1	Voltage less than the failure threshold
3	Reserved	0	
4	WarningPhaseC Voltage < warning threshold in the register "SagTh" on page 559	0	Voltage within permitted range
		1	Voltage less than the warning threshold
5	WarningPhaseB Voltage < warning threshold in the register "SagTh" on page 559	0	Voltage within permitted range
		1	Voltage less than the warning threshold
6	WarningPhaseA Voltage < warning threshold in the register "SagTh" on page 559	0	Voltage within permitted range
		1	Voltage less than the warning threshold
7 - 15	Reserved	0	

1.22.5.7 Analog RMS value registers

1.22.5.7.1 Current RMS value neutral line measured

Name:
IrmsN

Measured value of the neutral current between the P and N connections on the current terminal, multiplied with the transfer factor of the transformer.

Data type	Value	Information
UINT	0 to 65535	Measured value 0.001 Arms

1.22.5.7.2 Voltage RMS value phase A/B/C

Name:
UrmsA
UrmsB
UrmsC

Measured value for N-terminal or virtual zero point.

Data type	Value	Information
UINT	0 to 65535	Measured value 0.01 Vrms

1.22.5.7.3 Current RMS value neutral line calculated

Name:
IrmsNcalc

Calculated value of neutral current derived from the other 3 phases.

Data type	Value	Information
UINT	0 to 65535	Measured value 0.001 Arms

1.22.5.7.4 Current RMS value phase A/B/C

Name:
IrmsA
IrmsB
IrmsC

Measured value of the phase current between the P and N connections on the current terminal, multiplied with the transfer factor of the transformer.

Data type	Value	Information
UINT	0 to 65535	Measured value 0.001 Arms

1.22.5.8 Analog total harmonic distortion (THD) and angle registers

1.22.5.8.1 THD and N value voltage phase A/B/C

Name:
THDNUA
THDNUB
THDNUC

Harmonic ratio = (SQR(RMS value$_{total}$^2 - RMS value$_{fundamental}$^2))/RMS value$_{fundamental}$

Data type	Value	Information
UINT	0 to 10000	Resolution 0.01%

1.22.5.8.2 THD and N value of current phase A/B/C

Name:
THDNIA
THDNIB
THDNIC

Harmonics ratio = (SQR(RMS value$_{total}$^2 - RMS value$_{fundamental}$^2))/RMS value$_{fundamental}$

Data type	Values	Information
UINT	0 to 10000	Resolution 0.01%

1.22.5.8.3 Fundamental frequency measured

Name:
Freq

Measured fundamental frequency of phases A, B and C.

Data type	Value	Information
UINT	0 to 10000	Resolution 0.01 Hz

1.22.5.8.4 Phase angle of power on phase A/B/C

Name:
PAngleA
PAngleB
PAngleC

Middle phase angle (power angle) of the current to the voltage based on the zero-crossing detection.

Data type	Value	Information
INT	-1800 to 1800	Resolution 0.1°

1.22.5.8.5 Temperature of the converter

Name:
Temperature

This register contains the internal temperature of the transformer component. The temperature is recorded in a 100 ms interval.

Data type	Value	Information
INT	-200 to 200	Resolution 1°C

1.22.5.8.6 Phase angle of voltage on phase A/B/C

Name:
UAngleA
UAngleB
UAngleC

The value for phase A is always 0. On the other phases, the angle corresponds with the offset to A. This is based on the zero-crossing detection.

Data type	Value	Information
INT	-1800 to 1800	Resolution 0.1°

1.22.5.9 Analog power registers

1.22.5.9.1 Vector sum of total apparent power decimal places

Name:
SVmeanTLSB

The value in this register corresponds to a quarter of the actual power and can be converted in the application according to the example below.

Conversion example

Actual vector sum of the total apparent power = ((REAL)SVmeanT * 4) + ((REAL)SVmeanTLSB * 4/256)

Data type	Value	Information
UINT	0 to 65535	Resolution unit/LSB corresponds to 4/265 VA.

1.22.5.9.2 Vector sum of the total apparent power MSW

Name:
SVmeanT

The value in the register equals a fourth of the actual power. The calculation is made in accordance with IEEE 1459.

This value must be multiplied by 4 by the application. Calculation formula for actual power:

Actual vector sum of the total apparent power MSW = register value * 4 (complex sum)

Data type	Value	Information
UINT	0 to 32767	Resolution 4 VA

1.22.5.9.3 Total active power

Name:
PmeanT

The value in the register equals a fourth of the actual power. The calculation can be performed in either absolute or arithmetic mode (see register "MeteringMode" on page 561 <Bit 3>). Each phase can be separately enabled for the power calculation (see register "MeteringMode" on page 561 <Bits 0, 1 and 2>).

This value must be multiplied by 4 by the application. Calculation formula for actual power:

Actual total active power = Register value * 4

Data type	Value	Information
INT	-32767 to 32767	Resolution 4 W

1.22.5.9.4 Active power on phase A/B/C

Name:
PmeanA
PmeanB
PmeanC

Active power on the phase. Each phase can be separately enabled for the power calculation (see register "MeteringMode" on page 561 <Bits 0, 1 and 2>).

Data type	Value	Information
INT	-32767 to 32767	Resolution 1 W

1.22.5.9.5 Total reactive power

Name:
QmeanT

The value in the register equals a fourth of the actual power. The calculation can be performed in either absolute or arithmetic mode (see register "MeteringMode" on page 561 <Bit 4>). Each phase can be separately enabled for the power calculation (see register "MeteringMode" on page 561 <Bits 0, 1 and 2>).

This value must be multiplied by 4 by the application. Calculation formula for actual power:

Actual total reactive power = Register value * 4

Data type	Value	Information
INT	-32767 to 32767	Resolution 4 var

1.22.5.9.6 Reactive power on phase A/B/C

Name:
QmeanA
QmeanB
QmeanC

Reactive power on the phase. Each phase can be separately enabled for the power calculation (see register "MeteringMode" on page 561 <Bits 0, 1 and 2>).

Data type	Value	Information
INT	-32767 to 32767	Resolution 1 var

1.22.5.9.7 Total apparent power

Name:
SmeanT

The value in the register equals a fourth of the actual power. The power is calculated in arithmetic mode. Each phase can be separately enabled for the power calculation (see register "MeteringMode" on page 561 <Bits 0, 1 and 2>).

This value must be multiplied by 4 by the application. Calculation formula for actual power:

Actual total apparent power = Register value * 4

Data type	Value	Information
INT	0 to 32767	Resolution 4 VA

1.22.5.9.8 Apparent power on phase A/B/C

Name:
SmeanA
SmeanB
SmeanC

Apparent power on the phase. Each phase can be separately enabled for the power calculation (see register "MeteringMode" on page 561 <Bits 0, 1 and 2>).

Data type	Value	Information
INT	0 to 32767	Resolution 1 VA

1.22.5.9.9 Total power factor

Name:
PFmeanT

Data type	Value	Information
INT	-1000 to 1000	Resolution 0.001

1.22.5.9.10 Power factor on phase A/B/C

Name:
PFmeanA
PFmeanB
PFmeanC

Data type	Value	Information
INT	-1000 to 1000	Resolution 0.001

1.22.5.9.11 Total active power of fundamental wave

Name:
PmeanTF

The value in the register equals a fourth of the actual power.

This value must be multiplied by 4 by the application. Calculation formula for actual power:

Actual total active power of fundamental wave = Register value * 4

Data type	Value	Information
INT	-32767 to 32767	Resolution 4 W

1.22.5.9.12 Fundamental wave active power on phase A/B/C

Name:
PmeanAF
PmeanBF
PmeanCF

Active power of fundamental wave on the phase.

Data type	Value	Information
INT	-32767 to 32767	Resolution 1 W

1.22.5.9.13 Total active power of harmonics

Name:
PmeanTH

The value in the register equals a fourth of the actual power.

This value must be multiplied by 4 by the application. Calculation formula for actual power:

Actual total active power of harmonics = Register value * 4

Data type	Value	Information
INT	-32767 to 32767	Resolution 4 W

1.22.5.9.14 Harmonics active power on phase A/B/C

Name:
PmeanAH
PmeanBH
PmeanCH

Active power of harmonics on the phase.

Data type	Value	Information
INT	-32767 to 32767	Resolution 1 W

1.22.5.10 Analog energy registers

1.22.5.10.1 Read timestamp for energy register (+0x0022 = 16-bit)

Name:
SampleTime02_32bit

NetTime timestamp for the readout time of the energy registers.

For additional information about NetTime and timestamps, see "NetTime Technology" on page 598.

Data type	Value	Information
DINT	-2,147,483,647 to 2,147,483,647	NetTime timestamp in µs

1.22.5.10.2 Forward total active energy

Name:
APenergyT

Total active energy in forward direction.

Data type	Value	Information
UDINT	0 to 4294967295	Resolution corresponding to setting in register "Power line constants" on page 560.

Notes:

- The register is updated automatically after being enabled, see register "ControlOutput" on page 535 <bit 1>
- The register is deleted upon request, see register "ControlOutput" on page 535 <bit 2>
- The register is set upon request, see register "ControlOutput" on page 535 <bit 3>
- For information about energy unit; see register "Power line constants" on page 560

1.22.5.10.3 Forward active energy on phase A/B/C

Name:
APenergyA
APenergyB
APenergyC

Active energy in forward direction of the phase.

Data type	Value	Information
UDINT	0 to 4294967295	Resolution corresponding to setting in register "Power line constants" on page 560.

Notes:

- The register is updated automatically after being enabled, see register "ControlOutput" on page 535 <bit 1>
- The register is deleted upon request, see register "ControlOutput" on page 535 <bit 2>
- The register is set upon request, see register "ControlOutput" on page 535 <bit 3>
- For information about energy unit; see register "Power line constants" on page 560

1.22.5.10.4 Reverse total active energy

Name:
ANenergyT

Total active energy in reverse direction.

Data type	Value	Information
UDINT	0 to 4294967295	Resolution corresponding to setting in register "Power line constants" on page 560.

Notes:

- The register is updated automatically after being enabled, see register "ControlOutput" on page 535 <bit 1>
- The register is deleted upon request, see register "ControlOutput" on page 535 <bit 2>
- The register is set upon request, see register "ControlOutput" on page 535 <bit 3>
- For information about energy unit; see register "Power line constants" on page 560

1.22.5.10.5 Reverse active energy on phase A/B/C

Name:
ANenergyA
ANenergyB
ANenergyC

Active energy in reverse direction of the phase.

Data type	Value	Information
UDINT	0 to 4294967295	Resolution corresponding to setting in register "Power line constants" on page 560.

Notes:

- The register is updated automatically after being enabled, see register "ControlOutput" on page 535 <bit 1>
- The register is deleted upon request, see register "ControlOutput" on page 535 <bit 2>
- The register is set upon request, see register "ControlOutput" on page 535 <bit 3>
- For information about energy unit; see register "Power line constants" on page 560

1.22.5.10.6 Forward total reactive energy

Name:
RPenergyT

Total reactive energy in forward direction.

Data type	Value	Information
UDINT	0 to 4294967295	Resolution corresponding to setting in register "Power line constants" on page 560.

Notes:

- The register is updated automatically after being enabled, see register "ControlOutput" on page 535 <bit 1>
- The register is deleted upon request, see register "ControlOutput" on page 535 <bit 2>
- The register is set upon request, see register "ControlOutput" on page 535 <bit 3>
- For information about energy unit; see register "Power line constants" on page 560

1.22.5.10.7 Forward reactive energy on phase A/B/C

Name:
RPenergyA
RPenergyB
RPenergyC

Reactive energy in forward direction of the phase.

Data type	Value	Information
UDINT	0 to 4294967295	Resolution corresponding to setting in register "Power line constants" on page 560.

Notes:

- The register is updated automatically after being enabled, see register "ControlOutput" on page 535 <bit 1>
- The register is deleted upon request, see register "ControlOutput" on page 535 <bit 2>
- The register is set upon request, see register "ControlOutput" on page 535 <bit 3>
- For information about energy unit; see register "Power line constants" on page 560

1.22.5.10.8 Reverse total reactive energy

Name:
RNenergyT

Total reactive energy in reverse direction.

Data type	Value	Information
UDINT	0 to 4294967295	Resolution corresponding to setting in register "Power line constants" on page 560.

Notes:

- The register is updated automatically after being enabled, see register "ControlOutput" on page 535 <bit 1>
- The register is deleted upon request, see register "ControlOutput" on page 535 <bit 2>
- The register is set upon request, see register "ControlOutput" on page 535 <bit 3>
- For information about energy unit; see register "Power line constants" on page 560

1.22.5.10.9 Reverse reactive energy of the phase A/B/C

Name:
RNenergyA
RNenergyB
RNenergyC

Reactive energy in reverse direction of the phase.

Data type	Value	Information
UDINT	0 to 4294967295	Resolution corresponding to setting in register "Power line constants" on page 560.

Notes:

- The register is updated automatically after being enabled, see register "ControlOutput" on page 535 <bit 1>
- The register is deleted upon request, see register "ControlOutput" on page 535 <bit 2>
- The register is set upon request, see register "ControlOutput" on page 535 <bit 3>
- For information about energy unit; see register "Power line constants" on page 560

1.22.5.10.10 Arithmetic total apparent energy

Name:
SAenergyT

Data type	Value	Information
UDINT	0 to 4294967295	Resolution corresponding to setting in register "Power line constants" on page 560.

Notes:

- The register is updated automatically after being enabled, see register "ControlOutput" on page 535 <bit 1>
- The register is deleted upon request, see register "ControlOutput" on page 535 <bit 2>
- The register is set upon request, see register "ControlOutput" on page 535 <bit 3>
- For information about energy unit; see register "Power line constants" on page 560

1.22.5.10.11 Apparent energy on phase A/B/C

Name:
SenergyA
SenergyB
SenergyC

Data type	Value	Information
UDINT	0 to 4294967295	Resolution corresponding to setting in register "Power line constants" on page 560.

Notes:

- The register is updated automatically after being enabled, see register "ControlOutput" on page 535 <bit 1>
- The register is deleted upon request, see register "ControlOutput" on page 535 <bit 2>
- The register is set upon request, see register "ControlOutput" on page 535 <bit 3>
- For information about energy unit; see register "Power line constants" on page 560

1.22.5.10.12 Vectorized total apparent energy

Name:
SVenergyT

Data type	Value	Information
UDINT	0 to 4294967295	Resolution corresponding to setting in register "Power line constants" on page 560.

Notes:

- The register is updated automatically after being enabled, see register "ControlOutput" on page 535 <bit 1>
- The register is deleted upon request, see register "ControlOutput" on page 535 <bit 2>
- The register is set upon request, see register "ControlOutput" on page 535 <bit 3>
- For information about energy unit; see register "Power line constants" on page 560

1.22.5.10.13 Forward fundamental wave total active energy

Name:
APenergyTF

Fundamental wave of total active energy in forward direction.

Data type	Value	Information
UDINT	0 to 4294967295	Resolution corresponding to setting in register "Power line constants" on page 560.

Notes:

- The register is updated automatically after being enabled, see register "ControlOutput" on page 535 <bit 1>
- The register is deleted upon request, see register "ControlOutput" on page 535 <bit 2>
- The register is set upon request, see register "ControlOutput" on page 535 <bit 3>
- For information about energy unit; see register "Power line constants" on page 560

1.22.5.10.14 Forward fundamental wave active energy on phase A/B/C

Name:
APenergyAF
APenergyBF
APenergyCF

Fundamental wave of active energy in forward direction of the phase.

Data type	Value	Information
UDINT	0 to 4294967295	Resolution corresponding to setting in register "Power line constants" on page 560.

Notes:

- The register is updated automatically after being enabled, see register "ControlOutput" on page 535 <bit 1>
- The register is deleted upon request, see register "ControlOutput" on page 535 <bit 2>
- The register is set upon request, see register "ControlOutput" on page 535 <bit 3>
- For information about energy unit; see register "Power line constants" on page 560

1.22.5.10.15 Reverse fundamental wave total active energy

Name:
ANenergyTF

Fundamental wave of total active energy in reverse direction.

Data type	Value	Information
UDINT	0 to 4294967295	Resolution corresponding to setting in register "Power line constants" on page 560.

Notes:

- The register is updated automatically after being enabled, see register "ControlOutput" on page 535 <bit 1>
- The register is deleted upon request, see register "ControlOutput" on page 535 <bit 2>
- The register is set upon request, see register "ControlOutput" on page 535 <bit 3>
- For information about energy unit; see register "Power line constants" on page 560

1.22.5.10.16 Reverse fundamental wave active energy on phase A/B/C

Name:
ANenergyAF
ANenergyBF
ANenergyCF

Fundamental wave of active energy in reverse direction of the phase.

Data type	Value	Information
UDINT	0 to 4294967295	Resolution corresponding to setting in register "Power line constants" on page 560.

Notes:

- The register is updated automatically after being enabled, see register "ControlOutput" on page 535 <bit 1>
- The register is deleted upon request, see register "ControlOutput" on page 535 <bit 2>
- The register is set upon request, see register "ControlOutput" on page 535 <bit 3>
- For information about energy unit; see register "Power line constants" on page 560

1.22.5.10.17 Forward harmonics total active energy

Name:
APenergyTH

Harmonics of total active energy in forward direction.

Data type	Value	Information
UDINT	0 to 4294967295	Resolution corresponding to setting in register "Power line constants" on page 560.

Notes:

- The register is updated automatically after being enabled, see register "ControlOutput" on page 535 <bit 1>
- The register is deleted upon request, see register "ControlOutput" on page 535 <bit 2>
- The register is set upon request, see register "ControlOutput" on page 535 <bit 3>
- For information about energy unit; see register "Power line constants" on page 560

1.22.5.10.18 Forward harmonics active energy on phase A/B/C

Name:
APenergyAH
APenergyBH
APenergyCH

Harmonics of active energy in forward direction of the phase.

Data type	Value	Information
UDINT	0 to 4294967295	Resolution corresponding to setting in register "Power line constants" on page 560.

Notes:

- The register is updated automatically after being enabled, see register "ControlOutput" on page 535 <bit 1>
- The register is deleted upon request, see register "ControlOutput" on page 535 <bit 2>
- The register is set upon request, see register "ControlOutput" on page 535 <bit 3>
- For information about energy unit; see register "Power line constants" on page 560

1.22.5.10.19 Reverse harmonics total active energy

Name:
ANenergyTH

Harmonics of total active energy in forward direction.

Data type	Value	Information
UDINT	0 to 4294967295	Resolution corresponding to setting in register "Power line constants" on page 560.

Notes:

- The register is updated automatically after being enabled, see register "ControlOutput" on page 535 <bit 1>
- The register is deleted upon request, see register "ControlOutput" on page 535 <bit 2>
- The register is set upon request, see register "ControlOutput" on page 535 <bit 3>
- For information about energy unit; see register "Power line constants" on page 560

1.22.5.10.20 Reverse harmonics active energy on phase A/B/C

Name:
ANenergyAH
ANenergyBH
ANenergyCH

Harmonics of active energy in reverse direction of the phase.

Data type	Value	Information
UDINT	0 to 4294967295	Resolution corresponding to setting in register "Power line constants" on page 560.

Notes:

- The register is updated automatically after being enabled, see register "ControlOutput" on page 535 <bit 1>
- The register is deleted upon request, see register "ControlOutput" on page 535 <bit 2>
- The register is set upon request, see register "ControlOutput" on page 535 <bit 3>
- For information about energy unit; see register "Power line constants" on page 560

1.22.5.10.21 Total active energy combined

Name:
AEnergyT

Total active energy in forward and backward direction.

Internal calculation formula for the total active energy:

AEnergyT = (DINT)(APenergyT - ANenergyT) Calculation overflows are ignored

Data type	Value	Information
DINT	-2,147,483,647 to 2,147,483,647	Resolution corresponding to setting in register "Power line constants" on page 560.

Notes:

- The register is updated automatically after being enabled, see register "ControlOutput" on page 535 <bit 1>
- The register is deleted upon request, see register "ControlOutput" on page 535 <bit 2>
- The register is set upon request, see register "ControlOutput" on page 535 <bit 3>
- For information about energy unit; see register "Power line constants" on page 560

1.22.5.10.22 Total reactive energy combined

Name:
REnergyT

Total reactive power in the forward and reverse directions.

Internal calculation formula for the total reactive energy:

Data type	Value	Information
DINT	-2,147,483,647 to 2,147,483,647	Resolution corresponding to setting in register "Power line constants" on page 560.

Notes:

- The register is updated automatically after being enabled, see register "ControlOutput" on page 535 <bit 1>
- The register is deleted upon request, see register "ControlOutput" on page 535 <bit 2>
- The register is set upon request, see register "ControlOutput" on page 535 <bit 3>
- For information about energy unit; see register "Power line constants" on page 560

1.22.5.11 Analog discrete Fourier transformation register (DFT)

1.22.5.11.1 Read timestamp for DFT register (+0x0022 = 16-bit)

Name:
SampleTime03_32bit

NetTime timestamp for the readout time of the DFT registers.

Data type	Value	Information
DINT	-2,147,483,647 to 2,147,483,647	NetTime timestamp in µs

1.22.5.11.2 Harmonic distortion register (HD) current I and voltage V for phases A/B/C

Name:
DftAI0 to DftAI30
DftAV0 to DftAV30
DftBI0 to DftBI30
DftBV0 to DftBV30
DftCI0 to DftCI30
DftCV0 to DftCV30

Ratio of 2nd to 32nd order harmonic wave components.

Conversion from % = register value / 163.84

Data type	Value	Information
UINT	0 to 32767	Ratio of frequency component

1.22.5.11.3 THD register current I and voltage V for phases A/B/C

Name:
DftAI31
DftAV31
DftBI31
DftBV31
DftCI31
DftCV31

Ratio of total harmonic distortion.

Conversion from % = register value / 163.84

Data type	Value	Information
UINT	0 to 32767	Total harmonic distortion

1.22.5.11.4 Fundamental wave current on phase A/B/C

Name:
DftAI_Fund
DftBI_Fund
DftCI_Fund

Calculation of the fundamental wave current

Data type	Values	Information
UINT	0 to 32767	Fundamental wave current in mA

The fundamental wave current is calculated according to the following formula:

Standard calculation

$$\text{Fundamental wave}_{mA} = \text{Register value} * 3.2656 * \frac{\text{Ratio}_{Real}}{\text{Ratio}_{Configured}}$$

Inverted calculation

$$\text{Fundamental wave}_{mA} = \text{Register value} * 3.2656 * \frac{\text{Ratio}_{Configured}}{\text{Ratio}_{Real}}$$

Legend

Register value — The value of this register

$\text{Ratio}_{Configured}$ — Configured rated value divided by 10.
See "Current transformer rating phase A/B/C/N" on page 556.

Ratio_{Real} — The real rated value depends on the AP module being used:

Module	Value
X20AP3111	25000
X20AP3121	500
X20AP3131	100
X20AP3161	500
X20AP3171	Default: 5000 Inverted: 1
All others	1

1.22.5.11.5 Fundamental wave voltage on phase A/B/C

Name:
DftAV_Fund
DftBV_Fund
DftCV_Fund

Calculation of the fundamental wave voltage

Data type	Values	Information
UINT	0 to 32767	Fundamental value voltage in volts

The fundamental wave voltage is calculated according to the following formula:

$$\text{Fundamental wave}_{Voltage} = \text{Register value} * 3.2656 * 10^{-2}$$

1.22.5.12 Environment variables

1.22.5.12.1 Operating time

Name:
ulUpTime

Total operating time of the module.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Operating time in seconds

1.22.5.12.2 Switch-on and reset counter

Name:
ulUpCount

Switch-on and reset counter of the module.

Data type	Value	Information
UDINT	0 to 4,294,967,295	Switch-on and reset counter

1.22.5.12.3 Minimum operating temperature

Name:
ssMinTemp

Lowest measured module temperature since the last time it was started.

Data type	Value	Information
INT	-200 to 200	Resolution 1°C

1.22.5.12.4 Maximum operating temperature

Name:
ssMaxTemp

Highest measured module temperature since the last time it was started.

Data type	Value	Information
INT	-200 to 200	Resolution 1°C

1.22.5.13 Module configuration

1.22.5.13.1 Mode register

Name:
ChanControl

Data type	Value	Bus controller default setting
UINT	See bit structure.	15

Bit structure:

Bit	Name	Value	Information
0	Channel status LED for phase A	0	Off
		1	On (bus controller default setting)
1	Channel status LED for phase B	0	Off
		1	On (bus controller default setting)
2	Channel status LED for phase C	0	Off
		1	On (bus controller default setting)
3	Reserved	0	
4	Neutral current monitor and status LED	0	Off (bus controller default setting)
		1	On
5	Neutral current status derived from the calculated or measured value	0	Derived from the calculated value (bus controller default setting)
		1	Derived from the measured value
6	Conversion of energy register to Wh and kWh[2)]	0	Disabled (1 Ws, 10 Ws, 100 Ws, 1 kWs) (bus controller default setting)
		1	Enabled (1 Wh and 1 kWh)
7	Display current values despite power failure[3)]	0	Off[3)] (bus controller default setting)
		1	On
8 - 15	Oversampling with prescaler	0	Disabled (bus controller default setting)
		1 - 255	Enabled Sample cycle time as a multiple of 125 µs; only in the "Oversampling" function model

1) When 1 Wh and 1 kWh are set, the energy pulses on the register "Status signals and responses" on page 534 may not be used.
2) When a power failure occurs, all current values are held at 0 by default.
3) According to the power failure status of the individual phases, the following values are held at 0 by default.

- Mains frequency, phase angle, power factor
- Effective voltage and current values
- Active, reactive and apparent power values

1.22.5.13.2 Analog minimum current for active current channel LEDs

Name:
IDispTh

The indicator threshold defines the RMS value of the current at which the status LED for the phase current is illuminated. The default values vary from module to module and should be adjusted to the maximum primary current.
Suggestion: 1% of maximum value

Data type	Value	Information
UINT	1 to 65000	RMS indicator threshold in mA. Bus controller default setting:

Module	Indicator threshold
X20AP3111	200 mA
X20AP3121/22	500 mA
X20AP3131/32	500 mA
X20AP3161	500 mA
X20AP3171	500 mA

1.22.5.13.3 Current transformer rating phase A/B/C/N

Name:
I_RatioA
I_RatioB
I_RatioC
I_RatioN

The following current transformer measurements are applied in these registers. The permissible values are module-dependent (0.1 resolution).

- **X20AP3111, 3121/22 and 3131/32:** The measured current is multiplied by the current transformation ratio.
- **X20AP3161:** The maximum primary current of the transformer is configured.
- **X20AP3171:** The current transformation ratio of the Rogowski coil is entered. This is the voltage in µV that the coil provides at 10 A primary current (0.1 µV/A).

Data type	Value	Information
UINT	x	Current transformer measurement. Bus controller default setting:

Module	Rating
X20AP3111	Transformation ratio: 10 to 32500. Bus controller default setting: 25000
X20AP3121/22	Transformation ratio: 10 to 650. Bus controller default setting: 500
X20AP3131/32	Transformation ratio: 10 to 130. Bus controller default setting: 100
X20AP3161	Measurement range: 50 to 650. Bus controller default setting: 500
X20AP3171	Current transformation ratio: 2600 to 8000. Bus controller default setting: 5000

Information:

The maximum resulting current must not exceed the value of 65000 mA.

1.22.5.14 Update requests

1.22.5.14.1 User configuration

The following procedure has to be complied with to apply the new values in a configuration change.

1) Writing update register
   - CfgUpdate = 0xFFFF
   - Cs0Update = 0xFFFF
2) Writing the desired configuration register
3) Writing update register
   - CfgUpdate = 0x1
   - Cs0Update = 0x1

1.22.5.14.2 Update request status configuration register

Name:
CfgUpdate

The registers in section "A/D converter status configuration" on page 558 are only applied after changing this register. Writing with 0xFFFF only resets this register without applying the values.

Data type	Value	Information
UINT	0 to 65535	Update request. Bus controller default setting: 65535

1.22.5.14.3 Update request A/D converter Cs0, Cs1 and Cs3 register

Name:
Cs0Update
Cs1Update
Cs3Update

The registers of the respective section are only applied after changing the corresponding CsxUpdate register. These include:

- Cs0Update: 3 registers in section "A/D converter measurement configuration checksum 0" on page 560
- Cs1Update: 3 registers in "A/D converter power calibration checksum 1" on page 565
- Cs3Update: 14 registers in section "A/D converter RMS value synchronization checksum 3" on page 563

Writing with 0xFFFF only resets the affected register without applying the value.

Data type	Value	Information
UINT	0 to 65535	Update request. Bus controller default setting: 65535

1.22.5.14.4 Reading update request A/D converter Cs1 and Cs3 register

Name:
Cs1UpdateFB
Cs3UpdateFB

The A/D converter configuration registers in the sections "A/D converter status configuration" on page 558 and "A/D converter measurement configuration checksum 0" on page 560 are only transferred to the feedback buffer after transfer to the A/D converter is complete.

Data type	Value	Information
UINT	0 to 65535	

1.22.5.15 A/D converter status configuration

Changes in the registers in this section are only applied after an update request in register "CfgUpdate" on page 556.

1.22.5.15.1 A/D converter hardware signal pinout

Name:
ZXConfig

Data type	Value	Bus controller default setting
UINT	See bit structure.	0x4400

Bit structure:

Bit	Name	Value	Information
0	Zero cross signals	0	Enabled (bus controller default setting)
		1	Disabled
1 - 2	ZX20Con Trigger zero crossing	00	Positive zero crossing (bus controller default setting)
		01	Negative zero crossing
		10	Both zero cross-overs
		11	No zero crossing
3 - 4	ZX1Con Trigger zero crossing	00	Positive zero crossing (bus controller default setting)
		01	Negative zero crossing
		10	Both zero cross-overs
		11	No zero crossing
5 - 6	ZX2Con Trigger zero crossing	00	Positive zero crossing (bus controller default setting)
		01	Negative zero crossing
		10	Both zero cross-overs
		11	No zero crossing
7 - 9	ZX0Src Signal source for ZX0 hardware signal	000	Voltage A (bus controller default setting)
		001	Voltage B
		010	Voltage C
		011	Fix 0
		100	Current A
		101	Current B
		110	Current C
		111	Fix 0
10 - 12	ZX1Src Signal source for ZX1 hardware signal	000	Voltage A
		001	Voltage B (bus controller default setting)
		010	Voltage C
		011	Fix 0
		100	Current A
		101	Current B
		110	Current C
		111	Fix 0
13 - 15	ZX2Src Signal source for ZX2 hardware signal	000	Voltage A
		001	Voltage B
		010	Voltage C (bus controller default setting)
		011	Fix 0
		100	Current A
		101	Current B
		110	Current C
		111	Fix 0

1.22.5.15.2 Voltage warning threshold

Name:
SagTh

This register defines an RMS voltage value for monitoring the voltage warning signals.

Data type	Value	Information
UINT	5000 to 50000	Resolution 0.01 V. Bus controller default setting: 12368

1.22.5.15.3 Power failure threshold

Name:
PhaseLoseTh

This register defines an RMS voltage value for monitoring the power failure signals.

Data type	Value	Information
UINT	1000 to 6000	Resolution 0.01 V. Bus controller default setting: 2420

1.22.5.15.4 Warning threshold for the calculated neutral current

Name:
INWarnTh0

Current value for monitoring the calculated neutral line current.

Data type	Value	Information
UINT	0 to 65000	Resolution 0.001 A. Bus controller default setting: 50

1.22.5.15.5 Warning threshold for the measured neutral current.

Name:
INWarnTh1

Current value for monitoring the measured neutral line current.

Data type	Value	Information
UINT	0 to 65000	Resolution 0.001 A. Bus controller default setting: 50

1.22.5.15.6 Warning threshold for voltage THD overshoot

Name:
THDNUTh

Percentage value defining warning threshold for THD ratio.

Data type	Value	Information
UINT	0 to 10000	Resolution 0.01%. Bus controller default setting: 1000

1.22.5.15.7 Warning threshold for current THD overshoot

Name:
THDNITh

Percentage value defining warning threshold for THD ratio.

Data type	Value	Information
UINT	0 to 10000	Resolution 0.01%. Bus controller default setting: 1000

1.22.5.16 A/D converter measurement configuration checksum 0

Changes in the registers in this section are only applied after an update request in register "Cs0Update" on page 557.

1.22.5.16.1 Power line constants

Name:
PLconstH
PLconstL

Base value for power line constant.

10 increments in the energy register result in 1 energy pulse. Base value 0x4A81 7C80 = 1,250,000,000 corresponds to 360 energy pulses per kWh or 0.1 energy pulses per kWs. In the energy registers, this results in 1 kWs per position.

The two registers can be set to the following values. Other values are not allowed

Data type	PLConstH	PLConstL	1 increment in the energy register corresponds to:
UINT	0x0013	0x12D0	1 Ws[1)]
	0x00BE	0xBC20	10 Ws[1)]
	0x0773	0x5940	100 Ws[1)]
	0x4A81	0x7C80	1 kWs[1)] (bus controller default setting)
	0x0010	0x0034	1 Wh[2)]
	0x417B	0xCE6C	1 kWh[2)]

1) Register "ChanControl" on page 555, bit 6 = 0
2) Register "ChanControl" on page 555, bit 6 = 1

Information:

When 1 Wh and 1 kWh are set, the energy pulses on the register "StatusInput" on page 534 may not be used.

1.22.5.16.2 Analog A/D converter measurement setting 1

Name:
MeteringMode

Data type	Value	Bus controller default setting
UINT	See bit structure.	135

Bit structure:

Bit	Name	Value	Information
0	Enables phase C for adding the power and energy values together	0	Not released
		1	Enabled (bus controller default setting)
1	Enables phase B for adding the power and energy values together	0	Not released
		1	Enabled (bus controller default setting)
2	Enables phase A for adding the power and energy values together	0	Not released
		1	Enabled (bus controller default setting)
3	Calculation method for adding active power and active energy	0	Arithmetic sum (bus controller default setting)
		1	Absolute sum
4	Calculation method for adding reactive power and reactive energy	0	Arithmetic sum (bus controller default setting)
		1	Absolute sum
5	Reserved	0	
6	Selects apparent energy for Energypulse2-Source	0	Arithmetic sum (bus controller default setting)
		1	Vector sum
7	Energypulse2-Source	0	Apparent energy
		1	Reactive energy (bus controller default setting)
8	Measuring configuration	0	3P4W (bus controller default setting)
		1	3P3W
9	Resolution of energy register	0	Must be 0!
10	Integrator for DIDT current transformer	0	Off (bus controller default setting)
		1	On
11	High-pass filter	0	On (bus controller default setting)
		1	Off
12	Basis frequency	0	50 Hz (bus controller default setting)
		1	60 Hz
13	Phase assignment	0	I1 to phase A and I3 to phase C (bus controller default setting)
		1	I1 to Phase C and I3 to Phase A
14 - 15	Reserved	0	

Comments regarding measurement configurations:

Measuring configuration	Note
3P4W	Monitors the phasing of voltages and currents: Phase A before phase B before phase C
3P3W	Measuring configuration: Phase A and phase C, N connection bridges to phase B or open
	Measurement: e.g. the 2 phases A and C and the 2 corresponding currents are measured, phase B disabled
	Monitors the phasing of voltages and currents: Phase difference between A and C >180°

1.22.5.17 User calibration of current and voltage values

Use the following procedure to properly calculate gain and offset:

- Read out the predefined values:
  See "A/D converter RMS value synchronization – read" on page 562.
- Calculate and set new values:
  See "A/D converter RMS value synchronization checksum 3" on page 563.
- Update predefined values by setting the register "Cs3Update" on page 557. The predefined values have been updated when the value in the register "Cs3UpdateFB" on page 557 is equal to the value of <Cs3Update>.

1.22.5.18 A/D converter RMS value synchronization – read

1.22.5.18.1 General information

The values in the registers specified in this section must be read at the beginning of the calibration. This is the only way to ensure that the gain and offset will be calculated correctly.

The values contained in the registers correspond to the $value_{old}$ in the calculation formulas for gain and offset (see "A/D converter RMS value synchronization checksum 3" on page 563).

1.22.5.18.2 Voltage RMS value gain phase A/B/C

Name:
UGainA_R
UGainB_R
UGainC_R

Data type	Value
UINT	0 to 65535

1.22.5.18.3 Current RMS value gain phase A/B/C/N

Name:
IGainA_R
IGainB_R
IGainC_R
IGainN_R

Data type	Value
UINT	0 to 65535

1.22.5.18.4 Voltage RMS value offset phase A/B/C

Name:
UoffsetA_R
UoffsetB_R
UoffsetC_R

Data type	Value
INT	-32767 to 32767

1.22.5.18.5 Current RMS value offset phase A/B/C/N

Name:
IoffsetA_R
IoffsetB_R
IoffsetC_R
IoffsetN_R

Data type	Value
INT	-32767 to 32767

1.22.5.19 A/D converter RMS value synchronization checksum 3

Changes in the registers in this section are only applied after an update request in register "Cs3Update" on page 557.

1.22.5.19.1 Voltage RMS value gain phase A/B/C

Name:
UGainA_W
UGainB_W
UGainC_W

The resulting gain is calculated using the following formula:

$Value_{new} = Value_{old} * correction\ factor,\ determined\ when\ U = U_n$

Data type	Value	Information
UINT	0 to 65535	Voltage RMS value gain, phase-based. Bus controller default setting: 26400

1.22.5.19.2 Current RMS value gain phase A/B/C/N

Name:
IGainA_W
IGainB_W
IGainC_W
IGainN_W

The resulting gain is calculated using the following formula:

$Value_{new} = Value_{old} * correction\ factor,\ determined\ when\ I = I_n$

Data type	Value	Information
UINT	0 to 65535	Current RMS value gain, phase-based. Bus controller default setting: X20AP3111, X20AP312x: 31248 X20AP313x: 38704 X20AP3161: 23339 X20AP3171: 16653

1.22.5.19.3 Voltage RMS value offset phase A/B/C

Name:
UoffsetA_W
UoffsetB_W
UoffsetC_W

Corresponds to the negated value of the corresponding RMS value register when U = 0.

Data type	Value	Information
INT	-32767 to 32767	RMS value voltage offset, phase-based. Bus controller default setting: 0

1.22.5.19.4 Current RMS value offset phase A/B/C/N

Name:
IoffsetA_W
IoffsetB_W
IoffsetC_W
IoffsetN_W

Corresponds to the negated value of the corresponding RMS value register when I = 0.

Data type	Value	Information
INT	-32767 to 32767	RMS value current offset, phase-based. Bus controller default setting: 0

1.22.5.20 User calibration of power values

Use the following procedure to properly calculate the power angle correction:

1) Calculate the values
2) Write the value 0xFFFF to register "Cs1Update" on page 557
3) Read register "Cs1UpdateFB" on page 557 until 0xFFFF is returned
4) Write the calculated values to the registers "PhiA_W, PhiB_W, PhiC_W" on page 565
5) Write the value 0x0001 to register Cs1Update
6) Read register Cs1UpdateFB until 0x0001 is returned

Information:

These registers are NOT nonvolatile, and the procedure must be repeated at each startup or on each positive edge of bit ModulOK.

1.22.5.20.1 A/D converter power angle correction phase A/B/C

Name:
PhiA_R
PhiB_R
PhiC_R

These registers can be used to read out the configured values at runtime, but are not nonvolatile and have the value 0 after the system is started.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 9	Delay time for energy phase angle correction	x	The clock base is 2.048 MHz. Maximum 0.499 ms
10 - 14	Reserved	0	
15	Delay times	0	Effect on current channel
		1	Effect on voltage channel

1.22.5.20.2 A/D converter power calibration checksum 1

Name:
PhiA_W
PhiB_W
PhiC_W

These registers can be used to correct phase shifts at runtime. This can be necessary if the transformers used distort the phase shift.

Changes in these registers are only applied after an update request in register "Cs1Update" on page 557.

Data type	Values	Bus controller default setting
UINT	See the bit structure.	0

Bit structure:

Bit	Name	Value	Information
0 - 9	Delay time for energy phase angle correction	0 to 1023	See description for bits 0 to 9. Bus controller default setting: 0
10 - 14	Reserved	0	
15	Delay times	0 or 1	See description for Bit 15

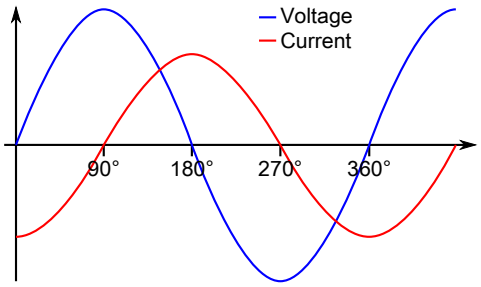
Description - Bits 0 to 9

The maximum correction 0x3FF = 1023 dec. corresponds to 0.49951 ms.

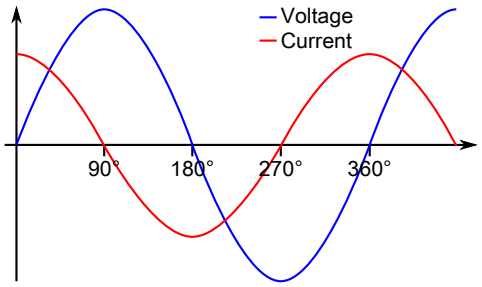
At 50 Hz mains this corresponds to a change of 8.99 degrees

At 60 Hz mains this corresponds to a change of 10.79 degrees

Schematic representation of inductive load: Voltage ahead of current



Schematic representation of capacitive load: Current ahead of voltage



Description - Bit 15

0	Delay affects current channel	
	Effect with inductive load	Reduced angle between I and U, and therefore an increased power factor
	Effect with capacitive load	Increased angle between U and I, and therefore an reduced power factor
1	Delay affects voltage channel	
	Effect with inductive load	Reduced angle between U and I, and therefore an increased power factor
	Effect with capacitive load	Increased angle between I and U, and therefore an reduced power factor

1.22.5.21 Force analog energy registers

The registers are described under "Analog energy registers" on page 545. A corresponding comparison attached:

Force registers	Read registers
Frc_APenergyT Frc_APenergyTF Frc_APenergyTH	"APenergyT"
Frc_APenergyA Frc_APenergyAF Frc_APenergyAH	"APenergyA"
Frc_APenergyB Frc_APenergyBF Frc_APenergyBH	"APenergyB"
Frc_APenergyC Frc_APenergyCF Frc_APenergyCH	"APenergyC"
Frc_ANenergyT Frc_ANenergyTF Frc_ANenergyTH	"ANenergyT"
Frc_ANenergyA Frc_ANenergyAF Frc_ANenergyAH	"ANenergyA"
Frc_ANenergyB Frc_ANenergyBF Frc_ANenergyBH	"ANenergyB"
Frc_ANenergyC Frc_ANenergyCF Frc_ANenergyCH	"ANenergyC"
Frc_RPenergyT	"RPenergyT"
Frc_RPenergyA	"RPenergyA"
Frc_RPenergyB	"RPenergyB"
Frc_RPenergyC	"RPenergyC"
Frc_RNenergyT	"RNenergyT"
Frc_RNenergyA	"RNenergyA"
Frc_RNenergyB	"RNenergyB"
Frc_RNenergyC	"RNenergyC"
Frc_SAenergyT	"SAenergyT"
Frc_SenergyA	"SenergyA"
Frc_SenergyB	"SenergyB"
Frc_SenergyC	"SenergyC"
Frc_SVenergyT	"SVenergyT"

These registers can be used to set the energy counter to a specific value after a module has been replaced.

Data type	Value	Information
UDINT	0 to 4294967295	Bus controller default setting: 0

1.22.5.21.1 Force forward total active energy

Name:
Frc_APenergyT

The registers are described under "Analog energy registers" on page 545.

These registers can be used to set the energy counter to a specific value after a module has been replaced. The register is updated to the current values when triggered by register "ControlOutput" on page 535, bit 3.

Data type	Value
UDINT	0 to 4294967295

1.22.5.22 Oversampling buffer

1.22.5.22.1 General information

A sample line contains the instantaneous values of currents (4 channels) and voltages (3 channels) as well as a sequential number and the NetTime at the time of transfer from the converter. These values are measured in a grid of 125 µs * Prescaler.

The user must then normalize the values to the respective physical values:

Voltage: Vrms = (INT32)Vs * 4 / Sqrt(2)
Current: Irms = (INT32)Is * 4 / Sqrt(2)

1.22.5.22.2 Sample - Neutral current

Name:
IactN_Sample1 to IactN_Sample16

Current value of the neutral current
The value of these registers must be converted by the application: See "General information" on page 567.

Data type	Value	Information
INT	-32767 to 32767	Resolution 0.001 A

1.22.5.22.3 Sample - Current on phase A

Name:
IactA_Sample1 to IactA_Sample16

Present current value on phase A.
The value of these registers must be converted by the application: See "General information" on page 567.

Data type	Value	Information
INT	-32767 to 32767	Resolution 0.001 A

1.22.5.22.4 Sample - Voltage on phase A

Name:
UactA_Sample1 to UactA_Sample16

Present voltage value on phase A.
The value of these registers must be converted by the application: See "General information" on page 567.

Data type	Value	Information
INT	-32767 to 32767	Resolution 0.01 V

1.22.5.22.5 Sample - Current on phase B

Name:
IactB_Sample1 to IactB_Sample16

Present current value on phase B.
The value of these registers must be converted by the application: See "General information" on page 567.

Data type	Value	Information
INT	-32767 to 32767	Resolution 0.001 A

1.22.5.22.6 Sample - Voltage of phase B

Name:
UactB_Sample1 to UactB_Sample16

Current value of the voltage of phase B.
The value of these registers must be converted by the application: See "General information" on page 567.

Data type	Values	Information
INT	-32767 to 32767	Resolution 0.01 V

1.22.5.22.7 Sample - Current on phase C

Name:
IactC_Sample1 to IactC_Sample16

Present current value on phase C.
The value of these registers must be converted by the application: See "General information" on page 567.

Data type	Value	Information
INT	-32767 to 32767	Resolution 0.001 A

1.22.5.22.8 Sample - Voltage on phase C

Name:
UactC_Sample1 to UactC_Sample16

Present voltage value on phase C.
The value of these registers must be converted by the application: See "General information" on page 567.

Data type	Value	Information
INT	-32767 to 32767	Resolution 0.01 V

1.22.5.22.9 Sample number

Name:
SampleCount1 to Samplecount16

Sample line number, ascending, cyclic.
Number of new sample lines since last readout.

Data type	Value
SINT	-127 to 127
INT	-32767 to 32767

1.22.5.22.10 Sample time

Name:
Timestamp

NetTime timestamp of sample line 1.
The older sample lines must be recalculated with 125 µs each.

For additional information about NetTime and timestamps, see "NetTime Technology" on page 598.

Data type	Value
INT	-32767 to 32767
DINT	-2,147,483,647 to 2,147,483,647

1.22.5.23 Environment variables

1.22.5.23.1 Operating time in seconds

Name:
OnTime

The operating time since startup is saved in seconds in this register.

Data type	Value
UDINT	0 to 4294967295

1.22.5.23.2 Startup counter

Name:
UpCounter

The number of restarts since startup is saved in this register.

Data type	Value
UDINT	0 to 4294967295

1.22.5.23.3 Minimum operating temperature

Name:
MinTemp

The lowest transformer temperature [°C] since startup is saved in this register.

Data type	Value	Information
INT	-200 to 200	Resolution 1°C

1.22.5.23.4 Maximum operating temperature

Name:
MaxTemp

The highest transformer temperature [°C] since startup is saved in this register.

Data type	Value	Information
INT	-200 to 200	Resolution 1°C

1.22.5.24 Flatstream registers

At the absolute minimum, registers "InputMTU" and "OutputMTU" must be set. All other registers are filled in with default values at the beginning and can be used immediately. These registers are used for additional options, e.g. to transfer data in a more compact way or to increase the efficiency of the general procedure.

Information:

For detailed information about Flatstream, see "Flatstream communication" on page 572.

1.22.5.24.1 Number of enabled Tx and Rx bytes

Name:
OutputMTU
InputMTU

These registers define the number of enabled Tx or Rx bytes and thus also the maximum size of a sequence. The user must consider that the more bytes made available also means a higher load on the bus system.

Data type	Values
USINT	See the register overview.

1.22.5.24.2 Transporting payload data and control bytes

Name:
TxByte1 to TxByteN
RxByte1 to RxByteN

(The value the number N is different depending on the bus controller model used.)

The Tx and Rx bytes are cyclic registers used to transport the payload data and the necessary control bytes. The number of active Tx and Rx bytes is taken from the configuration of registers "OutputMTU" and "InputMTU", respectively.

- "T" - "Transmit" → Controller *transmits* data to the module.
- "R" - "Receive" → Controller *receives* data from the module.

Data type	Values
USINT	0 to 255

1.22.5.24.3 Communication status of the controller

Name:
OutputSequence

This register contains information about the communication status of the controller. It is written by the controller and read by the module.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	OutputSequenceCounter	0 - 7	Counter for the sequences issued in the output direction
3	OutputSyncBit	0	Output direction (disable)
		1	Output direction (enable)
4 - 6	InputSequenceAck	0 - 7	Mirrors InputSequenceCounter
7	InputSyncAck	0	Input direction not ready (disabled)
		1	Input direction ready (enabled)

OutputSequenceCounter

The OutputSequenceCounter is a continuous counter of sequences that have been issued by the controller. The controller uses OutputSequenceCounter to direct the module to accept a sequence (the output direction must be synchronized when this happens).

OutputSyncBit

The controller uses OutputSyncBit to attempt to synchronize the output channel.

InputSequenceAck

InputSequenceAck is used for acknowledgment. The value of InputSequenceCounter is mirrored if the controller has received a sequence successfully.

InputSyncAck

The InputSyncAck bit acknowledges the synchronization of the input channel for the module. This indicates that the controller is ready to receive data.

1.22.5.24.4 Communication status of the module

Name:
InputSequence

This register contains information about the communication status of the module. It is written by the module and should only be read by the controller.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	InputSequenceCounter	0 - 7	Counter for sequences issued in the input direction
3	InputSyncBit	0	Not ready (disabled)
		1	Ready (enabled)
4 - 6	OutputSequenceAck	0 - 7	Mirrors OutputSequenceCounter
7	OutputSyncAck	0	Not ready (disabled)
		1	Ready (enabled)

InputSequenceCounter

The InputSequenceCounter is a continuous counter of sequences that have been issued by the module. The module uses InputSequenceCounter to direct the controller to accept a sequence (the input direction must be synchronized when this happens).

InputSyncBit

The module uses InputSyncBit to attempt to synchronize the input channel.

OutputSequenceAck

OutputSequenceAck is used for acknowledgment. The value of OutputSequenceCounter is mirrored if the module has received a sequence successfully.

OutputSyncAck

The OutputSyncAck bit acknowledges the synchronization of the output channel for the controller. This indicates that the module is ready to receive data.

1.22.5.24.5 Flatstream mode

Name:
FlatstreamMode

A more compact arrangement can be achieved with the incoming data stream using this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	MultiSegmentMTU	0	Not allowed (default)
		1	Permitted
1	Large segments	0	Not allowed (default)
		1	Permitted
2 - 7	Reserved		

1.22.5.24.6 Number of unacknowledged sequences

Name:
Forward

With register "Forward", the user specifies how many unacknowledged sequences the module is permitted to transmit.

Recommendation:
X2X Link: Max. 5
POWERLINK: Max. 7

Data type	Values
USINT	1 to 7 Default: 1

1.22.5.24.7 Delay time

Name:
ForwardDelay

This register is used to specify the delay time in microseconds.

Data type	Values
UINT	0 to 65535 [µs] Default: 0

1.22.5.25 Flatstream communication with function blocks

As an additional option for Flatstream communication, communication with the module can be easily carried out with the "AsFltGen" library.

The library function blocks handle all incoming tasks with Flatstream mode, such as forwarding, sequencing, generation and evaluation of control bytes.

1.22.5.26 Flatstream communication

1.22.5.26.1 Introduction

B&R offers an additional communication method for some modules. "Flatstream" was designed for X2X and POWERLINK networks and allows data transfer to be adapted to individual demands. Although this method is not 100% real-time capable, it still allows data transfer to be handled more efficiently than with standard cyclic polling.

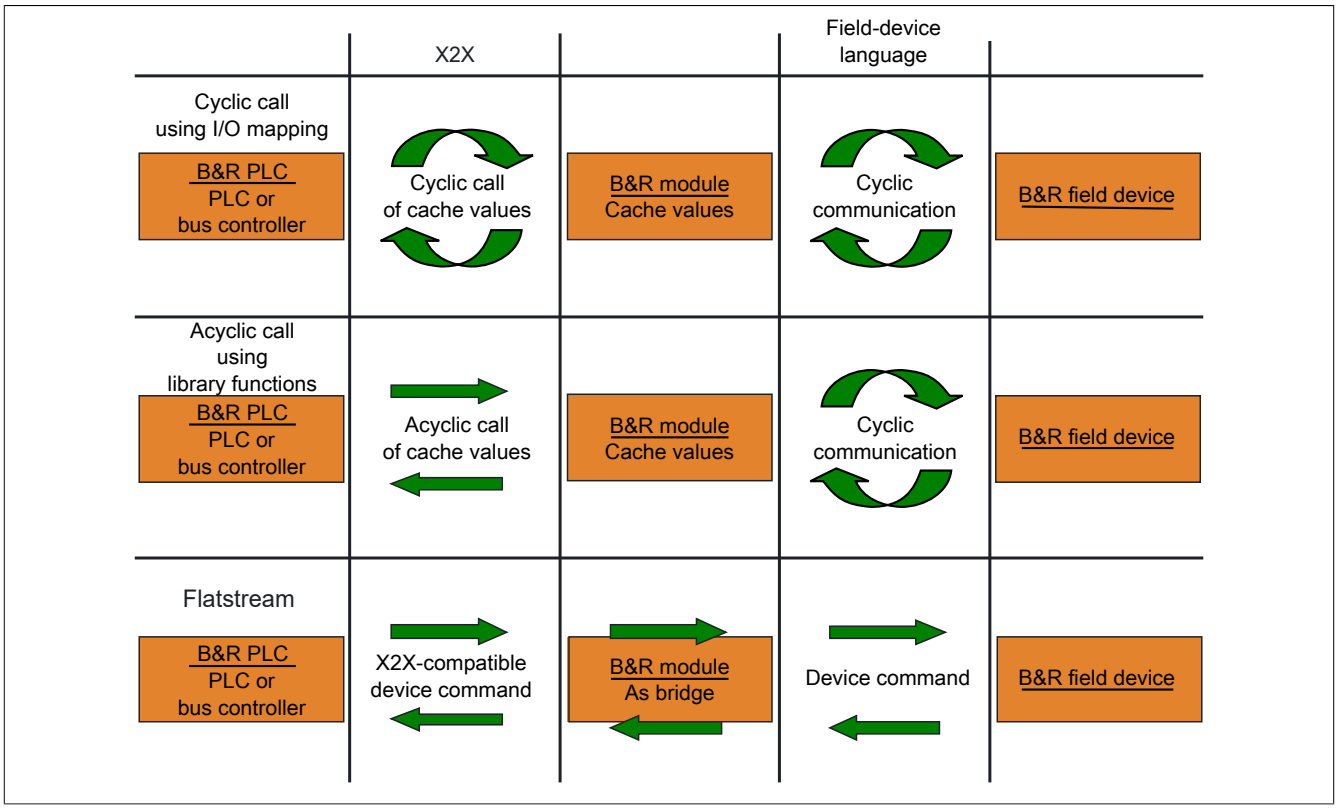


Figure 58: 3 types of communication

Flatstream extends cyclic and acyclic data queries. With Flatstream communication, the module acts as a bridge. The module is used to pass controller requests directly on to the field device.

1.22.5.26.2 Message, segment, sequence, MTU

The physical properties of the bus system limit the amount of data that can be transmitted during one bus cycle. With Flatstream communication, all messages are viewed as part of a continuous data stream. Long data streams must be broken down into several fragments that are sent one after the other. To understand how the receiver puts these fragments back together to get the original information, it is important to understand the difference between a message, a segment, a sequence and an MTU.

Message

A message refers to information exchanged between 2 communicating partner stations. The length of a message is not restricted by the Flatstream communication method. Nevertheless, module-specific limitations must be considered.

Segment (logical division of a message):

A segment has a finite size and can be understood as a section of a message. The number of segments per message is arbitrary. So that the recipient can correctly reassemble the transferred segments, each segment is preceded by a byte with additional information. This control byte contains information such as the length of a segment and whether the approaching segment completes the message. This makes it possible for the receiving station to interpret the incoming data stream correctly.

Sequence (how a segment must be arranged physically):

The maximum size of a sequence corresponds to the number of enabled Rx or Tx bytes (later: "MTU"). The transmitting station splits the transmit array into valid sequences. These sequences are then written successively to the MTU and transferred to the receiving station where they are lined up together again. The receiver stores the incoming sequences in a receive array, obtaining an image of the data stream in the process.
With Flatstream communication, the number of sequences sent are counted. Successfully transferred sequences must be acknowledged by the receiving station to ensure the integrity of the transfer.

MTU (Maximum Transmission Unit) - Physical transport:

MTU refers to the enabled USINT registers used with Flatstream. These registers can accept at least one sequence and transfer it to the receiving station. A separate MTU is defined for each direction of communication. OutputMTU defines the number of Flatstream Tx bytes, and InputMTU specifies the number of Flatstream Rx bytes. The MTUs are transported cyclically via the X2X Link network, increasing the load with each additional enabled USINT register.

Properties

Flatstream messages are not transferred cyclically or in 100% real time. Many bus cycles may be needed to transfer a particular message. Although the Rx and Tx registers are exchanged between the transmitter and the receiver cyclically, they are only processed further if explicitly accepted by register "InputSequence" or "OutputSequence".

Behavior in the event of an error (brief summary)

The protocol for X2X and POWERLINK networks specifies that the last valid values should be retained when disturbances occur. With conventional communication (cyclic/acyclic data queries), this type of error can generally be ignored.
In order for communication to also take place without errors using Flatstream, all of the sequences issued by the receiver must be acknowledged. If Forward functionality is not used, then subsequent communication is delayed for the length of the disturbance.
If Forward functionality is being used, the receiving station receives a transmission counter that is incremented twice. The receiver stops, i.e. it no longer returns any acknowledgments. The transmitting station uses SequenceAck to determine that the transfer was faulty and that all affected sequences must be repeated.

1.22.5.26.3 The Flatstream principle

Requirement

Before Flatstream can be used, the respective communication direction must be synchronized, i.e. both communication partners cyclically query the sequence counter on the remote station. This checks to see if there is new data that should be accepted.

Communication

If a communication partner wants to transmit a message to its remote station, it should first create a transmit array that corresponds to Flatstream conventions. This allows the Flatstream data to be organized very efficiently without having to block other important resources.

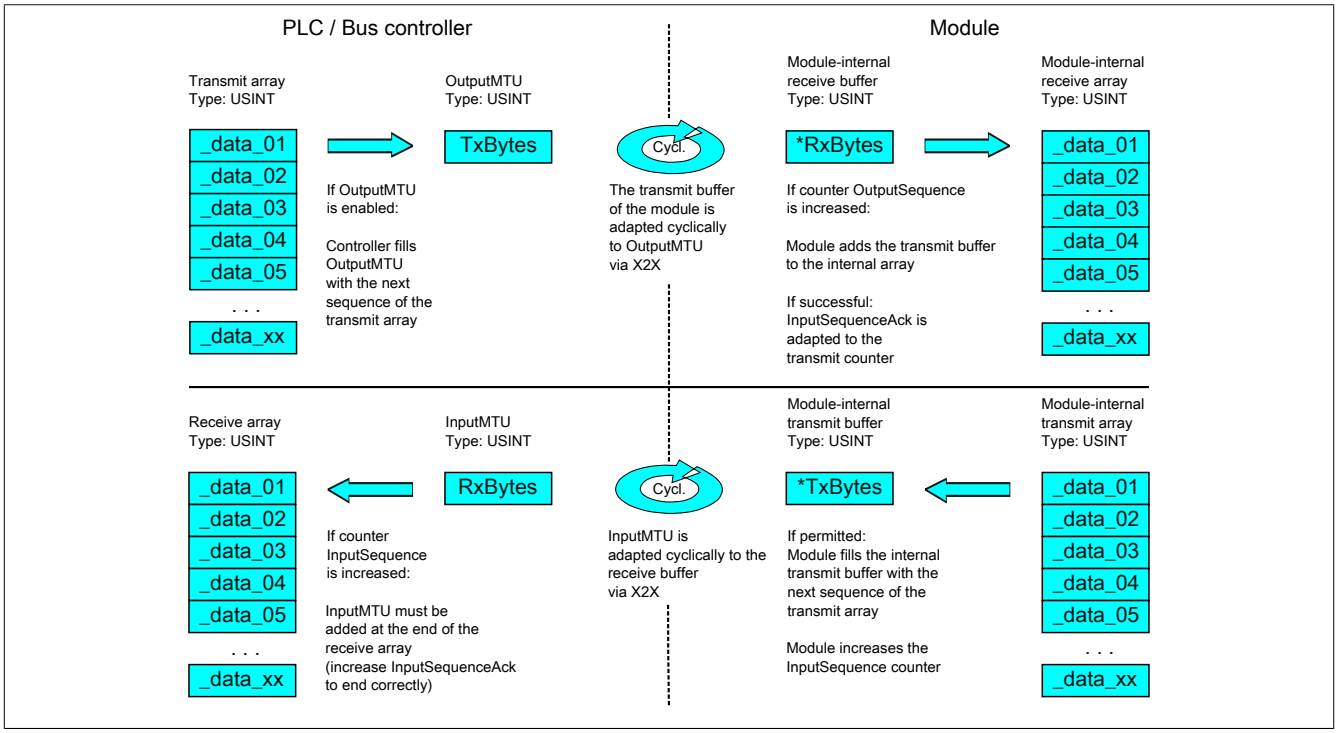


Figure 59: Flatstream communication

Procedure

The first thing that happens is that the message is broken into valid segments of up to 63 bytes, and the corresponding control bytes are created. The data is formed into a data stream made up of one control bytes per associated segment. This data stream can be written to the transmit array. The maximum size of each array element matches that of the enabled MTU so that one element corresponds to one sequence.
If the array has been completely created, the transmitter checks whether the MTU is permitted to be refilled. It then copies the first element of the array or the first sequence to the Tx byte registers. The MTU is transported to the receiver station via X2X Link and stored in the corresponding Rx byte registers. To signal that the data should be accepted by the receiver, the transmitter increases its SequenceCounter.
If the communication direction is synchronized, the remote station detects the incremented SequenceCounter. The current sequence is appended to the receive array and acknowledged by SequenceAck. This acknowledgment signals to the transmitter that the MTU can now be refilled.

If the transfer is successful, the data in the receive array will correspond 100% to the data in the transmit array. During the transfer, the receiving station must detect and evaluate the incoming control bytes. A separate receive array should be created for each message. This allows the receiver to immediately begin further processing of messages that are completely transferred.

1.22.5.26.4 Registers for Flatstream mode

5 registers are available for configuring Flatstream. The default configuration can be used to transmit small amounts of data relatively easily.

Information:

The controller communicates directly with the field device via registers "OutputSequence" and "InputSequence" as well as the enabled Tx and RxBytes bytes. For this reason, the user must have sufficient knowledge of the communication protocol being used on the field device.

1.22.5.26.4.1 Flatstream configuration

To use Flatstream, the program sequence must first be expanded. The cycle time of the Flatstream routines must be set to a multiple of the bus cycle. Other program routines should be implemented in Cyclic #1 to ensure data consistency.

At the absolute minimum, registers "InputMTU" and "OutputMTU" must be set. All other registers are filled in with default values at the beginning and can be used immediately. These registers are used for additional options, e.g. to transfer data in a more compact way or to increase the efficiency of the general procedure.

The Forward registers extend the functionality of the Flatstream protocol. This functionality is useful for substantially increasing the Flatstream data rate, but it also requires quite a bit of extra work when creating the program sequence.

Information:

In the rest of this description, the names "OutputMTU" and "InputMTU" do not refer to the registers names. Instead, they are used as synonyms for the currently enabled Tx or Rx bytes.

Information:

Registers are described in section "Flatstream registers" on page 569.

1.22.5.26.4.2 Flatstream operation

When using Flatstream, the communication direction is very important. For transmitting data to a module (output direction), Tx bytes are used. For receiving data from a module (input direction), Rx bytes are used.
Registers "OutputSequence" and "InputSequence" are used to control or secure communication, i.e. the transmitter uses them to give instructions to apply data and the receiver confirms a successfully transferred sequence.

Information:

Registers are described in section "Flatstream registers" on page 569.

Format of input and output bytes

Name:

"Format of Flatstream" in Automation Studio

On some modules, this function can be used to set how the Flatstream input and output bytes (Tx or Rx bytes) are transferred.

- **Packed:** Data is transferred as an array.
- **Byte-by-byte:** Data is transferred as individual bytes.

Transport of payload data and control bytes

The Tx and Rx bytes are cyclic registers used to transport the payload data and the necessary control bytes. The number of active Tx and Rx bytes is taken from the configuration of registers "OutputMTU" and "InputMTU", respectively.
In the user program, only the Tx and Rx bytes from the controller can be used. The corresponding counterparts are located in the module and are not accessible to the user. For this reason, the names were chosen from the point of view of the controller.

- "T" - "Transmit" → Controller *transmits* data to the module.
- "R" - "Receive" → Controller *receives* data from the module.

Control bytes

In addition to the payload data, the Tx and Rx bytes also transfer the necessary control bytes. These control bytes contain additional information about the data stream so that the receiver can reconstruct the original message from the transferred segments.

Bit structure of a control byte

Bit	Name	Value	Information
0 - 5	SegmentLength	0 - 63	Size of the subsequent segment in bytes (default: Max. MTU size - 1)
6	nextCBPos	0	Next control byte at the beginning of the next MTU
		1	Next control byte directly after the end of the current segment
7	MessageEndBit	0	Message continues after the subsequent segment
		1	Message ended by the subsequent segment

SegmentLength

The segment length lets the receiver know the length of the coming segment. If the set segment length is insufficient for a message, then the information must be distributed over several segments. In these cases, the actual end of the message is detected using bit 7 (control byte).

Information:

The control byte is not included in the calculation to determine the segment length. The segment length is only derived from the bytes of payload data.

nextCBPos

This bit indicates the position where the next control byte is expected. This information is especially important when using option "MultiSegmentMTU".
When using Flatstream communication with MultiSegmentMTUs, the next control byte is no longer expected in the first Rx byte of the subsequent MTU, but transferred directly after the current segment.

MessageEndBit

"MessageEndBit" is set if the subsequent segment completes a message. The message has then been completely transferred and is ready for further processing.

Information:

In the output direction, this bit must also be set if one individual segment is enough to hold the entire message. The module will only process a message internally if this identifier is detected.
The size of the message being transferred can be calculated by adding all of the message's segment lengths together.

Flatstream formula for calculating message length:

Message [bytes] = Segment lengths (all CBs without ME) + Segment length (of the first CB with ME)	CB	Control byte
	ME	MessageEndBit

Communication status

The communication status is determined via registers "OutputSequence" and "InputSequence".

- OutputSequence contains information about the communication status of the controller. It is written by the controller and read by the module.
- InputSequence contains information about the communication status of the module. It is written by the module and should only be read by the controller.

Relationship between OutputSequence and InputSequence

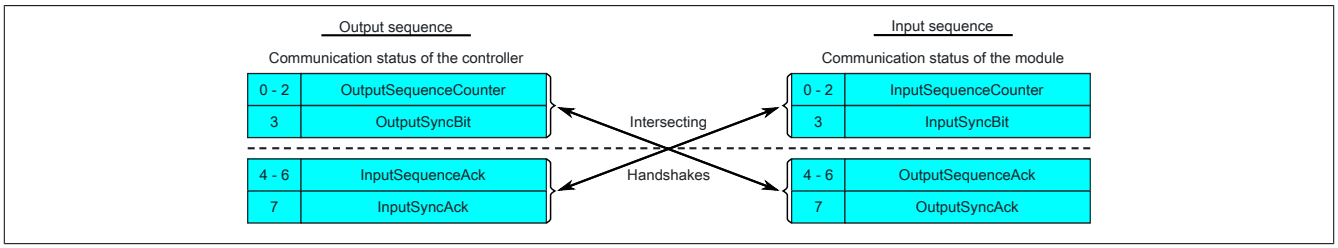


Figure 60: Relationship between OutputSequence and InputSequence

Registers "OutputSequence" and "InputSequence" are logically composed of 2 half-bytes. The low part indicates to the remote station whether a channel should be opened or whether data should be accepted. The high part is to acknowledge that the requested action was carried out.

SyncBit and SyncAck

If SyncBit and SyncAck are set in one communication direction, then the channel is considered "synchronized", i.e. it is possible to send messages in this direction. The status bit of the remote station must be checked cyclically. If SyncAck has been reset, then SyncBit on that station must be adjusted. Before new data can be transferred, the channel must be resynchronized.

SequenceCounter and SequenceAck

The communication partners cyclically check whether the low nibble on the remote station changes. When one of the communication partners finishes writing a new sequence to the MTU, it increments its SequenceCounter. The current sequence is then transmitted to the receiver, which acknowledges its receipt with SequenceAck. In this way, a "handshake" is initiated.

Information:

If communication is interrupted, segments from the unfinished message are discarded. All messages that were transferred completely are processed.

1.22.5.26.4.3 Synchronization

During synchronization, a communication channel is opened. It is important to make sure that a module is present and that the current value of SequenceCounter is stored on the station receiving the message.
Flatstream can handle full-duplex communication. This means that both channels / communication directions can be handled separately. They must be synchronized independently so that simplex communication can theoretically be carried out as well.

Synchronization in the output direction (controller as the transmitter):

The corresponding synchronization bits (OutputSyncBit and OutputSyncAck) are reset. Because of this, Flatstream cannot be used at this point in time to transfer messages from the controller to the module.

Algorithm

1) The controller must write 000 to OutputSequenceCounter and reset OutputSyncBit. The controller must cyclically query the high nibble of register "InputSequence" (checks for 000 in OutputSequenceAck and 0 in OutputSyncAck).
The module does not accept the current contents of InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
2) If the controller registers the expected values in OutputSequenceAck and OutputSyncAck, it is permitted to increment OutputSequenceCounter. The controller continues cyclically querying the high nibble of register "OutputSequence" (checks for 001 in OutputSequenceAck and 0 in InputSyncAck).
The module does not accept the current contents of InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
3) If the controller registers the expected values in OutputSequenceAck and OutputSyncAck, it is permitted to increment OutputSequenceCounter. The controller continues cyclically querying the high nibble of register "OutputSequence" (checks for 001 in OutputSequenceAck and 1 in InputSyncAck). **Note:** Theoretically, data can be transferred from this point forward. However, it is still recommended to wait until the output direction is completely synchronized before transferring data.
The module sets OutputSyncAck.
The output direction is synchronized, and the controller can transmit data to the module.

Synchronization in the input direction (controller as the receiver):

The corresponding synchronization bits (InputSyncBit and InputSyncAck) are reset. Because of this, Flatstream cannot be used at this point in time to transfer messages from the module to the controller.

Algorithm

The module writes 000 to InputSequenceCounter and resets InputSyncBit. *The module monitors the high nibble of register "OutputSequence" and expects 000 in InputSequenceAck and 0 in InputSyncAck.*
1) The controller is not permitted to accept the current contents of InputMTU since the channel is not yet synchronized. The controller must match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it increments InputSequenceCounter. *The module monitors the high nibble of register "OutputSequence" and expects 001 in InputSequenceAck and 0 in InputSyncAck.*
2) The controller is not permitted to accept the current contents of InputMTU since the channel is not yet synchronized. The controller must match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it sets InputSyncBit. *The module monitors the high nibble of register "OutputSequence" and expects 1 in InputSyncAck.*
3) The controller is permitted to set InputSyncAck. **Note:** Theoretically, data could already be transferred in this cycle. If InputSyncBit is set and InputSequenceCounter has been increased by 1, the values in the enabled Rx bytes must be accepted and acknowledged (see also "Communication in the input direction").
The input direction is synchronized, and the module can transmit data to the controller.

1.22.5.26.4.4 Transmitting and receiving

If a channel is synchronized, then the remote station is ready to receive messages from the transmitter. Before the transmitter can send data, it must first create a transmit array in order to meet Flatstream requirements.

The transmitting station must also generate a control byte for each segment created. This control byte contains information about how the subsequent part of the data being transferred should be processed. The position of the next control byte in the data stream can vary. For this reason, it must be clearly defined at all times when a new control byte is being transmitted. The first control byte is always in the first byte of the first sequence. All subsequent positions are determined recursively.

Flatstream formula for calculating the position of the next control byte:

Position (of the next control byte) = Current position + 1 + Segment length

Example

3 autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The rest of the configuration corresponds to the default settings.

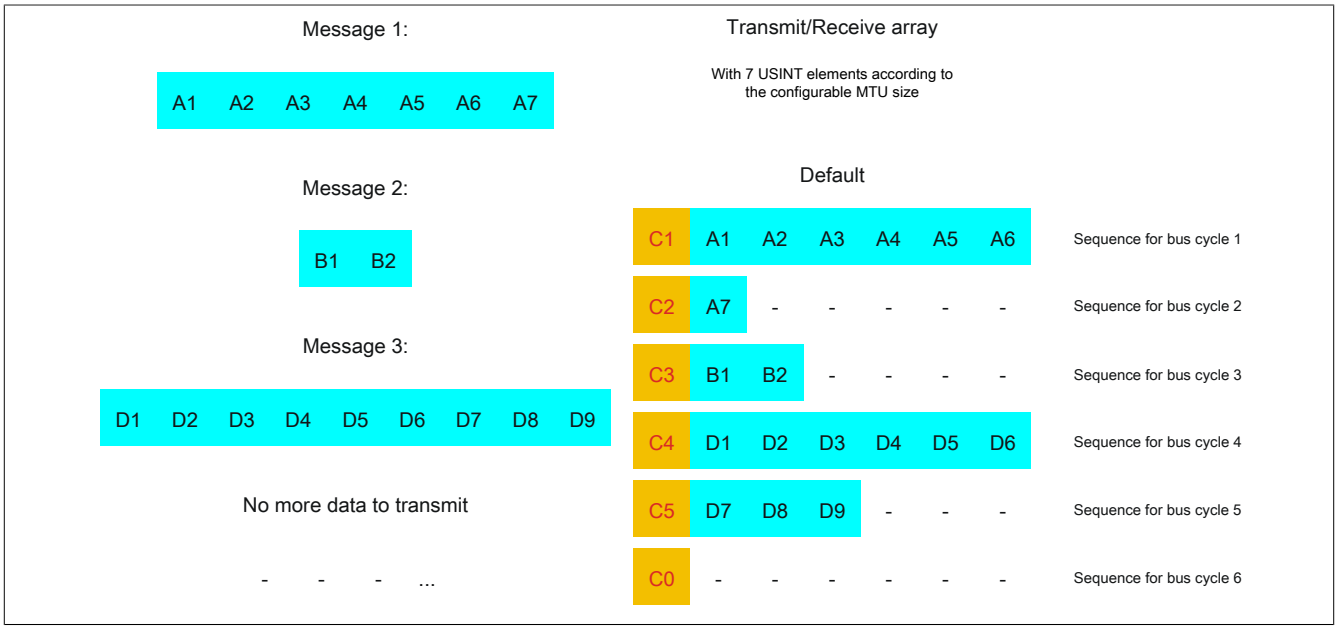


Figure 61: Transmit/Receive array (default)

The messages must first be split into segments. In the default configuration, it is important to ensure that each sequence can hold an entire segment, including the associated control byte. The sequence is limited to the size of the enable MTU. In other words, a segment must be at least 1 byte smaller than the MTU.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 1 data byte
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 3 data bytes
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C0 (control byte 0)			**C1 (control byte 1)**			**C2 (control byte 2)**		
- SegmentLength (0)	=	0	- SegmentLength (6)	=	6	- SegmentLength (1)	=	1
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (0)	=	0	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	0	Control byte	Σ	6	Control byte	Σ	129

Table 75: Flatstream determination of the control bytes for the default configuration example (part 1)

C3 (control byte 3)			**C4 (control byte 4)**			**C5 (control byte 5)**		
- SegmentLength (2)	=	2	- SegmentLength (6)	=	6	- SegmentLength (3)	=	3
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	130	Control byte	Σ	6	Control byte	Σ	131

Table 76: Flatstream determination of the control bytes for the default configuration example (part 2)

Transmitting data to a module (output)

When transmitting data, the transmit array must be generated in the application program. Sequences are then transferred one by one using Flatstream and received by the module.

Information:

Although all B&R modules with Flatstream communication always support the most compact transfers in the output direction, it is recommended to use the same design for the transfer arrays in both communication directions.

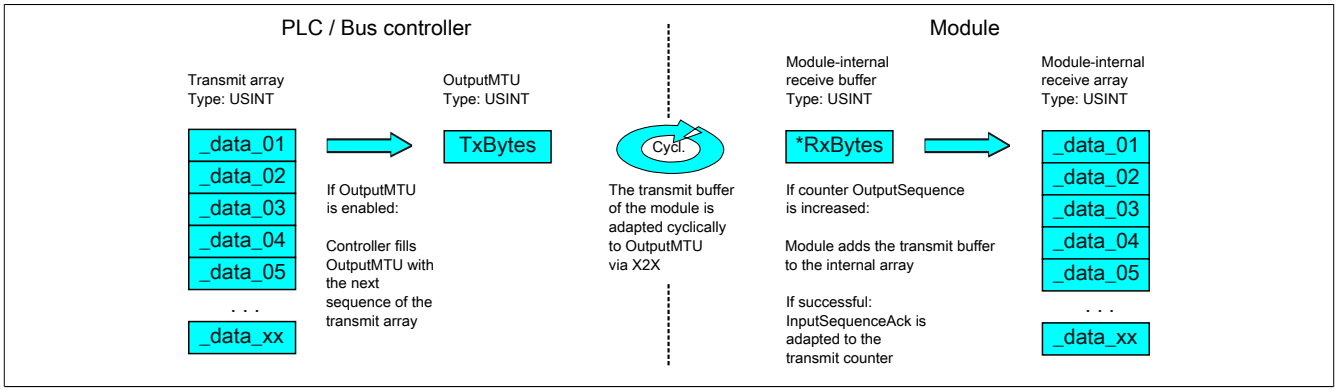


Figure 62: Flatstream communication (output)

Message smaller than OutputMTU

The length of the message is initially smaller than OutputMTU. In this case, one sequence would be sufficient to transfer the entire message and the necessary control byte.

Algorithm

Cyclic status query: *- The module monitors OutputSequenceCounter.*
0) Cyclic checks: - The controller must check OutputSyncAck. → If OutputSyncAck = 0: Reset OutputSyncBit and resynchronize the channel. - The controller must check whether OutputMTU is enabled. → If OutputSequenceCounter > InputSequenceAck: MTU is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The controller must split up the message into valid segments and create the necessary control bytes. - The controller must add the segments and control bytes to the transmit array.
2) Transmit: - The controller transfers the current element of the transmit array to OutputMTU. → OutputMTU is transferred cyclically to the module's transmit buffer but not processed further. - The controller must increase OutputSequenceCounter.
Reaction: *- The module accepts the bytes from the internal receive buffer and adds them to the internal receive array.* *- The module transmits acknowledgment and writes the value of OutputSequenceCounter to OutputSequenceAck.*
3) Completion: - The controller must monitor OutputSequenceAck. → A sequence is only considered to have been transferred successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transfer errors in the last sequence as well, it is important to make sure that the length of the *Completion* phase is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transfer can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost. (The relationship of bus to task cycle can be influenced by the user so that the threshold value must be determined individually.) - Subsequent sequences are only permitted to be transmitted in the next bus cycle after the completion check has been carried out successfully.

Message larger than OutputMTU

The transmit array, which must be created in the program sequence, consists of several elements. The user must arrange the control and data bytes correctly and transfer the array elements one after the other. The transfer algorithm remains the same and is repeated starting at the point *Cyclic checks*.

General flowchart

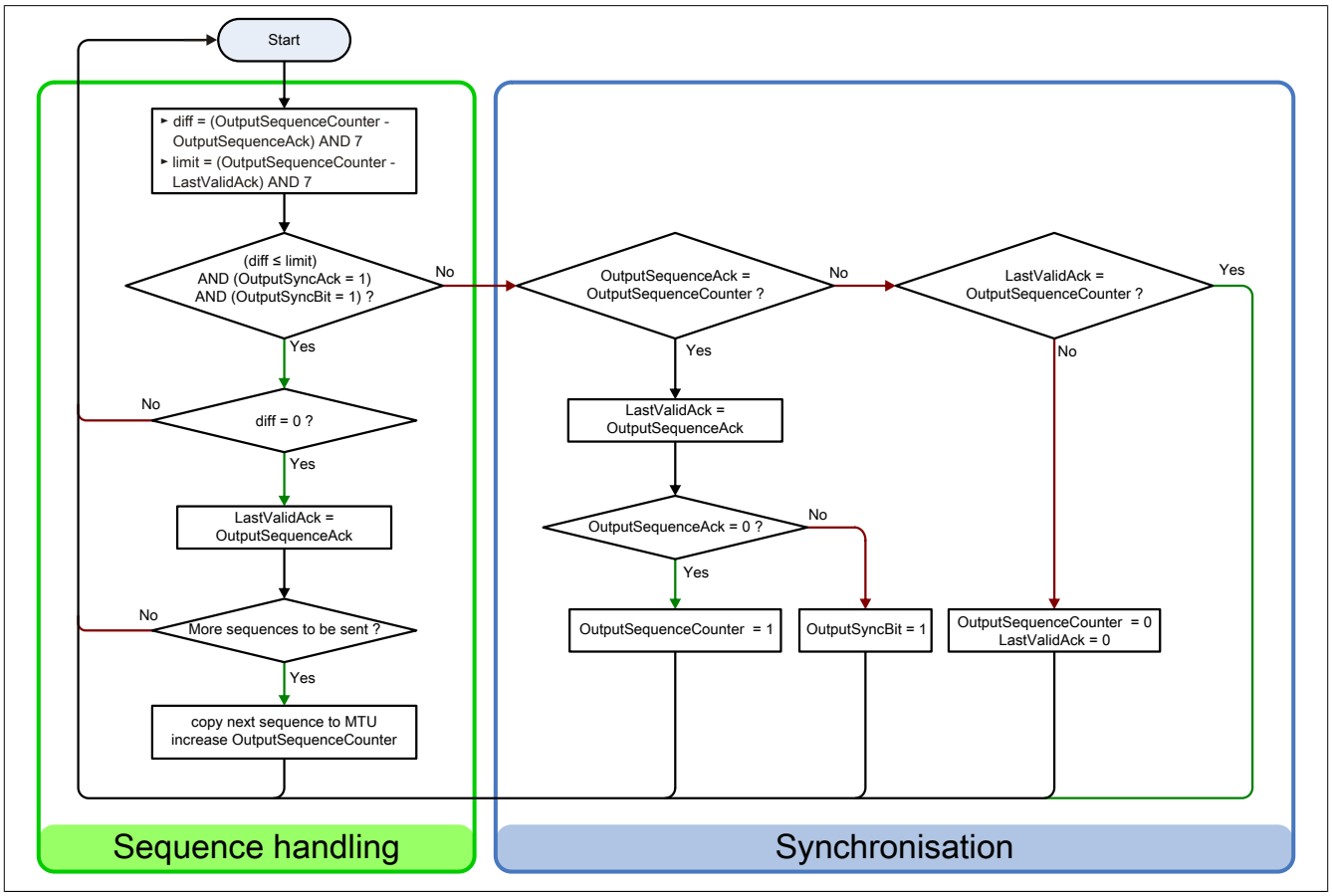


Figure 63: Flowchart for the output direction

Receiving data from a module (input)

When receiving data, the transmit array is generated by the module, transferred via Flatstream and must then be reproduced in the receive array. The structure of the incoming data stream can be set with the mode register. The algorithm for receiving the data remains unchanged in this regard.

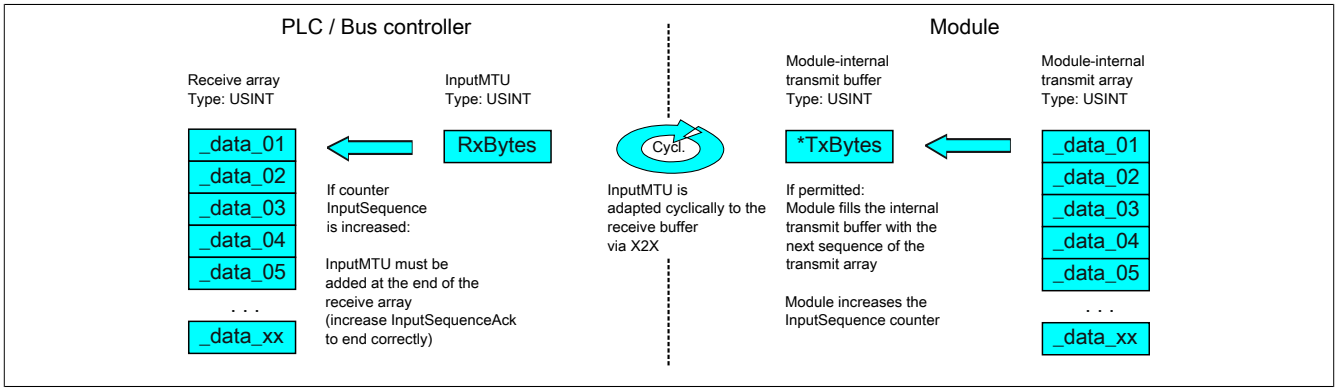


Figure 64: Flatstream communication (input)

Algorithm

0) Cyclic status query: - The controller must monitor InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck.* *- The module checks InputSequenceAck.*
Preparation: *- The module forms the segments and control bytes and creates the transmit array.*
Action: *- The module transfers the current element of the internal transmit array to the internal transmit buffer.* *- The module increases InputSequenceCounter.*
1) Receiving (as soon as InputSequenceCounter is increased): - The controller must apply data from InputMTU and append it to the end of the receive array. - The controller must match InputSequenceAck to InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck.* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.* *- Subsequent sequences are only transmitted in the next bus cycle after the completion check has been carried out successfully.*

General flowchart

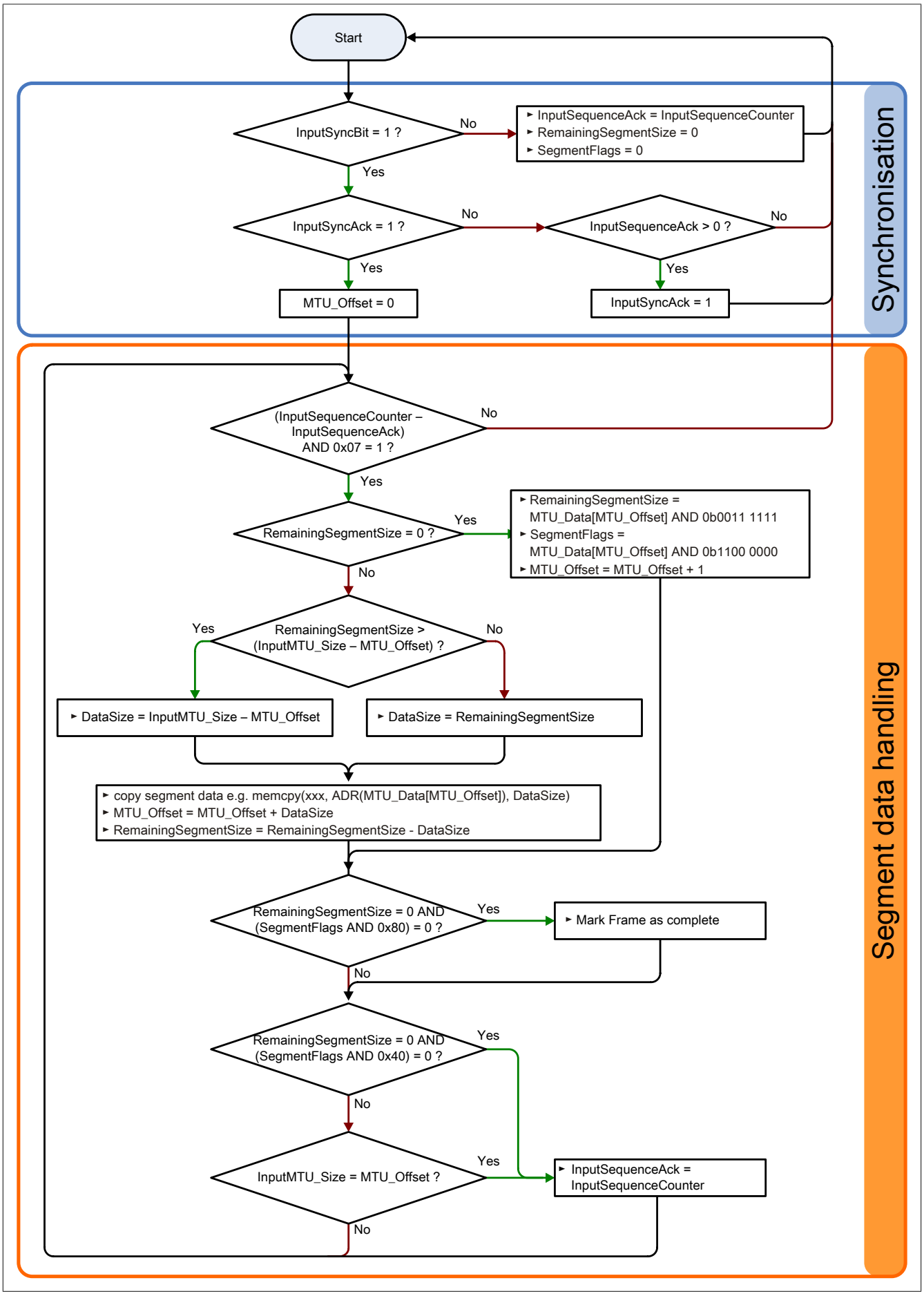


Figure 65: Flowchart for the input direction

Details

It is recommended to store transferred messages in separate receive arrays.

After a set MessageEndBit is transmitted, the subsequent segment should be added to the receive array. The message is then complete and can be passed on internally for further processing. A new/separate array should be created for the next message.

Information:

When transferring with MultiSegmentMTUs, it is possible for several small messages to be part of one sequence. In the program, it is important to make sure that a sufficient number of receive arrays can be managed. The acknowledge register is only permitted to be adjusted after the entire sequence has been applied.

If SequenceCounter is incremented by more than one counter, an error is present.

In this case, the receiver stops. All additional incoming sequences are ignored until the transmission with the correct SequenceCounter is retried. This response prevents the transmitter from receiving any more acknowledgments for transmitted sequences. The transmitter can identify the last successfully transferred sequence from the remote station's SequenceAck and continue the transfer from this point.

Information:

This situation is very unlikely when operating without "Forward" functionality.

Acknowledgments must be checked for validity.

If the receiver has successfully accepted a sequence, it must be acknowledged. The receiver takes on the value of SequenceCounter sent along with the transmission and matches SequenceAck to it. The transmitter reads SequenceAck and registers the successful transmission. If the transmitter acknowledges a sequence that has not yet been dispatched, then the transfer must be interrupted and the channel resynchronized. The synchronization bits are reset and the current/incomplete message is discarded. It must be sent again after the channel has been resynchronized.

1.22.5.26.4.5 Flatstream mode

In the input direction, the transmit array is generated automatically. Flatstream mode offers several options to the user that allow an incoming data stream to have a more compact arrangement. These include:

- Standard
- MultiSegmentMTU allowed
- Large segments allowed:

Once enabled, the program code for evaluation must be adapted accordingly.

Information:

All B&R modules that offer Flatstream mode support options "Large segments" and "MultiSegmentMTU" in the output direction. Compact transfer must be explicitly allowed only in the input direction.

Standard

By default, both options relating to compact transfer in the input direction are disabled.

1. The module only forms segments that are at least one byte smaller than the enabled MTU. Each sequence begins with a control byte so that the data stream is clearly structured and relatively easy to evaluate.
2. Since a Flatstream message is permitted to be any length, the last segment of the message frequently does not fill up all of the MTU's space. By default, the remaining bytes during this type of transfer cycle are not used.

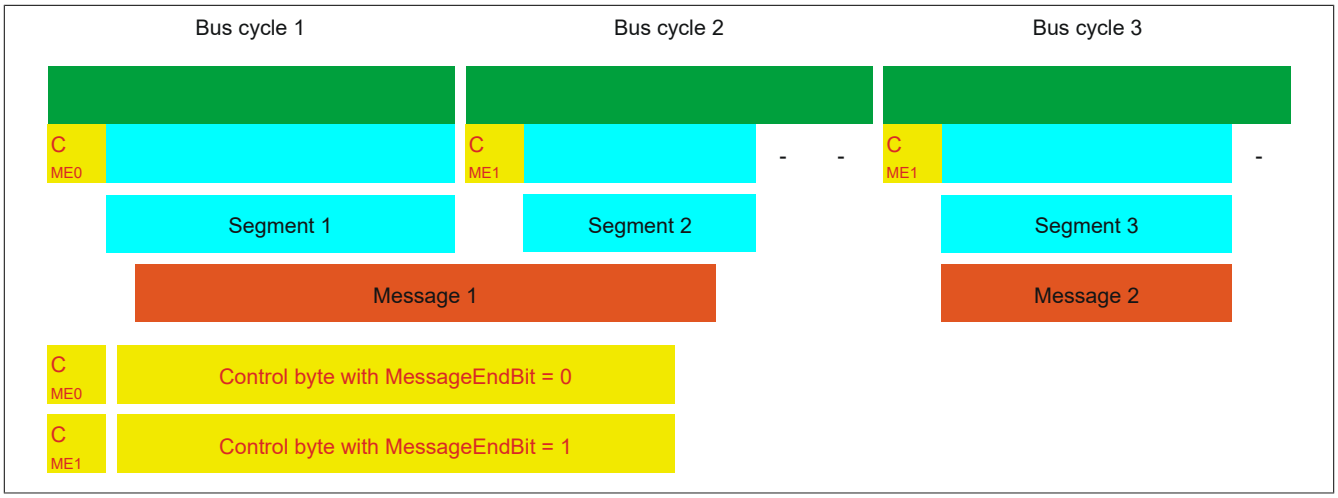


Figure 66: Message arrangement in the MTU (default)

MultiSegmentMTU allowed

With this option, InputMTU is completely filled (if enough data is pending). The previously unfilled Rx bytes transfer the next control bytes and their segments. This allows the enabled Rx bytes to be used more efficiently.

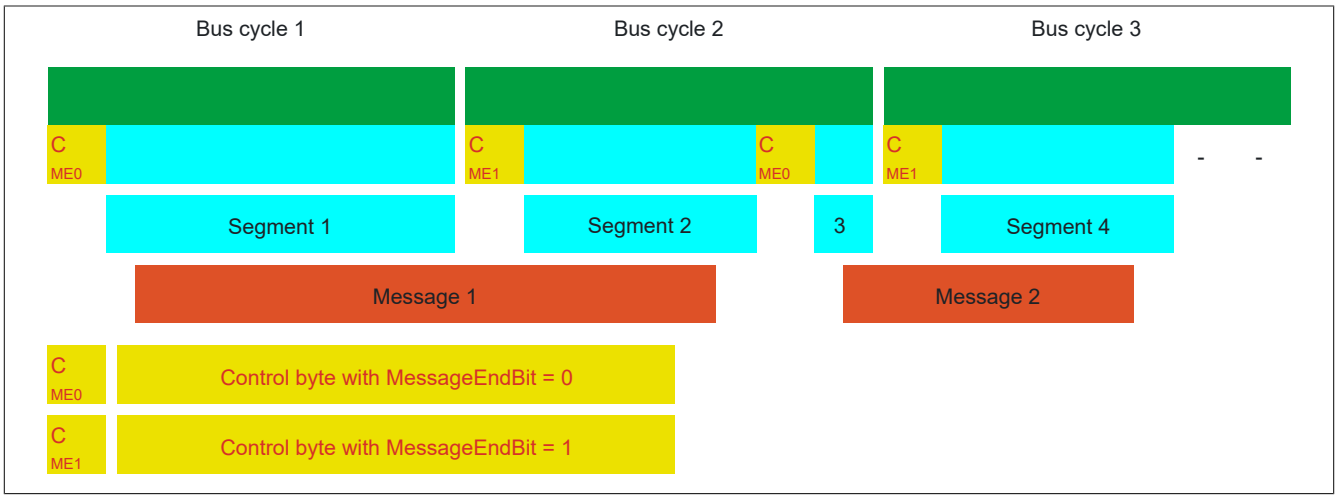


Figure 67: Arrangement of messages in the MTU (MultiSegmentMTU)

Large segments allowed:

When transferring very long messages or when enabling only very few Rx bytes, then a great many segments must be created by default. The bus system is more stressed than necessary since an additional control byte must be created and transferred for each segment. With option "Large segments", the segment length is limited to 63 bytes independently of InputMTU. One segment is permitted to stretch across several sequences, i.e. it is possible for "pure" sequences to occur without a control byte.

Information:

It is still possible to split up a message into several segments, however. If this option is used and messages with more than 63 bytes occur, for example, then messages can still be split up among several segments.

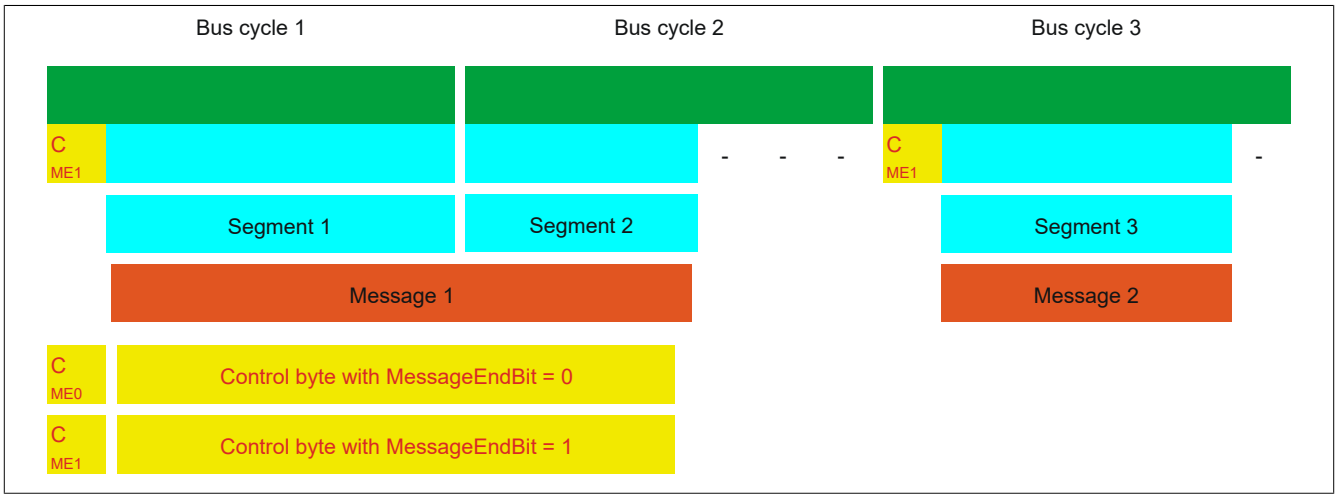


Figure 68: Arrangement of messages in the MTU (large segments)

Using both options

Using both options at the same time is also permitted.

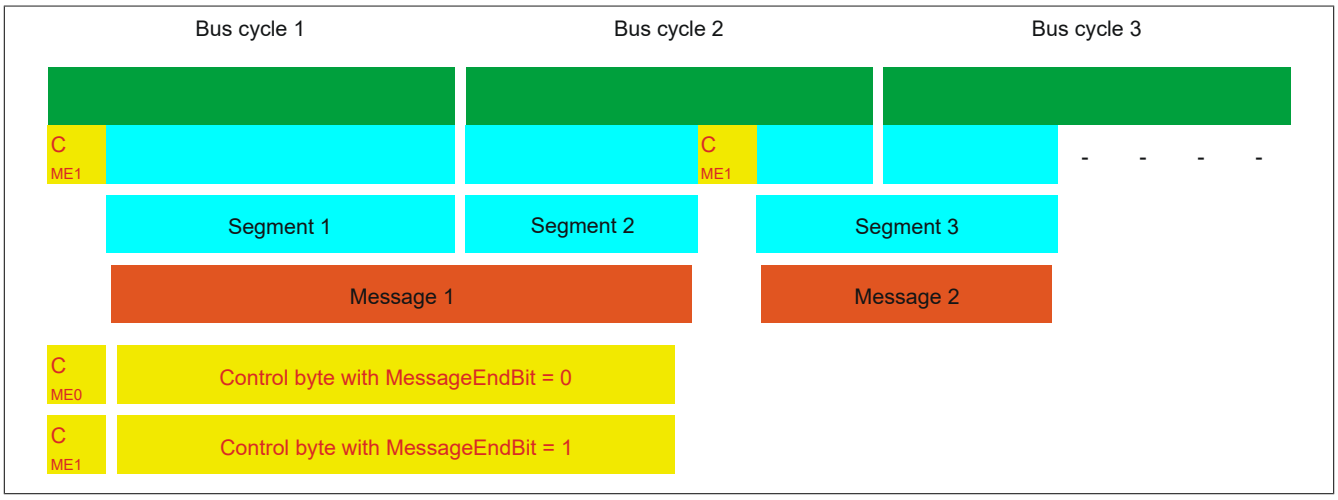


Figure 69: Arrangement of messages in the MTU (large segments and MultiSegmentMTU)

1.22.5.26.4.6 Adjusting the Flatstream

If the way messages are structured is changed, then the way data in the transmit/receive array is arranged is also different. The following changes apply to the example given earlier.

MultiSegmentMTU

If MultiSegmentMTUs are allowed, then "open positions" in an MTU can be used. These "open positions" occur if the last segment in a message does not fully use the entire MTU. MultiSegmentMTUs allow these bits to be used to transfer the subsequent control bytes and segments. In the program sequence, the "nextCBPos" bit in the control byte is set so that the receiver can correctly identify the next control byte.

Example

3 autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows the transfer of MultiSegmentMTUs.

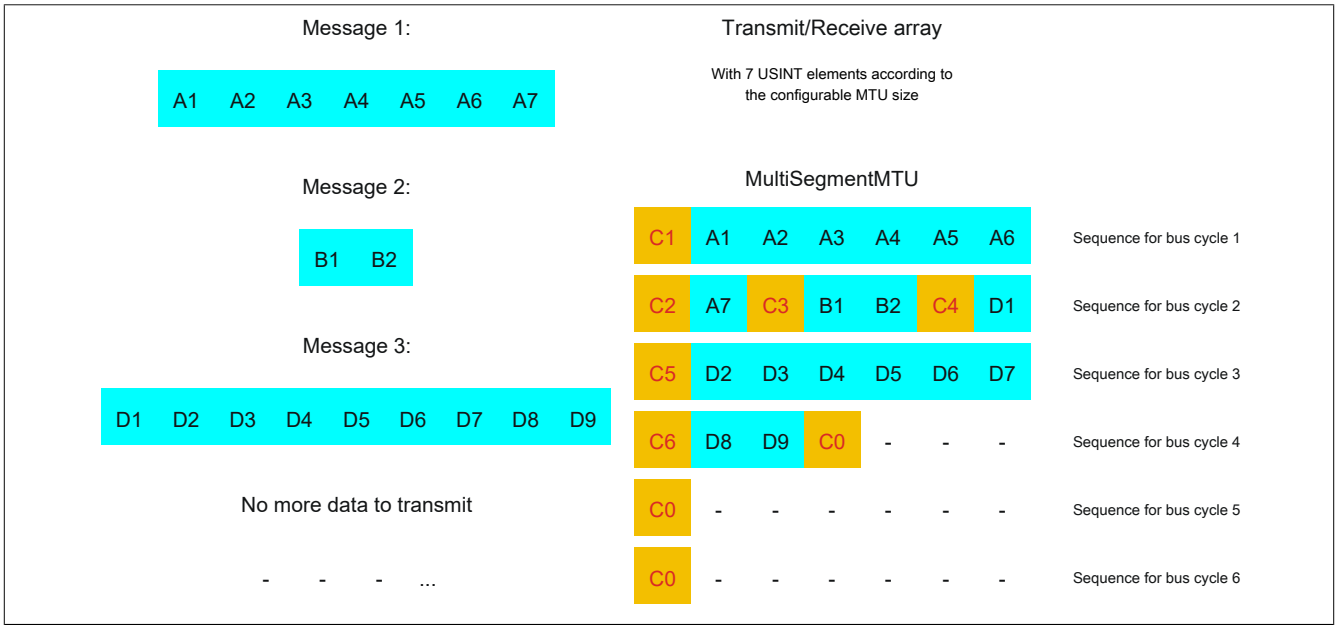


Figure 70: Transmit/receive array (MultiSegmentMTUs)

First, the messages must be split into segments. As in the default configuration, it is important for each sequence to begin with a control byte. The free bits in the MTU at the end of a message are filled with data from the following message, however. With this option, the "nextCBPos" bit is always set if payload data is transferred after the control byte.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Second segment = Control byte + 1 byte of data (MTU still has 5 open bytes)
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data (MTU still has 2 open bytes)
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 1 byte of data (MTU full)
  - ⇨ Second segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Third segment = Control byte + 2 bytes of data (MTU still has 4 open bytes)
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (6)	=	6	- SegmentLength (1)	=	1	- SegmentLength (2)	=	2
- nextCBPos (1)	=	64	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	70	Control byte	Σ	193	Control byte	Σ	194

Table 77: Flatstream determination of the control bytes for the MultiSegmentMTU example (part 1)

Warning!

The second sequence is only permitted to be acknowledged via SequenceAck if it has been completely processed. In this example, there are 3 different segments within the second sequence, i.e. the program must include enough receive arrays to handle this situation.

C4 (control byte 4)			C5 (control byte 5)			C6 (control byte 6)		
- SegmentLength (1)	=	1	- SegmentLength (6)	=	6	- SegmentLength (2)	=	2
- nextCBPos (6)	=	6	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	7	Control byte	Σ	70	Control byte	Σ	194

Table 78: Flatstream determination of the control bytes for the MultiSegmentMTU example (part 2)

Large segments

Segments are limited to a maximum of 63 bytes. This means they can be larger than the active MTU. These large segments are divided among several sequences when transferred. It is possible for sequences to be completely filled with payload data and not have a control byte.

Information:

It is still possible to subdivide a message into several segments so that the size of a data packet does not also have to be limited to 63 bytes.

Example

3 autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows the transfer of large segments.

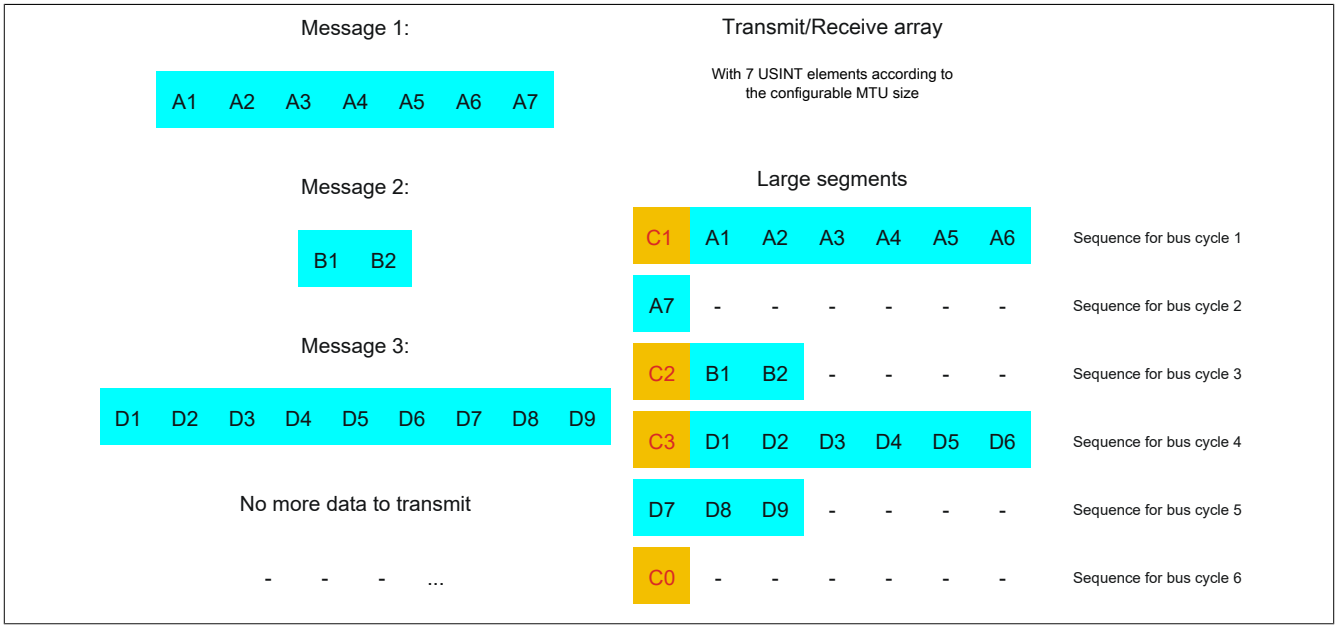


Figure 71: Transmit/receive array (large segments)

First, the messages must be split into segments. The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 7 bytes of data
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 9 bytes of data
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 79: Flatstream determination of the control bytes for the large segment example

Large segments and MultiSegmentMTU

Example

3 autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transfer of large segments as well as MultiSegmentMTUs.

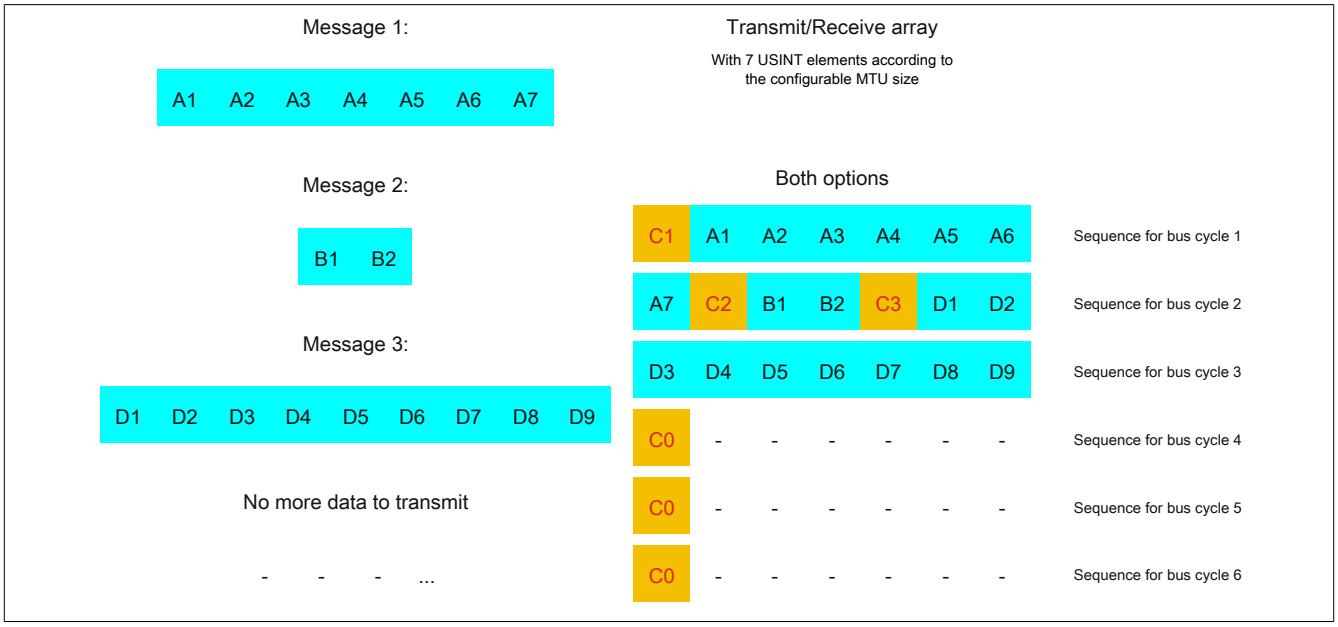


Figure 72: Transmit/receive array (large segments and MultiSegmentMTUs)

First, the messages must be split into segments. If the last segment of a message does not completely fill the MTU, it is permitted to be used for other data in the data stream. Bit "nextCBPos" must always be set if the control byte belongs to a segment with payload data.
The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated. Control bytes are generated in the same way as with option "Large segments".

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 7 bytes of data
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 9 bytes of data
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 80: Flatstream determination of the control bytes for the large segment and MultiSegmentMTU example

1.22.5.26.5 Example of function "Forward" with X2X Link

Function "Forward" is a method that can be used to substantially increase the Flatstream data rate. The basic principle is also used in other technical areas such as "pipelining" for microprocessors.

1.22.5.26.5.1 Function principle

X2X Link communication cycles through 5 different steps to transfer a Flatstream sequence. At least 5 bus cycles are therefore required to successfully transfer the sequence.

	Step I	Step II	Step III	Step IV	Step V
Actions	Transfer sequence from transmit array, increase SequenceCounter	Cyclic synchronization of MTU and module buffer	Append sequence to receive array, adjust SequenceAck	Cyclic synchronization MTU and module buffer	Check SequenceAck
Resource	Transmitter (task to transmit)	Bus system (direction 1)	Recipients (task to receive)	Bus system (direction 2)	Transmitter (task for Ack checking)

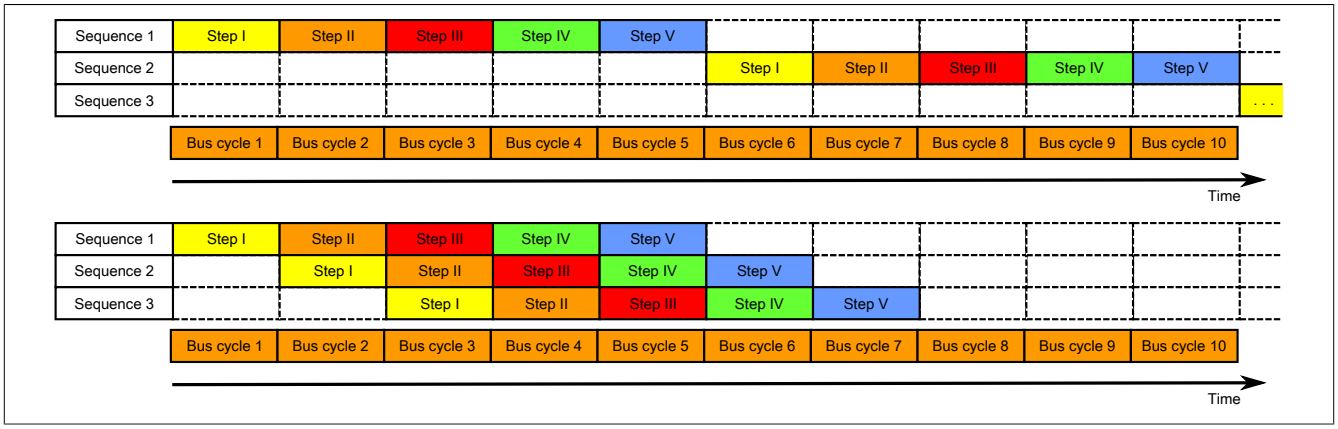


Figure 73: Comparison of transfer without/with Forward

Each of the 5 steps (tasks) requires different resources. If Forward functionality is not used, the sequences are executed one after the other. Each resource is then only active if it is needed for the current sub-action.
With Forward, a resource that has executed its task can already be used for the next message. The condition for enabling the MTU is changed to allow for this. Sequences are then passed to the MTU according to the timing. The transmitting station no longer waits for an acknowledgment from SequenceAck, which means that the available bandwidth can be used much more efficiently.
In the most ideal situation, all resources are working during each bus cycle. The receiver must still acknowledge every sequence received. Only when SequenceAck has been changed and checked by the transmitter is the sequence considered as having been transferred successfully.

1.22.5.26.5.2 Configuration

The Forward function must only be enabled for the input direction. Flatstream modules have been optimized in such a way that they support this function. In the output direction, the Forward function can be used as soon as the size of OutputMTU is specified.

Information:

Registers are described in section "Flatstream registers" on page 569.

Delay time

The delay time is specified in microseconds. This is the amount of time the module must wait after sending a sequence until it is permitted to write new data to the MTU in the following bus cycle. The program routine for receiving sequences from a module can therefore be run in a task class whose cycle time is slower than the bus cycle.

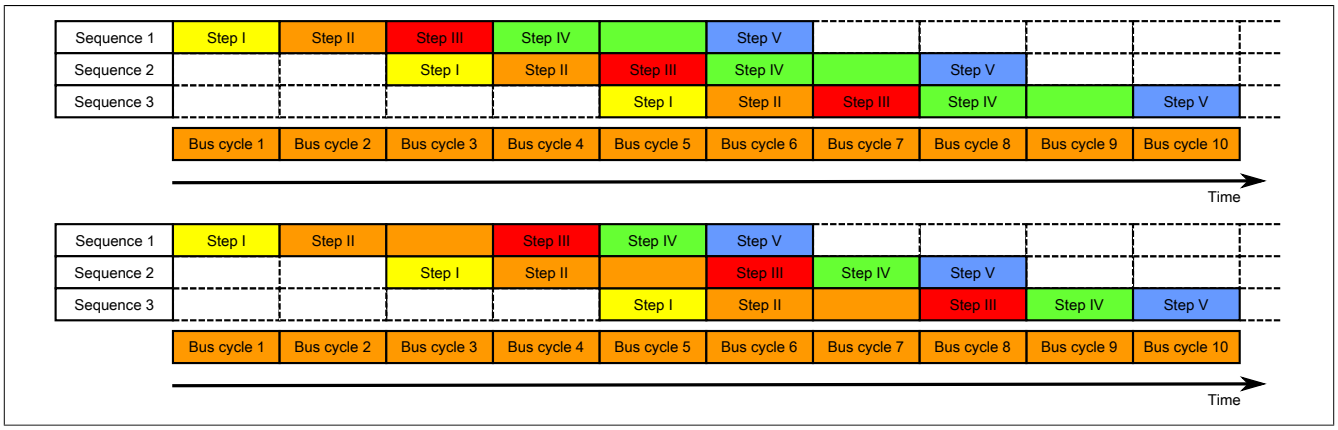


Figure 74: Effect of ForwardDelay when using Flatstream communication with the Forward function

In the program, it is important to make sure that the controller is processing all of the incoming InputSequences and InputMTUs. The ForwardDelay value causes delayed acknowledgment in the output direction and delayed reception in the input direction. In this way, the controller has more time to process the incoming InputSequence or InputMTU.

1.22.5.26.5.3 Transmitting and receiving with Forward

The basic algorithm for transmitting and receiving data remains the same. With the Forward function, up to 7 unacknowledged sequences can be transmitted. Sequences can be transmitted without having to wait for the previous message to be acknowledged. Since the delay between writing and response is eliminated, a considerable amount of additional data can be transferred in the same time window.

Algorithm for transmitting

Cyclic status query: *- The module monitors OutputSequenceCounter.*
0) Cyclic checks: - The controller must check OutputSyncAck. → If OutputSyncAck = 0: Reset OutputSyncBit and resynchronize the channel. - The controller must check whether OutputMTU is enabled. → If OutputSequenceCounter > OutputSequenceAck + 7, then it is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The controller must split up the message into valid segments and create the necessary control bytes. - The controller must add the segments and control bytes to the transmit array.
2) Transmit: - The controller must transfer the current part of the transmit array to OutputMTU. - The controller must increase OutputSequenceCounter for the sequence to be accepted by the module. - The controller is then permitted to *transmit* in the next bus cycle if the MTU has been enabled.
The module responds since OutputSequenceCounter > OutputSequenceAck: *- The module accepts data from the internal receive buffer and appends it to the end of the internal receive array.* *- The module is acknowledged and the currently received value of OutputSequenceCounter is transferred to OutputSequenceAck.* *- The module queries the status cyclically again.*
3) Completion (acknowledgment): - The controller must check OutputSequenceAck cyclically. → A sequence is only considered to have been transferred successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transfer errors in the last sequence as well, it is important to make sure that the algorithm is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transfer can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost (the relationship of bus to task cycle can be influenced by the user so that the threshold value must be determined individually).

Algorithm for receiving

0) Cyclic status query: - The controller must monitor InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck.* *- The module checks if InputMTU for enabling.* *→ Enabling criteria: InputSequenceCounter > InputSequenceAck + Forward*
Preparation: *- The module forms the control bytes / segments and creates the transmit array.*
Action: *- The module transfers the current part of the transmit array to the receive buffer.* *- The module increases InputSequenceCounter.* *- The module waits for a new bus cycle after time from ForwardDelay has expired.* *- The module repeats the action if InputMTU is enabled.*
1) Receiving (InputSequenceCounter > InputSequenceAck): - The controller must apply data from InputMTU and append it to the end of the receive array. - The controller must match InputSequenceAck to InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck.* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.*

Details/Background

1. Illegal SequenceCounter size (counter offset)
   Error situation: MTU not enabled
   If the difference between SequenceCounter and SequenceAck during transmission is larger than permitted, a transfer error occurs. In this case, all unacknowledged sequences must be repeated with the old Sequence-Counter value.
2. Checking an acknowledgment
   After an acknowledgment has been received, a check must verify whether the acknowledged sequence has been transmitted and had not yet been unacknowledged. If a sequence is acknowledged multiple times, a severe error occurs. The channel must be closed and resynchronized (same behavior as when not using Forward).

   > **Information:**
   >
   > **In exceptional cases, the module can increment OutputSequenceAck by more than 1 when using Forward.**
   > **An error does not occur in this case. The controller is permitted to consider all sequences up to the one being acknowledged as having been transferred successfully.**

3. Transmit and receive arrays
   The Forward function has no effect on the structure of the transmit and receive arrays. They are created and must be evaluated in the same way.

1.22.5.26.5.4 Errors when using Forward

In industrial environments, it is often the case that many different devices from various manufacturers are being used side by side. The electrical and/or electromagnetic properties of these technical devices can sometimes cause them to interfere with one another. These kinds of situations can be reproduced and protected against in laboratory conditions only to a certain point.

Precautions have been taken for transfer via X2X Link in case such interference should occur. For example, if an invalid checksum occurs, the I/O system will ignore the data from this bus cycle and the receiver receives the last valid data once more. With conventional (cyclic) data points, this error can often be ignored. In the following cycle, the same data point is again retrieved, adjusted and transferred.

Using Forward functionality with Flatstream communication makes this situation more complex. The receiver receives the old data again in this situation as well, i.e. the previous values for SequenceAck/SequenceCounter and the old MTU.

Loss of acknowledgment (SequenceAck)

If a SequenceAck value is lost, then the MTU was already transferred properly. For this reason, the receiver is permitted to continue processing with the next sequence. The SequenceAck is aligned with the associated SequenceCounter and sent back to the transmitter. Checking the incoming acknowledgments shows that all sequences up to the last one acknowledged have been transferred successfully (see sequences 1 and 2 in the image).

Loss of transmission (SequenceCounter, MTU):

If a bus cycle drops out and causes the value of SequenceCounter and/or the filled MTU to be lost, then no data reaches the receiver. At this point, the transmission routine is not yet affected by the error. The time-controlled MTU is released again and can be rewritten to.
The receiver receives SequenceCounter values that have been incremented several times. For the receive array to be put together correctly, the receiver is only permitted to process transmissions whose SequenceCounter has been increased by one. The incoming sequences must be ignored, i.e. the receiver stops and no longer transmits back any acknowledgments.
If the maximum number of unacknowledged sequences has been sent and no acknowledgments are returned, the transmitter must repeat the affected SequenceCounter and associated MTUs (see sequence 3 and 4 in the image).

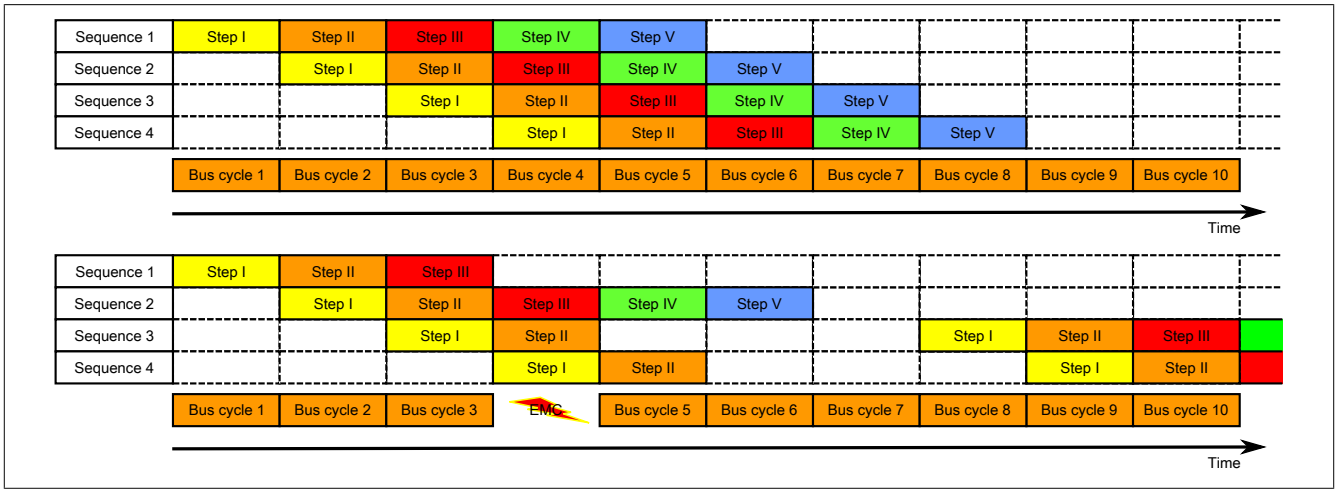


Figure 75: Effect of a lost bus cycle

Loss of acknowledgment

In sequence 1, the acknowledgment is lost due to disturbance. Sequences 1 and 2 are therefore acknowledged in Step V of sequence 2.

Loss of transmission

In sequence 3, the entire transmission is lost due to disturbance. The receiver stops and no longer sends back any acknowledgments.
The transmitting station continues transmitting until it has issued the maximum permissible number of unacknowledged transmissions.
5 bus cycles later at the earliest (depending on the configuration), it begins resending the unsuccessfully sent transmissions.

1.22.5.27 NetTime Technology

NetTime refers to the ability to precisely synchronize and transfer system times between individual components of the controller or network (controller, I/O modules, X2X Link, POWERLINK, etc.).

This allows the moment that events occur to be determined system-wide with microsecond precision. Upcoming events can also be executed precisely at a specified moment.

1.22.5.27.1 Time information

Various time information is available in the controller or on the network:

- System time (on the PLC, Automation PC, etc.)
- X2X Link time (for each X2X Link network)
- POWERLINK time (for each POWERLINK network)
- Time data points of I/O modules

The NetTime is based on 32-bit counters, which are increased with microsecond resolution. The sign of the time information changes after 35 min, 47 s, 483 ms and 648 µs; an overflow occurs after 71 min, 34 s, 967 ms and 296 µs.

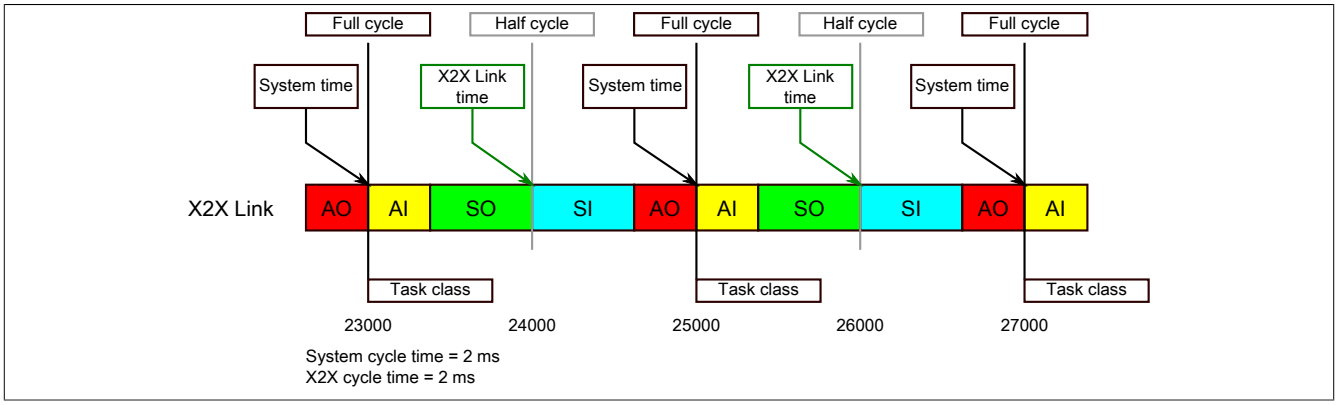
The initialization of the times is based on the system time during the startup of the X2X Link, the I/O modules or the POWERLINK interface.

Current time information in the application can also be determined via library AsIOTime.

1.22.5.27.1.1 Controller data points

The NetTime I/O data points of the controller are latched to each system clock and made available.

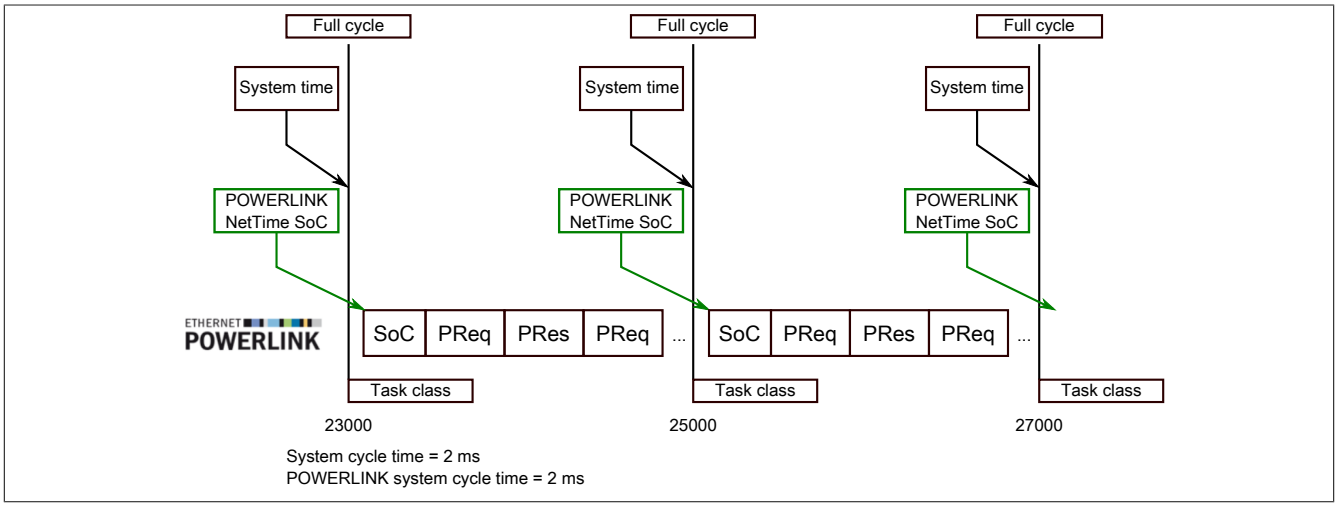
1.22.5.27.1.2 X2X Link - Reference time point



The reference time point on the X2X Link network is always calculated at the half cycle of the X2X Link cycle. This results in a difference between the system time and the X2X Link reference time point when the reference time is read out.

In the example above, this results in a difference of 1 ms, i.e. if the system time and X2X Link reference time are compared at time 25000 in the task, then the system time returns the value 25000 and the X2X Link reference time returns the value 24000.

1.22.5.27.1.3 POWERLINK - Reference time point

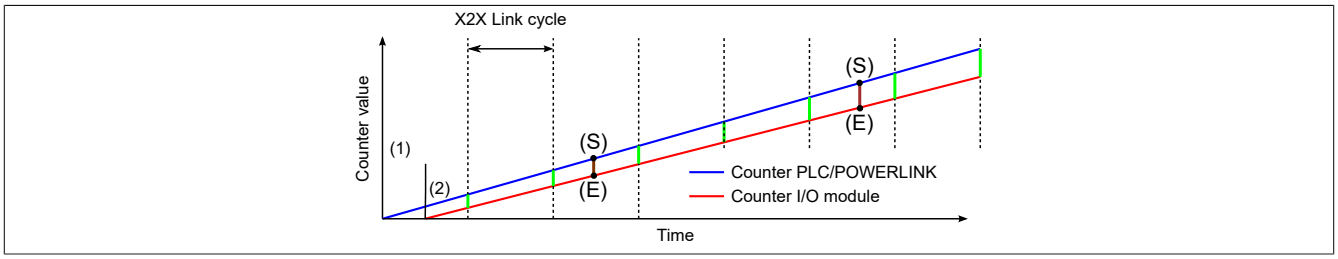


The reference time point on the POWERLINK network is always calculated at the start of cycle (SoC) of the POWERLINK network. The SoC starts 20 µs after the system clock due to the system. This results in the following difference between the system time and the POWERLINK reference time:

POWERLINK reference time = System time - POWERLINK cycle time + 20 µs.

In the example above, this means a difference of 1980 µs, i.e. if the system time and POWERLINK reference time are compared at time 25000 in the task, then the system time returns the value 25000 and the POWERLINK reference time returns the value 23020.

1.22.5.27.1.4 Synchronization of system time/POWERLINK time and I/O module



At startup, the internal counters for the controller/POWERLINK (1) and the I/O module (2) start at different times and increase the values with microsecond resolution.

At the beginning of each X2X Link cycle, the controller or POWERLINK network sends time information to the I/O module. The I/O module compares this time information with the module's internal time and forms a difference (green line) between the two times and stores it.

When a NetTime event (E) occurs, the internal module time is read out and corrected with the stored difference value (brown line). This means that the exact system moment (S) of an event can always be determined, even if the counters are not absolutely synchronous.

Note

The deviation from the clock signal is strongly exaggerated in the picture as a red line.

1.22.5.27.2 Timestamp functions

NetTime-capable modules provide various timestamp functions depending on the scope of functions. If a timestamp event occurs, the module immediately saves the current NetTime. After the respective data is transferred to the controller, including this precise moment, the controller can then evaluate the data using its own NetTime (or system time), if necessary.

1.22.5.27.2.1 Time-based inputs

NetTime Technology can be used to determine the exact moment of a rising edge at an input. The rising and falling edges can also be detected and the duration between 2 events can be determined.

Information:

The determined moment always lies in the past.

1.22.5.27.2.2 Time-based outputs

NetTime Technology can be used to specify the exact moment of a rising edge on an output. The rising and falling edges can also be specified and a pulse pattern generated from them.

Information:

The specified time must always be in the future, and the set X2X Link cycle time must be taken into account for the definition of the moment.

1.22.5.27.2.3 Time-based measurements

NetTime Technology can be used to determine the exact moment of a measurement that has taken place. Both the starting and end moment of the measurement can be transmitted.

1.22.5.28 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

1.22.5.29 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time	
Voltage and current sampling rate for calculation of RMS value, power and energy	1 MHz
Derived values: RMS value, power, energy, power factor, phase angle, frequency (mean values over 16 full waves)	Approx. 3 Hz
FFT on request (sample rate: 8 kHz)	2 Hz

1.23 For reference only

Information:

The data sheets in this section are for reference only when the modules are already in use.

1.23.1 X20AI2632-1

1.23.1.1 General information

The module is equipped with 2 inputs with 16-bit digital converter resolution. It is possible to select between the current and voltage signal using different terminals.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

- 2 analog inputs
- Either current or voltage signal possible
- Extended signal range
- 16-bit digital converter resolution
- Simultaneous input conversion
- Very fast conversion time

1.23.1.1.1 Other applicable documents

For additional and supplementary information, see the following documents.

Other applicable documents

Document name	Title
MAX20	X20 System user's manual
MAEMV	Installation / EMC guide

1.23.1.2 Order data

Order number	Short description	Figure
	Analog inputs	
X20AI2632-1	X20 analog input module, 2 inputs, ±11 V or 0 to 22 mA, 16-bit converter resolution, configurable input filter	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 81: X20AI2632-1 - Order data

1.23.1.3 Technical description

1.23.1.3.1 Technical data

Order number	X20AI2632-1
Short description	
I/O module	2 analog inputs ±11 V or 0 to 22 mA
General information	
B&R ID code	0xA29E
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using LED status indicator and software
Inputs	Yes, using LED status indicator and software
Channel type	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	1.2 W [1)]
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
UKCA	Yes
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
DNV	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
LR	ENV1
KR	Yes
ABS	Yes
EAC	Yes
KC	Yes
Analog inputs	
Input	±11 V or 0 to 22 mA, via different terminal connections
Input type	Differential input
Digital converter resolution	
Voltage	±15-bit
Current	15-bit
Conversion time	50 µs for all inputs
Output format	INT
Output format	
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0001 = 335.693 µV
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 671.387 nA
Input impedance in signal range	
Voltage	20 MΩ
Current	-
Load	
Voltage	-
Current	<400 Ω
Input protection	Protection against wiring with supply voltage
Permissible input signal	
Voltage	Max. ±30 V
Current	Max. ±50 mA
Output of digital value during overload	
Undershoot	
Voltage	0x8001
Current	0x0000
Overshoot	
Voltage	0x7FFF
Current	0x7FFF
Conversion procedure	SAR
Input filter	Hardware - Third-order low-pass filter / cutoff frequency 10 kHz

Table 82: X20AI2632-1 - Technical data

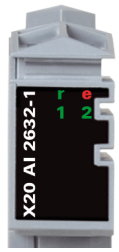
Order number	X20AI2632-1
Max. error	
Voltage	
Gain	0.08% 2)
Offset	0.01% 3)
Current	
Gain	0.08% 2)
Offset	0.02% 4)
Max. gain drift	
Voltage	0.01%/°C 2)
Current	0.01%/°C 2)
Max. offset drift	
Voltage	0.001%/°C 3)
Current	0.002%/°C 4)
Common-mode rejection	
DC	70 dB
50 Hz	70 dB
Common-mode range	±12 V
Crosstalk between channels	<-70 dB
Nonlinearity	
Voltage	<0.01% 3)
Current	<0.015% 4)
Insulation voltage between channel and bus	500 V_{eff}
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x terminal block X20TB06 or X20TB12 separately. Order 1x bus module X20BM11 separately.
Pitch	$12.5^{+0.2}$ mm

Table 82: X20AI2632-1 - Technical data

1) To reduce power dissipation, B&R recommends bridging unused inputs on the terminals or configuring them as current signals.
2) Based on the current measured value.
3) Based on the 22 V measurement range.
4) Based on the 22 mA measurement range.

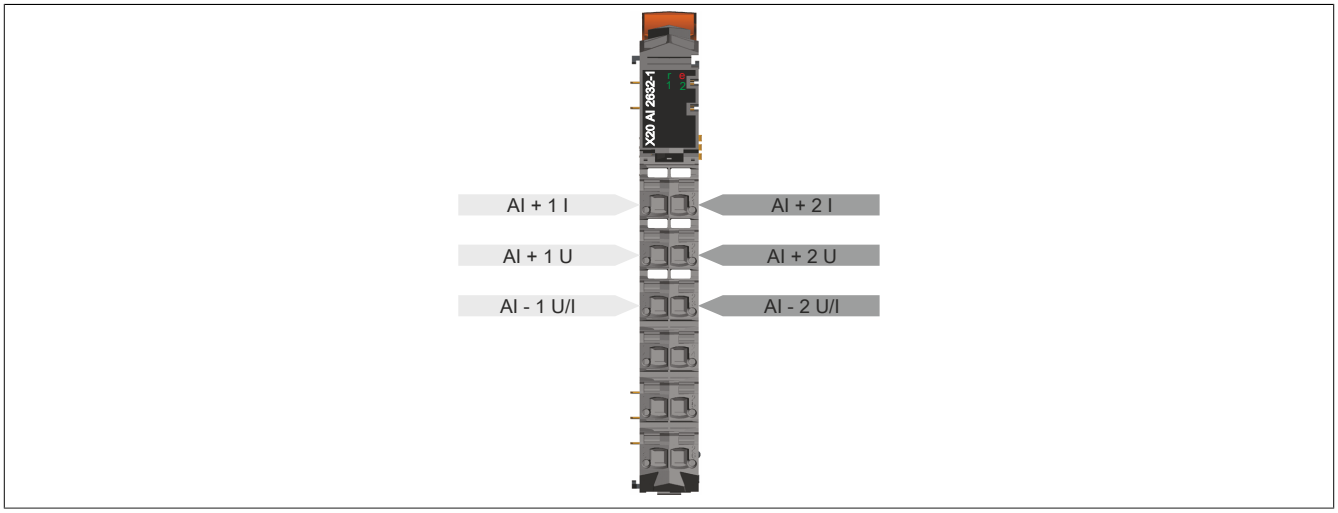
1.23.1.3.2 LED status indicators

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 System user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
			Double flash	System error: • Violation of the scan time • Synchronization error
	1 - 2	Green	Off	Open line[2] or sensor is disconnected
			On	Analog/digital converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.
2) Open line detection only possible when measuring voltage.

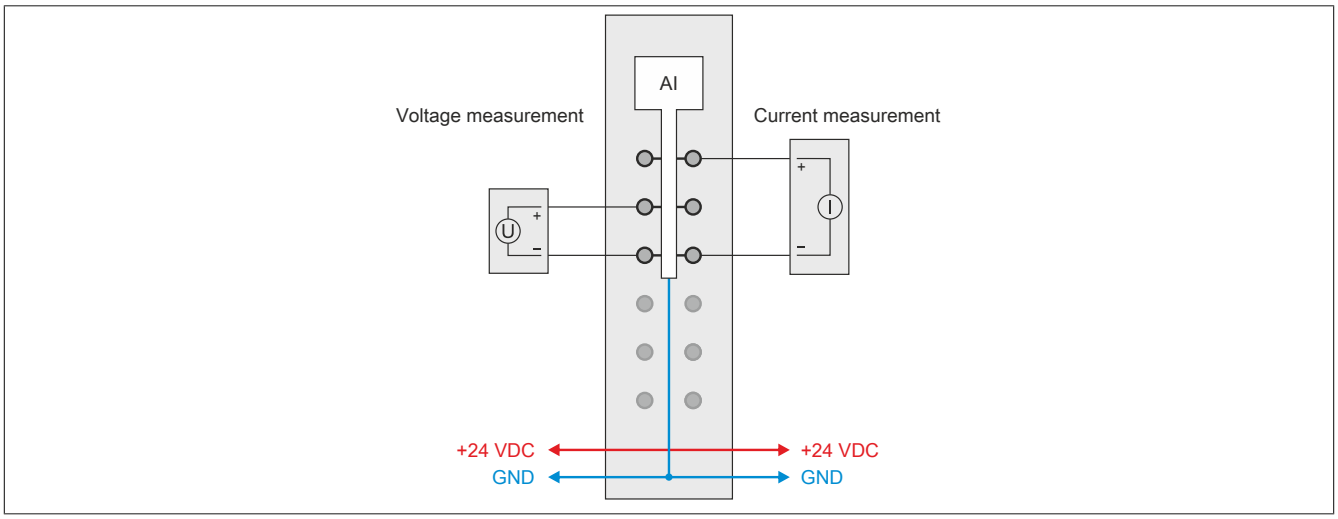
1.23.1.3.3 Pinout



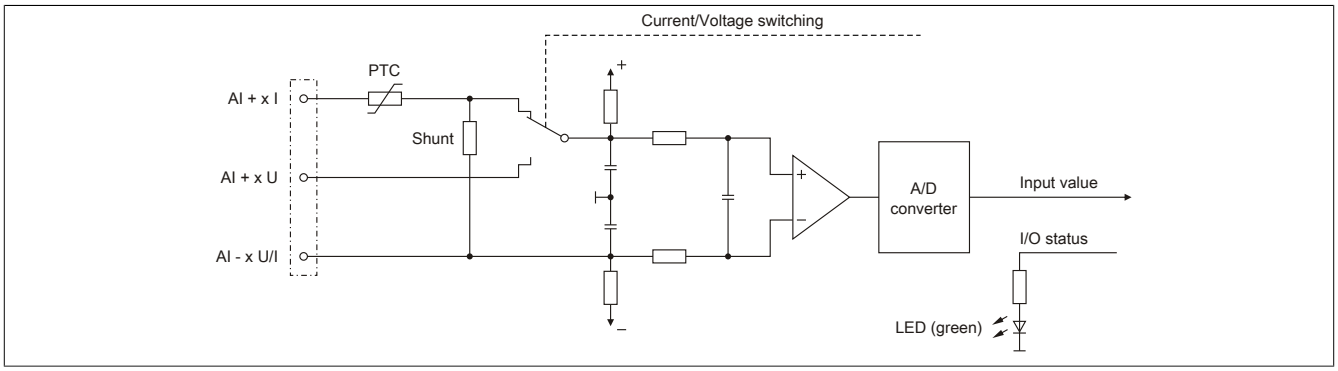
1.23.1.3.4 Connection example

To prevent disturbances, the following modules must be separated by at least one module:

- Bus receiver X20BR9300
- Supply module X20PS3300/X20PS3310
- Supply module X20PS9400/X20PS9402
- Supply module X20PS9500/X20PS9502
- Controller



1.23.1.3.5 Input circuit diagram



1.23.1.4 Register description

1.23.1.4.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 System user's manual.

1.23.1.4.2 Function model 0 - default

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration - Frame size						
-	AsynSize	-				
Configuration						
257	ConfigOutput01 (channel configuration)	USINT				•
289	ConfigOutput06 (channel configuration)	USINT				•
	Sampling time					
390	ConfigOutput24 (sampling time)	UINT				•
	Filtering					
259	ConfigOutput26 (filter order)	USINT				•
291	ConfigOutput28 (filter order)	USINT				•
262	ConfigOutput27 (filter cutoff frequency)	UINT				•
294	ConfigOutput29 (filter cutoff frequency)	UINT				•
	Scaling					
276	ConfigOutput04 (user-defined gain)	DINT				•
308	CongifOutput09 (user-defined gain)	DINT				•
284	ConfigOutput05 (user-defined offset)	DINT				•
316	ConfigOutput10 (user-defined offset)	DINT				•
	User-defined limit values					
266	ConfigOutput02 (minimum limit value)	UINT				•
298	ConfigOutput07 (minimum limit value)	UINT				•
270	ConfigOutput03 (maximum limit value)	UINT				•
302	ConfigOutput08 (maximum limit value)	UINT				•
Communication						
0	AnalogInput01	INT	•			
4	AnalogInput02	INT	•			
650	SampleCycleCounter	UINT		•		
	Error monitoring and counters					
641	Channel status	USINT	•			
	Channel01OK	Bit 0				
	Channel02OK	Bit 1				
	SyncStatus	Bit 6				
	ConvertionCycle	Bit 7				
654	SampleCycleViolationErrorCounter	UINT		•		
658	SynchronizationViolationErrorCounter	UINT		•		
2097	Range violation (neg. and pos.)	USINT	•			
	Channel01underflow	Bit 0				
	Channel02underflow	Bit 1				
	Channel01overflow	Bit 4				
	Channel02overflow	Bit 5				
2099	Working range violation (pos.)	USINT	•			
	Channel01outofrange	Bit 0				
	Channel02outofrange	Bit 1				
518	Ch01OutOfRange	UINT		•		
550	Ch02OutOfRange	UINT		•		
522	Ch01Underflow	UINT		•		
554	Ch02Underflow	UINT		•		
526	Ch01Overflow	UINT		•		
558	Ch02Overflow	UINT		•		
Additional analysis functions						
133	ConfigOutput21 (trigger condition on falling edge)	USINT				•
135	ConfigOutput22 (trigger condition on rising edge)	USINT				•
129	Analysis control byte	USINT			•	
	TraceTrigger01	Bit 0				
	MinMaxStart01	Bit 4				
	MinMaxStart02	Bit 5				
129	Analysis status byte	USINT	•			
	MinMaxStart01Readback	Bit 4				
	MinMaxStart02Readback	Bit 5				
	Limit values					
530	MinInput01	INT	•			

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
562	MinInput02	INT	•			
534	MaxInput01	INT	•			
566	MaxInput02	INT	•			
538	Ch01MinMaxLatchCounter	UINT		•		
570	Ch02MinMaxLatchCounter	UINT		•		
	Trace configuration					
1026	TraceChannelEnable	USINT				•
1030	TraceSampleDepth	UINT				•
4157	ConfigOutput25 (recording priority)	USINT				•
1037	Starting a recording	USINT			•	
	TraceEnable01	Bit 0				
1089	Recording status	USINT	•			
	TraceEnabled	Bit 0				
	TraceWriteActive	Bit 2				
	TraceReadActive	Bit 3				
	ReadyForTrigger	Bit 4				
	TriggerActive	Bit 5				
	TraceOK	Bit 6				
	TraceError	Bit 7				
1094	FreeBufferSize	UINT	•			
1098	TriggerCount	UINT	•			
1102	TriggerFailCount	UINT	•			
	Comparator					
450	cfgComp_LowLimitCh01	INT			(•)	•
458	cfgComp_LowLimitCh02	INT			(•)	•
454	cfgComp_HighLimitCh01	INT			(•)	•
462	cfgComp_HighLimitCh02	INT			(•)	•
662	CompStateCollection	UINT	•			
490	cfgComp_NominalState	UINT				•
482	cfgComp_EnableMask	UINT				•
486	cfgComp_ConditionTypeMask	UINT				•
	Time-offset trace					
1042	TraceTriggerStart	INT				•
1046	TraceTriggerStop	UINT				•

1.23.1.4.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration - Frame size							
-	-	AsynSize	-				
Configuration							
257	-	ConfigOutput01 (channel configuration)	USINT				•
289	-	ConfigOutput06 (channel configuration)	USINT				•
	Sampling time						
390	-	ConfigOutput24 (sampling time)	UINT				•
	Filtering						
259	-	ConfigOutput26 (filter order)	USINT				•
291	-	ConfigOutput28 (filter order)	USINT				•
262	-	ConfigOutput27 (filter cutoff frequency)	UINT				•
294	-	ConfigOutput29 (filter cutoff frequency)	UINT				•
	Scaling						
276	-	ConfigOutput04 (user-defined gain)	DINT				•
308	-	CongifOutput09 (user-defined gain)	DINT				•
284	-	ConfigOutput05 (user-defined offset)	DINT				•
316	-	ConfigOutput10 (user-defined offset)	DINT				•
	User-defined limit values						
266	-	ConfigOutput02 (minimum limit value)	UINT				•
298	-	ConfigOutput07 (minimum limit value)	UINT				•
270	-	ConfigOutput03 (maximum limit value)	UINT				•
302	-	ConfigOutput08 (maximum limit value)	UINT				•
Communication							
0	0	AnalogInput01	INT	•			
4	2	AnalogInput02	INT	•			
650	-	SampleCycleCounter	UINT		•		
	Error monitoring and counters						
641	-	Channel status	USINT		•		
		Channel01OK	Bit 0				
		Channel02OK	Bit 1				
		SyncStatus	Bit 6				
		ConvertionCycle	Bit 7				
654	-	SampleCycleViolationErrorCounter	UINT		•		
658	-	SynchronizationViolationErrorCounter	UINT		•		
2097	-	Range violation (neg. and pos.)	USINT		•		
		Channel01underflow	Bit 0				
		Channel02underflow	Bit 1				
		Channel01overflow	Bit 4				
		Channel02overflow	Bit 5				
2099	-	Working range violation (pos.)	USINT		•		
		Channel01outofrange	Bit 0				
		Channel02outofrange	Bit 1				
518	-	Ch01OutOfRange	UINT		•		
550	-	Ch02OutOfRange	UINT		•		
522	-	Ch01Underflow	UINT		•		
554	-	Ch02Underflow	UINT		•		
526	-	Ch01Overflow	UINT		•		
558	-	Ch02Overflow	UINT		•		
Additional analysis functions							
133	-	ConfigOutput21 (trigger condition on falling edge)	USINT				•
135	-	ConfigOutput22 (trigger condition on rising edge)	USINT				•
129	-	Analysis control byte	USINT				•
		TraceTrigger01	Bit 0				
		MinMaxStart01	Bit 4				
		MinMaxStart02	Bit 5				
129	-	Analysis status byte	USINT		•		
		MinMaxStart01Readback	Bit 4				
		MinMaxStart02Readback	Bit 5				
	Limit values						
530	-	MinInput01	INT		•		
562	-	MinInput02	INT		•		
534	-	MaxInput01	INT		•		
566	-	MaxInput02	INT		•		
538	-	Ch01MinMaxLatchCounter	UINT		•		
570	-	Ch02MinMaxLatchCounter	UINT		•		

1) The offset specifies the position of the register within the CAN object.

1.23.1.4.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

1.23.1.4.3.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

1.23.1.4.4 Configuration

This module is equipped with analog inputs with connected 16-bit A/D converters. Each of the inputs can be configured separately from one another either on the voltage or current input for the following areas:

- Permitted voltage: ±11 V at 20 Ω
- Permitted current: 22 mA (maximum 40 mA) (<400 Ω)

1.23.1.4.4.1 Channel configuration

Name:
ConfigOutput01 for channel 01
ConfigOutput06 for channel 02

The individual inputs for processing the current or voltage signal are configured in these registers. This configuration must be made in addition to using suitable terminals.

Filtering, analysis and error monitoring (bits 4 to 6) can only be used if the channel is enabled (bit 7 = 0).

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	Terminal selector	0	Voltage terminal for ±11 VDC (bus controller default setting)
		1	Current terminal for 0 to 22 mA
1	Gain selector	0	Voltage ±11 VDC (bus controller default setting)
		1	Current 0 to 22 mA
2 - 3	Reserved	-	
4	Filtering active (only if bit 7 = 0)	0	Inactive (bus controller default setting)
		1	Active
5	Minimum/Maximum analysis active (only if bit 7 = 0)	0	Inactive (bus controller default setting)
		1	Active
6	Error monitoring active (only if bit 7 = 0)	0	Inactive (bus controller default setting)
		1	Active
7	Enables channel	0	Channel enabled (bus controller default setting)
		1	Channel disabled

1.23.1.4.4.2 Sampling and conversion

The analog signal is sampled in 2 steps.

- **Conversion task**

  The A/D converter digitalizes the inputs signals for the enabled inputs once per conversion cycle. Then the results are available internally in the module. To ensure that this process is executed without delays, the corresponding task will be handled with very high priority.

  The timespan needed for conversion results from the set sampling time.
- **Processing task**

  The converted A/D converter values are further processed according to the user settings (filtering, scaling, limit values, error statistics, min/max analysis, hysteresis comparison). The task for this process has low priority. The timespan needed for further processing depends on the configured functions and is the second portion of the sampling time.

Cycle time violation

In normal operation, further processing is triggered after each conversion. The conversion and sampling tasks run synchronous to one another. If the predefined sampling time is not sufficient to convert all enabled channels and complete the configured functions, a cycle time violation occurs.

Sampling time

Name:
ConfigOutput24

The sampling time is set to µs in this register. This makes it possible to improve the sampling cycle (resolution = 1 µs). The lowest configurable cycle time is 50 µs.

Data type	Value	Information
UINT	50 to 10,000	Bus controller default setting: 100

Information:

Values that are too low for the cycle time will result in cycle time violations.

1.23.1.4.4.3 Filtering (optional)

If filtering is enabled in the "Channel configuration" on page 610 register, the basic data of the A/D converter is filtered per channel. The following registers are available to specify the filter order and respective cutoff frequency for configuring the low-pass filter:

- "Filter order" on page 611
- "Filter cutoff frequency" on page 611

Filter order

Name:
ConfigOutput26 for channel 1
ConfigOutput28 for channel 2

The filter order is specified in this register. The "Filter cutoff frequency" on page 611 register is used to configure the respective cutoff frequency of the filter.

Data type	Value	Information
USINT	1 to 4	Bus controller default setting: 0

Internal filter orders greater than 1 are implemented as cascaded first-order filters.

Calculating the cutoff frequency of an nth-order filter:

Cutoff frequency = Cutoff frequency$_N$ / ((2 ^ (1 / n) - 1) ^ 0.5)

Approximate calculation

yn = a * xn + b * y(n-1)

a = Sampling time$_{Sec}$ / (Sampling time$_{Sec}$ + 1 / (2 Pi * Cutoff frequency$_{Hz}$))

b = 1 - a

Information:

Since low-pass filtering takes place using an approximation procedure with fixed-point arithmetic, there are discrepancies to the effective cutoff frequency that depend on the sampling cycle and filter sequence.

Filter cutoff frequency

Name:
ConfigOutput27 for channel 1
ConfigOutput29 for channel 2

The cutoff frequency of the respective filter is configured in these registers.

Data type	Value	Information
UINT	1 to 65,535	Cutoff frequency in hertz. Bus controller default setting: 0

Information:

The highest cutoff frequency is limited by the Nyquist Shannon sampling theorem (based on the sampling cycle time). The system does not check for violations of this sampling theorem.

1.23.1.4.4.4 Scaling (optional)

Scaling A/D converter data is an option for the user. The following registers are available for this:

- "User-defined gain" on page 612 (= ku)
- "User-defined offset" on page 612 (= du)

Scaling calculation:

Scaled value = k * A/C value + d

Gain k = $k_{Calibration}$ * ku

Offset d = $d_{Calibration}$ + du

The value has to be limited since it can exceed the 16-bit constraints. To provide the greatest degree of flexibility, limiting is possible using the registers "Minimum limit value" on page 612 and "Maximum limit value" on page 613.

User-defined gain

Name:
ConfigOutput04 for channel 1
ConfigOutput09 for channel 2

The user-defined gain for the A/D converter data of the respective physical channel can be specified in these registers.

The value 65,536 (0x10000) corresponds to a gain of 1.

Data type	Values	Information
DINT	-2,147,483,648 to 2,147,483,647	Bus controller default setting: 65,536

User-defined offset

Name:
ConfigOutput05 for channel 1
ConfigOutput10 for channel 2

The user-defined offset for the A/D converter data of the respective physical channel can be specified in this register.

The value 65,536 (0x10000) corresponds to an offset of 1.

Data type	Values	Information
DINT	-2,147,483,648 to 2,147,483,647	Bus controller default setting: 0

1.23.1.4.4.5 User-defined limit values

If the application requires a limitation of the range of values, then the user can define his own limit values. These values will also be use for the module's error statistics. The following registers are available for this:

- "Minimum limit value" on page 612
- "Maximum limit value" on page 613

Information:

32-bit numbers are used inside the module. A limit value violation can therefore also be determined if the permitted range of values was defined from -32768 to 32767.

Minimum limit value

Name:
ConfigOutput02 for channel 1
ConfigOutput07 for channel 2

The minimum limit value is configured in this register. This limit value is also used for the underflow error statistics (see register "Ch0xUnderflow" on page 616).

Data type	Values	Information
INT	-32768 to 32767	Bus controller default setting: -32768

Maximum limit value

Name:
ConfigOutput03 for channel 1
ConfigOutput08 for channel 2

The maximum limit value is configured in this register. This limit value is also used for the overflow error statistics (see register "Ch0xOverflow" on page 616).

Data type	Values	Information
INT	-32767 to 32767	Bus controller default setting: 32767

1.23.1.4.5 Communication - General

The module's analog inputs convert current and voltage values with 16-bit resolution. This information can be used by the application with the help of the registers listed here.

1.23.1.4.5.1 Analog input channels

Name:
AnalogInput01 to AnalogInput02

The analog input value is mapped in this register depending on the configured operating mode.

Data type	Value	Input signal:
INT	-32,768 to 32,767	Voltage signal ±11 VDC
	0 to 32,767	Current signal 0 to 22 mA

1.23.1.4.5.2 Sampling cycle counter

Name:
SampleCycleCounter

The number of times the input signal has been sampled is provided in this register.

Data type	Values
UINT	0 to 65,535

1.23.1.4.5.3 Error monitoring and counters

Channel status

Name:
Channel01OK to Channel02OK
SyncStatus
ConvertionCycle

This register collects error messages synchronously with the network cycle. Temporary error states that were registered in a conversion cycle remain active for at least 2 network cycles. In order to receive detailed error information, the corresponding error counters and X2X network events should also be observed.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01OK	0	OK
		1	Errors
1	Channel02OK	0	OK
		1	Errors
2 - 5	Reserved	-	
6	SyncStatus[1)]	0	OK
		1	Not synchronized
7	ConvertionCycle[2)]	0	OK
		1	Errors

1) Identical to bit 0 of the registers "SynchronizationViolationErrorCounter" on page 614.
2) Identical to bit 0 of the registers "SampleCycleViolationErrorCounter" on page 614.

Counter for synchronization errors

Name:
SynchronizationViolationErrorCounter

This register counts how often the conversion task was triggered more than 5 µs after the next-coming X2X cycle. In this case, the module is considered being no longer synchronized with X2X Link.

The counters in this register follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

Counter for faulty sampling cycles

Name:
SampleCycleViolationErrorCounter

This register is used to indicate the number of cycle time violations that have occurred thus far. A cycle time violation occurs if the conversion tasks initiates a sampling task before the last sampling cycle has finished. See "Sampling and conversion" on page 610.

The counters in this register follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

Range violation (neg. and pos.)

Name:
Channel01underflow to Channel02underflow
Channel01overflow to Channel02overflow

This register indicates whether the limit values defined by registers "Minimum limit value" on page 612 and "Maximum limit value" on page 613 have been overshot or undershot. The individual bits in this register are identical to the values of the lowest bits of registers "Ch0xUnderflow" on page 616 and "Ch0xOverflow" on page 616.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01underflow	0	No error
		1	Range exceeded (.neg) on channel 1
1	Channel02underflow	0	No error
		1	Range exceeded (.neg) on channel 2
2 - 3	Reserved	-	
4	Channel01overflow	0	No error
		1	Range exceeded (.pos) on channel 1
5	Channel02overflow	0	No error
		1	Range exceeded (.pos) on channel 2
6 - 7	Reserved	-	

Working range violation (pos.)

Name:
Channel01outofrange to Channel02outofrange

This register indicates whether the input value overshoots the module's maximum measurement range. The individual bits in this register are identical to the values of the lowest bits of register "Ch0xOutOfRange" on page 615.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel01outofrange	0	No error
		1	Working range violation (pos.) of channel 1
1	Channel02outofrange	0	No error
		1	Working range violation (pos.) of channel 2
2 - 7	Reserved	-	

Counter for work range violations (pos.)

Name:
Ch01OutOfRange to Ch02OutOfRange

Errors outside of the module's maximum possible measurement range are indicated in this register. These errors lead to full-scale deflection of the A/D converter.

The counters in these registers follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

This counter is only active if the static error counter is enabled (see register "Channel configuration" on page 610).

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

Counter for range exceeded violations (neg.)

Name:
Ch01Underflow to Ch02Underflow

This register indicates range exceeded violations (neg.) of the value configured in the register "Minimum limit value" on page 612.

The counters in these registers follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

This counter is only active if the static error counter is enabled (see register "Channel configuration" on page 610).

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

Counter for range exceeded violations (pos.)

Name:
Ch01Overflow to Ch02Overflow

This register indicates range exceeded violations (pos.) of the value configured in the register "Maximum limit value" on page 613.

The counters in these registers follow the rules of the event error counter, i.e. the count increased each time an error occurs or is reset. The last bit of the counter indicates the error status:

- Last bit = 1 → Error pending
- Last bit = 0 → No error

This counter is only active if the static error counter is enabled (see register "Channel configuration" on page 610).

Data type	Value	Information
UINT	0 to 65535	Counter value
	0 to 1	Bit 0: Error status

1.23.1.4.6 Additional analysis functions

In addition to sampling the analog input signal, this module can also be used to perform additional analysis of the values obtained.

- **Limit value analysis**
  If limit value analysis has been enabled for a channel, the sampled minimum and maximum values are latched internally in the module. A measurement period can be triggered using the control byte. When the respective configured edge is generated by the application, the limit values from the previous measurement period are displayed and the internal latch register is reset.
- **Recording sampled values**
  If recording sampled values has been enabled for a channel, then the sampled values are additionally recorded in the module's internal FIFO memory. If the configured event occurs, the contents of the FIFO memory are transmitted to the application.

Information:

Recording of sampled values can only be used if the module is operated on an X2X master that is a type SG4 controller.

1.23.1.4.6.1 Trigger condition on falling edge

Name:
ConfigOutput21

This register configures whether the falling edge is used to trigger the trace and determination of the input value in the register "Analysis control byte" on page 618.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	No trigger (bus controller default setting)
		1	Falling edge active as trigger
1 - 3	Reserved	-	
4	MinMaxStart01	0	No determination (bus controller default setting)
		1	Falling edge determines input value of channel 1
5	MinMaxStart02	0	No determination (bus controller default setting)
		1	Falling edge determines input value of channel 2
6 - 7	Reserved	0	

1.23.1.4.6.2 Trigger condition on rising edge

Name:
ConfigOutput22

This register configures whether the rising edge is used to trigger the trace and determination of the input value in the register "Analysis control byte" on page 618.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	Trigger not initiated on positive edge (bus controller default setting)
		1	Rising edge active as trigger
1 - 3	Reserved	-	
4	MinMaxStart01	0	No determination (bus controller default setting)
		1	Rising edge determines input value of channel 1
5	MinMaxStart02	0	No determination (bus controller default setting)
		1	A positive edge determines the input value of channel 2.
6 - 7	Reserved	0	

1.23.1.4.6.3 Analysis control byte

Name:
TraceTrigger01
MinMaxStart01 to MinMaxStart02

The trace function and determination of the minimum/maximum input values can be started in this register. Whether the rising and/or falling edge is used to trigger the functions can be configured using the registers "Trigger condition on falling edge" on page 617 and "Trigger condition on rising edge" on page 617.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	TraceTrigger01	0	Trigger/Trace not triggered (bus controller default setting)
		1	Initiates trigger/trace
1 - 3	Reserved	-	
4	MinMaxStart01	0	Determination not triggered (bus controller default setting)
		1	Initiates determination of input value of channel 1
5	MinMaxStart02	0	Determination not triggered (bus controller default setting)
		1	Initiates determination of input value of channel 2
6 - 7	Reserved	-	

Information:

To reduce the cyclic data transfer, this register combines the trace and limit value determination functions.

1.23.1.4.6.4 Analysis status byte

Name:
MinMaxStart01Readback to MinMaxStart02Readback

The currently requested module-internal analyses can be checked in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 3	Reserved	-	
4	MinMaxStart01Readback	0 or 1	Current state of the trigger bits for determining the limit values on channel 1
5	MinMaxStart02Readback	0 or 1	Current state of the trigger bits for determining the limit values on channel 2
6 - 7	Reserved	-	

1.23.1.4.7 Limit values

Limit value analysis must be enabled for the desired channel. See "Channel configuration" on page 610. The sampled value of the channel is then compared to the minimum and maximum values that are stored internally in the module. If a new measurement period is initiated with the "Analysis control byte" on page 618 register, then the values of the previous measurement period can be read from the respective registers intended for this.

1.23.1.4.7.1 Maximum input values

Name:
MaxInput01 to MaxInput02

The maximum value of the preceding trigger period is saved in this register based on the filtered, scaled and user-defined limit values. The register value is 0 if the channel is inactive.

Data type	Value
INT	-32,768 to 32,767

1.23.1.4.7.2 Minimum input values

Name:
MinInput01 to MinInput02

The minimum value of the preceding trigger period is saved in this register based on the filtered, scaled and user-defined limit values. The register value is 0 if the channel is inactive.

Data type	Value
INT	-32,768 to 32,767

1.23.1.4.7.3 Limit value trigger counter

Name:
Ch01MinMaxLatchCounter to Ch02MinMaxLatchCounter

The number of valid events that trigger a new measurement period for the limit value analysis is counted in this register.

Data type	Value
UINT	0 to 65535

1.23.1.4.8 Trace

If the module is operated on a type SG4 controller, the digitized input values can be recorded by the module. Module monitoring must be enabled to use measured value recording.

Recording must be enabled for the desired channel. The enable bits can then control the recording at runtime. The sampled values are recorded in the module's internal FIFO memory.

If the previously defined state occurs on the channel, the contents of the FIFO memory are transmitted to the application. Whether the FIFO memory continued to be filled depends on how recording is configured.

Information:

The trace mechanism cannot be used if the module is operated behind a bus controller, but only when it is directly connected to the controller.

1.23.1.4.8.1 Enable recording

Name:
TraceChannelEnable

The respective channel is enabled for the trace with this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Channel disabled
		1	Channel enabled
1	Channel 2	0	Channel disabled
		1	Channel enabled
2 - 7	Reserved	-	

1.23.1.4.8.2 Number of values to be recorded

Name:
TraceSampleDepth

16 kB are available on the module for the trace. The FIFO memory limitation means that a maximum of 8192 analog values can be recorded. This memory is divided up equally among the enabled channels. The actual number of maximum possible recordings therefore depends on the number of channels enabled for trace:

1 channel enabled: Up to 8192 recordings
2 channels enabled: Up to 4096 recordings per channel

Data type	Value	Function
UINT	2 to 8192	Default value = 1024

1.23.1.4.8.3 Recording priority

Name:
ConfigOutput25

The priority of the trace can be increased with this register.

Data type	Value	Function
USINT	3	Standard
	6	Trace priority higher than X2X Link communication

1.23.1.4.8.4 Starting a recording

Name:

TraceEnable01

This register starts the recording according to the specifications for edge control or the comparator.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	TraceEnable01	0	Disables the trace function
		1	Enables the trace function
1 - 7	Reserved	-	

1.23.1.4.8.5 Recording status

Name:
TraceEnabled
TraceWriteActive
TraceReadActive
ReadyForTrigger
TriggerActive
TraceOk
TraceError

The status of the trace is represented in this register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	TraceEnabled	0	Trace inactive
		1	Trace active
1	Reserved	-	
2	TraceWriteActive	0	Data not recorded
		1	Data recorded
3	TraceReadActive	0	Data not output/read
		1	Data output/read
4	ReadyForTrigger	0	Not ready for triggering
		1	Ready for triggering
5	TriggerActive	0	No trigger active or already executed
		1	Trigger active
6	TraceOk	0	Overflow or inactive
		1	No overflow
7	TraceError	0	No error or inactive
		1	Trace buffer full

1.23.1.4.8.6 Free trace buffer

Name:
FreeBufferSize

Specifies the available FIFO memory area in bytes for the trace

Data type	Values
UINT	0 to 65,535

1.23.1.4.8.7 Counter for trace triggers

Name:
TriggerCount

The number of trigger events that have occurred since starting the trace is indicated in this register.

Data type	Values
UINT	0 to 65,535

1.23.1.4.8.8 Counter for faulty recording triggers

Name:
TriggerFailCount

Counts the trigger events for which the trace could not be performed.

Data type	Values
UINT	0 to 65,535

1.23.1.4.8.9 Comparator for trigger conditions

In order to adapt the trace as closely as possible to the requirements of the application, the trace function can also be controlled using the comparator. Threshold values (hysteresis) can be defined within the permitted range of values to do so. 2 status bits are then generated for each enabled channel:

- **InRange bit**
  The InRange status is "1" if the measured value falls within the defined limits.
  The InRange status is "0" if the measured value falls outside the defined limits.
- **Threshold value bit**
  The threshold value bit is "1" if the measured value exceeds the upper threshold value.
  The threshold value bit is "0" if the measured value falls below the lower threshold value.

The InRange and threshold value bits for all channels are grouped together in the lower-value byte of the "CompStateCollection" on page 623 register. In addition, the states of the previous sampling are stored in the higher-value byte.

The 4 status messages of each channel can be linked according to the following logic via a logical connective mask using AND or OR operators and used as a trace trigger:

```
delta = (Current_HysteresisStatus ^ NominalValues)// Difference between current status and preset
cond = delta & Selected_HysteresisStatusBits// Eliminate irrelevant status messages
cond = Selected_HysteresisStatusBits (Current_HysteresisStatus ^ NominalValues)
if((0==(cond & ~LogicalOperators)) &&
(0!=(~cond & LogicalOperators))) {=> Generate trigger event}
```

	Corresponds to register:
Selected_HysteresisStatusBits	"cfgComp_EnableMask" on page 624
Current_HysteresisStatus	"CompStateCollection" on page 623
Nominal values	"cfgComp_NominalState" on page 624
Logical operators	"cfgComp_ConditionTypeMask" on page 625

Lower limit value for hysteresis

Name:
cfgComp_LowLimitCh01 to cfgComp_LowLimitCh02

The lower limit value for hysteresis is configured in this register.

Data type	Values
INT	-32768 to 32767

Upper limit value for hysteresis

Name:
cfgComp_HighLimitCh01 to cfgComp_HighLimitCh02

The upper limit value for hysteresis is configured in this register.

Data type	Values
INT	-32768 to 32767

Hysteresis status of the channels

Name:
CompStateCollection

The hysteresis status of the input channels for the current and last cycle are represented in this register.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
1	Channel01 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
2	Channel02 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
3	Channel02 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
4 - 7	Reserved	-	
8	Channel01 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
9	Channel01 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
10	Channel02 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
11	Channel02 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
12 - 15	Reserved	-	

Comparison state of the channels

Name:
cfgComp_NominalState

The desired comparison state for the hysteresis status is indicated in this register.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
1	Channel01 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
2	Channel02 hysteresis status in the current cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
3	Channel02 InRange status in the current cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
4 - 7	Reserved	-	
8	Channel01 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
9	Channel01 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
10	Channel02 hysteresis status in the last cycle	0	Lower limit value exceeded
		1	Upper limit value exceeded
11	Channel02 InRange status in the last cycle	0	Value lies outside of range defined by the limit values
		1	Value between lower and upper limit values
12 - 15	Reserved	-	

Information:

This is a "whitelist", i.e. the trace starts as soon as the current status message takes on the state predefined here.

One or more matches will be necessary depending on the selection of the relevant hysteresis status bits and logical connective operators.

Selecting the relevant hysteresis status bits

Name:
cfgComp_EnableMask

This register selects which status bits of the hysteresis comparison should be used to generate the trigger.

For more information about using this register, see "Comparator for trigger conditions" on page 622.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Do not use
		1	Use for generation
1	Channel01 InRange status in the current cycle	0	Do not use
		1	Use for generation
2	Channel02 hysteresis status in the current cycle	0	Do not use
		1	Use for generation
3	Channel02 InRange status in the current cycle	0	Do not use
		1	Use for generation
4 - 7	Reserved	-	
8	Channel01 hysteresis status in the last cycle	0	Do not use
		1	Use for generation
9	Channel01 InRange status in the last cycle	0	Do not use
		1	Use for generation
10	Channel02 hysteresis status in the last cycle	0	Do not use
		1	Use for generation
11	Channel02 InRange status in the last cycle	0	Do not use
		1	Use for generation
12 - 15	Reserved	-	

Logical connective operators for hysteresis status bits

Name:
cfgComp_ConditionTypeMask

The desired state operators with which the status bits are linked to one another to generate a trigger are selected in this register.

At least one OR operation must be configured, but it does not necessarily have to be located on a channel configured with "1" in the "cfgComp_EnableMask" on page 624 register.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Channel01 hysteresis status in the current cycle	0	Use AND operation
		1	Use OR operation
1	Channel01 InRange status in the current cycle	0	Use AND operation
		1	Use OR operation
2	Channel02 hysteresis status in the current cycle	0	Use AND operation
		1	Use OR operation
3	Channel02 InRange status in the current cycle	0	Use AND operation
		1	Use OR operation
4 - 7	Reserved	-	
8	Channel01 hysteresis status in the last cycle	0	Use AND operation
		1	Use OR operation
9	Channel01 InRange status in the last cycle	0	Use AND operation
		1	Use OR operation
10	Channel02 hysteresis status in the last cycle	0	Use AND operation
		1	Use OR operation
11	Channel02 InRange status in the last cycle	0	Use AND operation
		1	Use OR operation
12 - 15	Reserved	-	

1.23.1.4.8.10 Time-offset trace

Additional conditions for shifting the starting and stopping points can be defined if the trace should be chronologically offset to the trigger.

Starting the trace

Name:
TraceTriggerStart

The starting position is defined relative to the configured trigger condition in this register. Positive values mean that the trace takes place x samples after the trigger condition. Negative values mean that the trace takes place x samples before the trigger condition.

The value -32768 performs the trace without regard for the configured trigger condition. If the trace memory is completely full, then the oldest recorded value is overwritten (FIFO principle).

"Trace start" in the I/O configuration or the registers "Trigger condition on falling edge" on page 617 and "Trigger condition on rising edge" on page 617 determine whether a positive, negative or any edge must be triggered.

Data type	Value	Information
INT	-32767 to 32767	
	-32768	Continuous trace without a stopping point

Stopping the trace

Name:
TraceTriggerStop

The stopping position is defined relative to the configured trigger condition in this register.

- When configuring an early trigger event, this value refers to the trigger event.
- When configuring a delayed trigger event, this value refers to the starting event.

Data type	Values
UINT	0 to 65,535

1.23.1.4.9 Acyclic frame size

Name:
AsynSize

When using the stream, the data is exchanged internally between the module and controller. A defined number of acyclic bytes is reserved for this slot for this purpose.
Increasing the acyclic frame size results in increased data throughput on this slot.

Information:

This configuration involves a driver setting that cannot be changed during runtime!

Data type	Values	Information
-	8 to 28	Acyclic frame size in bytes. Default = 24

1.23.1.4.10 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time	
Standard priority	200 µs
High priority with trace function	300 µs

1.23.1.4.11 Minimum I/O update time

There is no limitation or dependency on the bus cycle time.

The I/O update time is defined using the "Sampling time" register. The fastest possible sampling time depends on the number of channels to be converted and the configuration.

1.24 Safety module

1.24.1 X20(c)SA4430

Information:

B&R makes every effort to keep data sheets as current as possible. From a safety point of view, however, the current version of the data sheet must always be used.
The certified, currently valid data sheet is available for download on the B&R website (www.br-automation.com).

Information:

This data sheet must be used with mapp Safety.
B&R safety technology can still be used in Safety Releases ≤1.10, however. The documentation is available for download on the B&R website (www.br-automation.com).

For additional information about mapp Safety, additional technical descriptions (e.g. connection examples and error detection) as well as generally valid contents (intended use, etc.), see section Safety technology in Automation Help.

Organization of notices

Safety notices

Contain **only** information that warns of dangerous functions or situations.

Signal word	Description
Danger!	Failure to observe these safety guidelines and notices will result in death, severe injury or substantial damage to property.
Warning!	Failure to observe these safety guidelines and notices can result in death, severe injury or substantial damage to property.
Caution!	Failure to observe these safety guidelines and notices can result in minor injury or damage to property.
Notice!	Failure to observe these safety guidelines and notices can result in damage to property.

Table 83: Organization of safety notices

General notices

Contain **useful** information for users and instructions for avoiding malfunctions.

Signal word	Description
Information:	Useful information, application tips and instructions for avoiding malfunctions.

Table 84: Organization of general notices

1.24.1.1 General information

The modules are equipped with 2 safe analog input pairs for current measurement. Each input pair has its own sensor power supply. The channels with their respective sensor supplies are galvanically isolated from each other. It is possible to acquire current signals in the range of 0.5 to 25 mA.

The safe analog input modules are suitable for safely acquiring current signals for safety-related applications up to PL e or SIL 3.

These modules are designed for X20 16-pin terminal blocks.

- 2 safe analog input pairs for current measurement 0.5 to 25 mA
- 24-bit digital converter resolution
- Channels individually galvanically isolated
- Sensor power supplies galvanically isolated
- Input filter configurable

1.24.1.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation.
The modules' electronics are fully compatible with the corresponding X20 modules.

Information:

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, Method 4, exposure 21 days

Contrary to the specifications for X20 system modules without safety certification and despite the tests performed, X20 safety modules are **NOT suited for applications with corrosive gases (EN 60068-2-60)!**

1.24.1.2.1 Starting temperature

The starting temperature describes the minimum permissible ambient temperature in a voltage-free state at the time the coated module is switched on. This is permitted to be as low as -40°C. During operation, the conditions as specified in the technical data continue to apply.

Information:

It is important to absolutely ensure that there is no forced cooling by air currents in the closed control cabinet, e.g. due to the use of a fan or ventilation slots.

1.24.1.3 Order data

Order number	Short description	Figure
	Analog input modules	
X20SA4430	X20 safe current input module, 2x 2 safe type A analog inputs, 0.5 to 25 mA, channels individually galvanically isolated, configurable input filter and switching thresholds	
X20cSA4430	X20 safe current input module, coated, 2x 2 safe type A analog inputs, 0.5 to 25 mA, channels individually galvanically isolated, configurable input filter and switching thresholds	
	Required accessories	
	Bus modules	
X20BM33	X20 bus module, for X20 SafeIO modules, internal I/O power supply connected through	
X20BM36	X20 bus module, for X20 SafeIO modules, with node number switch, internal I/O power supply connected through	
X20cBM33	X20 bus module, coated, for X20 SafeIO modules, internal I/O power supply connected through	
	Terminal blocks	
X20TB5F	X20 terminal block, 16-pin, safety-keyed	

Table 85: X20SA4430, X20cSA4430 - Order data

1.24.1.4 Technical data

Order number	X20SA4430	X20cSA4430
Short description		
I/O module	2x 2 safe type A analog inputs, 0.5 to 25 mA, channels individually galvanically isolated	
General information		
B&R ID code	0xB8B5	0xDD9F
System requirements		
Automation Studio	3.0.81.15 or later	4.0.16 or later
Automation Runtime	3.00 or later	V3.08 or later
SafeDESIGNER	2.81 or later	3.1.0 or later
Safety Release	1.4 or later	1.7 or later
mapp Technology Package [1]	mapp Safety 5.7.0 or later	
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using LED status indicator and software	
Inputs	Yes, using LED status indicator and software	
Blackout mode		
Scope	Module	
Function	Module functionality	
Standalone mode	No	
Max. I/O cycle time	2 ms	
Power consumption		
Bus	0.25 W	
Internal I/O	1.7 W	
Additional power dissipation caused by actuators (resistive) [W] [2]	0.36	
Electrical isolation		
Channel - Bus	Yes	
Channel - Channel	Yes	
Channel pair - Channel pair	Yes	
Certifications		
CE	Yes	
UKCA	Yes	
Functional safety	cULus FSPC E361559 Energy and industrial systems Certified for functional safety ANSI UL 1998:2013	
Functional safety	IEC 61508:2010, SIL 3 EN 62061:2005/A2:2015, SIL 3 EN ISO 13849-1:2015, Cat. 4 / PL e IEC 61511:2004, SIL 3	
Functional safety	EN 50156-1:2004	
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X	
UL	cULus E115267 Industrial control equipment	
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5	
DNV	Temperature: **A** (0 to 45°C) Humidity: **B** (up to 100%) Vibration: **A** (0.7 g) EMC: **B** (bridge and open deck)	
LR	ENV1	
KR	Yes	
ABS	Yes	
BV	**EC21B** Temperature: 5 - 45°C Vibration: 0.7 g EMC: Bridge and open deck	
EAC	Yes	-
KC	Yes	-
Safety characteristics		
Note	The following characteristic values apply only to the use of input channel pairs. Assessing the channels from a safety point of view when they are used individually is not possible. [3]	
EN ISO 13849-1:2015		
Category	Cat. 4 (SHUNTTEST enabled), Cat. 3 (SHUNTTEST disabled)	
PL	PL e (SHUNTTEST enabled), PL d (SHUNTTEST disabled)	
DC	>94% (regardless of whether SHUNTTEST is enabled or disabled)	
MTTFD per channel	2200 years (regardless of whether SHUNTTEST is enabled or disabled)	
Mission time	Max. 20 years	

Table 86: X20SA4430, X20cSA4430 - Technical data

Order number	X20SA4430	X20cSA4430
IEC 61508:2010, IEC 61511:2004, EN 62061:2013		
SIL CL	SIL 3 (regardless of whether SHUNTTEST is enabled or disabled)	
SFF	>90% (regardless of whether SHUNTTEST is enabled or disabled)	
PFH / PFH_d per channel	$<1*10^{-9}$ (regardless of whether SHUNTTEST is enabled or disabled)	
PFH / PFH_d		
openSAFETY wired	Negligible	
openSAFETY wireless	$<1*10^{-14}$ * Number of openSAFETY packets per hour	
PFD per channel	$<1*10^{-4}$ (regardless of whether SHUNTTEST is enabled or disabled)	
Proof test interval (PT)	20 years	
I/O power supply		
Nominal voltage	24 VDC	
Voltage range	24 VDC -15% / +20%	
Safe analog inputs		
Quantity	2 safe input channel pairs	
Variant	Type A	
Input type	Differential input	
Digital converter resolution	24-bit	
Conversion time	See chapter "I/O update time".	
Output format	SAFEINT	
Load	Up to hardware revision D3: 230 to 420 Ω, hardware revision E0 or later: 185 to 245 Ω	
Input protection	Protection against external supply voltages and overcurrent	
Open-circuit detection	Yes, using software	
Permissible input signal		
Voltage	Max. 30.5 V	
Conversion procedure	Sigma-delta	
Max. error at 25°C		
Gain		
0.5 to <4 mA	<0.3% [4)]	
4 to 25 mA	<0.08% [4)]	
Offset		
0.5 to <4 mA	<2 µA	
4 to 25 mA	<6.3 µA	
Max. gain drift		
0.5 to <4 mA	<1.225 µA/°C	
4 to 25 mA	<1.225 µA/°C	
Max. offset drift		
0.5 to <4 mA	<0.735 µA/°C	
4 to 25 mA	<0.735 µA/°C	
Common-mode rejection		
DC	>70 dB	
50 Hz	>70 dB	
Common-mode range	Between the inputs ±50 V	
Nonlinearity	<0.003%	
Measurement range	0.5 to 25 mA	
Input filter		
Hardware	First-order low-pass filter / cutoff frequency 500 Hz	
Software	$Sinc^3$ filter	
Resolution	1 µA/LSB	
Overload detection	Yes, using software	
Test voltage		
Channel - Bus	500 VDC	
Channel pair - Channel pair	500 VDC	
Channel - Ground	500 VDC	
Safety-related accuracy per channel		
Cat. 3	0.184 mA	
Cat. 4	0.49 mA	
Filter time	Configurable between 1 and 66.7 ms	
Sensor power supply		
Nominal voltage	29 VDC ±5%	
Nominal output current	Max. 60 mA	
Short-circuit proof	Yes, continuous	
Electrical isolation		
Sensor power supply - Channel	No	
Sensor power supply - Sensor power supply	Yes	
$R_{DS(on)}$	50 Ω	
Behavior on short circuit	Voltage cutoff	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation elevation above sea level	0 to 2000 m, no limitation	

Table 86: X20SA4430, X20cSA4430 - Technical data

Order number	X20SA4430	X20cSA4430
Degree of protection per EN 60529	IP20	
Ambient conditions		
Temperature		
Operation		
Horizontal mounting orientation	0 to 60°C	-25 to 60°C
Vertical mounting orientation	0 to 40°C	-25 to 40°C
Derating	See section "Derating".	
Starting temperature	-	Yes, -40°C
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical properties		
Note	Order 1x safety-keyed terminal block separately. Order 1x safety-keyed bus module separately.	
Pitch	$25^{+0.2}$ mm	

Table 86: X20SA4430, X20cSA4430 - Technical data

1) The system requirements of the mapp Technology Package must be observed (see Automation Help).
2) Number of outputs x $R_{DS(on)}$ x Nominal output current². This value also applies to sensors that are supplied via these outputs. For a calculation example, see section "Mechanical and electrical configuration" in the X20 system user's manual.
3) In addition, the danger notices in the technical data sheet and section "Safety technology" in Automation Help must be observed.
4) Based on the current measured value

Derating

Only modules with a maximum power consumption of 1 W are permitted to be operated next to the X20SA4430. Starting at 50°C (horizontal mounting orientation) and 35°C (vertical mounting orientation), a dummy module must be connected to the left and right of the X20SA4430.

	Number of usable signal pairs
Horizontal mounting orientation up to 50°C	2
Horizontal mounting orientation up to 55°C	1
Vertical mounting orientation up to 35°C	2
Vertical mounting orientation from 35 to 40°C	1

Table 87: Derating in relation to operating temperature and mounting orientation

Danger!

Operation outside the technical data is not permitted and can result in dangerous states.

Information:

For additional information about installation, see section "Installation notes for X20 modules" in Automation Help.

1.24.1.5 LED status indicators

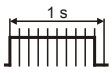
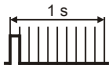
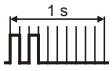
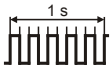
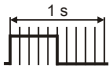
Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	Mode "Reset"
			Double flash	Updating firmware
			Blinking	Mode PREOPERATIONAL
			On	Mode RUN
	e	Red	Off	Module not supplied with power or everything OK
			Pulsating	Bootloader mode
			Triple flash	Updating safety-related firmware
			On	Error or I/O component not provided with voltage
	e + r	Solid red / Single green flash		Invalid firmware
	1 to 4	Input state of the corresponding analog input		
		Red	On	Warning/Error on an input channel
			Blinking	Open circuit on corresponding channel
			All on	Error on all channels, connection to the SafeLOGIC controller not OK or startup not yet completed
		Green	On	Channel being used and signal OK
			Blinking	Channel outside of the limits configured in SafeDESIGNER
			Off	Channel not used
	12, 34	Input state of the corresponding analog input channel pair		
		Red	On	Warning/Error on this channel pair
			All on	Error on all channels, connection to the SafeLOGIC controller not OK or startup not yet completed
		Green	On	Signal on channel pair OK
			Off	Signal on channel pair not OK
	SE	Red	Off	Mode RUN or I/O component not provided with voltage
				Boot phase, missing X2X Link or defective processor
				Safety PREOPERATIONAL state Modules that are not used in the SafeDESIGNER application remain in state PREOPERATIONAL.
				Safe communication channel not OK
				The firmware for this module is a non-certified pilot customer version.
				Boot phase, faulty firmware
			On	Safety state active for the entire module (= state "FailSafe")
		The "SE" LEDs separately indicate the status of safety processor 1 ("S" LED) and safety processor 2 ("E" LED).		

Table 88: Status indicators

Danger!

Constantly lit "SE" LEDs indicate a defective module that must be replaced immediately.
It is your responsibility to ensure that all necessary repair measures are initiated after an error occurs since subsequent errors can result in a hazard!

1.24.1.6 Pinout

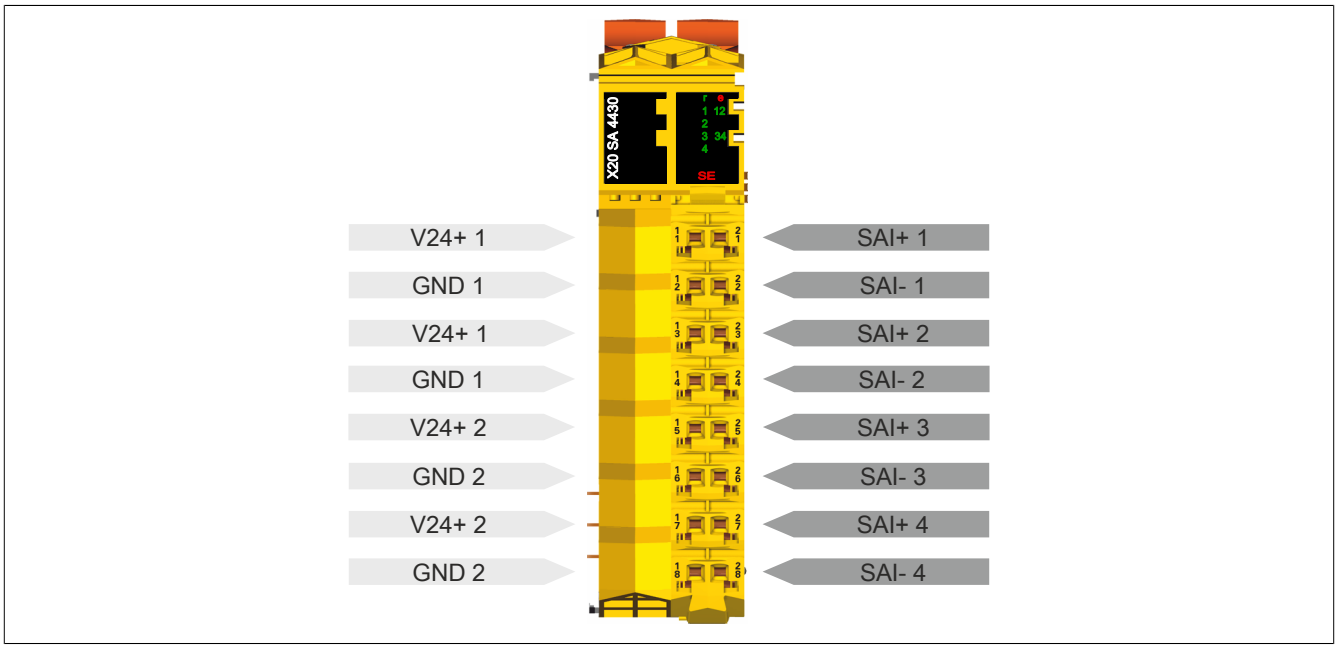


Figure 76: X20SA4430 - Pinout

1.24.1.7 Input circuit diagram

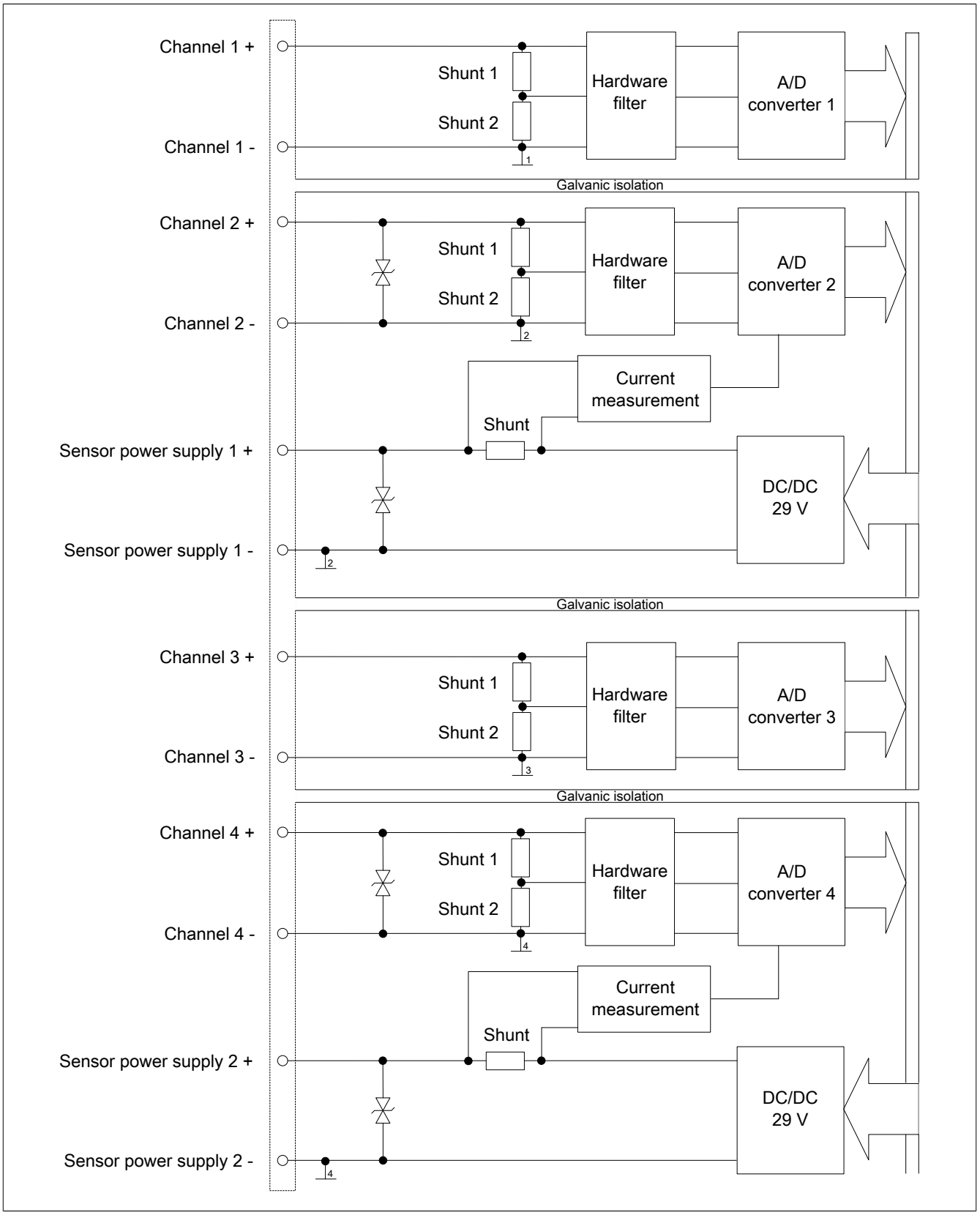


Figure 77: Input circuit diagram

1.24.1.8 Register description

1.24.1.8.1 Parameters in the I/O configuration

Group: Function model

Parameter	Description	Default value	Unit
Function model	This parameter is reserved for future functional expansions.	Default	-

Table 89: I/O configuration parameters: Function model

Group: General

Parameter	Description	Default value	Unit
Module supervised	System behavior when a module is missing	On	-
	Parameter value / **Description** On – A missing module triggers service mode. Off – A missing module is ignored.		
Blackout mode	This parameter enables blackout mode (see section Blackout mode in Automation Help under: Hardware → X20 system → Additional information → Blackout mode).	Off	-
	Parameter value / **Description** On – Blackout mode is enabled. Off – Blackout mode is disabled.		
SafeDOMAIN ID	In applications with multiple SafeLOGIC controllers, this parameter defines the module's association with a particular SafeLOGIC controller. • Permissible values: 1 to 1000	Assigned automatically	-
SafeNODE ID	Unique safety address of the module • Permissible values: 2 to 1023	Assigned automatically	-

Table 90: I/O configuration parameters: General

1.24.1.8.2 Parameters in SafeDESIGNER

Group: Basic

Parameter	Description	Default value	Unit
Min. required firmware revision	This parameter is reserved for future functional expansions.	Basic release	-
Availability	This parameter can be used to configure the module as "optional". Optional modules do not have to be present, i.e. the SafeLOGIC controller will not indicate that these modules are not present. However, this parameter does not influence the module's signal or status data.	Permanent	-

Parameter value	Description
Permanent	This module is mandatory for the application. The module must be in OPERATIONAL mode after startup, and safe communication with the SafeLOGIC controller must be established without errors (SafeModuleOK = SAFETRUE). Processing of the safety application on the SafeLOGIC controller is delayed after startup until this state is achieved for all modules with "Availability = Permanent". After startup, module problems are indicated by a quickly blinking "MXCHG" LED on the SafeLOGIC controller. An entry is also made in the logbook.
Optional	The module is not required for the application. The module is not taken into account during startup, which means the safety application is started regardless of whether the modules with "Availability = Optional" are in OPERATIONAL mode or if safe communication is properly established between these modules and the SafeLOGIC controller. After startup, module problems are NOT indicated by a quickly blinking "MXCHG" LED on the SafeLOGIC controller. An entry is NOT made in the logbook.
Startup	This module is optional. The system determines how the module will proceed during startup. If it is determined that the module is physically present during startup (regardless of whether it is in OPERATIONAL mode or not), then the module behaves as if "Availability = Permanent" is set. If it is determined that the module is not physically present during startup, then the module behaves as if "Availability = Optional" is set.
Never	The module is not required for the application. The module is not taken into account during startup, which means the safety application is started regardless of whether the modules with "Availability = Never" are physically present. Unlike when "Availability = Optional" is configured, the module is not started with "Availability = Never", which optimizes system startup behavior. After startup, module problems are NOT indicated by a quickly blinking "MXCHG" LED on the SafeLOGIC controller. An entry is NOT made in the logbook.

Table 91: SafeDESIGNER parameters: Basic

Group: Safety response time

Parameter	Description	Default value	Unit
Manual configuration	This parameter makes it possible to manually and individually configure the safety response time for the module. The parameters for the safety response time are generally set in the same way for all stations involved in the application. For this reason, these parameters are configured for the SafeLOGIC controller in SafeDESIGNER. For application situations in which individual safety functions require optimal response time behavior, the parameters for the safety response time can be configured individually on the respective module.	No	-
	Parameter value / **Description** Yes: Data from the module's "Safety response time" group is used to calculate the safety response time for the module's signals. No: The parameters for the safety response time are taken from the "Safety response time" group on the SafeLOGIC controller.		
Safe data duration	This parameter specifies the maximum permissible data transmission time between the SafeLOGIC controller and SafeIO module. For additional information about the actual data transmission time, see section Diagnostics and service → Diagnostics tools → Network analyzer → Editor → Calculation of safety runtime in Automation Help. The following formula can be used as the lower limit: "Value of the Network Analyzer" * 2 + SafeLOGIC cycle time * 2 The stability of the system cannot be ensured for smaller values. • Permissible values: 2000 to 10,000,000 µs (corresponds to 2 ms to 10 s)	20000	µs
Additional tolerated packet loss	This parameter specifies the number of additional tolerated lost packets during data transfer. • Permissible values: 0 to 10	1	Packets
Node guarding packets	This parameter specifies the maximum number of packets used for node guarding. • Permissible values: 1 to 255 **Note** • The larger the configured value, the greater the amount of asynchronous data traffic. • This setting is not critical to safety functionality. The time for safely cutting off actuators is determined independently of this.	5	Packets

Table 92: SafeDESIGNER parameters: Safety response time

Group: Module configuration

Parameter	Description	Default value	Unit
Input filter	This parameter sets the filter time of A/D converters. • Permissible values: 1 ms, 2 ms, 10 ms, 16.7 ms, 20 ms, 33.3 ms, 40 ms, 66.7 ms	1	ms
Disable shunt test	This parameter can be used to disable automatic testing of the measurement shunts for all of the module's channels. This increases the tolerance of the module in relation to the interference on the input signal.	No	-
	Parameter value / **Description** Yes - Warning: Automatic testing of the measurement shunts is disabled ("Yes - Warning" = SHUNTTEST disabled). No: Automatic testing of the measurement shunts is not disabled ("No" = SHUNTTEST enabled).		

Table 93: SafeDESIGNER parameters: Module configuration

Danger!

With "Disable shunt test = Yes - Warning", the module has reduced error detection capabilities and no longer meets the requirements of Cat. 4 per EN ISO 13849-1:2015.
As a result, the module meets the requirements up to max. Cat. 3 per EN ISO 13849-1:2015.

Group: SafeCurrentxxyy

Parameter	Description	Default value	Unit
Limit threshold equivalent x	This parameter specifies the maximum permissible deviation between the analog input values. • Permissible values: 0 to 25,000 µA (corresponds to 0 to 25 mA)	100	µA
Discrepancy time x	This parameter specifies the maximum time for the "Dual-channel evaluation" function in which the difference between both analog input values is permitted to exceed the limit value. • Permissible values: 0 to 10,000 ms (corresponds to 0 to 10 s)	0	ms

Table 94: SafeDESIGNER parameters: SafeCurrentxxyy

Parameters "Limit threshold equivalent x" and "Discrepancy time x" together form a parameter set. Channels "SafeThresholdSelector_xxyy_Bit1" and "SafeThresholdSelector_xxyy_Bit2" are available in the SafeDESIGNER application to determine which parameter set in the module is enabled, i.e. it is possible to change the parameter set at runtime.

1.24.1.8.3 Channel list

<table>
<tr><th>Channel name</th><th>Access via Automation Studio</th><th>Access via SafeDESIGNER</th><th>Data type</th><th>Description</th></tr>
<tr><td>ModuleOk</td><td>Read</td><td>-</td><td>BOOL</td><td>Indicates whether the module is physically present in the slot and configured</td></tr>
<tr><td>SerialNumber</td><td>Read</td><td>-</td><td>UDINT</td><td>Module serial number</td></tr>
<tr><td>ModuleID</td><td>Read</td><td>-</td><td>UINT</td><td>Module ID</td></tr>
<tr><td>HardwareVariant</td><td>Read</td><td>-</td><td>UINT</td><td>Hardware variant</td></tr>
<tr><td>FirmwareVersion</td><td>Read</td><td>-</td><td>UINT</td><td>Firmware version of the module</td></tr>
<tr><td>UDID_low</td><td>(Read) 1)</td><td>-</td><td>UDINT</td><td>UDID, lower 4 bytes</td></tr>
<tr><td>UDID_high</td><td>(Read) 1)</td><td>-</td><td>UINT</td><td>UDID, upper 2 bytes</td></tr>
<tr><td>SafetyFWversion1</td><td>(Read) 1)</td><td>-</td><td>UINT</td><td>Firmware version - Safety processor 1</td></tr>
<tr><td>SafetyFWversion2</td><td>(Read) 1)</td><td>-</td><td>UINT</td><td>Firmware version - Safety processor 2</td></tr>
<tr><td>SafetyFWcrc1</td><td>(Read) 1)</td><td>-</td><td>UINT</td><td>CRC of the firmware header on safety processor 1</td></tr>
<tr><td>SafetyFWcrc2</td><td>(Read) 1)</td><td>-</td><td>UINT</td><td>CRC of the firmware header on safety processor 2</td></tr>
<tr><td>Bootstate</td><td>(Read) 1)</td><td>-</td><td>UINT</td><td>Startup state of the module.
Notes:
• Some of the boot states do not occur during normal startup or are cycled through so quickly that they are not visible externally.
• The boot states usually cycle through in ascending order. There are cases, however, in which a previous value is captured.
<table><tr><th>Value</th><th>Description</th></tr><tr><td>0x0003</td><td>Startup communication processor OK, no communication with the safety processors (check 24 V supply voltage!)</td></tr><tr><td>0x0010</td><td>FAILSAFE. At least one of the safety processors is in the safe state.</td></tr><tr><td>0x0020</td><td>Internal communication with safety processors started</td></tr><tr><td>0x0024</td><td>Firmware update of safety processors</td></tr><tr><td>0x0040</td><td>Firmware of safety processors started</td></tr><tr><td>0x0440</td><td>Firmware of safety processors running</td></tr><tr><td>0x0840</td><td>Waiting for openSAFETY "Operational" (loading the SafeDESIGNER application or no valid application available; waiting for acknowledgments such as module replacement)</td></tr><tr><td>0x1040</td><td>Evaluating the configuration according to the SafeDESIGNER application</td></tr><tr><td>0x3440</td><td>Stabilizing cyclic openSAFETY data exchange.
Note:
If the boot state remains here, SafeDESIGNER parameters "(Default) Safe data duration" and "(Default) Additional tolerated packet loss" must be checked.</td></tr><tr><td>0x4040</td><td>RUN. Final state, startup completed.</td></tr></table></td></tr>
<tr><td>Diag1_Temp</td><td>(Read) 1)</td><td>-</td><td>INT</td><td>Module temperature in °C</td></tr>
<tr><td>oS_PropDelayStat (hardware upgrade 2.3.0.0 or later)</td><td>(Read) 1)</td><td>-</td><td>UDINT</td><td>Propagation delay statistics (average value of the data transmission time).
The unit depends on parameter "Process data transfer rate" of the SafeLOGIC controller.
• If the value of the parameter is "High", the unit is 100 µs.
• If the value of the parameter is "Low", the unit is 1 ms.
This value corresponds to the measurement of the forward and return channels and thus twice the theoretical runtime that is determined by the Network Analyzer.</td></tr>
<tr><td>SafeModuleOK</td><td>Read</td><td>Read</td><td>SAFEBOOL</td><td>Indicates whether the safe communication channel is OK</td></tr>
<tr><td>SafeCurrentOKxx</td><td>Read</td><td>Read</td><td>SAFEBOOL</td><td>Status of current range evaluation of channel xx</td></tr>
<tr><td>SafeCurrentOKxxyy</td><td>Read</td><td>Read</td><td>SAFEBOOL</td><td>Status of dual-channel current evaluation of channel xxyy</td></tr>
<tr><td>TestActive</td><td>Read</td><td>Read</td><td>BOOL</td><td>Indication of an active channel test</td></tr>
<tr><td>EquivalentThresholdxxyy</td><td>(Read) 1)</td><td>-</td><td>UINT</td><td>Limit value "Limit threshold equivalent" currently in use (see "SafeDESIGNER parameters: SafeCurrentxxyy")</td></tr>
<tr><td>DiscrepancyTimeThresholdxxyy</td><td>(Read) 1)</td><td>-</td><td>UINT</td><td>Limit value "Discrepancy time" currently in use (see "SafeDESIGNER parameters: SafeCurrentxxyy")</td></tr>
<tr><td>SafeCurrentxxyy</td><td>Read</td><td>Read</td><td>SAFEINT</td><td>(Current channel xx + Current channel yy)/2
<table><tr><th>Values</th><th>Input signal</th></tr><tr><td>0 to 20000</td><td>Current signal 0 to 20 mA</td></tr></table></td></tr>
</table>

Table 95: Channel list

<table>
<tr><th>Channel name</th><th>Access via Automation Studio</th><th>Access via SafeDESIGNER</th><th>Data type</th><th>Description</th></tr>
<tr><td>Currentxx</td><td>Read</td><td>Read</td><td>INT</td><td>Current channel xx
<table><tr><th>Values</th><th>Input signal</th></tr><tr><td>0 to 20000</td><td>Current signal 0 to 20 mA</td></tr></table></td></tr>
<tr><td>SafeThresholdSelector_xxyy_Bit1</td><td>-</td><td>Write</td><td>SAFEBOOL</td><td rowspan="2"><table><tr><th>**_Bit1</th><th>**_Bit2</th><th>Parameters currently being used</th></tr><tr><td>0</td><td>0</td><td>Parameter set 1</td></tr><tr><td>1</td><td>0</td><td>Parameter set 2</td></tr><tr><td>0</td><td>1</td><td>Parameter set 3</td></tr><tr><td>1</td><td>1</td><td>Parameter set 4</td></tr></table></td></tr>
<tr><td>SafeThresholdSelector_xxyy_Bit2</td><td>-</td><td>Write</td><td>SAFEBOOL</td></tr>
<tr><td>SafeReleasexxyy</td><td>-</td><td>Write</td><td>SAFEBOOL</td><td>Release signal - Channel xxyy</td></tr>
</table>

Table 95: Channel list

1) This data is accessed in Automation Studio using library ASIOACC.

Danger!

The validity of analog signals is represented by the associated status signals. These binary status signals (data type SAFEBOOL) must also be evaluated each time the analog signals are used. A binary status signal with the status FALSE indicates an invalid value in the analog signal. In these situations, the analog signal is no longer permitted to be used for safety-related assessments.

1.24.1.9 Minimum cycle time

The minimum cycle time specifies the time up to which the bus cycle can be reduced without communication errors occurring.

Minimum cycle time
200 µs

1.24.1.10 I/O update time

The time needed by the module to generate a sample is specified by the I/O update time.

Configured filter	Maximum I/O update time
1 ms	17 ms
2 ms	19 ms
10 ms	35 ms
16.7 ms	50 ms
20 ms	55 ms
33.3 ms	82 ms
40 ms	95 ms
66.7 ms	122 ms

1.24.1.11 Version history

Version	Date	Comment
2.20	February 2024	Updated chapters 1.24.1.3 "Order data" and 1.24.1.4 "Technical data".
2.14	May 2022	• Chapter 1.24.1.4 "Technical data": – Safety characteristics: Editorial change for PFH / PFH_d – Updated DNV certification. • Updated chapter 1.24.1.12 "Declaration of conformity".
2.10	May 2021	Chapter 1.24.1.4 "Technical data": • Updated display of system requirements. • Safety characteristics: Updated footnote.
2.08	November 2020	Chapter 1.24.1.4 "Technical data": Safe analog inputs: Added number of channels.
2.07	August 2020	• Chapter 1.24.1.4 "Technical data": – General information: Added additional power dissipation caused by actuators (resistive) [W]. – Updated certifications. – Sensor power supply: Added $R_{DS(on)}$. • Editorial changes.
2.06	May 2020	• Chapter 1.24.1.2 "Coated modules": Added description of starting temperature. • Chapter 1.24.1.4 "Technical data": – Added footnote for system requirements. – Updated certifications. – Coated module: Updated operating temperature. – Coated module: Added starting temperature. • Chapter 1.24.1.8.3 "Channel list": Added channel "oS_PropDelayStat". • Editorial changes.
2.05	February 2020	Editorial changes.
2.04	November 2019	• Chapter 1.24.1.4 "Technical data": Updated certifications. • Editorial changes.
2.02	May 2019	First edition for mapp Safety

Table 96: Version history

1.24.1.12 Declaration of conformity

This document was originally written in the German language. The German edition therefore represents the original documentation in accordance with Machinery Directive 2006/42/EC. Documents in other languages should be interpreted as translations of the original documentation.

Product manufacturer:

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office@br-automation.com

Commercial register number: FN 111651 v
Commercial registry: Regional court Ried im Innkreis
UID number: ATU62367156
Legal structure: Limited liability company
Corporate headquarters: Municipality of Eggelsberg (Upper Austria)

Declarations of conformity for B&R products are available for download on the B&R website (www.br-automation.com).

Analog output modules

Data sheets

Version: **1.10 (March 2024)**
Order no.: **Analog output modules**

2.1 X20(c)AO2437

2.1.1 General information

The module is equipped with 2 current outputs with 16-bit digital converter resolution. The 2 channels are electrically isolated from each other. The user can select between the 3 output ranges 4 to 20 mA, 0 to 20 mA and 0 to 24 mA.

- 2 analog current outputs
- Electrically isolated analog channels
- 16-bit digital converter resolution

2.1.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, method 4, exposure 21 days

2.1.2.1 Starting temperature

The starting temperature describes the minimum permissible ambient temperature in a voltage-free state at the time the coated module is switched on. This is permitted to be as low as -40°C. During operation, the conditions as specified in the technical data continue to apply.

Information:

It is important to absolutely ensure that there is no forced cooling by air currents in the closed control cabinet, e.g. due to the use of a fan or ventilation slots.

2.1.3 Order data

Order number	Short description	Figure
	Analog outputs	
X20AO2437	X20 analog output module, 2 outputs, 4 to 20 mA / 0 to 20 mA or 0 to 24 mA, 16-bit converter resolution, single channel electrically isolated	
X20cAO2437	X20 analog output module, coated, 2 outputs, 4 to 20 mA / 0 to 20 mA or 0 to 24 mA, 16-bit converter resolution, single channel electrically isolated	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 97: X20AO2437, X20cAO2437 - Order data

2.1.4 Technical data

Order number	X20AO2437	X20cAO2437
Short description		
I/O module	2 analog outputs 4 to 20 mA, 0 to 20 mA or 0 to 24 mA	
General information		
B&R ID code	0xB785	0xE1F2
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using status LED and software	
Outputs	Yes, using status LED and software	
Power consumption		
Bus	0.05 W	
Internal I/O	1.6 W	
Additional power dissipation caused by actuators (resistive) [W]	-	
Certifications		
CE	Yes	
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X	
UL	cULus E115267 Industrial control equipment	
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5	
DNV GL	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)	
LR	ENV1	
KR	Yes	
EAC	Yes	
KC	Yes	-
Analog outputs		
Output	4 to 20 mA, 0 to 20 mA or 0 to 24 mA, configurable using software	
Digital converter resolution	16-bit	
Settling time on output change over entire range	2 ms to 20 s, configurable using software	
Data output rate	1 ms without ramp	
Max. error		
Gain		
4 to 20 mA	0.025% [1]	
0 to 20 mA	0.022% [1]	
0 to 24 mA	0.02% [1]	
Offset		
4 to 20 mA	0.025% [2]	
0 to 20 mA	0.022% [2]	
0 to 24 mA	0.02% [2]	
Output protection	Short circuit protection, overvoltage protection (up to 30 VDC)	
Open-circuit detection	Yes, using hardware and software	
Data format	INT	
Output format		
4 to 20 mA	INT 0x0000 to 0x7FFF / 1 LSB = 0x0001 = 488.281 nA	
0 to 20 mA	INT 0x0000 bis 0x7FFF / 1 LSB = 0x0001 = 610.352 nA UINT 0x0000 to 0xFFFF / 1 LSB = 0x0001 = 305.176 nA	
0 to 24 mA	INT 0x0000 to 0x5DC0 / 1 LSB = 0x0001 = 1000 nA	
Load per channel	Max. 600 Ω	
Short-circuit proof	Yes, continuous	
Output filter	Active 2nd-order low pass / cutoff frequency 4 kHz Configurable slew rate	
Max. gain drift		
4 to 20 mA	0.0055 %/°C [1]	
0 to 20 mA	0.005 %/°C [1]	
0 to 24 mA	0.005 %/°C [1]	
Max. offset drift		
4 to 20 mA	0.0035 %/°C [2]	
0 to 20 mA	0.002 %/°C [2]	
0 to 24 mA	0.002 %/°C [2]	
Error caused by load change [3]		
4 to 20 mA	0.14%	
0 to 20 mA	0.1%	
0 to 24 mA	0.1%	
Nonlinearity	<0.003% [4]	

Table 98: X20AO2437, X20cAO2437 - Technical data

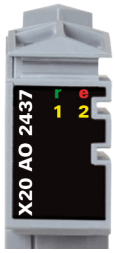
Order number	X20AO2437	X20cAO2437
Test voltage		
Channel - Channel	1000 VAC	
Channel - Bus	1000 VAC	
Channel - Ground	1000 VAC	
Electrical properties		
Electrical isolation	Channel isolated from channel and bus	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation elevation above sea level		
0 to 2000 m	No limitations	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
Degree of protection per EN 60529	IP20	
Ambient conditions		
Temperature		
Operation		
Horizontal mounting orientation	-25 to 60°C	
Vertical mounting orientation	-25 to 50°C	
Derating	See section "Derating"	
Starting temperature	-	Yes, -40°C
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical properties		
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Pitch	12.5$^{+0.2}$ mm	

Table 98: X20AO2437, X20cAO2437 - Technical data

1) Based on the current output value.
2) Based on the respective output range
3) Load change from 1 Ω → 600 Ω, resistive
4) Based on the entire output range.

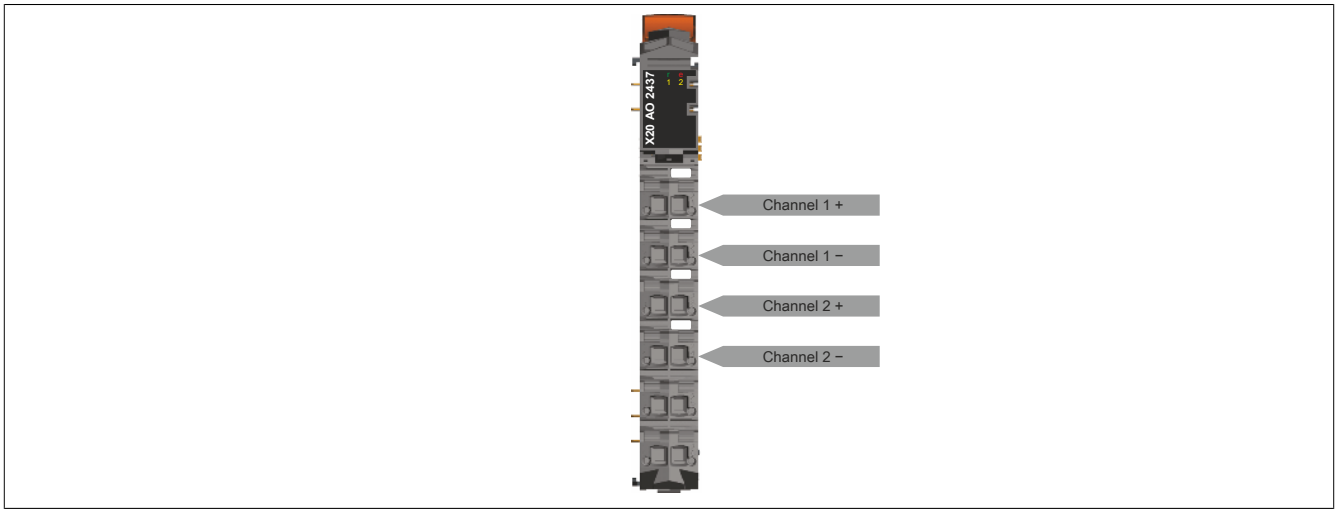
2.1.5 LED status indicators

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 system user's manual.

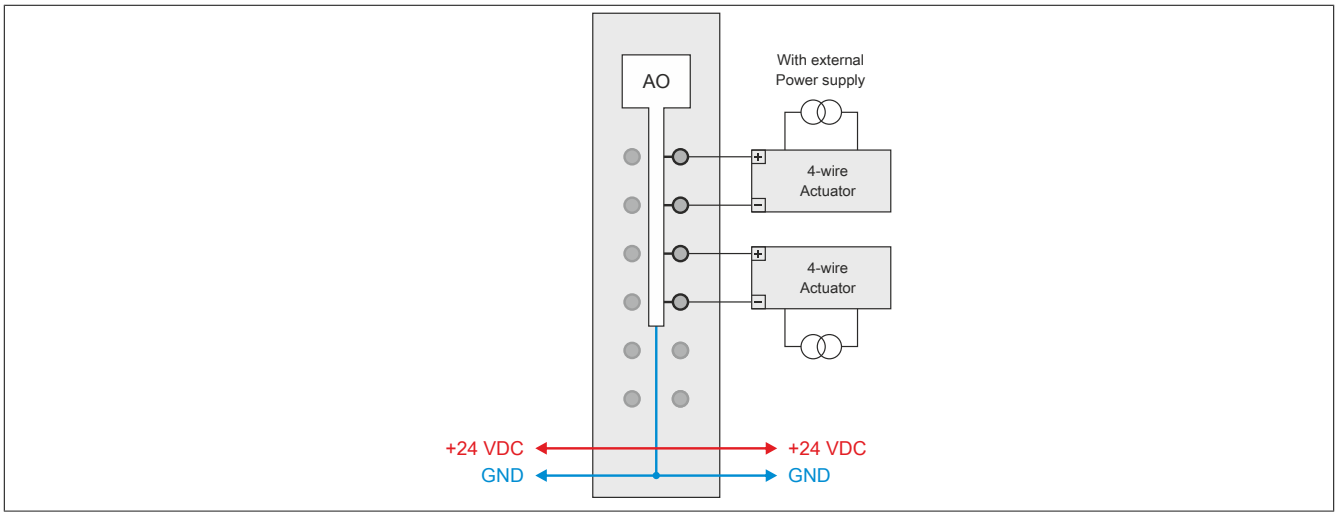
Figure	LED	Color	Status	Description
	**Operating status**			
	r	Green	Off	No power to module
			Single flash	UNLINK mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking quickly	SYNC mode
			Blinking slowly	PREOPERATIONAL mode
			On	RUN mode
			Flickering (approx. 10 Hz)	Module is in OSP mode
	Module status			
	e	Red	Off	No power to module or everything OK
			Single flash	A conversion error has occurred. When an error occurs, the LED of the faulty analog output channel begins to double flash and this status is output.
			On	Error or reset status
	Analog output			
	1 - 2	Orange	Off	Indicates one of the following cases: • No power to module • Channel disabled
			Single flash	Open line
			Double flash	A conversion error has occurred. A single flash is output on the red "e" module status LED.
			On	Digital/analog converter running, value OK

1) Depending on the configuration, a firmware update can take up to several minutes.

2.1.6 Pinout



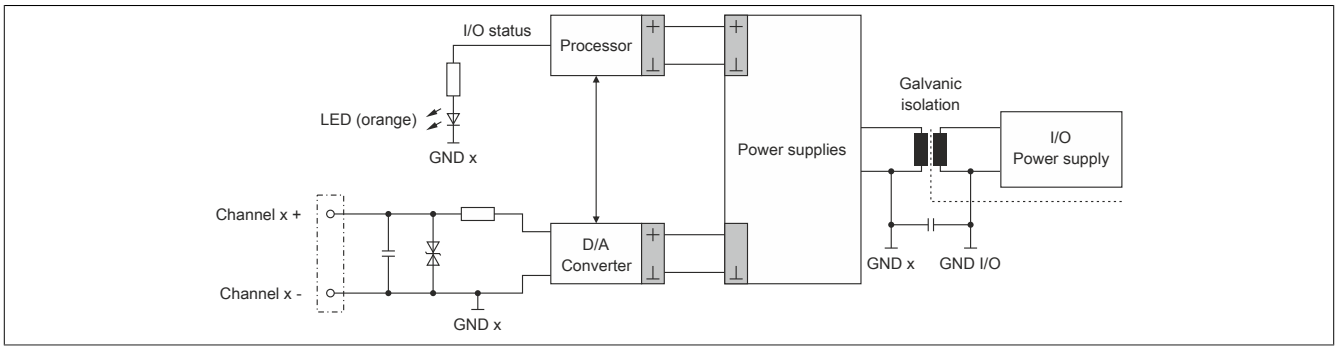
2.1.7 Connection example



2.1.8 OSP hardware requirements

In order to use OSP mode sensibly, it should be ensured that the power supply of the output module and CPU are independent of each other when the application is set up.

2.1.9 Output circuit diagram



2.1.10 Derating

To ensure proper operation, the derating values listed below must be adhered to:

Horizontal installation

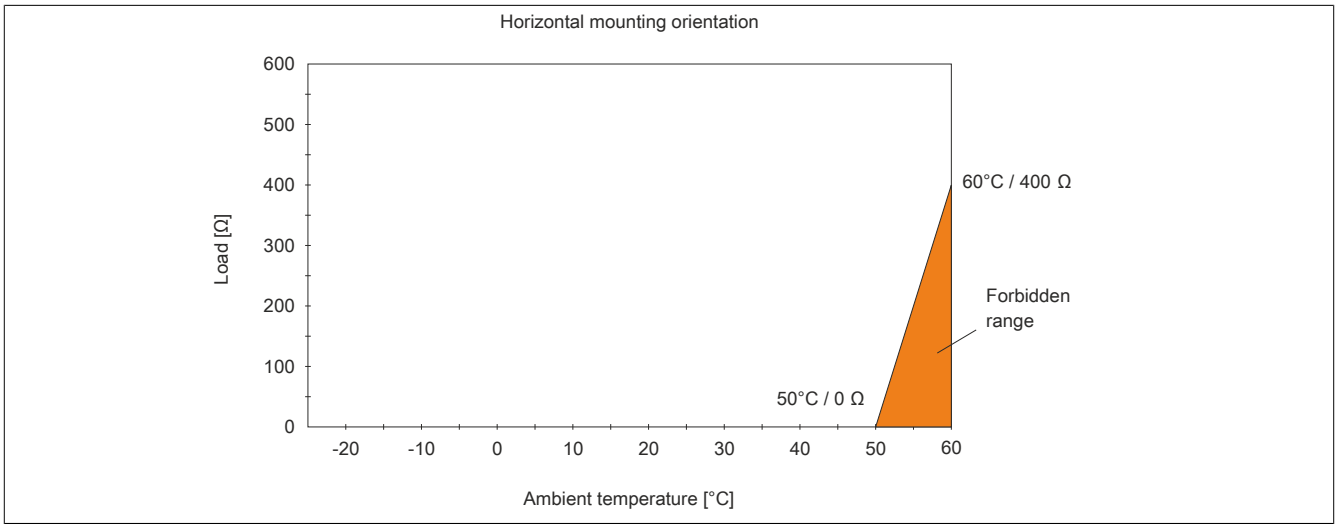


Figure 78: Derating the load with horizontal mounting

Vertical installation

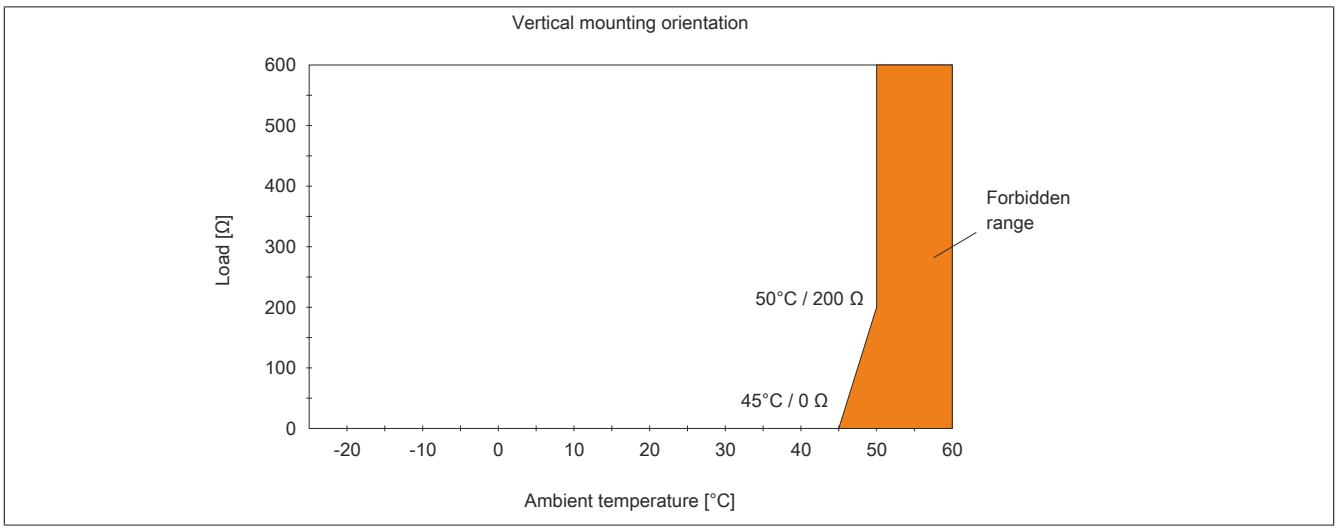


Figure 79: Derating the load with vertical mounting

2.1.11 Register description

2.1.11.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 system user's manual.

2.1.11.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration						
386 394	AnalogMode01 AnalogMode02	UINT				•
390 398	DACSlewrate01 DACSlewrate02	UINT				•
Analog signal - Communication						
0 2	AnalogOutput01 AnalogOutput02	(U)INT			•	
30 31	AnalogStatus01 AnalogStatus02	USINT	•			
	OpenLineAnalogOutput01 or OpenLineAnalogOutput02	Bit 2				
	ConversionErrorAnalogOutput01 or ConversionErrorAnalogOutput02	Bit 3				
	IoSuppErrorAnalogOutput01 or IoSuppErrorAnalogOutput02	Bit 7				

2.1.11.3 Function model 1 - OSP

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration						
386 394	AnalogMode01 AnalogMode02	UINT				•
390 398	DACSlewrate01 DACSlewrate02	UINT				•
Analog signal - Communication						
0 2	AnalogOutput01 AnalogOutput02	(U)INT			•	
30 31	AnalogStatus01 AnalogStatus02	USINT	•			
	OpenLineAnalogOutput01 or OpenLineAnalogOutput02	Bit 2				
	ConversionErrorAnalogOutput01 or ConversionErrorAnalogOutput02	Bit 3				
	IoSuppErrorAnalogOutput01 or IoSuppErrorAnalogOutput02	Bit 7				
The OSP function model						
32	OSPComByte	USINT			•	
	OSPValid	Bit 0				
401 403	CfgOSPMode01 CfgOSPMode02	USINT				•
34 36	CfgOSPValue01 CfgOSPValue02	INT				•

2.1.11.4 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration							
386 394	-	AnalogMode01 AnalogMode02	UINT				•
390 398	-	DACSlewrate01 DACSlewrate02	UINT				•
Analog signal - Communication							
0 2	0 2	AnalogOutput01 AnalogOutput02	(U)INT			•	
30 31	-	AnalogStatus01 AnalogStatus02	USINT		•		
		OpenLineAnalogOutput01 or OpenLineAnalogOutput02	Bit 2				
		ConversionErrorAnalogOutput01 or ConversionErrorAnalogOutput02	Bit 3				
		IoSuppErrorAnalogOutput01 or IoSuppErrorAnalogOutput02	Bit 7				

1) The offset specifies the position of the register within the CAN object.

2.1.11.4.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

2.1.11.4.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

2.1.11.5 Analog signal - Configuration

The module has 2 electrically isolated channels. All registers have a dual design. Channels can be configured and operated independently of one another.

Specific features

- Electrical isolation by channel
- Configurable output ramp DAC slew rate (Default: 210 ms full scale)

2.1.11.5.1 AnalogMode

Name:
AnalogMode01 to AnalogMode02

These registers are used to predefine the operating parameters that the module will be using for the respective channel. Each channel must be activated and configured separately.

Information:

When you select the operating mode "Scaling 0 to 20 mA (Resolution 0 to 65535)", then the corresponding "AnalogOutput" registers are interpreted internally as UINT instead of INT.
The entire program must be rebuilt for the data type change to take effect. The data type cannot be changed during runtime (e.g. using a library).

Data type	Values	Bus controller default setting
UINT	See the bit structure.	33

Bit structure:

Bit	Name	Value	Information
0	Channel	0	Disabled
		1	Enabled (bus controller default setting)
1	Check - D/A converter configuration/status	0	Enabled (bus controller default setting)
		1	Disabled
2 - 3	Reserved	-	
4	Scaling 0 to 20 mA (Resolution 0 to 32767)	0	Disabled
		1	Enabled
5	Scaling 4 to 20 mA (Resolution 0 to 32767)	0	Disabled
		1	Enabled (bus controller default setting)
6	Scaling 0 to 24 mA (Resolution 0 to 24000)	0	Disabled
		1	Enabled
7	Scaling 0 to 20 mA (Resolution 0 to 65535)	0	Disabled
		1	Enabled
8 - 15	Reserved	-	

2.1.11.5.2 DACSlewrate

Name:
DACSlewrate01 to DACSlewrate02

These registers limit the rate at which the analog signal is modified. This makes it possible to define a sort of upper limit frequency.

The following formula applies: f(Analog) = f(Output rate) * Permitted change / max. Δ(standardized output value)

Data type	Values	Bus controller default setting
UINT	See the bit structure.	514

Bit structure:

Bit	Name	Value	Information
0 - 2	Permitted change per rate	000	1-bit
		001	2-bit
		010	4-bit (bus controller default setting)
		011	8-bit
		100	16-bit
		101	32-bit
		110	64-bit
		111	128-bit
3 - 7	Reserved	-	
8 - 11	Output rate	0000	257730 Hz
		0001	198410 Hz
		0010	152440 Hz (bus controller default setting)
		0011	131580 Hz
		0100	115740 Hz
		0101	69440 Hz
		0110	37590 Hz
		0111	25770 Hz
		1000	20160 Hz
		1001	16030 Hz
		1010	10290 Hz
		1011	8280 Hz
		1100	6900 Hz
		1101	5530 Hz
		1110	4240 Hz
		1111	3300 Hz
12 - 14	Reserved	-	
15	Slewrate enable (ramp functionality)	0	Disabled (undefined jump behavior)
		1	Enabled (defined transitions)

2.1.11.6 Analog signal - Communication

In order to output the desired current signal (default: 4 to 20 mA), the module must be provided with the normalized output value (default: 0 to 32767).

2.1.11.6.1 AnalogOutput

Name:
AnalogOutput01 to AnalogOutput02

These registers provide the normalized output values. Depending on the scaling selected (see register "Analog-Mode" on page 653), the range of values and the data type can be adapted to the requirements of the application. Once a permissible value is transferred, the module outputs the corresponding current.

Information:

The value "0" disables the channel status LED.

Data type	Value
INT	0 to 32767
Optional: UINT	0 to 65535

2.1.11.6.2 AnalogStatus

Name:
AnalogStatus01 to AnalogStatus02

The status register gives the user feedback about whether the respective channel is functioning properly.

Data type	Value
USINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0 - 1	Reserved	-	
2	OpenLineAnalogOutput01, 02	0	Line OK
		1	Open line
3	ConversionErrorAnalogOutput01, 02	0	Conversion temperature OK
		1	Conversion temperature too high
4 - 6	Reserved	-	
7	IoSuppErrorAnalogOutput01, 02	0	Module supply OK
		1	Module supply error

2.1.11.7 Function model "OSP"

In function model "OSP" (Operator Set Predefined), the user defines an analog value or digital pattern. This OSP value is output as soon as the communication between the module and master is aborted.

Functionality

The user has the choice between 2 OSP modes:

- Retain last valid value
- Replace with static value

In the first case, the module retains the last value recognized as a valid output status.

When selecting mode "Replace with static value", a plausible output value must be entered in the associated value register. When an OSP event occurs, this value is output instead of the value currently requested by the task.

2.1.11.7.1 Activating the OSP output in the module

Name:
OSPValid

This data point offers the possibility to start module output and request OSP operation during running operation.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	OSPValid	0	Request OSP operation (after initial start or module in Standby)
		1	Request normal operation
1 - 7	Reserved	0	

There is one OSPValid bit on the module, which is managed by the user task. It must be set when the enabled channels are started. As long as the OSPValid bit remains set in the module, the module behaves the same as the "Standard" function model.

If an OSP event occurs (e.g. communication between the module and master CPU interrupted) then the OSPValid bit will be reset on the module. The module enters OSP mode and the output occurs in the "OSPMode" on page 657 register according to the configuration.

The following applies:

The OSP replacement value remains even after the communication channel has recovered. OSP mode is only exited when a set OSPValid bit is transferred.

When the master CPU is restarted, the OSPValid bit is re-initialized on the master CPU. It must once more be set by the application and transferred via the bus.
When temporary communication errors occur between the module and master CPU (e.g. due to EMC), a few bus cycles will pass without refreshing the cyclic registers. The OSPValid bit is reset internally in the module - the bit in the CPU however remains set. Upon the next successful transfer, the OSPValid bit in the module is set again and the module returns to normal operation.

The ModulOK bit can be evaluated if the task in the master CPU needs to know which output mode the module is currently in.

Warning!

If the OSPValid bit is reset to "0" on the module, then the output state no longer depends on the relevant task in the master CPU. However, an output still occurs depending on the configuration of the OSP replacement value.

2.1.11.7.2 Setting the OSP mode

Name:
CfgOSPMode01 to CfgOSPMode02

This register essentially controls a channel's behavior when OSP is being used.

Data type	Value	Description
USINT	0	Replace with static value
	1	Retain last valid value

2.1.11.7.3 Define the OSP analog output value

Name:
CfgOSPValue01 to CfgOSPValue02

This register contains the analog output value, which is output in "Replace with static value" mode during OSP operation.

Data type	Value
Corresponds to AnalogOutput0x	Corresponds to AnalogOutput0x

Warning!

"OSPValue" is only applied by the module if bit "OSPValid" has been set in the module.

2.1.11.8 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

2.1.11.9 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time
200 µs

2.2 X20(c)AO2438

2.2.1 General information

The module is equipped with 2 current outputs with 16-bit digital converter resolution. It supports the HART communication standard for data transfer, parameter configuration and diagnostics.

The 2 channels are electrically isolated from each other. The user can select between the 3 output ranges 4 to 20 mA, 0 to 20 mA and 0 to 24 mA.

- 2 analog current outputs
- HART protocol integration
- Support for HART variables
- Electrically isolated analog channels
- 16-bit digital converter resolution
- OSP mode
- NetTime timestamp: HART image

NetTime timestamp of the HART image

For many applications, not only the HART values are important, but also the exact time of reception. For this purpose, the module has a NetTime timestamp function that provides the reception time with a timestamp with microsecond accuracy.

The timestamp function is based on synchronized timers. If a timestamp event occurs, the module immediately saves the current NetTime. After the respective data is transferred to the CPU, including this precise moment, the CPU can then evaluate the data using its own NetTime (or system time), if necessary.

OSP mode

In function model "OSP" (Operator Set Predefined), the user defines an analog value. This OSP value is always output as soon as the communication between the module and master is interrupted. Alternatively, the last valid output value can also be obtained.

This ensures that the module does not fall into an undefined state in the event of communication failure.

2.2.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, method 4, exposure 21 days

2.2.3 Order data

Order number	Short description	Figure
	Analog outputs	
X20AO2438	X20 analog output module, 2 outputs, 4 to 20 mA / 0 to 20 mA or 0 to 24 mA, 16-bit converter resolution, single-channel galvanically isolated, supports the HART protocol, NetTime function	
X20cAO2438	X20 analog output module coated, 2 outputs, 4 to 20 mA / 0 to 20 mA or 0 to 24 mA, 16-bit converter resolution, single-channel galvanically isolated, supports the HART protocol, NetTime function	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 99: X20AO2438, X20cAO2438 - Order data

2.2.4 Technical data

Order number	X20AO2438	X20cAO2438
Short description		
I/O module	2 analog outputs 4 to 20 mA, 0 to 20 mA or 0 to 24 mA	
General information		
B&R ID code	0xB3AA	0xE211
Status indicators	I/O function per channel, operating state, module status, HART	
Diagnostics		
Module run/error	Yes, using LED status indicator and software	
Outputs	Yes, using LED status indicator and software	
HART link	Yes, using LED status indicator and software	
HART error	Yes, using LED status indicator and software	
Power consumption		
Bus	0.05 W	
Internal I/O	1.65 W	
Additional power dissipation caused by actuators (resistive) [W]	-	
Certifications		
CE	Yes	
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X	
UL	cULus E115267 Industrial control equipment	
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5	
DNV GL	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)	
LR	ENV1	
KR	Yes	
ABS	Yes	
EAC	Yes	
KC	Yes	-
Analog outputs		
Output	4 to 20 mA, 0 to 20 mA or 0 to 24 mA configurable using software	
Digital converter resolution	16-bit	
Settling time on output change over entire range	2 ms to 20 s, configurable using software	
Data output rate		
With HART	210 ms (default)	
Analog	1 ms without ramp	
Max. error		
Gain		
4 to 20 mA	0.025% [1]	
0 to 20 mA	0.022% [1]	
0 to 24 mA	0.02% [1]	
Offset		
4 to 20 mA	0.025% [2]	
0 to 20 mA	0.022% [2]	
0 to 24 mA	0.02% [2]	
Output protection	Short-circuit proof, overvoltage protection (up to 30 VDC)	
Open-circuit detection	Yes, using hardware and software	
Data format	INT	
Output format		
4 to 20 mA	INT 0x0000 to 0x7FFF / 1 LSB = 0x0001 = 488.281 nA	
0 to 20 mA	INT 0x0000 to 0x7FFF / 1 LSB = 0x0001 = 610.352 nA UINT 0x0000 to 0xFFFF / 1 LSB = 0x0001 = 305.176 nA	
0 to 24 mA	INT 0x0000 to 0x5DC0 / 1 LSB = 0x0001 = 1000 nA	
Load per channel	Max. 600 Ω	
Short-circuit proof	Yes, continuous	
Output filter	Active second-order low-pass filter / cutoff frequency 19 Hz Configurable slew rate	
Max. gain drift		
4 to 20 mA	0.0055 %/°C [1]	
0 to 20 mA	0.005 %/°C [1]	
0 to 24 mA	0.005 %/°C [1]	
Max. offset drift		
4 to 20 mA	0.0035 %/°C [2]	
0 to 20 mA	0.002%/°C [2]	
0 to 24 mA	0.002%/°C [2]	

Table 100: X20AO2438, X20cAO2438 - Technical data

Order number	X20AO2438	X20cAO2438
Error caused by load change [3]		
4 to 20 mA	0.14%	
0 to 20 mA	0.1%	
0 to 24 mA	0.1%	
Nonlinearity	<0.003% [4]	
Test voltage		
Channel - Channel	1000 VAC	
Channel - Bus	1000 VAC	
Channel - Ground	1000 VAC	
HART		
Transfer rate	1200 bit/s	
Operating frequencies	1200 Hz / 2200 Hz	
Burst operation possible	Yes	
Multi-drop operation		
Possible	Yes	
Stations	Up to 15	
Transmission amplitude		
Minimum	400 mV_{pp}	
Typical	500 mV_{pp}	
Maximum	600 mV_{pp}	
Receiving amplitude		
Minimum	120 mV_{pp}	
Maximum	1500 mV_{pp}	
Electrical properties		
Electrical isolation	Channel isolated from channel and bus	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation elevation above sea level		
0 to 2000 m	No limitation	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
Degree of protection per EN 60529	IP20	
Ambient conditions		
Temperature		
Operation		
Horizontal mounting orientation	-25 to 60°C	
Vertical mounting orientation	-25 to 50°C	
Derating	See section "Derating".	
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical properties		
Note	Order 1x terminal block X20TB12 separately. Order 1x bus module X20BM11 separately.	Order 1x terminal block X20TB12 separately. Order 1x bus module X20cBM11 separately.
Pitch	$12.5^{+0.2}$ mm	

Table 100: X20AO2438, X20cAO2438 - Technical data

1) Based on the current output value.
2) Based on the respective output range.
3) Load change from 1 Ω → 600 Ω, resistive
4) Based on the entire output range.

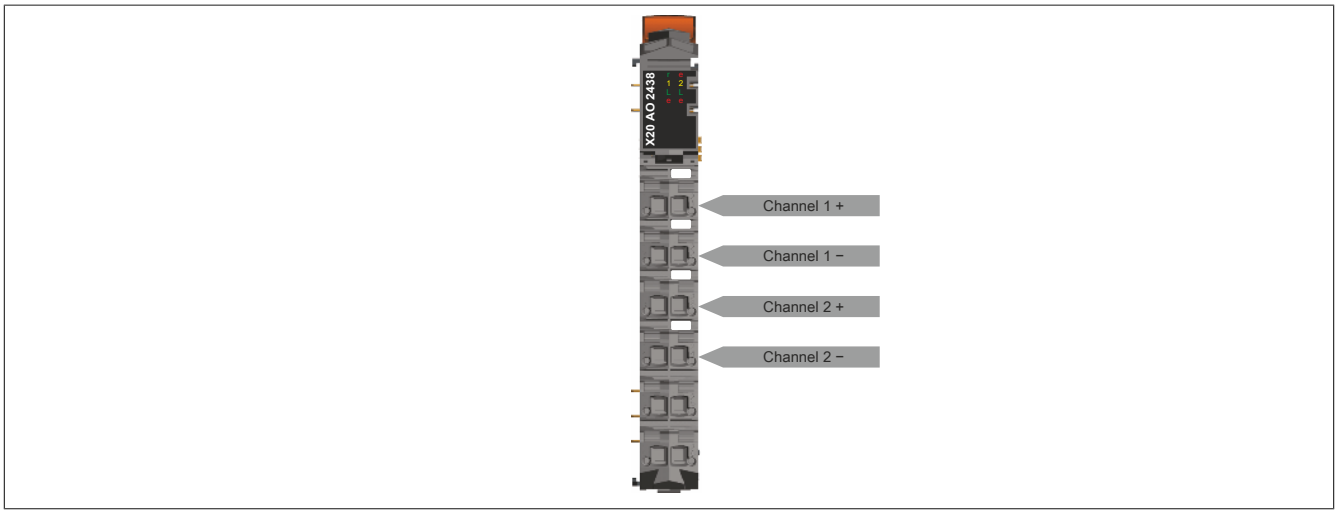
2.2.5 LED status indicators

For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 system user's manual.

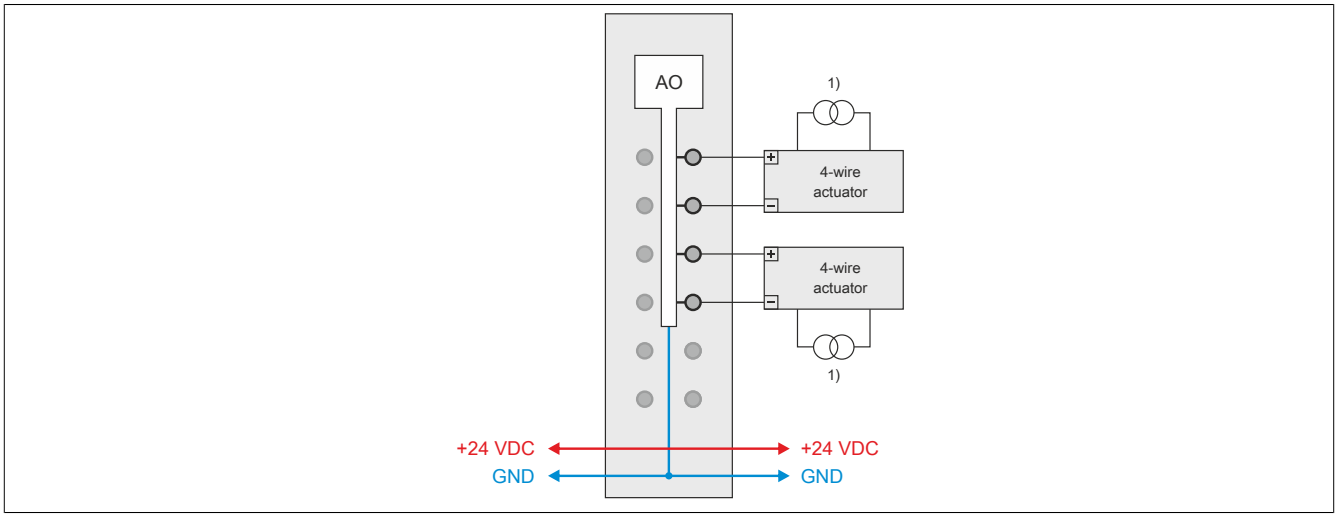
Figure	LED	Color	Status	Description
	**Operating status**			
	r	Green	Off	No power to module
			Single flash	UNLINK mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking quickly	SYNC mode
			Blinking slowly	PREOPERATIONAL mode
			On	RUN mode
			Flickering (approx. 10 Hz)	Module is in OSP mode
	Module status			
	e	Red	Off	No power to module or everything OK
			Single flash	A conversion error has occurred. When an error occurs, the LED of the faulty analog output channel begins to double flash and this status is output.
			On	Error or reset status
	Analog output			
	1 - 2	Orange	Off	Indicates one of the following cases: • No power to module • Channel disabled
			Single flash	Open line
			Double flash	A conversion error has occurred. A single flash is output on the red "e" module status LED.
			On	Digital/analog converter running, value OK
	HART link			
	L	Green	Off	Indicates one of the following cases: • No power to module • HART disabled for the respective channel
			Flickering	Carrier signal active (DCD or RTS)
	HART error			
	e	Red	Off	Indicates one of the following cases: • Communication taking place without errors • No power to module • HART disabled for the respective channel
			On	Communication error

1) Depending on the configuration, a firmware update can take up to several minutes.

2.2.6 Pinout



2.2.7 Connection example

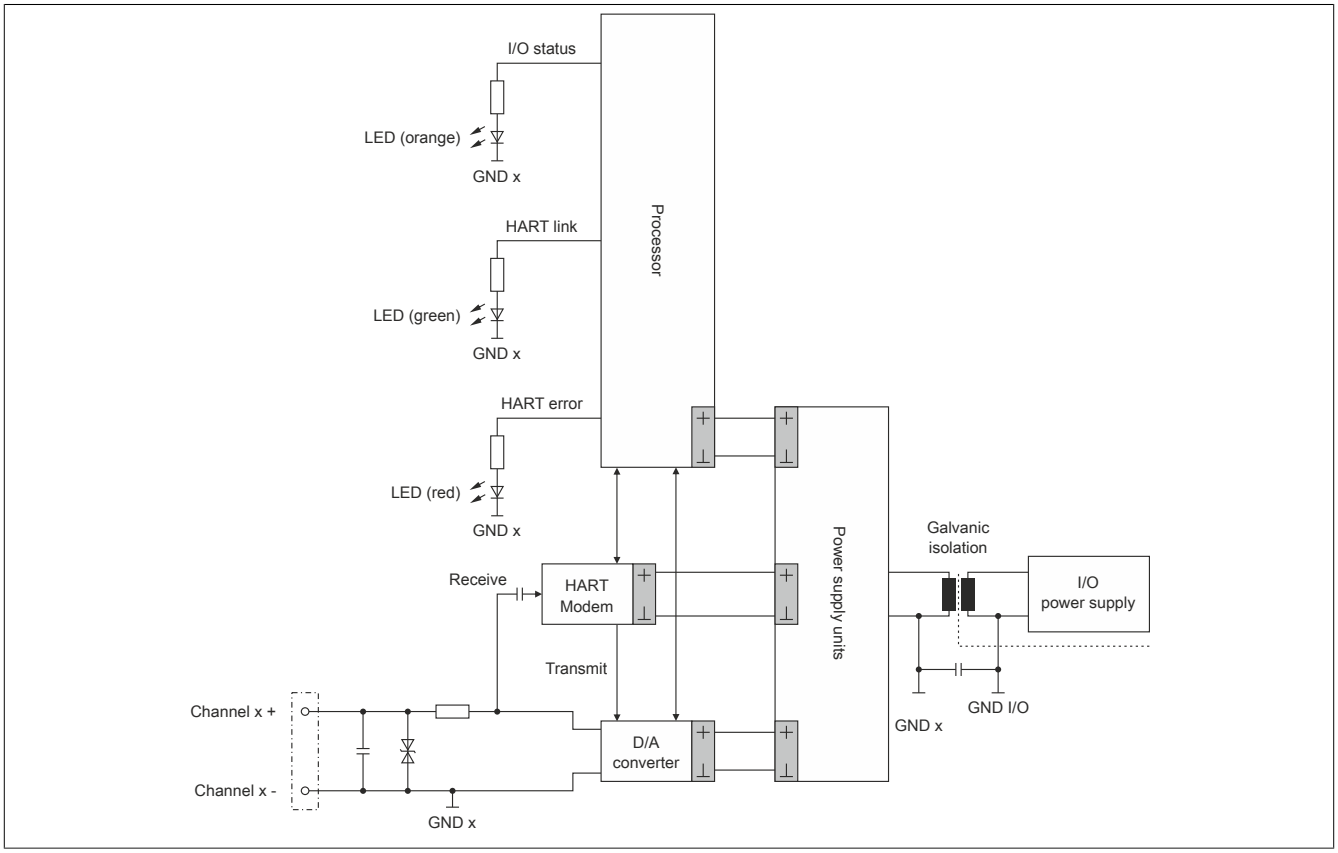


1) With external power supply.

2.2.8 OSP hardware requirements

In order to use OSP mode sensibly, it should be ensured that the power supply of the output module and CPU are independent of each other when the application is set up.

2.2.9 Output circuit diagram



2.2.10 Operation

2.2.10.1 Derating

To ensure proper operation, the derating values listed below must be adhered to:

Horizontal installation

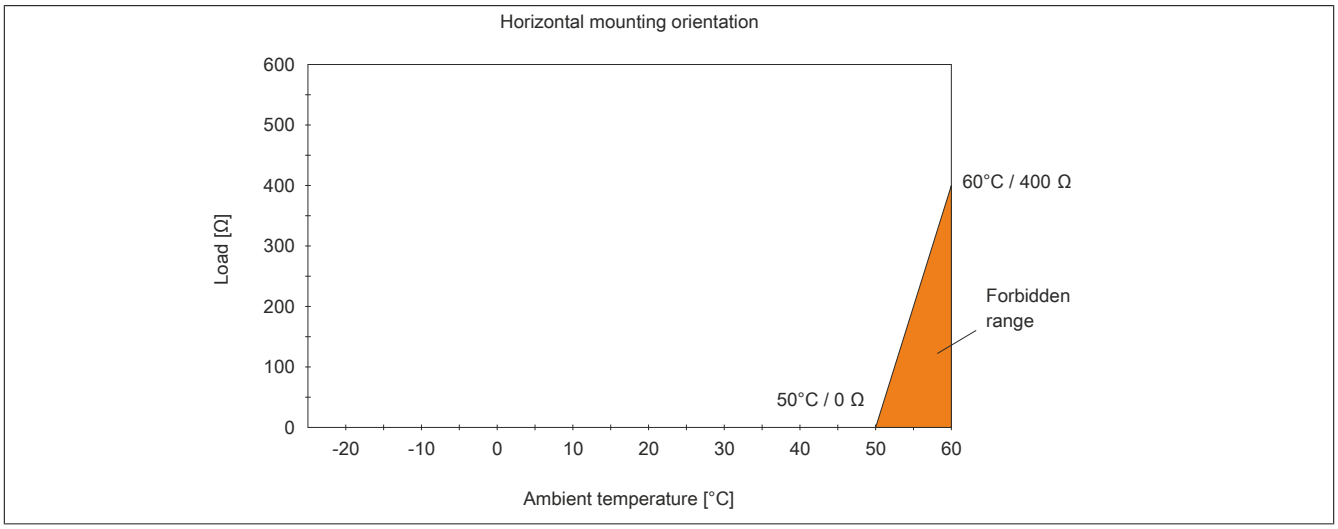


Figure 80: Derating the load with horizontal mounting

Vertical installation

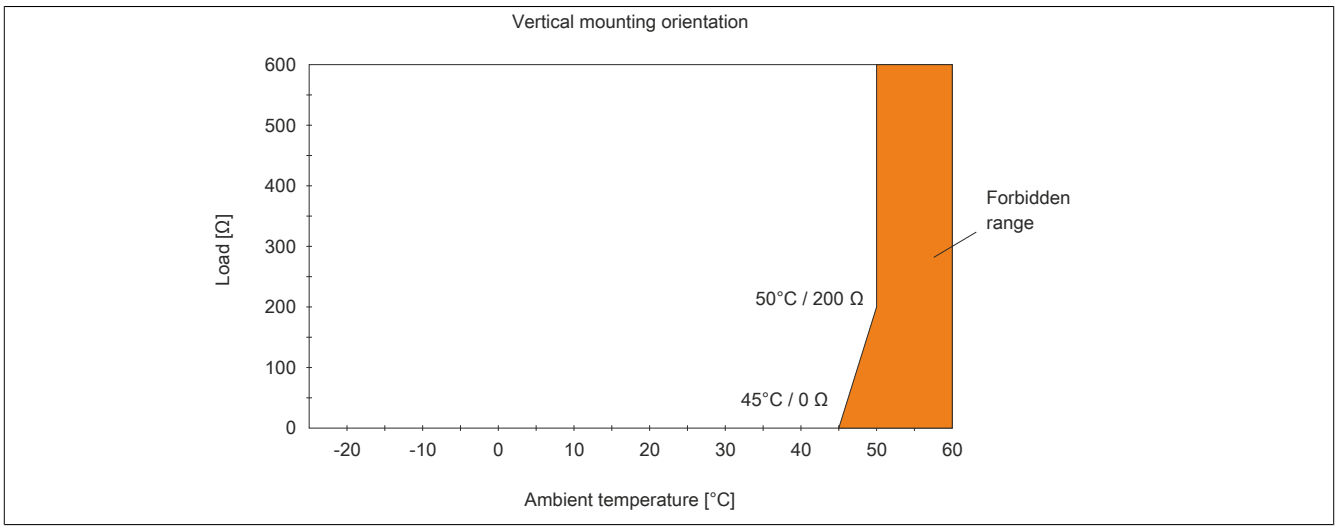


Figure 81: Derating the load with vertical mounting

2.2.10.2 Usage after the X20IF1091-1

If this module is operated after X2X Link module X20IF1091-1, delays may occur during the Flatstream transfer. For detailed information, see section "Data transfer on the Flatstream" in X20IF1091-1.

2.2.10.3 HART communication standard

This module supports the HART communication standard for data transfer, parameter configuration and diagnostics. The HART standard is used for the current range 4 to 20 mA. Be aware that the load is not permitted to fall below 230 Ω .

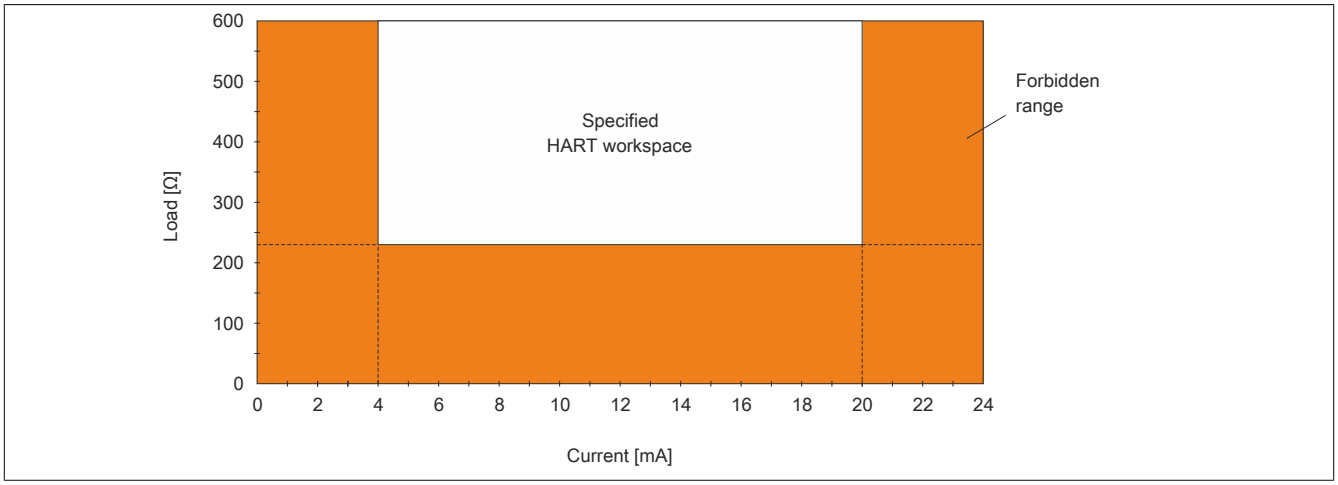


Figure 82: Specified HART operational range

Both current ranges 0 to 20 mA and 0 to 24 mA are supported by this module. HART communication can also be used in these ranges as well. It is important to make sure, however, that the output current lies within the specified HART operational range.

2.2.11 Register description

2.2.11.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 system user's manual.

2.2.11.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration						
386 394	AnalogMode01 AnalogMode02	UINT				•
390 398	DACSlewrate01 DACSlewrate02	UINT				•
Analog signal - Communication						
0 2	AnalogOutput01 AnalogOutput02	(U)INT			•	
30 31	AnalogStatus01 AnalogStatus02	USINT	•			
	OpenLineAnalogOutput01 or OpenLineAnalogOutput02	Bit 2				
	ConversionErrorAnalogOutput01 or ConversionErrorAnalogOutput02	Bit 3				
	IoSuppErrorAnalogOutput01 or IoSuppErrorAnalogOutput02	Bit 7				
HART - Configuration						
1537 1665	HartNodeCnt_1 HartNodeCnt_2	USINT				•
1539 1667	HartMode_1 HartMode_2	USINT				•
1541 1669	HartBurstNode_1 HartBurtNode_2	USINT				•
HART - Extended configuration						
1558 1668	HartNodeDisable_1 HartNodeDisable_2	UINT				•
1546 1674	HartProtTimeOut_1 HartProtTimeOut_2	UINT				•
1550 1678	HartProtRetry_1 HartProtRetry_2	UINT				•
1554 1682	HartPreamble_1 HartPreamble_2	UINT				•
HART - Communication (P2P)						
612 + Index*24 1124 + Index*24	PvInput01_N (Index N = 01 to 04) PvInput02_N (Index N = 01 to 04)	REAL	•	•[1)]		
617 + Index*24 1129 + Index*24	PvUnit01_N (Index N = 01 to 04) PvUnit02_N (Index N = 01 to 04)	USINT	•	•[1)]		
628 1140	PvSampleTime01 PvSampleTime02	DINT	•	•[1)]		
626 1138	PvSampleTime01 PvSampleTime02	INT	•			
566 1078	PvNodeComStatus01 PvNodeComStatus02	UINT		•		
HART - Communication (multidrop)						
612 + Index*24 1124 + Index*24	PvInput01_N (Index N = 01 to 15) PvInput02_N (Index N = 01 to 15)	REAL	•	•[1)]		
617 + Index*24 1129 + Index*24	PvUnit01_N (Index N = 01 to 15) PvUnit02_N (Index N = 01 to 15)	USINT	•	•[1)]		
604 + Index*24 1116 + Index*24	PvSampleTime01_N (Index N = 01 to 15) PvSampleTime02_N (Index N = 01 to 15)	DINT	•	•[1)]		
602 + Index*24 1114 + Index*24	PvSampleTime01_N (Index N = 01 to 15) PvSampleTime02_N (Index N = 01 to 15)	INT	•			
562 + Index*4 1074 + Index*4	PvNodeComStatus01_N (Index N = 01 to 15) PvNodeComStatus02_N (Index N = 01 to 15)	UINT		•		
HART - Extended communication						
522 1034	PvCountHartRequest01 PvCountHartRequest02	UINT	•			
530 1042	PvCountHartTimeout01 PvCountHartTimeout02	UINT	•			
538 1050	PvCountHartRxError01 PvCountHartRxError02	UINT	•			
546 1058	PvCountHartFrameError01 PvCountHartFrameError02	UINT	•			
554 1066	PvNodeFound01 PvNodeFound02	UINT	•			

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
558 1070	PvNodeError01 PvNodeError02	UINT	•			
Flatstream - Configuration						
1793	OutputMTU	USINT				•
1795	InputMTU	USINT				•
1797	FlatstreamMode	USINT				•
1799	Forward	USINT				•
1802	ForwardDelay	UINT				•
Flatstream - Communication						
1857	InputSequence	USINT	•			
1857 + Index*2	RxByteN (Index N = 1 to 15)	USINT	•			
1889	OutputSequence	USINT			•	
1889 + Index*2	TxByteN (Index N = 1 to 15)	USINT			•	

1) These HART registers are defined multiple times. Hence, they can be activated acyclically, if they are not registered during the cyclical phase of the X2X transmission.

2.2.11.3 Function model 1 - OSP

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration						
386 394	AnalogMode01 AnalogMode02	UINT				•
390 398	DACSlewrate01 DACSlewrate02	UINT				•
Analog signal - Communication						
0 2	AnalogOutput01 AnalogOutput02	(U)INT			•	
30 31	AnalogStatus01 AnalogStatus02	USINT	•			
	OpenLineAnalogOutput01 or OpenLineAnalogOutput02	Bit 2				
	ConversionErrorAnalogOutput01 or ConversionErrorAnalogOutput02	Bit 3				
	IoSuppErrorAnalogOutput01 or IoSuppErrorAnalogOutput02	Bit 7				
HART - Configuration						
1537 1665	HartNodeCnt_1 HartNodeCnt_2	USINT				•
1539 1667	HartMode_1 HartMode_2	USINT				•
1541 1669	HartBurstNode_1 HartBurtNode_2	USINT				•
HART - Extended configuration						
1558 1668	HartNodeDisable_1 HartNodeDisable_2	UINT				•
1546 1674	HartProtTimeOut_1 HartProtTimeOut_2	UINT				•
1550 1678	HartProtRetry_1 HartProtRetry_2	UINT				•
1554 1682	HartPreamble_1 HartPreamble_2	UINT				•
HART - Communication (P2P)						
612 + Index*24 1124 + Index*24	PvInput01_N (Index N = 01 to 04) PvInput02_N (Index N = 01 to 04)	REAL	•	•[1)]		
617 + Index*24 1129 + Index*24	PvUnit01_N (Index N = 01 to 04) PvUnit02_N (Index N = 01 to 04)	USINT	•	•[1)]		
628 1140	PvSampleTime01 PvSampleTime02	DINT	•	•[1)]		
626 1138	PvSampleTime01 PvSampleTime02	INT	•			
566 1078	PvNodeComStatus01 PvNodeComStatus02	UINT		•		
HART - Communication (multidrop)						
612 + Index*24 1124 + Index*24	PvInput01_N (Index N = 01 to 15) PvInput02_N (Index N = 01 to 15)	REAL	•	•[1)]		
617 + Index*24 1129 + Index*24	PvUnit01_N (Index N = 01 to 15) PvUnit02_N (Index N = 01 to 15)	USINT	•	•[1)]		
604 + Index*24 1116 + Index*24	PvSampleTime01_N (Index N = 01 to 15) PvSampleTime02_N (Index N = 01 to 15)	DINT	•	•[1)]		
602 + Index*24 1114 + Index*24	PvSampleTime01_N (Index N = 01 to 15) PvSampleTime02_N (Index N = 01 to 15)	INT	•			
562 + Index*4 1074 + Index*4	PvNodeComStatus01_N (Index N = 01 to 15) PvNodeComStatus02_N (Index N = 01 to 15)	UINT		•		
HART - Extended communication						
522 1034	PvCountHartRequest01 PvCountHartRequest02	UINT	•			

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
530 1042	PvCountHartTimeout01 PvCountHartTimeout02	UINT	•			
538 1050	PvCountHartRxError01 PvCountHartRxError02	UINT	•			
546 1058	PvCountHartFrameError01 PvCountHartFrameError02	UINT	•			
554 1066	PvNodeFound01 PvNodeFound02	UINT	•			
558 1070	PvNodeError01 PvNodeError02	UINT	•			
Flatstream - Configuration						
1793	OutputMTU	USINT				•
1795	InputMTU	USINT				•
1797	FlatstreamMode	USINT				•
1799	Forward	USINT				•
1802	ForwardDelay	UINT				•
Flatstream - Communication						
1857	InputSequence	USINT	•			
1857 + Index*2	RxByteN (Index N = 1 to 15)	USINT	•			
1889	OutputSequence	USINT			•	
1889 + Index*2	TxByteN (Index N = 1 to 15)	USINT			•	
The OSP function model						
32	OSPComByte	USINT			•	
	OSPValid	Bit 0				
401 403	CfgOSPMode01 CfgOSPMode02	USINT				•
34 36	CfgOSPValue01 CfgOSPValue02	INT				•

1) These HART registers are defined multiple times. Hence, they can be activated acyclically, if they are not registered during the cyclical phase of the X2X transmission.

2.2.11.4 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration							
386 394	- -	AnalogMode01 AnalogMode02	UINT				•
390 398	- -	DACSlewrate01 DACSlewrate02	UINT				•
Analog signal - Communication							
0 2	0 8	AnalogOutput01 AnalogOutput02	(U)INT			•	
30 31	- -	AnalogStatus01 AnalogStatus02	USINT		•		
		OpenLineAnalogOutput01 or OpenLineAnalogOutput02	Bit 2				
		ConversionErrorAnalogOutput01 or ConversionErrorAnalogOutput02	Bit 3				
		IoSuppErrorAnalogOutput01 or IoSuppErrorAnalogOutput02	Bit 7				
HART - Configuration							
1537 1665	- -	HartNodeCnt_1 HartNodeCnt_2	USINT				•
1539 1667	- -	HartMode_1 HartMode_2	USINT				•
1541 1669	- -	HartBurstNode_1 HartBurtNode_2	USINT				•
HART - Extended configuration							
1558 1668	- -	HartNodeDisable_1 HartNodeDisable_2	UINT				•
1546 1674	- -	HartProtTimeOut_1 HartProtTimeOut_2	UINT				•
1550 1678	- -	HartProtRetry_1 HartProtRetry_2	UINT				•
1554 1682	- -	HartPreamble_1 HartPreamble_2	UINT				•
HART - Communication (P2P)							
636 1148	4 12	PvInput01_01 PvInput02_01	REAL	•			
612 + Index*24 1124 + Index*24	- -	PvInput01_N (Index N = 02 to 04) PvInput02_N (Index N = 02 to 04)	REAL		•		
641 1153	2 10	PvUnit01_01 PvUnit02_01	USINT	•			
617 + Index*24 1129 + Index*24	- -	PvUnit01_N (Index N = 02 to 04) PvUnit02_N (Index N = 02 to 04)	USINT		•		
566 1078	- -	PvNodeComStatus01 PvNodeComStatus02	UINT		•		
HART - Communication (multidrop)							
636 1148	4 12	PvInput01_01 PvInput02_01	REAL	•			
612 + Index*24 1124 + Index*24	- -	PvInput01_N (Index N = 02 to 15) PvInput02_N (Index N = 02 to 15)	REAL		•		
641 1153	2 10	PvUnit01_01 PvUnit02_01	USINT	•			
617 + Index*24 1129 + Index*24	- -	PvUnit01_N (Index N = 02 to 15) PvUnit02_N (Index N = 02 to 15)	USINT		•		
562 + Index*4 1074 + Index*4	- -	PvNodeComStatus01_N (Index N = 01 to 15) PvNodeComStatus02_N (Index N = 01 to 15)	UINT		•		
HART - Extended communication							
522 1034	- -	PvCountHartRequest01 PvCountHartRequest02	UINT		•		
530 1042	- -	PvCountHartTimeout01 PvCountHartTimeout02	UINT		•		
538 1050	- -	PvCountHartRxError01 PvCountHartRxError02	UINT		•		
546 1058	- -	PvCountHartFrameError01 PvCountHartFrameError02	UINT		•		
554 1066	- -	PvNodeFound01 PvNodeFound02	UINT		•		
558 1070	- -	PvNodeError01 PvNodeError02	UINT		•		

1) The offset specifies the position of the register within the CAN object.

2.2.11.4.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

2.2.11.4.2 CAN I/O bus controller

The module occupies 2 analog logical slots on CAN I/O.

2.2.11.5 Analog signal - Configuration

The module has 2 independent electrically isolated channels with integrated HART modems. Both channels can be used to output an analog signal and handle HART communication. 2 registers need to be configured for one analog signal. The 2 channels operate independently, so 2 registers must be configured per channel to be used.

The current outputs (default: 4 to 20 mA) can be used as conventional analog signals. The integrated HART modems retrieve digital information from the memory on the HART slave using the same physical lines that modulate the HART signals.

Each channel can use one of the following connection variants:

- Point-to-point (connection of one HART node on the channel):
  → Evaluation of the analog signal
  and
  → Recording of up to 4 HART values
- Multidrop (connection of up to 15 HART nodes on the channel):
  → Recording of one HART value per connected node

Specific features

- Electrical isolation by channel
- Up to 4 or 15 HART input variables per channel
- Configurable output rate (DAC slew rate) to transfer HART and analog signal without interference (default: 210 ms full scale)
- Selectable error strategy (static replacement value or retention of the last permitted value)
- Cyclic "HART status" polling (HART command 0), the status information received is made available for channel diagnostics
- Compatible with an additional secondary master in the HART network (module acts as the primary master)
- "HART communication error bit" (shows loss of HART connection if a connection had already been established successfully)
- Optional: BURST mode for one node per channel
- Optional: Cyclic polling of "HART variables" (HART command 3 or 9)
- Optional: FlatStream functionality (module acts as bridge for HART packets)

2.2.11.5.1 AnalogMode

Name:
AnalogMode01 to AnalogMode02

These registers are used to predefine the operating parameters that the module will be using for the respective channel. Each channel must be activated and configured separately.

Information:

When you select the operating mode "Scaling 0 to 20 mA (Resolution 0 to 65535)", then the corresponding "AnalogOutput" registers are interpreted internally as UINT instead of INT.
The entire program must be rebuilt for the data type change to take effect. The data type cannot be changed during runtime (e.g. using a library).

Data type	Values	Bus controller default setting
UINT	See the bit structure.	33

Bit structure:

Bit	Name	Value	Information
0	Channel	0	Disabled
		1	Enabled (bus controller default setting)
1	Check - D/A converter configuration/status	0	Enabled (bus controller default setting)
		1	Disabled
2 - 3	Reserved	-	
4	Scaling 0 to 20 mA (Resolution 0 to 32767)	0	Disabled
		1	Enabled
5	Scaling 4 to 20 mA (Resolution 0 to 32767)	0	Disabled
		1	Enabled (bus controller default setting)
6	Scaling 0 to 24 mA (Resolution 0 to 24000)	0	Disabled
		1	Enabled
7	Scaling 0 to 20 mA (Resolution 0 to 65535)	0	Disabled
		1	Enabled
8 - 15	Reserved	-	

Information:

The "AnalogMode" registers provide the option of avoiding the cyclic check of the D/A converter configuration. To manage communication reliably, this option should only be used if no HART communication is taking place on the channel.

2.2.11.5.2 DACSlewrate

Name:
DACSlewrate01 to DACSlewrate02

These registers limit the rate at which the analog signal is modified. This makes it possible to define a sort of upper limit frequency.

The following formula applies: f(Analog) = f(Output rate) * Permitted change / max. Δ(standardized output value)

To ensure communication takes place without errors, it's important that the frequency range of the digital HART signal is not influenced by the analog output. HART communication takes place in the frequency range 950 to 2500 Hz.

Example (standard): f(Analog) = 152440 Hz * 4 / (32767 - 0)
Conclusion: f(Analog) = **~20 Hz << 950 Hz** = f(HART)

Data type	Values	Bus controller default setting
UINT	See the bit structure.	514

Bit structure:

Bit	Name	Value	Information
0 - 2	Permitted change per rate	000	1-bit
		001	2-bit
		010	4-bit (bus controller default setting)
		011	8-bit
		100	16-bit
		101	32-bit
		110	64-bit
		111	128-bit
3 - 7	Reserved	-	
8 - 11	Output rate	0000	257730 Hz
		0001	198410 Hz
		0010	152440 Hz (bus controller default setting)
		0011	131580 Hz
		0100	115740 Hz
		0101	69440 Hz
		0110	37590 Hz
		0111	25770 Hz
		1000	20160 Hz
		1001	16030 Hz
		1010	10290 Hz
		1011	8280 Hz
		1100	6900 Hz
		1101	5530 Hz
		1110	4240 Hz
		1111	3300 Hz
12 - 14	Reserved	-	
15	Slewrate enable (ramp functionality)	0	Disabled (undefined jump behavior)
		1	Enabled (defined transitions)

2.2.11.6 Analog signal - Communication

In order to output the desired current signal (default: 4 to 20 mA), the module must be provided with the normalized output value (default: 0 to 32767). In this way, the X20AO2438 can be used as a conventional output module. The integrated HART modem physically uses the same line. Using higher frequency signals, the module can communicate with the HART slave and retrieve additional information.

2.2.11.6.1 AnalogOutput

Name:
AnalogOutput01 to AnalogOutput02

These registers provide the standardized output values. Depending on the scaling selected (see register "Analog-Mode" on page 671), the value range and the data type can be adapted to the requirements of the application. Once a permitted value is determined, the module outputs the respective current.

Information:

The value "0" disables the channel status LED.

Data type	Value
INT	0 to 32767
Optional: UINT	0 to 65535

2.2.11.6.2 AnalogStatus

Name:
AnalogStatus01 to AnalogStatus02

The status register gives the user feedback about whether the respective channel is functioning properly.

Data type	Value
USINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0 - 1	Reserved	-	
2	OpenLineAnalogOutput01, 02	0	Line OK
		1	Open line
3	ConversionErrorAnalogOutput01, 02	0	Conversion temperature OK
		1	Conversion temperature too high
4 - 6	Reserved	-	
7	IoSuppErrorAnalogOutput01, 02	0	Module supply OK
		1	Module supply error

2.2.11.7 HART

HART (Highway Addressable Remote Transducer) is a protocol for communicating with intelligent field devices. It was developed in order to more efficiently use the infrastructure for transferring analog signals. The digital HART notifications are modulated to the analog signal using Frequency Shift Keying (FSK). HART can thus use the same physical line as the analog signal without influencing the original function.
HART slaves are able to determine different process data independently and prepare HART concordantly. This protocol supports polling of the value of a process variable as well as its unit and status. Field devices usually supply their information after the master requests it. In newer revisions, it is also possible to transfer configuration data.

There are 2 different types of HART networks. In a *point-to-point* network, only one slave is connected to a HART master. Here, the analog signal and the HART signal can be transferred over the same line. Managing several slaves with HART requires what is known as a *multidrop* network. Here, each HART slave is assigned and identified by a unique address. Classic analog signals cannot be clearly traced in bus systems. As a result, the HART protocol does not support analog information transfers in multidrop networks up to and including HART Revision 5.

Information:

Split range operation with HART AO modules

Beginning with HART revision 6, bus stations that use an analog signal according to the split range method are written to separately. The HART protocol supports multidrop addressing as well as the use of analog signals for these applications.

The module was designed based on HART-Revision 5. Only single-channel FSK scheme is available for transmitting the signals.

Since all HART frames are generated and evaluated in the application when using the FlatStream interface, information that isn't specified until later revisions can also be read.

2.2.11.7.1 HART - Configuration

HART modules are analog modules equipped with a HART modem. For each channel, a separate HART network can be managed by the module, which acts as a primary master. Once configured successfully, the HART information is stored in the module where it can then be used by the PLC.

The number of HART slaves must be specified in the configuration.
If only one slave is connected to the HART channel, then it is part of a point-to-point network. The module can then prepare up to 4 process variables from the connected slave.
Multidrop mode allows up to 15 HART slaves to be connected. The primary process variable from each slave is then retrieved.

2.2.11.7.1.1 HartNodeCnt

Name:
HartNodeCnt_1 to HartNodeCnt_2

These registers tell the module how many HART slaves are connected to a channel.

Information:

If a slave is not connected to one of the HART channels, the value "0" should be defined in this register. This shortens the I/O update time and avoids superfluous error messages.

Data type	Value	Information	
USINT	0	HART communication disabled for this channel	
	1	Point-to-point	Standard HART communication (bus controller default setting)
	2 to 15	Multidrop	Number of HART slave nodes

2.2.11.7.1.2 HartBurstNode

Name:
HartBurstNode_1 to HartBurstNode_2

In addition to the type of network, the user can also choose from 2 different types of communication behavior. Conventional HART communication relies on polling. The module queries the data from the HART slave individually and receives the corresponding information from the slave as a response. If a HART node should be queried in short time intervals, the user can configure burst mode for a node on each channel. In this case, the slave transmits the information from this node cyclically without a new request by the master.
The node numbers (short address) whose information should be queried using burst mode are entered by channel in the "HartBurstNode" registers. Burst mode is enabled using register "HartMode" on page 675.

Data type	Value	Information
USINT	0 to 15	Point-to-point. Bus controller default setting: 0

2.2.11.7.1.3 HartMode

Name:
HartMode_1 to HartMode_2

The user can use these registers to configure the communication behavior of each of the HART channels. Generally, the HART nodes are polled individually. This register can still be used to start or stop burst mode when needed. In burst mode, a node transmits its information cyclically instead of continuously. As a result, the HART standard allows the simultaneous usage of both burst mode and polling.

Information:

Register "HartBurstNode" on page 675 must be configured correctly for burst queries.

Data type	Values	Bus controller default setting
UINT	See bit structure.	0

Bit structure:

Bit	Name	Value	Information
0	Slave polling mode	0	Polling mode enabled (bus controller default setting)
		1	Polling mode disabled
1	Start slave burst mode	0	No response to burst (bus controller default setting)
		1	Enables burst mode in the "HartBurstNode" on page 675 node
2	Stop slave burst mode	0	No response to burst (bus controller default setting)
		1	Disables burst mode, if enabled
3 - 7	Reserved	-	

2.2.11.7.2 HART - Communication

After the configuration is completed, the information is retrieved automatically and transferred to the module registers. A separate register is implemented in the module for each piece of information. HART modules are designed to query up to 15 pieces of information per channel. The module reads in the data, stores it in temporary memory and prepares it for retrieval. When the X2X master accesses the module registers, it is irrelevant whether the HART data originates from a point-to-point or multidrop network.

Overview of internal module mapping

	Point-to-point network (1 HART slave)	*Multidrop network (2 to 15 HART slaves)*
(Pv)Input_01	Primary piece of information from HART node 1	Primary piece of information from HART node 1
(Pv)Input_02	Secondary piece of information from HART node 1	Primary piece of information from HART node 2
...	...	...
(Pv)Input_04	Quaternary piece of information from HART node 1	Primary piece of information from HART node 4
(Pv)Input_05	Reserved	Primary piece of information from HART node 5
...	...	...
(Pv)Input_15	Reserved	Primary piece of information from HART node 15

The HART specifications stipulates that information from a HART node be split into various pieces. The value of a process variable is stored to the respective "PvInput" on page 676 register and has a size of 4 bytes (REAL) per the HART specification. Due to the length limitation of 30 bytes on the X2X Link network, there are limitations to the number of possible cyclic variables. It is recommended to transfer a maximum of 2 "PvInput" on page 676 registers cyclically to the X2X master. All other information should be read in a different way. To access HART information, the user can choose between the following methods:

- **Acyclic** - If library AsIOAcc is used, information is queried acyclically only when it is needed, i.e. communication can be adapted to the program sequence of the X2X master. In this way, all of the necessary module registers on the X2X Link network can be queried despite the length limitation.
  This type of information exchange is not real-time capable.
- **Cyclic:** Data points configured for cyclic transfer are read once per bus cycle. This procedure allows real-time capable information exchange between the module and X2X master. The length limitation may prevent all data from being queried within one cycle, however.
- **Multiplexed** - A runtime driver can be used to transfer the HART data points in the I/O mapping. In this case, the HART process data is transmitted alternately (time multiplexed). Communication remains real-time capable. Multiple bus cycles are needed to update all data points, however.

  > **Information:**
  >
  > **This mode cannot be used when using the module after a bus controller.**
  >
  > **"Multiplexed" data transfer is used only for HART data points.**
  >
  > **Information from the analog inputs/outputs is always transferred cyclically (see above).**

- **Flatstream** - HART modules are equipped with a Flatstream interface. When using Flatstream communication, the module is used as a bridge between the X2X master and HART slave, i.e. the X2X master communicates directly with the HART slave (see "Flatstream communication" on page 681).
  Flatstream communication is also not real-time capable. It allows unrestricted access to the HART slave. The user must have sufficient knowledge of the HART protocol command set as well as the capabilities of the corresponding HART slave.

2.2.11.7.2.1 PvInput

Name:
PvInput01_01 to PvInput01_15
PvInput02_01 to PvInput02_15

These registers return the current value of the process variable that has been read.

> **Information:**
>
> **These registers are of data type REAL, which means that the available bytes on the X2X Link are filled more quickly when operated cyclically. If information from several slave nodes is needed, it must be retrieved acyclically or using Flatstream .**

Data type	Value	Information
REAL	IEEE745 SPF	32-bit data type with valid value
	0x7FA00000	Not a number (NaN) with invalid value

2.2.11.7.2.2 PvUnit

Name:
PvUnit01_01 to PvUnit01_15
PvUnit02_01 to PvUnit02_15

These registers return a HART-specific code that specifies the unit for the measured value. The coding for this is established in the HART specification.

Data type	Value
USINT	See description of the HART slave See HART specification

2.2.11.7.2.3 PvSampleTime

Name:
PvSampleTime01 to PvSampleTime02
PvSampleTime01_01 to PvSampleTime01_15
PvSampleTime02_01 to PvSampleTime02_15

These registers return the timestamp for when the module reads the current channel mapping. The values are provided as signed 2-byte or 4-byte values.

For additional information about NetTime and timestamps, see "NetTime Technology" on page 712.

Data type	Values	Information
INT	-32,768 to 32767	NetTime timestamp of the current input value in µs
DINT	-2147483648 to 2147483647	NetTime timestamp of the current input value in µs

This refers to the point in time when the HART master receives the slave's response. This is a way to check whether new HART information has been read since the last X2X cycle.

Information:

The cycle times of a HART network are relatively long so that it is not possible to reliably determine when the measured value is retrieved with just this information.

2.2.11.7.2.4 PvNodeComStatus

Name:
PvNodeComStatus01 to PvNodeComStatus02
PvNodeComStatus01_01 to PvNodeComStatus01_15
PvNodeComStatus02_01 to PvNodeComStatus02_15

These registers provide information about whether a read value is valid. Per the HART specification, this type of status register consists of 2 parts. The "response code" is stored in the high byte; the "field device status" is stored in the low byte. This makes it possible to check the current state of a read process variable.

These registers can be checked before further processing information in temporary storage. If the current value is 0x0000, an error was not detected during the HART transfer and the information from the checked node can be used. If a different value is present, the situation in the HART network should be checked. This can be done using an extension register, for example.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Quality - Node information 2 to n	0	Digital measured value okay
		1	Measured value outside the permitted range
1	Quality - Node information 1	0	Digital measured value okay
		1	Measured value outside the permitted range
2	Limit violation	0	Parameter okay
		1	Invalid measured value(s) or encoder supply value
3	Static analog signal	0	Normal value change/fluctuation
		1	Constant analog value of Node 1 slave
4	Additional status information (only supported by a few slaves)	0	Not available
		1	Available (only using Flatstream command #48)
5	Restart	0	Normal operation
		1	Field device restarts
6	Device ID	0	Unchanged
		1	Changed
7	Device error	0	Measured value okay
		1	Questionable measured value information
8 - 14	Response code, if relevant	x	See **HART-specific response code**
15	Error - Communication	0	Error-free communication (response code irrelevant)
		1	Faulty communication (response code relevant)

HART-specific response code (excerpt):

0x82 … Receive buffer overflow 0x88 … Checksum incorrect 0x90 … Faulty protocol structure 0xA0 … Overrun 0xC0 … Parity not allowed 0xFF … Timeout	If a HART communication error occurs, the response code is written. Bit 15 is always set.

Retrieving information that has been read

After the node data has been transferred to the module registers, the information can be retrieved from the module. A separate register in the module is implemented for each piece of information.

2.2.11.7.2.5 PvCountHartRequest

Name:
PvCountHartRequest01 to PvCountHartRequest02

These registers are increased once the module is ready to transmit a message to the corresponding channel.

Data type	Values
UDINT	0 to 4,294,967,295

2.2.11.7.2.6 PvCountHartTimeout

Name:
PvCountHartTimeout01 to PvCountHartTimeout02

These registers are increased if the slave exceeds the maximum permitted time before responding to the module's request.

Data type	Values
UDINT	0 to 4,294,967,295

2.2.11.7.2.7 PvCountHartRxError

Name:
PvCountHartRxError01 to PvCountHartRxError02

These registers are increased if communication errors occur on Layer 1 of the OSI model (e.g. transmission error as per parity bit).

Data type	Values
UDINT	0 to 4,294,967,295

2.2.11.7.2.8 PvCountHartFrameError

Name:
PvCountHartFrameError01 to PvCountHartFrameError02

These registers are increased if communication errors occur on Layer 2 of the OSI model (e.g. faulty telegram structure).

Data type	Values
UDINT	0 to 4,294,967,295

2.2.11.7.2.9 PvNodeFound

Name:
PvNodeFound01 to PvNodeFound02

These registers provide information about which nodes were detected on which channel (slave identified successfully).

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Node 0 (default mode) Node 1 (multidrop mode)	0	Not detected as valid
		1	Detected as valid
1	Node 2 (multidrop mode)	0	Not detected as valid
		1	Detected as valid
...		...	
13	Node 14 (multidrop mode)	0	Not detected as valid
		1	Detected as valid
14	Node 15 (multidrop mode)	0	Not detected as valid
		1	Detected as valid
15	Reserved	-	

2.2.11.7.2.10 PvNodeError

Name:
PvNodeError01 to PvNodeError02

These registers contain the HART communications error bits. These bits are set if the connection to a node was established successfully but the node at some point no longer responds as it should (e.g. the HART slave exceeds the configured timeout / number of retries).

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	Node 0 (default mode) Node 1 (multidrop mode)	0	Detected as having no errors
		1	Detected as having errors
1	Node 2 (multidrop mode)	0	Detected as having no errors
		1	Detected as having errors
...		...	
13	Node 14 (multidrop mode)	0	Detected as having no errors
		1	Detected as having errors
14	Node 15 (multidrop mode)	0	Detected as having no errors
		1	Detected as having errors
15	Reserved	-	

2.2.11.7.3 Extended configuration

The additional configuration registers are specified values when the module is started. In most systems, the user does not need to make any adjustments here. Register values should only be changed if HART network communication is not taking place satisfactorily.

2.2.11.7.3.1 HartNodeDisable

Name:
HartNodeDisable_1 to HartNodeDisable_2

These registers are intended for things like maintenance. They make it possible to cut off configured HART nodes to suppress error messages for a certain period of time. During normal operation, the configured nodes must be switched active to guarantee that the procedure runs smoothly.

Data type	Values	Bus controller default setting
UINT	See bit structure.	0x3FFF

Bit structure:

Bit	Name	Value	Information
0	Node 0 (default mode) Node 1 (multidrop mode)	0	Enabled (bus controller default setting)
		1	Disabled
1	Node 2 (multidrop mode)	0	Enabled
		1	Disabled (bus controller default setting)
...		...	
13	Node 14 (multidrop mode)	0	Enabled
		1	Disabled (bus controller default setting)
14	Node 15 (multidrop mode)	0	Enabled
		1	Disabled (bus controller default setting)
15	Reserved	-	

2.2.11.7.3.2 HartProtTimeOut

Name:
HartProtTimeOut_1 to HartProtTimeOut_2

These registers specify the time span within which the slave must respond for the response to be valid.

Data type	Values [ms]	Information
UINT	0 to 65535	Bus controller default setting: 256 [ms]

2.2.11.7.3.3 HartProtRetry

Name:
HartProtRetry_1 to HartProtRetry_2

These registers determine how many times the master retries a request if it receives an invalid response or no response at all.

Data type	Value	Information
UINT	0 to 65535	Bus controller default setting: 3 attempts

2.2.11.7.3.4 HartPreamble

Name:
HartPreamble_1 to HartPreamble_2

The length of the preamble can be set in these registers. The preamble is used to synchronize the receiver to the transmitter. The longer the declared preamble, the less chance that a communication error will occur. Nevertheless, a useful signal is not transmitted during synchronization so the preamble should be kept as short as possible.

Data type	Value	Information
UINT	5 to 20	Bus controller default setting: 20

2.2.11.8 Flatstream communication

2.2.11.8.1 Introduction

B&R offers an additional communication method for some modules. "Flatstream" was designed for X2X and POWERLINK networks and allows data transmission to be adapted to individual demands. Although this method is not 100% real-time capable, it still allows data transfer to be handled more efficiently than with standard cyclic polling.

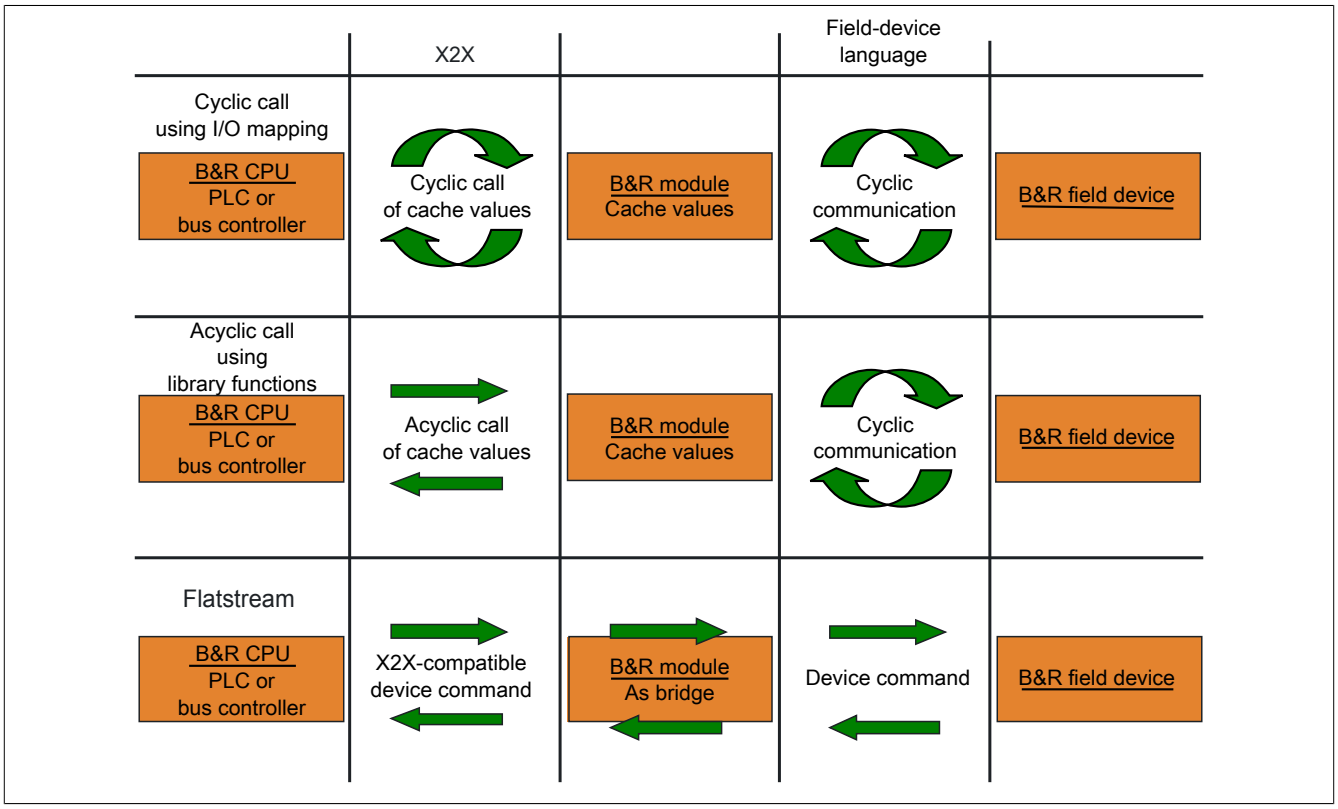


Figure 83: 3 types of communication

Flatstream extends cyclic and acyclic data queries. With Flatstream communication, the module acts as a bridge. The module is used to pass CPU queries directly on to the field device.

2.2.11.8.2 Message, segment, sequence, MTU

The physical properties of the bus system limit the amount of data that can be transmitted during one bus cycle. With Flatstream communication, all messages are viewed as part of a continuous data stream. Long data streams must be broken down into several fragments that are sent one after the other. To understand how the receiver puts these fragments back together to get the original information, it is important to understand the difference between a message, a segment, a sequence and an MTU.

Message

A message refers to information exchanged between 2 communicating partner stations. The length of a message is not restricted by the Flatstream communication method. Nevertheless, module-specific limitations must be considered.

Segment (logical division of a message):

A segment has a finite size and can be understood as a section of a message. The number of segments per message is arbitrary. So that the recipient can correctly reassemble the transferred segments, each segment is preceded by a byte with additional information. This control byte contains information such as the length of a segment and whether the approaching segment completes the message. This makes it possible for the receiving station to interpret the incoming data stream correctly.

Sequence (how a segment must be arranged physically):

The maximum size of a sequence corresponds to the number of enabled Rx or Tx bytes (later: "MTU"). The transmitting station splits the transmit array into valid sequences. These sequences are then written successively to the MTU and transferred to the receiving station where they are put back together again. The receiver stores the incoming sequences in a receive array, obtaining an image of the data stream in the process.
With Flatstream communication, the number of sequences sent are counted. Successfully transferred sequences must be acknowledged by the receiving station to ensure the integrity of the transfer.

MTU (Maximum Transmission Unit) - Physical transport:

MTU refers to the enabled USINT registers used with Flatstream. These registers can accept at least one sequence and transfer it to the receiving station. A separate MTU is defined for each direction of communication. OutputMTU defines the number of Flatstream Tx bytes, and InputMTU specifies the number of Flatstream Rx bytes. The MTUs are transported cyclically via the X2X Link network, increasing the load with each additional enabled USINT register.

Properties

Flatstream messages are not transferred cyclically or in 100% real time. Many bus cycles may be needed to transfer a particular message. Although the Rx and Tx registers are exchanged between the transmitter and the receiver cyclically, they are only processed further if explicitly accepted by register "InputSequence" or "OutputSequence".

Behavior in the event of an error (brief summary)

The protocol for X2X and POWERLINK networks specifies that the last valid values should be retained when disturbances occur. With conventional communication (cyclic/acyclic data queries), this type of error can generally be ignored.
In order for communication to also take place without errors using Flatstream, all of the sequences issued by the receiver must be acknowledged. If Forward functionality is not used, then subsequent communication is delayed for the length of the disturbance.
If Forward functionality is being used, the receiving station receives a transmission counter that is incremented twice. The receiver stops, i.e. it no longer returns any acknowledgments. The transmitting station uses SequenceAck to determine that the transmission was faulty and that all affected sequences must be repeated.

2.2.11.8.3 The Flatstream principle

Requirement

Before Flatstream can be used, the respective communication direction must be synchronized, i.e. both communication partners cyclically query the sequence counter on the opposite station. This checks to see if there is new data that should be accepted.

Communication

If a communication partner wants to transmit a message to its opposite station, it should first create a transmit array that corresponds to Flatstream conventions. This allows the Flatstream data to be organized very efficiently without having to block other important resources.

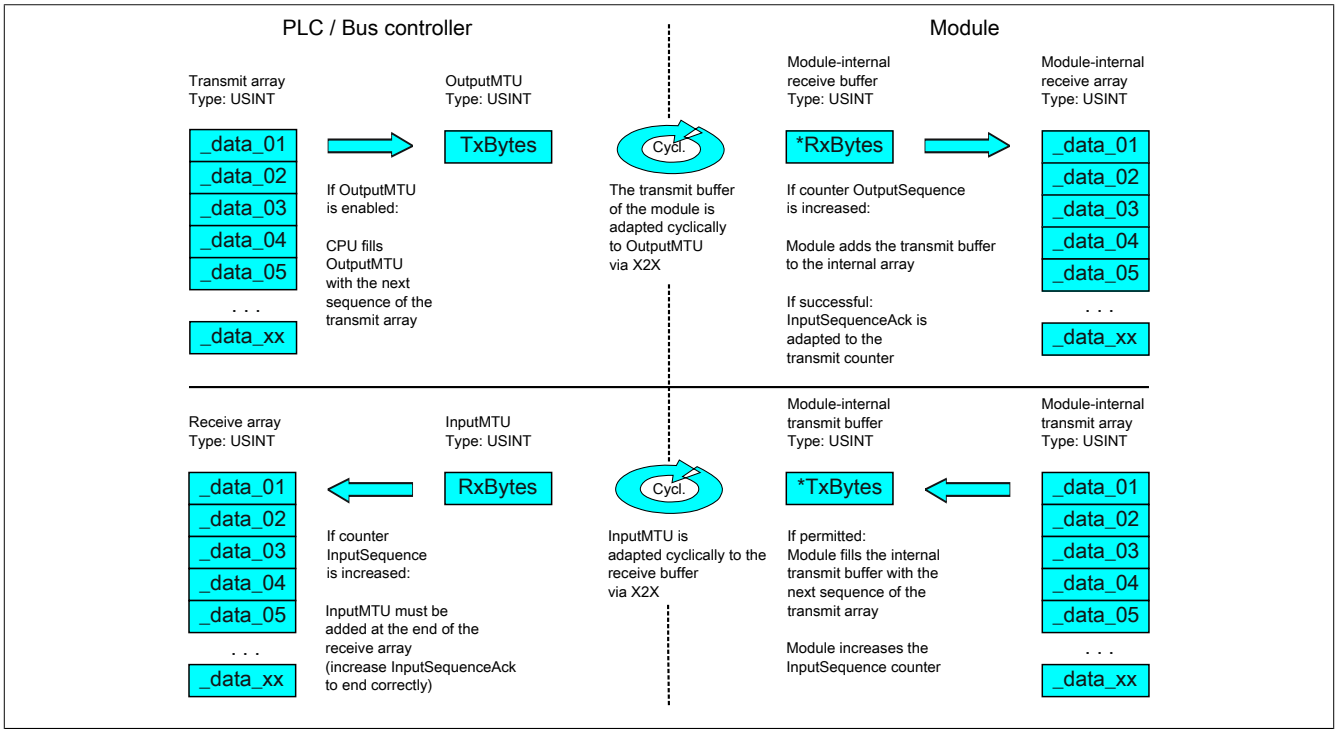


Figure 84: Flatstream communication

Procedure

The first thing that happens is that the message is broken into valid segments of up to 63 bytes, and the corresponding control bytes are created. The data is formed into a data stream made up of one control bytes per associated segment. This data stream can be written to the transmit array. The maximum size of each array element matches that of the enabled MTU so that one element corresponds to one sequence.
If the array has been completely created, the transmitter checks whether the MTU is permitted to be refilled. It then copies the first element of the array or the first sequence to the Tx byte registers. The MTU is transported to the receiver station via X2X Link and stored in the corresponding Rx byte registers. To signal that the data should be accepted by the receiver, the transmitter increases its SequenceCounter.
If the communication direction is synchronized, the opposite station detects the incremented SequenceCounter. The current sequence is appended to the receive array and acknowledged by SequenceAck. This acknowledgment signals to the transmitter that the MTU can now be refilled.

If the transfer is successful, the data in the receive array will correspond 100% to the data in the transmit array. During the transfer, the receiving station must detect and evaluate the incoming control bytes. A separate receive array should be created for each message. This allows the receiver to immediately begin further processing of messages that are completely transferred.

2.2.11.8.4 Registers for Flatstream mode

5 registers are available for configuring Flatstream. The default configuration can be used to transmit small amounts of data relatively easily.

Information:

The CPU communicates directly with the field device via registers "OutputSequence" and "InputSequence" as well as the enabled Tx and Rx bytes. For this reason, the user needs to have sufficient knowledge of the communication protocol being used on the field device.

2.2.11.8.4.1 Flatstream configuration

To use Flatstream, the program sequence must first be expanded. The cycle time of the Flatstream routines must be set to a multiple of the bus cycle. Other program routines should be implemented in Cyclic #1 to ensure data consistency.

At the absolute minimum, registers "InputMTU" and "OutputMTU" must be set. All other registers are filled in with default values at the beginning and can be used immediately. These registers are used for additional options, e.g. to transfer data in a more compact way or to increase the efficiency of the general procedure.

The Forward registers extend the functionality of the Flatstream protocol. This functionality is useful for substantially increasing the Flatstream data rate, but it also requires quite a bit of extra work when creating the program sequence.

Number of enabled Tx and Rx bytes

Name:
OutputMTU
InputMTU

These registers define the number of enabled Tx or Rx bytes and thus also the maximum size of a sequence. The user must consider that the more bytes made available also means a higher load on the bus system.

Information:

In the rest of this description, the names "OutputMTU" and "InputMTU" do not refer to the registers explained here. Instead, they are used as synonyms for the currently enabled Tx or Rx bytes.

Data type	Values
USINT	See the module-specific register overview (theoretically: 3 to 27).

2.2.11.8.4.2 Flatstream operation

When using Flatstream, the communication direction is very important. For transmitting data to a module (output direction), Tx bytes are used. For receiving data from a module (input direction), Rx bytes are used.
Registers "OutputSequence" and "InputSequence" are used to control and ensure that communication is taking place properly, i.e. the transmitter issues the directive that the data should be accepted and the receiver acknowledges that a sequence has been transferred successfully.

Format of input and output bytes

Name:

"Format of Flatstream" in Automation Studio

On some modules, this function can be used to set how the Flatstream input and output bytes (Tx or Rx bytes) are transferred.

- **Packed:** Data is transferred as an array.
- **Byte-by-byte:** Data is transferred as individual bytes.

Transport of payload data and control bytes

Name:
TxByte1 to TxByteN
RxByte1 to RxByteN

(The value the number N is different depending on the bus controller model used.)

The Tx and Rx bytes are cyclic registers used to transport the payload data and the necessary control bytes. The number of active Tx and Rx bytes is taken from the configuration of registers "OutputMTU" and "InputMTU", respectively.
In the user program, only the Tx and Rx bytes from the CPU can be used. The corresponding counterparts are located in the module and are not accessible to the user. For this reason, the names were chosen from the point of view of the CPU.

- "T" - "Transmit" →CPU *transmits* data to the module.
- "R" - "Receive" →CPU *receives* data from the module.

Data type	Values
USINT	0 to 255

Control bytes

In addition to the payload data, the Tx and Rx bytes also transfer the necessary control bytes. These control bytes contain additional information about the data stream so that the receiver can reconstruct the original message from the transferred segments.

Bit structure of a control byte

Bit	Name	Value	Information
0 - 5	SegmentLength	0 - 63	Size of the subsequent segment in bytes (default: Max. MTU size - 1)
6	nextCBPos	0	Next control byte at the beginning of the next MTU
		1	Next control byte directly after the end of the current segment
7	MessageEndBit	0	Message continues after the subsequent segment
		1	Message ended by the subsequent segment

SegmentLength

The segment length lets the receiver know the length of the coming segment. If the set segment length is insufficient for a message, then the information must be distributed over several segments. In these cases, the actual end of the message is detected using bit 7 (control byte).

Information:

The control byte is not included in the calculation to determine the segment length. The segment length is only derived from the bytes of payload data.

nextCBPos

This bit indicates the position where the next control byte is expected. This information is especially important when using option "MultiSegmentMTU".
When using Flatstream communication with MultiSegmentMTUs, the next control byte is no longer expected in the first Rx byte of the subsequent MTU, but transferred directly after the current segment.

MessageEndBit

"MessageEndBit" is set if the subsequent segment completes a message. The message has then been completely transferred and is ready for further processing.

Information:

In the output direction, this bit must also be set if one individual segment is enough to hold the entire message. The module will only process a message internally if this identifier is detected.
The size of the message being transferred can be calculated by adding all of the message's segment lengths together.

Flatstream formula for calculating message length:

Message [bytes] = Segment lengths (all CBs without ME) + Segment length (of the first CB with ME)	CB	Control byte
	ME	MessageEndBit

Communication status of the CPU

Name:
OutputSequence

Register "OutputSequence" contains information about the communication status of the CPU. It is written by the CPU and read by the module.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	OutputSequenceCounter	0 - 7	Counter for the sequences issued in the output direction
3	OutputSyncBit	0	Output direction disabled
		1	Output direction enabled
4 - 6	InputSequenceAck	0 - 7	Mirrors InputSequenceCounter
7	InputSyncAck	0	Input direction not ready (disabled)
		1	Input direction ready (enabled)

OutputSequenceCounter

The OutputSequenceCounter is a continuous counter of sequences that have been issued by the CPU. The CPU uses OutputSequenceCounter to direct the module to accept a sequence (the output direction must be synchronized when this happens).

OutputSyncBit

The CPU uses OutputSyncBit to attempt to synchronize the output channel.

InputSequenceAck

InputSequenceAck is used for acknowledgment. The value of InputSequenceCounter is mirrored if the CPU has received a sequence successfully.

InputSyncAck

The InputSyncAck bit acknowledges the synchronization of the input channel for the module. This indicates that the CPU is ready to receive data.

Communication status of the module

Name:
InputSequence

Register "InputSequence" contains information about the communication status of the module. It is written by the module and should only be read by the CPU.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 2	InputSequenceCounter	0 - 7	Counter for sequences issued in the input direction
3	InputSyncBit	0	Not ready (disabled)
		1	Ready (enabled)
4 - 6	OutputSequenceAck	0 - 7	Mirrors OutputSequenceCounter
7	OutputSyncAck	0	Not ready (disabled)
		1	Ready (enabled)

InputSequenceCounter

The InputSequenceCounter is a continuous counter of sequences that have been issued by the module. The module uses InputSequenceCounter to direct the CPU to accept a sequence (the input direction must be synchronized when this happens).

InputSyncBit

The module uses InputSyncBit to attempt to synchronize the input channel.

OutputSequenceAck

OutputSequenceAck is used for acknowledgment. The value of OutputSequenceCounter is mirrored if the module has received a sequence successfully.

OutputSyncAck

The OutputSyncAck bit acknowledges the synchronization of the output channel for the CPU. This indicates that the module is ready to receive data.

Relationship between OutputSequence and InputSequence

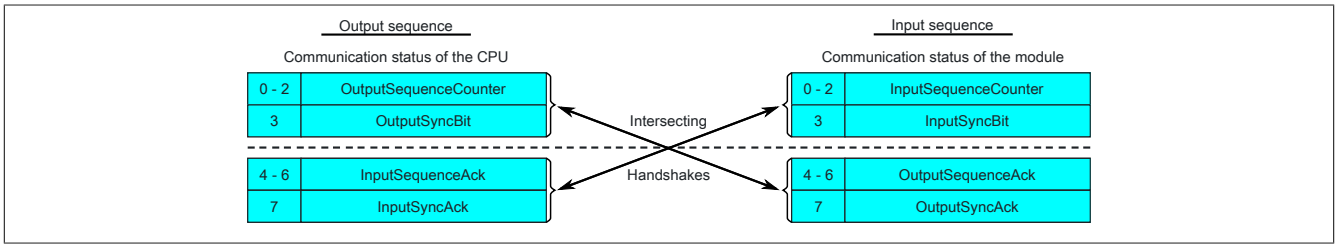


Figure 85: Relationship between OutputSequence and InputSequence

Registers "OutputSequence" and "InputSequence" are logically composed of 2 half-bytes. The low part signals to the opposite station whether a channel should be opened or if data should be accepted. The high part is to acknowledge that the requested action was carried out.

SyncBit and SyncAck

If SyncBit and SyncAck are set in one communication direction, then the channel is considered "synchronized", i.e. it is possible to send messages in this direction. The status bit of the opposite station must be checked cyclically. If SyncAck has been reset, then SyncBit on that station must be adjusted. Before new data can be transferred, the channel must be resynchronized.

SequenceCounter and SequenceAck

The communication partners cyclically check whether the low nibble on the opposite station changes. When one of the communication partners finishes writing a new sequence to the MTU, it increments its SequenceCounter. The current sequence is then transmitted to the receiver, which acknowledges its receipt with SequenceAck. In this way, a "handshake" is initiated.

Information:

If communication is interrupted, segments from the unfinished message are discarded. All messages that were transferred completely are processed.

2.2.11.8.4.3 Synchronization

During synchronization, a communication channel is opened. It is important to make sure that a module is present and that the current value of SequenceCounter is stored on the station receiving the message.
Flatstream can handle full-duplex communication. This means that both channels / communication directions can be handled separately. They must be synchronized independently so that simplex communication can theoretically be carried out as well.

Synchronization in the output direction (CPU as the transmitter):

The corresponding synchronization bits (OutputSyncBit and OutputSyncAck) are reset. Because of this, Flatstream cannot be used at this point in time to transfer messages from the CPU to the module.

Algorithm

1) The CPU must write 000 to OutputSequenceCounter and reset OutputSyncBit. The CPU must cyclically query the high nibble of register "InputSequence" (checks for 000 in OutputSequenceAck and 0 in OutputSyncAck).
The module does not accept the current contents of InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
2) If the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is permitted to increment OutputSequenceCounter. The CPU continues cyclically querying the high nibble of register "OutputSequence" (checks for 001 in OutputSequenceAck and 0 in InputSyncAck).
The module does not accept the current contents of InputMTU since the channel is not yet synchronized. *The module matches OutputSequenceAck and OutputSyncAck to the values of OutputSequenceCounter and OutputSyncBit.*
3) If the CPU registers the expected values in OutputSequenceAck and OutputSyncAck, it is permitted to increment OutputSequenceCounter. The CPU continues cyclically querying the high nibble of register "OutputSequence" (checks for 001 in OutputSequenceAck and 1 in InputSyncAck). **Note:** Theoretically, data can be transferred from this point forward. However, it is still recommended to wait until the output direction is completely synchronized before transferring data.
The module sets OutputSyncAck.
The output direction is synchronized, and the CPU can transmit data to the module.

Synchronization in the input direction (CPU as the receiver):

The corresponding synchronization bits (InputSyncBit and InputSyncAck) are reset. Because of this, Flatstream cannot be used at this point in time to transfer messages from the module to the CPU.

Algorithm

The module writes 000 to InputSequenceCounter and resets InputSyncBit. *The module monitors the high nibble of register "OutputSequence" and expects 000 in InputSequenceAck and 0 in InputSyncAck.*
1) The CPU is not permitted to accept the current contents of InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it increments InputSequenceCounter. *The module monitors the high nibble of register "OutputSequence" and expects 001 in InputSequenceAck and 0 in InputSyncAck.*
2) The CPU is not permitted to accept the current contents of InputMTU since the channel is not yet synchronized. The CPU has to match InputSequenceAck and InputSyncAck to the values of InputSequenceCounter and InputSyncBit.
If the module registers the expected values in InputSequenceAck and InputSyncAck, it sets InputSyncBit. *The module monitors the high nibble of register "OutputSequence" and expects 1 in InputSyncAck.*
3) The CPU is permitted to set InputSyncAck. **Note:** Theoretically, data could already be transferred in this cycle. If InputSyncBit is set and InputSequenceCounter has been increased by 1, the values in the enabled Rx bytes must be accepted and acknowledged (see also "Communication in the input direction").
The input direction is synchronized, and the module can transmit data to the CPU.

2.2.11.8.4.4 Transmitting and receiving

If a channel is synchronized, then the remote station is ready to receive messages from the transmitter. Before the transmitter can send data, it must first create a transmit array in order to meet Flatstream requirements.

The transmitting station must also generate a control byte for each segment created. This control byte contains information about how the subsequent part of the data being transferred should be processed. The position of the next control byte in the data stream can vary. For this reason, it must be clearly defined at all times when a new control byte is being transmitted. The first control byte is always in the first byte of the first sequence. All subsequent positions are determined recursively.

Flatstream formula for calculating the position of the next control byte:

Position (of the next control byte) = Current position + 1 + Segment length

Example

3 autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The rest of the configuration corresponds to the default settings.

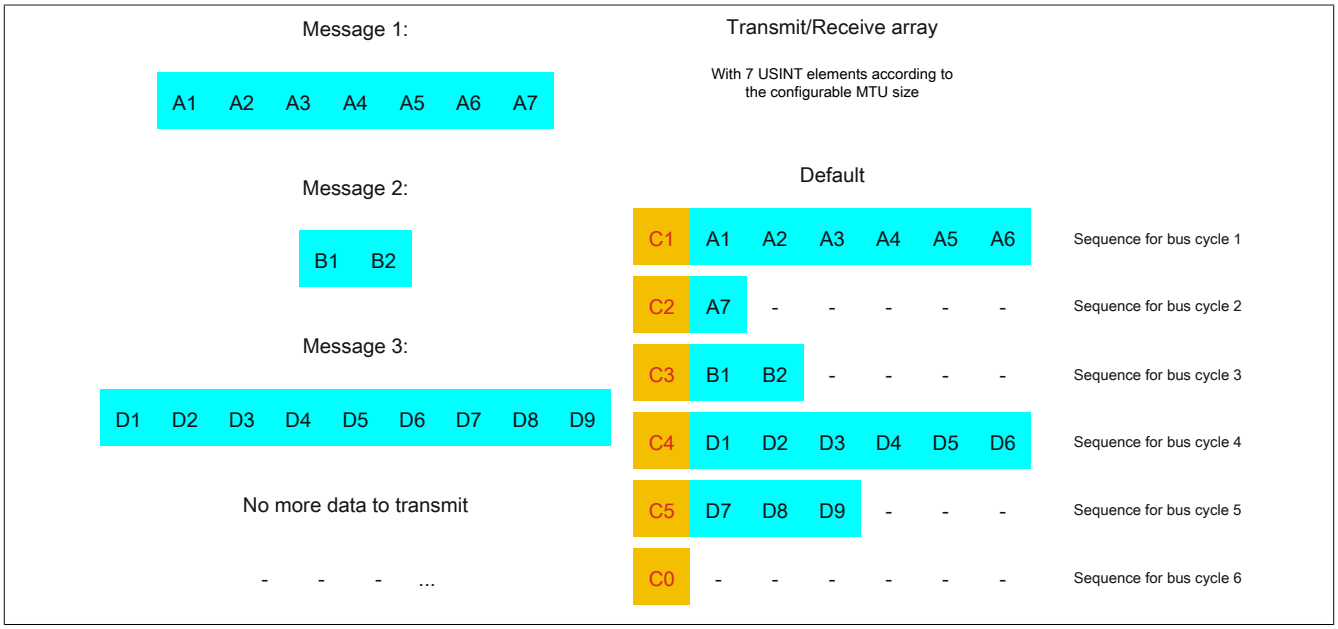


Figure 86: Transmit/Receive array (default)

The messages must first be split into segments. In the default configuration, it is important to ensure that each sequence can hold an entire segment, including the associated control byte. The sequence is limited to the size of the enable MTU. In other words, a segment must be at least 1 byte smaller than the MTU.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 1 data byte
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data
  - ⇨ Second segment = Control byte + 3 data bytes
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C0 (control byte 0)			**C1 (control byte 1)**			**C2 (control byte 2)**		
- SegmentLength (0)	=	0	- SegmentLength (6)	=	6	- SegmentLength (1)	=	1
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (0)	=	0	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	0	Control byte	Σ	6	Control byte	Σ	129

Table 101: Flatstream determination of the control bytes for the default configuration example (part 1)

C3 (control byte 3)			**C4 (control byte 4)**			**C5 (control byte 5)**		
- SegmentLength (2)	=	2	- SegmentLength (6)	=	6	- SegmentLength (3)	=	3
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	130	Control byte	Σ	6	Control byte	Σ	131

Table 102: Flatstream determination of the control bytes for the default configuration example (part 2)

2.2.11.8.4.5 Transmitting data to a module (output)

When transmitting data, the transmit array must be generated in the application program. Sequences are then transferred one by one using Flatstream and received by the module.

Information:

Although all B&R modules with Flatstream communication always support the most compact transfers in the output direction, it is recommended to use the same design for the transfer arrays in both communication directions.

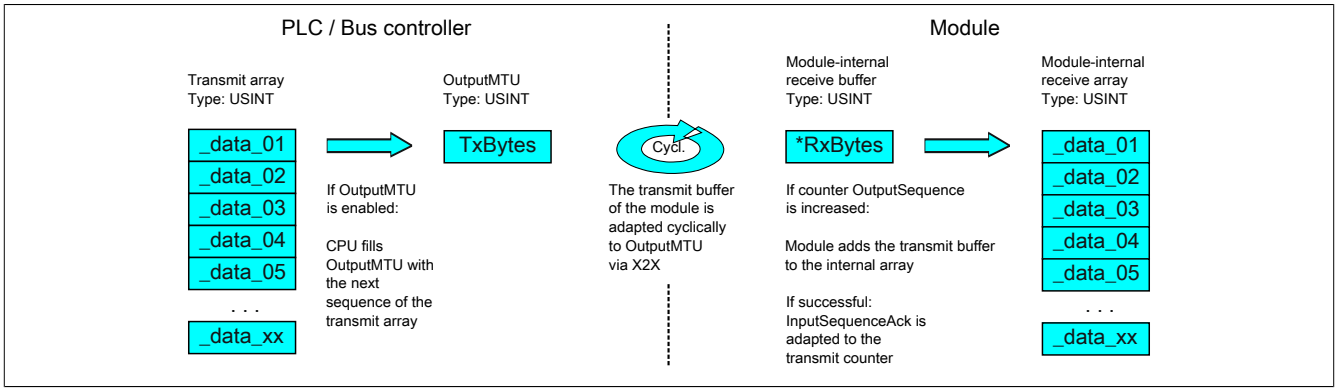


Figure 87: Flatstream communication (output)

Message smaller than OutputMTU

The length of the message is initially smaller than OutputMTU. In this case, one sequence would be sufficient to transfer the entire message and the necessary control byte.

Algorithm

Cyclic status query: *- The module monitors OutputSequenceCounter.*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > InputSequenceAck: MTU is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU transfers the current element of the transmit array to OutputMTU. → OutputMTU is transferred cyclically to the module's transmit buffer but not processed further. - The CPU must increase OutputSequenceCounter.
Reaction: *- The module accepts the bytes from the internal receive buffer and adds them to the internal receive array.* *- The module transmits acknowledgment and writes the value of OutputSequenceCounter to OutputSequenceAck.*
3) Completion: - The CPU must monitor OutputSequenceAck. → A sequence is only considered to have been transferred successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transfer errors in the last sequence as well, it is important to make sure that the length of the *Completion* phase is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transfer can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost. (The relationship of bus to task cycle can be influenced by the user so that the threshold value must be determined individually.) - Subsequent sequences are only permitted to be transmitted in the next bus cycle after the completion check has been carried out successfully.

Message larger than OutputMTU

The transmit array, which must be created in the program sequence, consists of several elements. The user has to arrange the control and data bytes correctly and transfer the array elements one after the other. The transfer algorithm remains the same and is repeated starting at the point *Cyclic checks*.

General flowchart

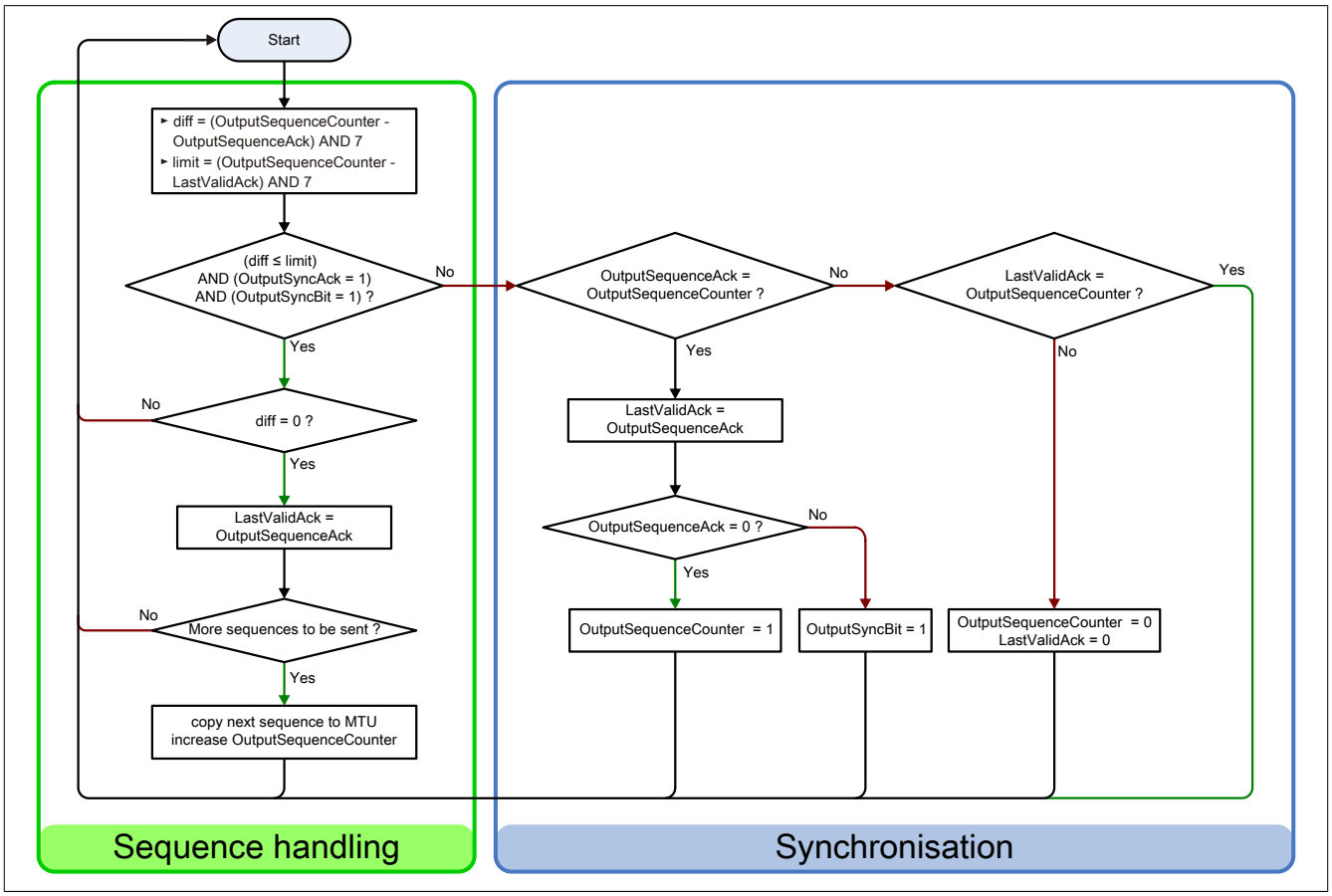


Figure 88: Flowchart for the output direction

2.2.11.8.4.6 Receiving data from a module (input)

When receiving data, the transmit array is generated by the module, transferred via Flatstream and must then be reproduced in the receive array. The structure of the incoming data stream can be set with the mode register. The algorithm for receiving the data remains unchanged in this regard.

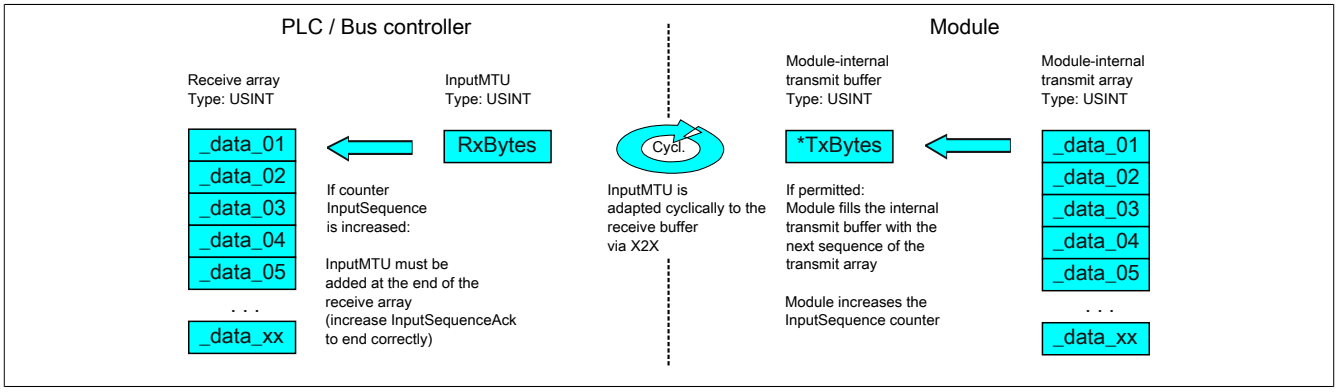


Figure 89: Flatstream communication (input)

Algorithm

0) Cyclic status query: - The CPU must monitor InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck.* *- The module checks InputSequenceAck.*
Preparation: *- The module forms the segments and control bytes and creates the transmit array.*
Action: *- The module transfers the current element of the internal transmit array to the internal transmit buffer.* *- The module increases InputSequenceCounter.*
1) Receiving (as soon as InputSequenceCounter is increased): - The CPU must apply data from InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck.* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.* *- Subsequent sequences are only transmitted in the next bus cycle after the completion check has been carried out successfully.*

General flowchart

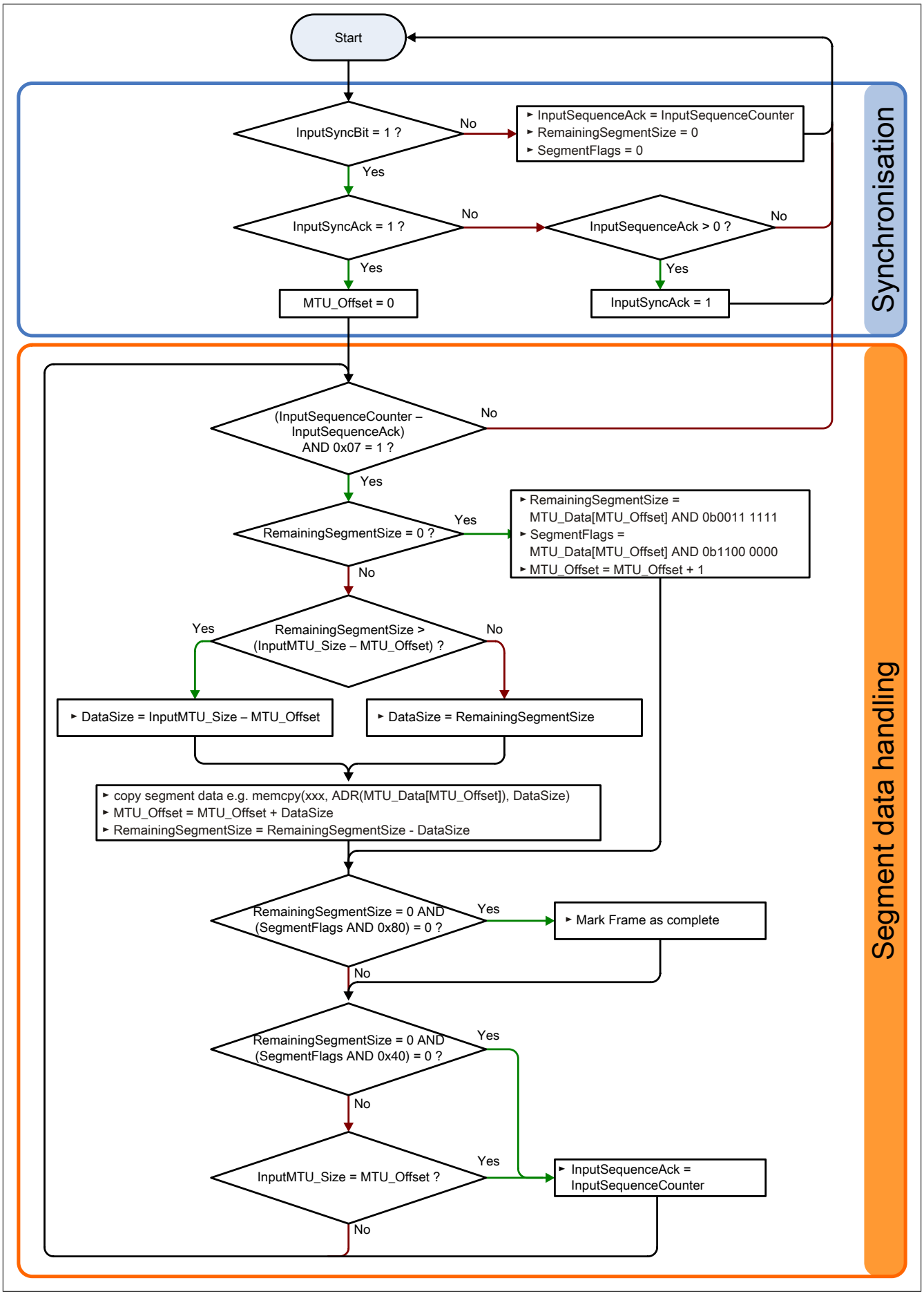


Figure 90: Flowchart for the input direction

2.2.11.8.4.7 Details

It is recommended to store transferred messages in separate receive arrays.

After a set MessageEndBit is transmitted, the subsequent segment should be added to the receive array. The message is then complete and can be passed on internally for further processing. A new/separate array should be created for the next message.

Information:

When transferring with MultiSegmentMTUs, it is possible for several small messages to be part of one sequence. In the program, it is important to make sure that a sufficient number of receive arrays can be managed. The acknowledge register is only permitted to be adjusted after the entire sequence has been applied.

If SequenceCounter is incremented by more than one counter, an error is present.

Note: This situation is very unlikely when operating without "Forward" functionality.

In this case, the receiver stops. All additional incoming sequences are ignored until the transmission with the correct SequenceCounter is retried. This response prevents the transmitter from receiving any more acknowledgments for transmitted sequences. The transmitter can identify the last successfully transferred sequence from the opposite station's SequenceAck and continue the transfer from this point.

Acknowledgments must be checked for validity.

If the receiver has successfully accepted a sequence, it must be acknowledged. The receiver takes on the value of SequenceCounter sent along with the transmission and matches SequenceAck to it. The transmitter reads SequenceAck and registers the successful transmission. If the transmitter acknowledges a sequence that has not yet been dispatched, then the transfer must be interrupted and the channel resynchronized. The synchronization bits are reset and the current/incomplete message is discarded. It must be sent again after the channel has been resynchronized.

2.2.11.8.4.8 Flatstream mode

Name:
FlatstreamMode

In the input direction, the transmit array is generated automatically. This register offers 2 options to the user that allow an incoming data stream to have a more compact arrangement. Once enabled, the program code for evaluation must be adapted accordingly.

Information:

All B&R modules that offer Flatstream mode support options "Large segments" and "MultiSegmentMTUs" in the output direction. Compact transfer must be explicitly allowed only in the input direction.

Bit structure:

Bit	Name	Value	Information
0	MultiSegmentMTU	0	Not allowed (default)
		1	Permitted
1	Large segments	0	Not allowed (default)
		1	Permitted
2 - 7	Reserved		

Standard

By default, both options relating to compact transfer in the input direction are disabled.

1. The module only forms segments that are at least one byte smaller than the enabled MTU. Each sequence begins with a control byte so that the data stream is clearly structured and relatively easy to evaluate.
2. Since a Flatstream message is permitted to be any length, the last segment of the message frequently does not fill up all of the MTU's space. By default, the remaining bytes during this type of transfer cycle are not used.

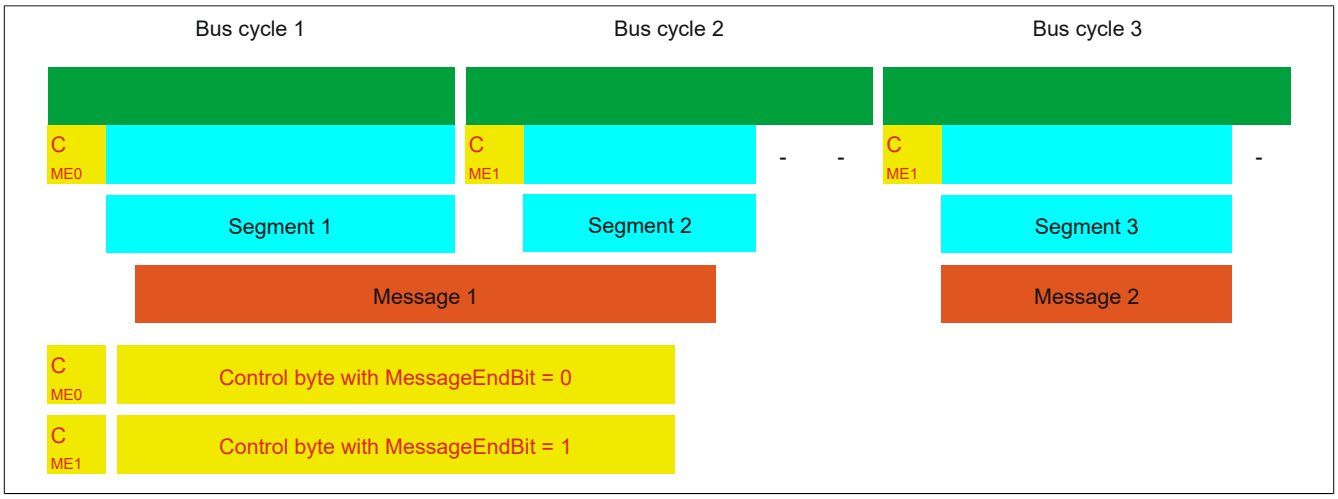


Figure 91: Message arrangement in the MTU (default)

MultiSegmentMTUs allowed

With this option, InputMTU is completely filled (if enough data is pending). The previously unfilled Rx bytes transfer the next control bytes and their segments. This allows the enabled Rx bytes to be used more efficiently.

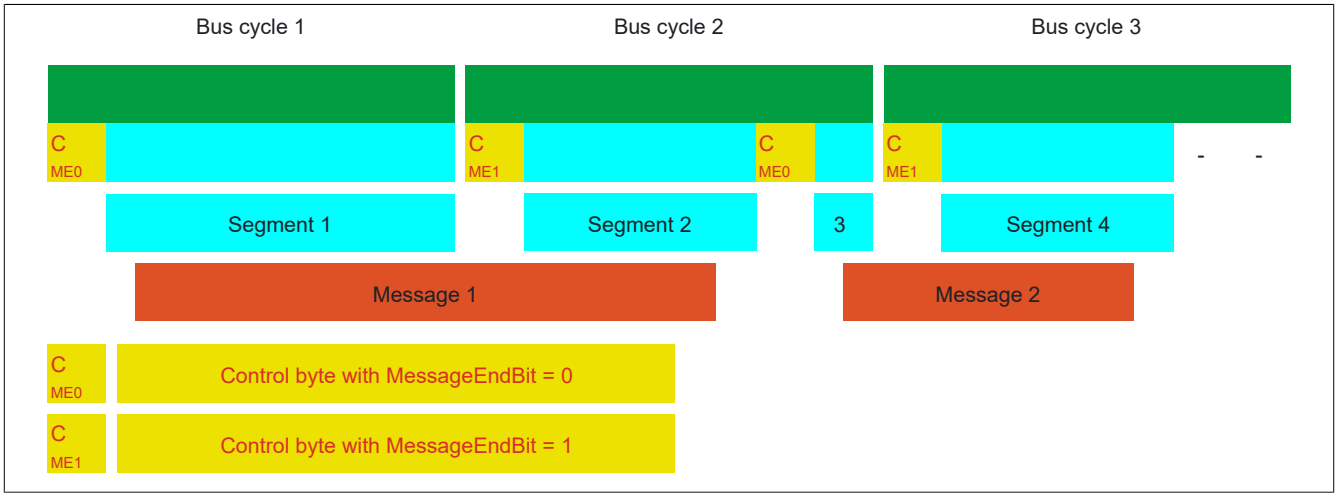


Figure 92: Arrangement of messages in the MTU (MultiSegmentMTUs)

Large segments allowed:

When transferring very long messages or when enabling only very few Rx bytes, then a great many segments must be created by default. The bus system is more stressed than necessary since an additional control byte must be created and transferred for each segment. With option "Large segments", the segment length is limited to 63 bytes independently of InputMTU. One segment is permitted to stretch across several sequences, i.e. it is possible for "pure" sequences to occur without a control byte.

Information:

It is still possible to split up a message into several segments, however. If this option is used and messages with more than 63 bytes occur, for example, then messages can still be split up among several segments.

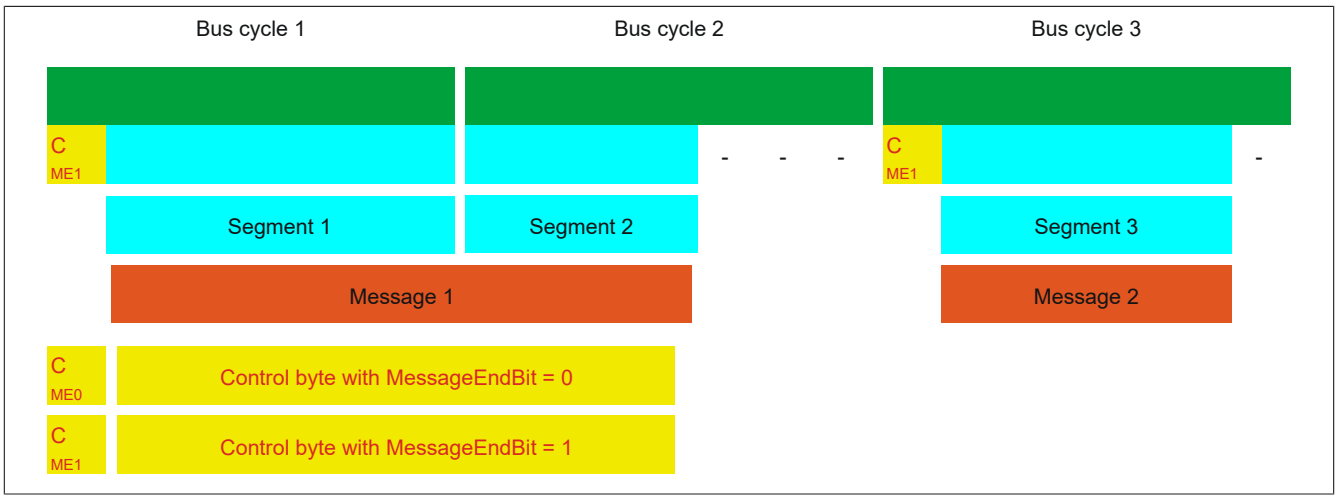


Figure 93: Arrangement of messages in the MTU (large segments)

Using both options

Using both options at the same time is also permitted.

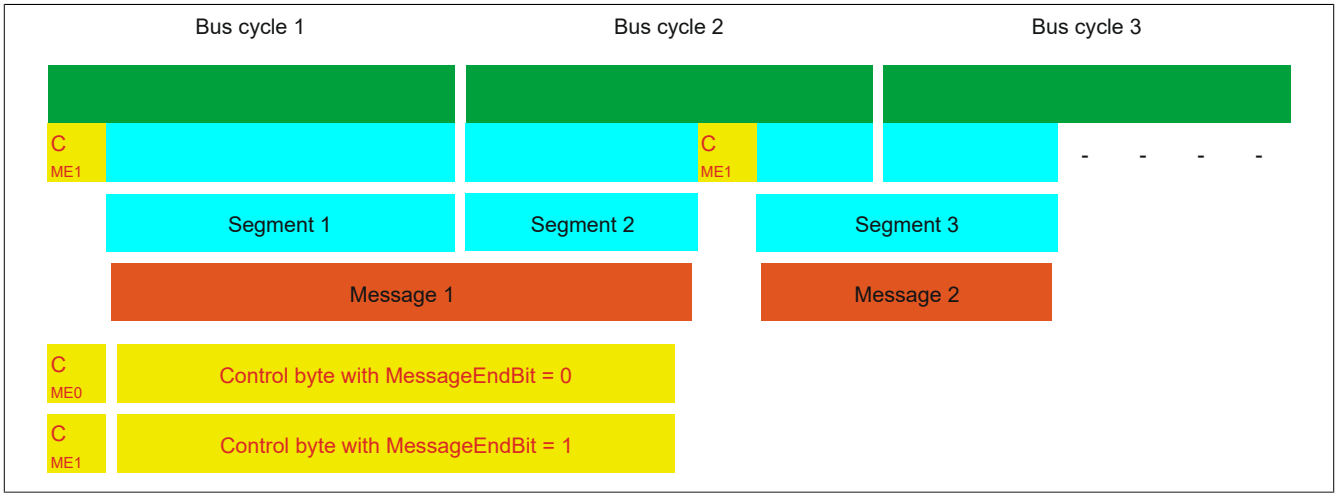


Figure 94: Arrangement of messages in the MTU (large segments and MultiSegmentMTUs)

2.2.11.8.4.9 Adjusting the Flatstream

If the way messages are structured is changed, then the way data in the transmit/receive array is arranged is also different. The following changes apply to the example given earlier.

MultiSegmentMTU

If MultiSegmentMTUs are allowed, then "open positions" in an MTU can be used. These "open positions" occur if the last segment in a message does not fully use the entire MTU. MultiSegmentMTUs allow these bits to be used to transfer the subsequent control bytes and segments. In the program sequence, the "nextCBPos" bit in the control byte is set so that the receiver can correctly identify the next control byte.

Example

3 autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows the transfer of MultiSegmentMTUs.

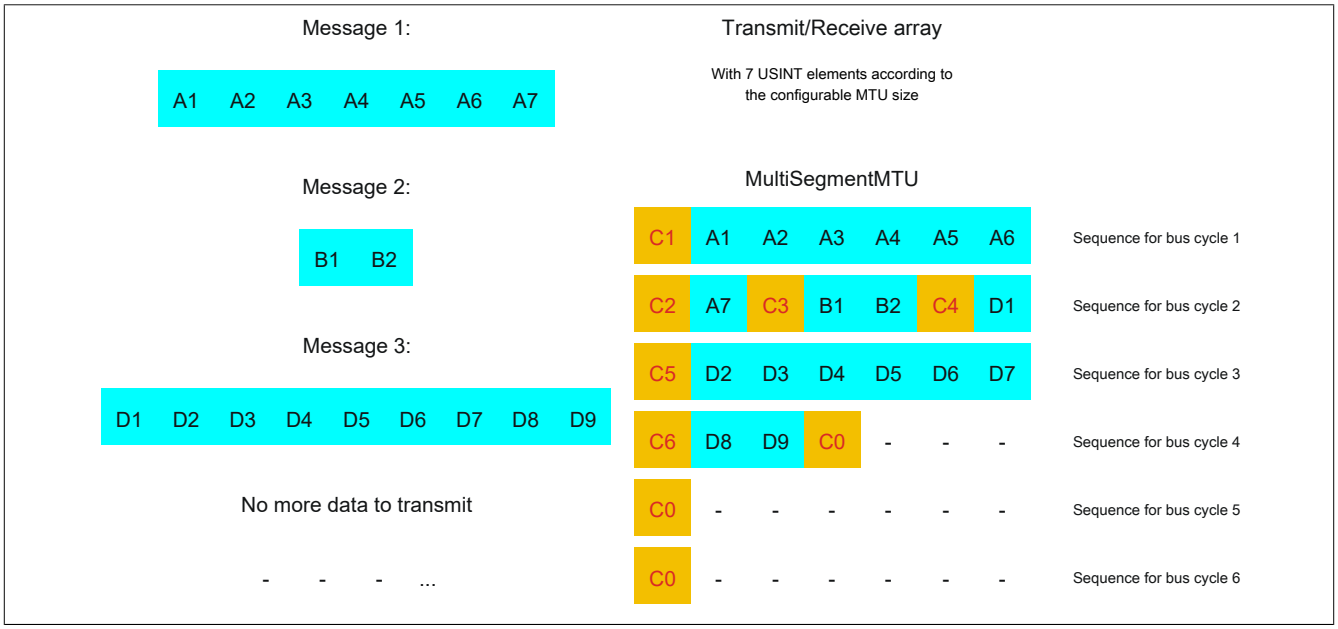


Figure 95: Transmit/receive array (MultiSegmentMTUs)

First, the messages must be split into segments. As in the default configuration, it is important for each sequence to begin with a control byte. The free bits in the MTU at the end of a message are filled with data from the following message, however. With this option, the "nextCBPos" bit is always set if payload data is transferred after the control byte.

MTU = 7 bytes → Max. segment length = 6 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Second segment = Control byte + 1 byte of data (MTU still has 5 open bytes)
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data (MTU still has 2 open bytes)
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 1 byte of data (MTU full)
  - ⇨ Second segment = Control byte + 6 bytes of data (MTU full)
  - ⇨ Third segment = Control byte + 2 bytes of data (MTU still has 4 open bytes)
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (6)	=	6	- SegmentLength (1)	=	1	- SegmentLength (2)	=	2
- nextCBPos (1)	=	64	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	70	Control byte	Σ	193	Control byte	Σ	194

Table 103: Flatstream determination of the control bytes for the MultiSegmentMTU example (part 1)

Warning!

The second sequence is only permitted to be acknowledged via SequenceAck if it has been completely processed. In this example, there are 3 different segments within the second sequence, i.e. the program must include enough receive arrays to handle this situation.

C4 (control byte 4)			C5 (control byte 5)			C6 (control byte 6)		
- SegmentLength (1)	=	1	- SegmentLength (6)	=	6	- SegmentLength (2)	=	2
- nextCBPos (6)	=	6	- nextCBPos (1)	=	64	- nextCBPos (1)	=	64
- MessageEndBit (0)	=	0	- MessageEndBit (1)	=	0	- MessageEndBit (1)	=	128
Control byte	Σ	7	Control byte	Σ	70	Control byte	Σ	194

Table 104: Flatstream determination of the control bytes for the MultiSegmentMTU example (part 2)

Large segments

Segments are limited to a maximum of 63 bytes. This means they can be larger than the active MTU. These large segments are divided among several sequences when transferred. It is possible for sequences to be completely filled with payload data and not have a control byte.

Information:

It is still possible to subdivide a message into several segments so that the size of a data packet does not also have to be limited to 63 bytes.

Example

3 autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows the transfer of large segments.

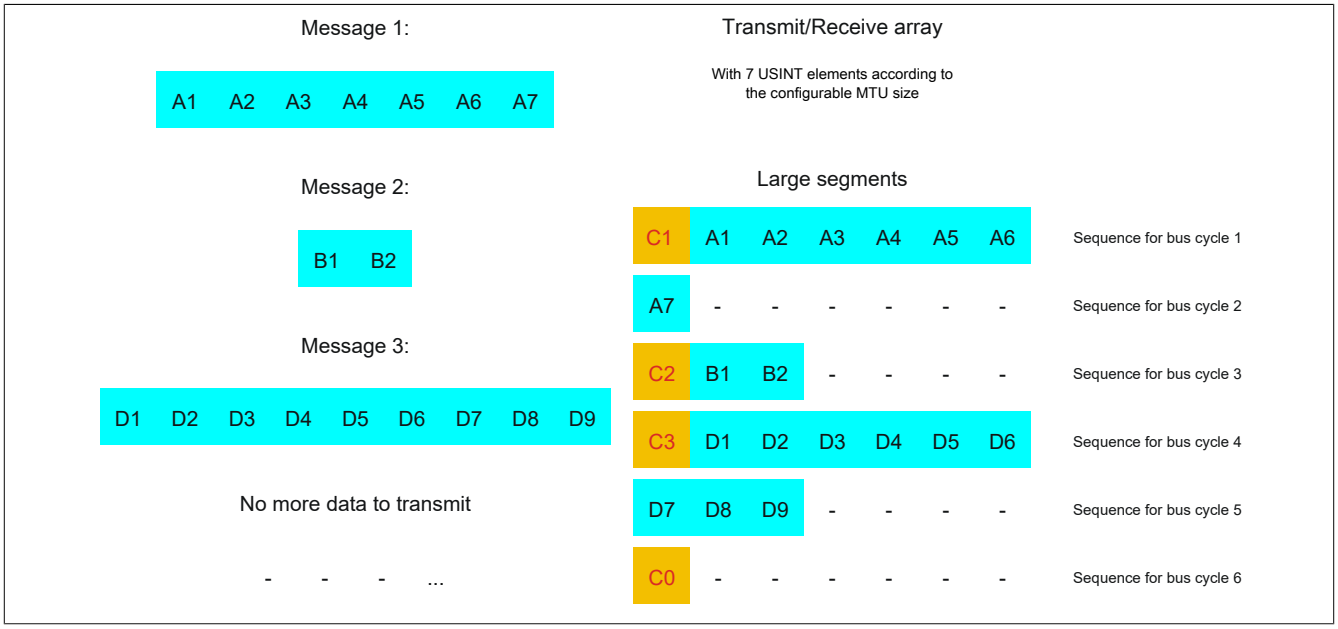


Figure 96: Transmit/receive array (large segments)

First, the messages must be split into segments. The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated.

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 7 bytes of data
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 9 bytes of data
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 105: Flatstream determination of the control bytes for the large segment example

Large segments and MultiSegmentMTU

Example

3 autonomous messages (7 bytes, 2 bytes and 9 bytes) are being transmitted using an MTU with a width of 7 bytes. The configuration allows transfer of large segments as well as MultiSegmentMTUs.

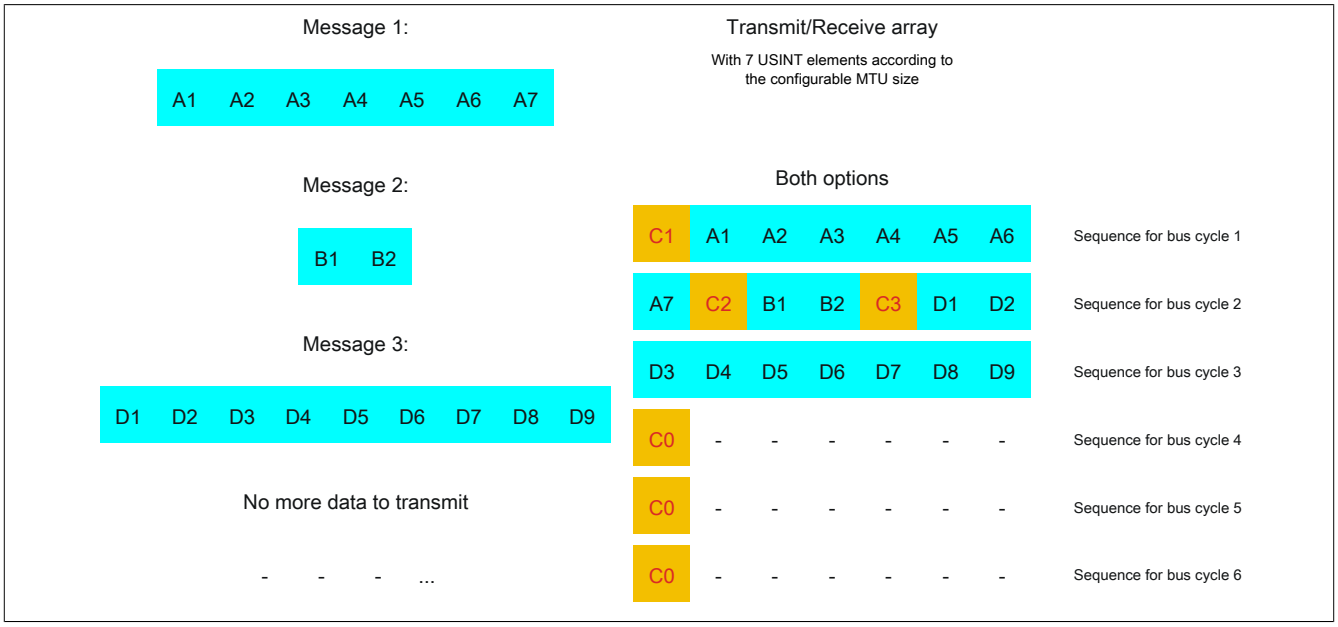


Figure 97: Transmit/receive array (large segments and MultiSegmentMTUs)

First, the messages must be split into segments. If the last segment of a message does not completely fill the MTU, it is permitted to be used for other data in the data stream. Bit "nextCBPos" must always be set if the control byte belongs to a segment with payload data.
The ability to form large segments means that messages are split up less frequently, which results in fewer control bytes generated. Control bytes are generated in the same way as with option "Large segments".

Large segments allowed → Max. segment length = 63 bytes

- Message 1 (7 bytes)
  - ⇨ First segment = Control byte + 7 bytes of data
- Message 2 (2 bytes)
  - ⇨ First segment = Control byte + 2 bytes of data
- Message 3 (9 bytes)
  - ⇨ First segment = Control byte + 9 bytes of data
- No more messages
  - ⇨ C0 control byte

A unique control byte must be generated for each segment. In addition, the C0 control byte is generated to keep communication on standby.

C1 (control byte 1)			C2 (control byte 2)			C3 (control byte 3)		
- SegmentLength (7)	=	7	- SegmentLength (2)	=	2	- SegmentLength (9)	=	9
- nextCBPos (0)	=	0	- nextCBPos (0)	=	0	- nextCBPos (0)	=	0
- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128	- MessageEndBit (1)	=	128
Control byte	Σ	135	Control byte	Σ	130	Control byte	Σ	137

Table 106: Flatstream determination of the control bytes for the large segment and MultiSegmentMTU example

2.2.11.8.5 Example of function "Forward" with X2X Link

Function "Forward" is a method that can be used to substantially increase the Flatstream data rate. The basic principle is also used in other technical areas such as "pipelining" for microprocessors.

2.2.11.8.5.1 Function principle

X2X Link communication cycles through 5 different steps to transfer a Flatstream sequence. At least 5 bus cycles are therefore required to successfully transfer the sequence.

	Step I	Step II	Step III	Step IV	Step V
Actions	Transfer sequence from transmit array, increase SequenceCounter	Cyclic synchronization of MTU and module buffer	Append sequence to receive array, adjust SequenceAck	Cyclic synchronization MTU and module buffer	Check SequenceAck
Resource	Transmitter (task to transmit)	Bus system (direction 1)	Recipients (task to receive)	Bus system (direction 2)	Transmitter (task for Ack checking)

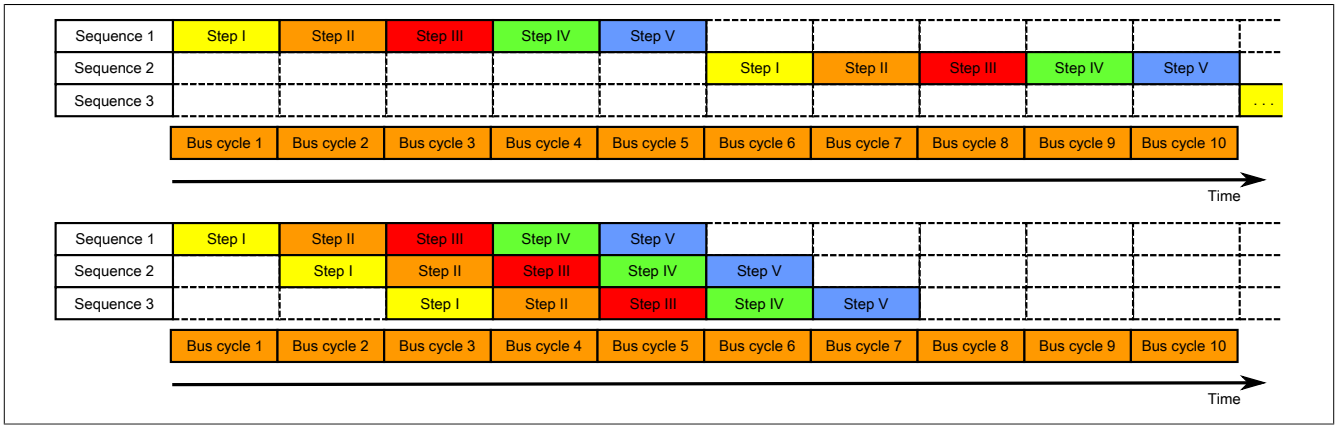


Figure 98: Comparison of transfer without/with Forward

Each of the 5 steps (tasks) requires different resources. If Forward functionality is not used, the sequences are executed one after the other. Each resource is then only active if it is needed for the current sub-action.
With Forward, a resource that has executed its task can already be used for the next message. The condition for enabling the MTU is changed to allow for this. Sequences are then passed to the MTU according to the timing. The transmitting station no longer waits for an acknowledgment from SequenceAck, which means that the available bandwidth can be used much more efficiently.
In the most ideal situation, all resources are working during each bus cycle. The receiver must still acknowledge every sequence received. Only when SequenceAck has been changed and checked by the transmitter is the sequence considered as having been transferred successfully.

2.2.11.8.5.2 Configuration

The Forward function must only be enabled for the input direction. 2 additional configuration registers are available for doing so. Flatstream modules have been optimized in such a way that they support this function. In the output direction, the Forward function can be used as soon as the size of OutputMTU is specified.

Number of unacknowledged sequences

Name:
Forward

With register "Forward", the user specifies how many unacknowledged sequences the module is permitted to transmit.

Recommendation:
X2X Link: Max. 5
POWERLINK: Max. 7

Data type	Values
USINT	1 to 7 Default: 1

Delay time

Name:
ForwardDelay

Register "ForwardDelay" is used to specify the delay time in microseconds. This is the amount of time the module has to wait after sending a sequence until it is permitted to write new data to the MTU in the following bus cycle. The program routine for receiving sequences from a module can therefore be run in a task class whose cycle time is slower than the bus cycle.

Data type	Values
UINT	0 to 65535 [µs] Default: 0

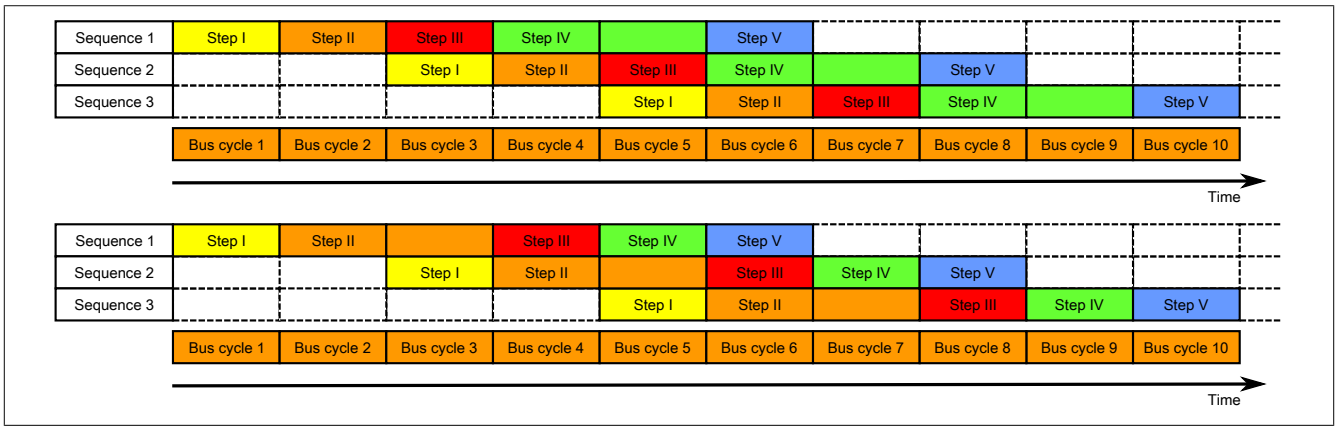


Figure 99: Effect of ForwardDelay when using Flatstream communication with the Forward function

In the program, it is important to make sure that the CPU is processing all of the incoming InputSequences and InputMTUs. The ForwardDelay value causes delayed acknowledgment in the output direction and delayed reception in the input direction. In this way, the CPU has more time to process the incoming InputSequence or InputMTU.

2.2.11.8.5.3 Transmitting and receiving with Forward

The basic algorithm for transmitting and receiving data remains the same. With the Forward function, up to 7 unacknowledged sequences can be transmitted. Sequences can be transmitted without having to wait for the previous message to be acknowledged. Since the delay between writing and response is eliminated, a considerable amount of additional data can be transferred in the same time window.

Algorithm for transmitting

Cyclic status query: *- The module monitors OutputSequenceCounter.*
0) Cyclic checks: - The CPU must check OutputSyncAck. → If OutputSyncAck = 0: Reset OutputSyncBit and resynchronize the channel. - The CPU must check whether OutputMTU is enabled. → If OutputSequenceCounter > OutputSequenceAck + 7, then it is not enabled because the last sequence has not yet been acknowledged.
1) Preparation (create transmit array): - The CPU must split up the message into valid segments and create the necessary control bytes. - The CPU must add the segments and control bytes to the transmit array.
2) Transmit: - The CPU must transfer the current part of the transmit array to OutputMTU. - The CPU must increase OutputSequenceCounter for the sequence to be accepted by the module. - The CPU is then permitted to *transmit* in the next bus cycle if the MTU has been enabled.
The module responds since OutputSequenceCounter > OutputSequenceAck: *- The module accepts data from the internal receive buffer and appends it to the end of the internal receive array.* *- The module is acknowledged and the currently received value of OutputSequenceCounter is transferred to OutputSequenceAck.* *- The module queries the status cyclically again.*
3) Completion (acknowledgment): - The CPU must check OutputSequenceAck cyclically. → A sequence is only considered to have been transferred successfully if it has been acknowledged via OutputSequenceAck. In order to detect potential transfer errors in the last sequence as well, it is important to make sure that the algorithm is run through long enough. **Note:** To monitor communication times exactly, the task cycles that have passed since the last increase of OutputSequenceCounter should be counted. In this way, the number of previous bus cycles necessary for the transfer can be measured. If the monitoring counter exceeds a predefined threshold, then the sequence can be considered lost (the relationship of bus to task cycle can be influenced by the user so that the threshold value must be determined individually).

Algorithm for receiving

0) Cyclic status query: - The CPU must monitor InputSequenceCounter.
Cyclic checks: *- The module checks InputSyncAck.* *- The module checks if InputMTU for enabling.* *→ Enabling criteria: InputSequenceCounter > InputSequenceAck + Forward*
Preparation: *- The module forms the control bytes / segments and creates the transmit array.*
Action: *- The module transfers the current part of the transmit array to the receive buffer.* *- The module increases InputSequenceCounter.* *- The module waits for a new bus cycle after time from ForwardDelay has expired.* *- The module repeats the action if InputMTU is enabled.*
1) Receiving (InputSequenceCounter > InputSequenceAck): - The CPU must apply data from InputMTU and append it to the end of the receive array. - The CPU must match InputSequenceAck to InputSequenceCounter of the sequence currently being processed.
Completion: *- The module monitors InputSequenceAck.* *→ A sequence is only considered to have been transferred successfully if it has been acknowledged via InputSequenceAck.*

Details/Background

1. Illegal SequenceCounter size (counter offset)
   Error situation: MTU not enabled
   If the difference between SequenceCounter and SequenceAck during transmission is larger than permitted, a transfer error occurs. In this case, all unacknowledged sequences must be repeated with the old Sequence-Counter value.
2. Checking an acknowledgment
   After an acknowledgment has been received, a check must verify whether the acknowledged sequence has been transmitted and had not yet been unacknowledged. If a sequence is acknowledged multiple times, a severe error occurs. The channel must be closed and resynchronized (same behavior as when not using Forward).

   > **Information:**
   >
   > **In exceptional cases, the module can increment OutputSequenceAck by more than 1 when using Forward.**
   > **An error does not occur in this case. The CPU is permitted to consider all sequences up to the one being acknowledged as having been transferred successfully.**

3. Transmit and receive arrays
   The Forward function has no effect on the structure of the transmit and receive arrays. They are created and must be evaluated in the same way.

2.2.11.8.5.4 Errors when using Forward

In industrial environments, it is often the case that many different devices from various manufacturers are being used side by side. The electrical and/or electromagnetic properties of these technical devices can sometimes cause them to interfere with one another. These kinds of situations can be reproduced and protected against in laboratory conditions only to a certain point.

Precautions have been taken for transfer via X2X Link in case such interference should occur. For example, if an invalid checksum occurs, the I/O system will ignore the data from this bus cycle and the receiver receives the last valid data once more. With conventional (cyclic) data points, this error can often be ignored. In the following cycle, the same data point is again retrieved, adjusted and transferred.

Using Forward functionality with Flatstream communication makes this situation more complex. The receiver receives the old data again in this situation as well, i.e. the previous values for SequenceAck/SequenceCounter and the old MTU.

Loss of acknowledgment (SequenceAck)

If a SequenceAck value is lost, then the MTU was already transferred properly. For this reason, the receiver is permitted to continue processing with the next sequence. The SequenceAck is aligned with the associated SequenceCounter and sent back to the transmitter. Checking the incoming acknowledgments shows that all sequences up to the last one acknowledged have been transferred successfully (see sequences 1 and 2 in the image).

Loss of transmission (SequenceCounter, MTU):

If a bus cycle drops out and causes the value of SequenceCounter and/or the filled MTU to be lost, then no data reaches the receiver. At this point, the transmission routine is not yet affected by the error. The time-controlled MTU is released again and can be rewritten to.
The receiver receives SequenceCounter values that have been incremented several times. For the receive array to be put together correctly, the receiver is only permitted to process transmissions whose SequenceCounter has been increased by one. The incoming sequences must be ignored, i.e. the receiver stops and no longer transmits back any acknowledgments.
If the maximum number of unacknowledged sequences has been sent and no acknowledgments are returned, the transmitter must repeat the affected SequenceCounter and associated MTUs (see sequence 3 and 4 in the image).

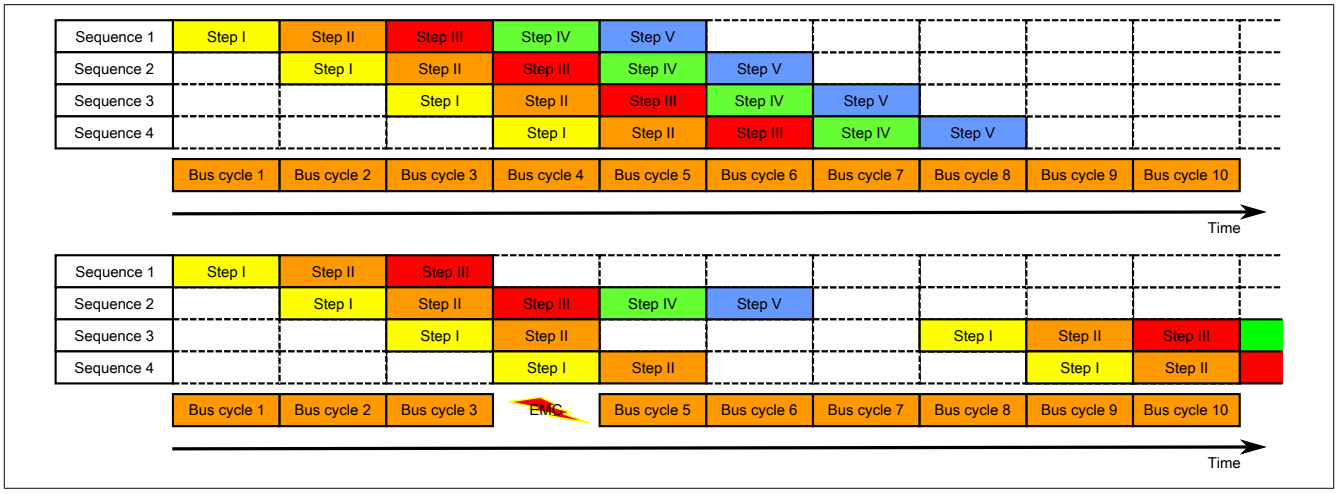


Figure 100: Effect of a lost bus cycle

Loss of acknowledgment

In sequence 1, the acknowledgment is lost due to disturbance. Sequences 1 and 2 are therefore acknowledged in Step V of sequence 2.

Loss of transmission

In sequence 3, the entire transmission is lost due to disturbance. The receiver stops and no longer sends back any acknowledgments.
The transmitting station continues transmitting until it has issued the maximum permissible number of unacknowledged transmissions.
5 bus cycles later at the earliest (depending on the configuration), it begins resending the unsuccessfully sent transmissions.

2.2.11.9 HART with Flatstream

When using Flatstream communication, the module acts as a bridge between the X2X master and an intelligent field device connected to the module. Flatstream mode can be used for either point-to-point connections as well as for multidrop systems. Specific algorithms such as timeout and checksum monitoring are usually managed automatically. During normal operation, the user does not have access to these details.

HART is considered a master-slave network where half-duplex communication takes place asynchronously. Various features have been included to ensure that signals are transmitted without errors.
For example, the user can increase the length of the preamble, thus making the transmission more secure. However, this also has an effect on the percentage of payload data and overhead.

Additional information about HART can be found at www.HARTcomm.org.

How it works

The module has 2 independent channels. When using Flatstream , the channel number must therefore be specified. The general structure of a Flatstream frame is extended as follows.

Input/Output sequence	Tx/Rx bytes		
(unchanged)	Control byte (unchanged)	Channel number	HART frame (without preamble and checksum)

HART frame with Flatstream					
Startup	ADDR	CMD	BCNT	(STS)	(DATA)

Startup Start identification
ADDR Address within the HART network
CMD HART command
BCNT Byte counters (number of remaining bytes)
*STS Status of the last command received. Information about the working mode of the HART Slave and communication errors (if supported, return data from the HART Slave)
*DATA Data (if necessary for the command)

Examples of HART commands

Command	Function
0x00	Read slave ID
0x03	Read current value and up to 4 variables
0x09	Read up to 4 variables including status
0x21	Read variables

2.2.11.10 Function model "OSP"

In function model "OSP" (Operator Set Predefined), the user defines an analog value or digital pattern. This OSP value is output as soon as the communication between the module and master is aborted.

Functionality

The user has the choice between 2 OSP modes:

- Retain last valid value
- Replace with static value

In the first case, the module retains the last value recognized as a valid output status.

When selecting mode "Replace with static value", a plausible output value must be entered in the associated value register. When an OSP event occurs, this value is output instead of the value currently requested by the task.

2.2.11.10.1 Activating the OSP output in the module

Name:
OSPValid

This data point offers the possibility to start module output and request OSP operation during running operation.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0	OSPValid	0	Request OSP operation (after initial start or module in Standby)
		1	Request normal operation
1 - 7	Reserved	0	

There is one OSPValid bit on the module, which is managed by the user task. It must be set when the enabled channels are started. As long as the OSPValid bit remains set in the module, the module behaves the same as the "Standard" function model.

If an OSP event occurs (e.g. communication between the module and master CPU interrupted) then the OSPValid bit will be reset on the module. The module enters OSP mode and the output occurs in the "OSPMode" on page 710 register according to the configuration.

The following applies:

The OSP replacement value remains even after the communication channel has recovered. OSP mode is only exited when a set OSPValid bit is transferred.

When the master CPU is restarted, the OSPValid bit is re-initialized on the master CPU. It must once more be set by the application and transferred via the bus.
When temporary communication errors occur between the module and master CPU (e.g. due to EMC), a few bus cycles will pass without refreshing the cyclic registers. The OSPValid bit is reset internally in the module - the bit in the CPU however remains set. Upon the next successful transfer, the OSPValid bit in the module is set again and the module returns to normal operation.

The ModulOK bit can be evaluated if the task in the master CPU needs to know which output mode the module is currently in.

Warning!

If the OSPValid bit is reset to "0" on the module, then the output state no longer depends on the relevant task in the master CPU. However, an output still occurs depending on the configuration of the OSP replacement value.

2.2.11.10.2 Setting the OSP mode

Name:
CfgOSPMode01 to CfgOSPMode02

This register essentially controls a channel's behavior when OSP is being used.

Data type	Value	Description
USINT	0	Replace with static value
	1	Retain last valid value

2.2.11.10.3 Define the OSP analog output value

Name:
CfgOSPValue01 to CfgOSPValue02

This register contains the analog output value, which is output in "Replace with static value" mode during OSP operation.

Data type	Value
Corresponds to AnalogOutput0x	Corresponds to AnalogOutput0x

Warning!

"OSPValue" is only applied by the module if bit "OSPValid" has been set in the module.

2.2.11.11 NetTime Technology

NetTime refers to the ability to precisely synchronize and transfer system times between individual components of the controller or network (CPU, I/O modules, X2X Link, POWERLINK, etc.).

This allows the moment that events occur to be determined system-wide with microsecond precision. Upcoming events can also be executed precisely at a specified moment.

NetTime TECHNOLOGY

2.2.11.11.1 Time information

Various time information is available in the controller or on the network:

- System time (on the PLC, Automation PC, etc.)
- X2X Link time (for each X2X Link network)
- POWERLINK time (for each POWERLINK network)
- Time data points of I/O modules

The NetTime is based on 32-bit counters, which are increased with microsecond resolution. The sign of the time information changes after 35 min, 47 s, 483 ms and 648 µs; an overflow occurs after 71 min, 34 s, 967 ms and 296 µs.

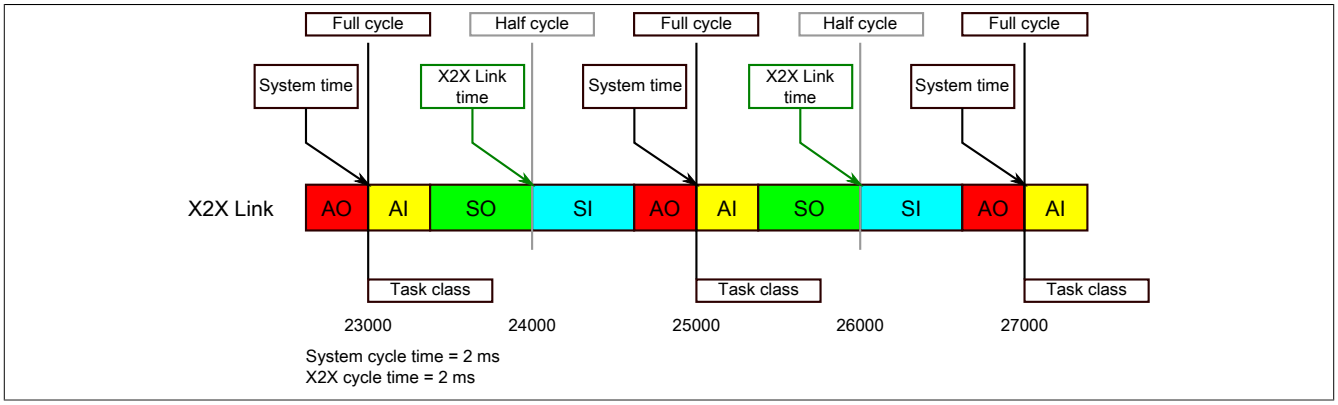
The initialization of the times is based on the system time during the startup of the X2X Link, the I/O modules or the POWERLINK interface.

Current time information in the application can also be determined via library AsIOTime.

2.2.11.11.1.1 PLC/Controller data points

The NetTime I/O data points of the PLC or the controller are latched to each system clock and made available.

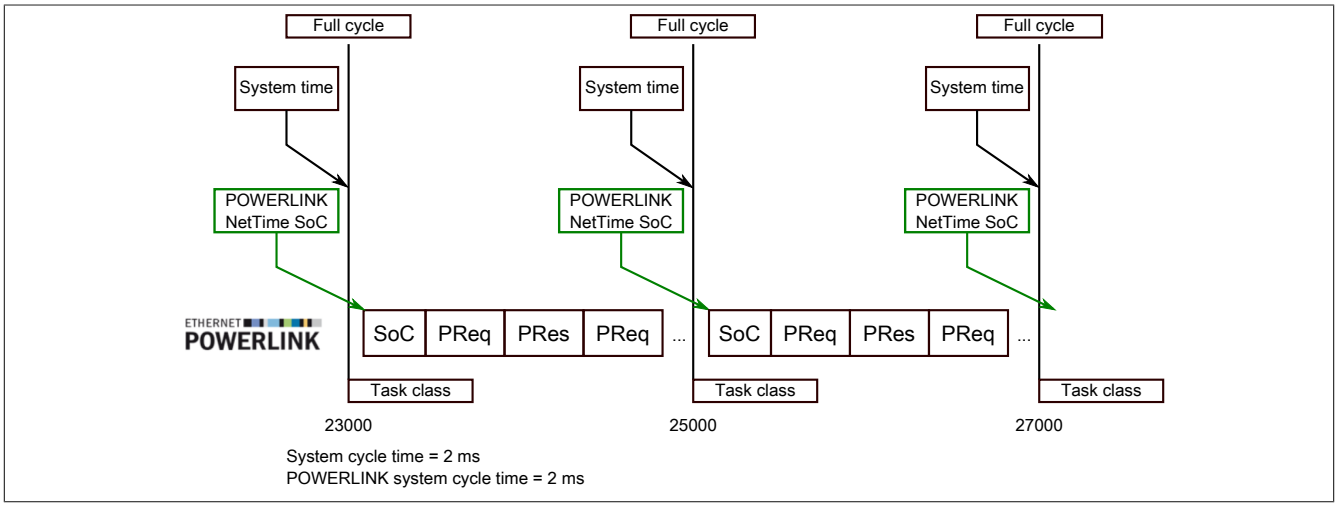
2.2.11.11.1.2 X2X Link reference moment



The reference moment on the X2X Link network is always calculated at the half cycle of the X2X Link cycle. This results in a difference between the system time and the X2X Link reference moment when the reference time is read out.

In the example above, this results in a difference of 1 ms, i.e. if the system time and X2X Link reference moment are compared at time 25000 in the task, then the system time returns the value 25000 and the X2X Link reference moment returns the value 24000.

2.2.11.11.1.3 POWERLINK - Reference time point

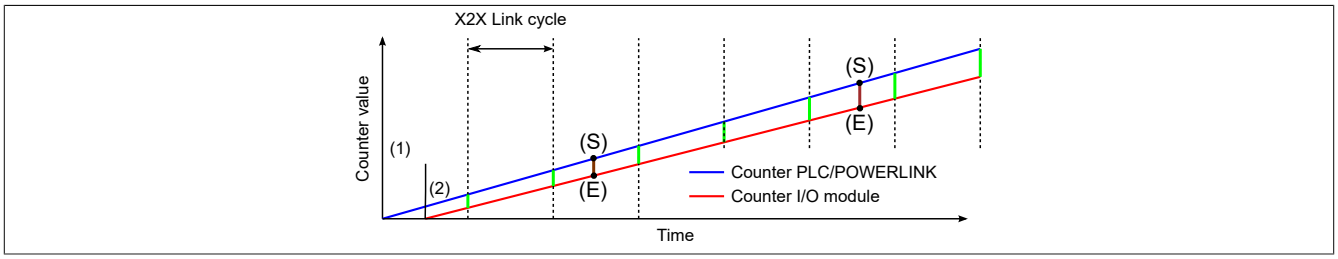


The reference time point on the POWERLINK network is always calculated at the start of cycle (SoC) of the POWERLINK network. The SoC starts 20 µs after the system clock due to the system. This results in the following difference between the system time and the POWERLINK reference time:

POWERLINK reference time = System time - POWERLINK cycle time + 20 µs.

In the example above, this means a difference of 1980 µs, i.e. if the system time and POWERLINK reference time are compared at time 25000 in the task, then the system time returns the value 25000 and the POWERLINK reference time returns the value 23020.

2.2.11.11.1.4 Synchronization of system time/POWERLINK time and I/O module



At startup, the internal counters for the PLC/POWERLINK (1) and the I/O module (2) start at different times and increase the values with microsecond resolution.

At the beginning of each X2X Link cycle, the PLC or the POWERLINK network sends time information to the I/O module. The I/O module compares this time information with the module's internal time and forms a difference (green line) between the two times and stores it.

When a NetTime event (E) occurs, the internal module time is read out and corrected with the stored difference value (brown line). This means that the exact system moment (S) of an event can always be determined, even if the counters are not absolutely synchronous.

Note

The deviation from the clock signal is strongly exaggerated in the picture as a red line.

2.2.11.11.2 Timestamp functions

NetTime-capable modules provide various timestamp functions depending on the scope of functions. If a timestamp event occurs, the module immediately saves the current NetTime. After the respective data is transferred to the CPU, including this precise moment, the CPU can then evaluate the data using its own NetTime (or system time), if necessary.

2.2.11.11.2.1 Time-based inputs

NetTime Technology can be used to determine the exact moment of a rising edge at an input. The rising and falling edges can also be detected and the duration between 2 events can be determined.

Information:

The determined moment always lies in the past.

2.2.11.11.2.2 Time-based outputs

NetTime Technology can be used to specify the exact moment of a rising edge on an output. The rising and falling edges can also be specified and a pulse pattern generated from them.

Information:

The specified time must always be in the future, and the set X2X Link cycle time must be taken into account for the definition of the moment.

2.2.11.11.2.3 Time-based measurements

NetTime Technology can be used to determine the exact moment of a measurement that has taken place. Both the starting and end moment of the measurement can be transmitted.

2.2.11.12 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

2.2.11.13 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time	
Analog outputs	1 ms

Minimum I/O update time Hart Communication	
Point-to-point	500 ms
Multidrop	500 ms * number of stations

2.3 X20AO2622

2.3.1 General information

2.3.1.1 Other applicable documents

For additional and supplementary information, see the following documents.

Other applicable documents

Document name	Title
MAX20	X20 System user's manual
MAEMV	Installation / EMC guide

2.3.1.2 Order data

Order number	Short description	Figure
	Analog outputs	
X20AO2622	X20 analog output module, 2 outputs, 10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 107: X20AO2622 - Order data

2.3.1.3 Module description

The module is equipped with 2 outputs with 13-bit (including sign) digital converter resolution. It is possible to select between the current and voltage signal using different terminals.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

Functions:

- Analog outputs

Analog outputs

The module is equipped with analog outputs with a configurable current and/or voltage signal.

2.3.2 Technical description

2.3.2.1 Technical data

Order number	X20AO2622
Short description	
I/O module	2 analog outputs ±10 V or 0 to 20 mA / 4 to 20 mA [1]
General information	
B&R ID code	0x1BA2
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using LED status indicator and software
Channel type	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	1.1 W
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
UKCA	Yes
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
DNV	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
LR	ENV1
KR	Yes
ABS	Yes
BV	**EC33B** Temperature: 5 - 55°C Vibration: 4 g EMC: Bridge and open deck
EAC	Yes
KC	Yes
Analog outputs	
Output	±10 V or 0 to 20 mA / 4 to 20 mA, via different terminal connections [1]
Max. output current	10 mA at voltage >5 V 15 mA at voltage <5 V
Digital converter resolution	
Voltage	±12-bit
Current	12-bit
Conversion time	200 µs for all outputs
Settling time on output change over entire range	1 ms
Switch on/off behavior	Internal enable relay for startup
Max. error	
Gain	0.15% [2]
Offset	0.05% [3]
Voltage	
Gain	0.15% [2]
Offset	0.05% [3]
Current	
Gain	0.15% [2]
Offset	0.05% [3]
Output protection	Short-circuit proof
Output format	
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0008 = 2.441 mV
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0008 = 4.883 µA
Load per channel	
Voltage	Max. ±10 mA, load ≥1 kΩ
Current	Load max. 600 Ω (Rev. ≥ J0), 500 Ω (Rev. < J0)
Short-circuit proof	Current limiting ±40 mA
Output filter	First-order low-pass filter / cutoff frequency 10 kHz
Max. gain drift	0.02 %/°C [2]
Max. gain drift	
Voltage	0.02 %/°C [2]
Current	0.02 %/°C [2]

Table 108: X20AO2622 - Technical data

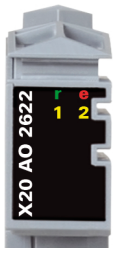
Order number	X20AO2622
Max. offset drift	0.032%/°C 3)
Max. offset drift	
Voltage	0.032%/°C 3)
Current	0.032%/°C 3)
Error caused by load change	
Voltage	Max. 0.11%, from 10 MΩ → 1 kΩ, resistive
Current	Max. 0.5%, from 1 Ω → 600 Ω, resistive
Nonlinearity	<0.007% 3)
Insulation voltage between channel and bus	500 V_{eff}
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x terminal block X20TB06 or X20TB12 separately. Order 1x bus module X20BM11 separately.
Pitch	$12.5^{+0.2}$ mm

Table 108: X20AO2622 - Technical data

1) 4 to 20 mA: Starting with upgrade version 1.0.2.0 or hardware revision "I0"
2) Based on the current output value.
3) Based on the entire output range.

2.3.2.2 LED status indicators

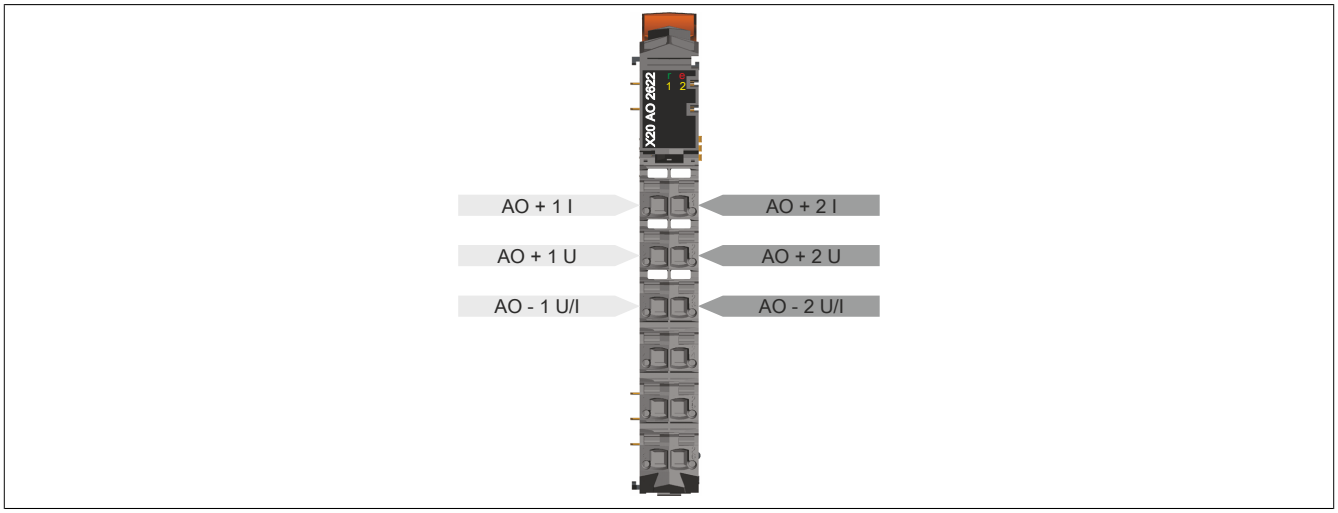
For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 System user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)1)
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 2	Orange	Off	Value = 0
			On	Value ≠ 0

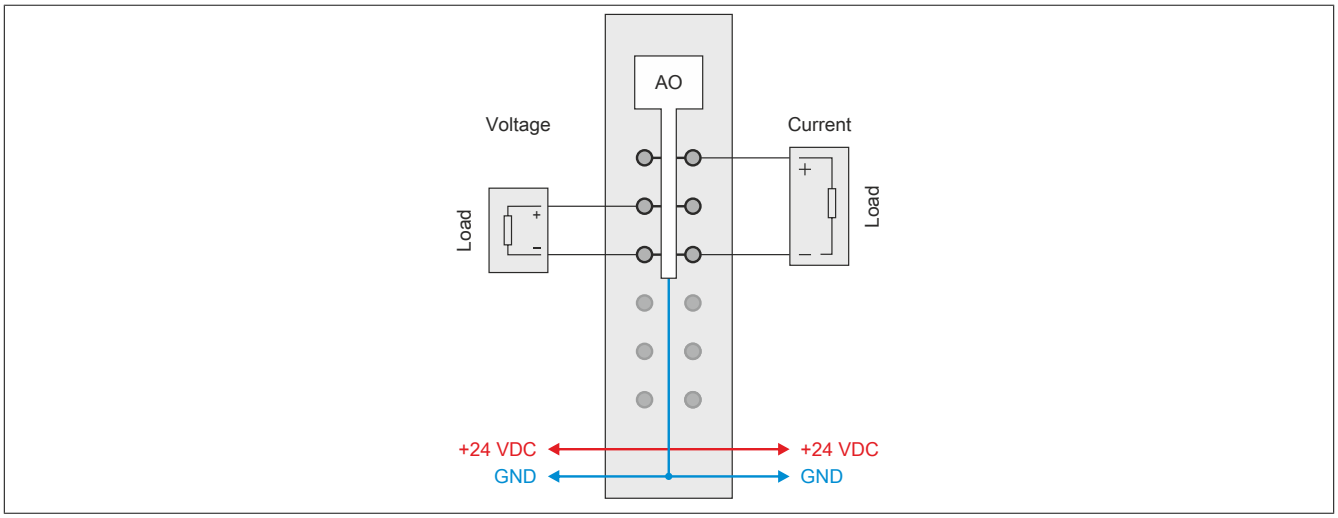
1) Depending on the configuration, a firmware update can take up to several minutes.

2.3.2.3 Pinout

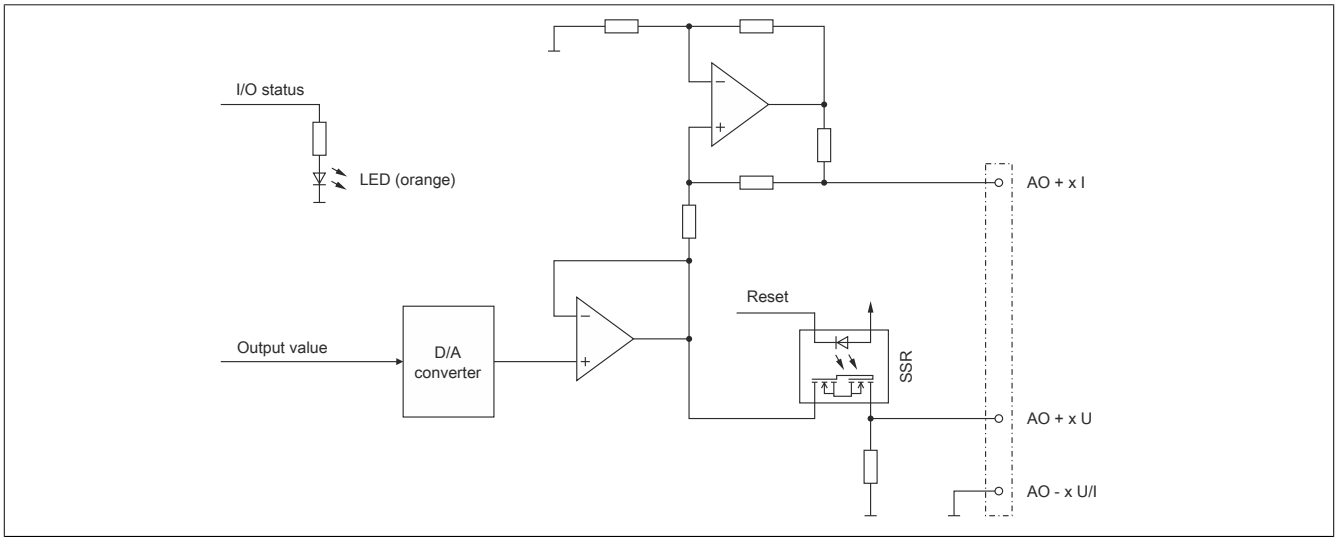
The individual channels can be configured for either current or voltage signals. The type of signal is also determined by the terminals used.



2.3.2.4 Connection example



2.3.2.5 Output circuit diagram



2.3.3 Function description

2.3.3.1 Analog outputs

The module is equipped with 2 analog outputs.

The individual channels are designed for current and voltage signals. The differentiation is made by different terminal connections; because of different adjustment values for current and voltage, the output signal must be selected. The following output signals can be set:

- ±10 V voltage signal (default)
- 0 to 20 mA current signal
- 4 to 20 mA current signal

Information:

The register is described in "Setting the channel type" on page 721.

2.3.4 Commissioning

2.3.4.1 Function model comparison

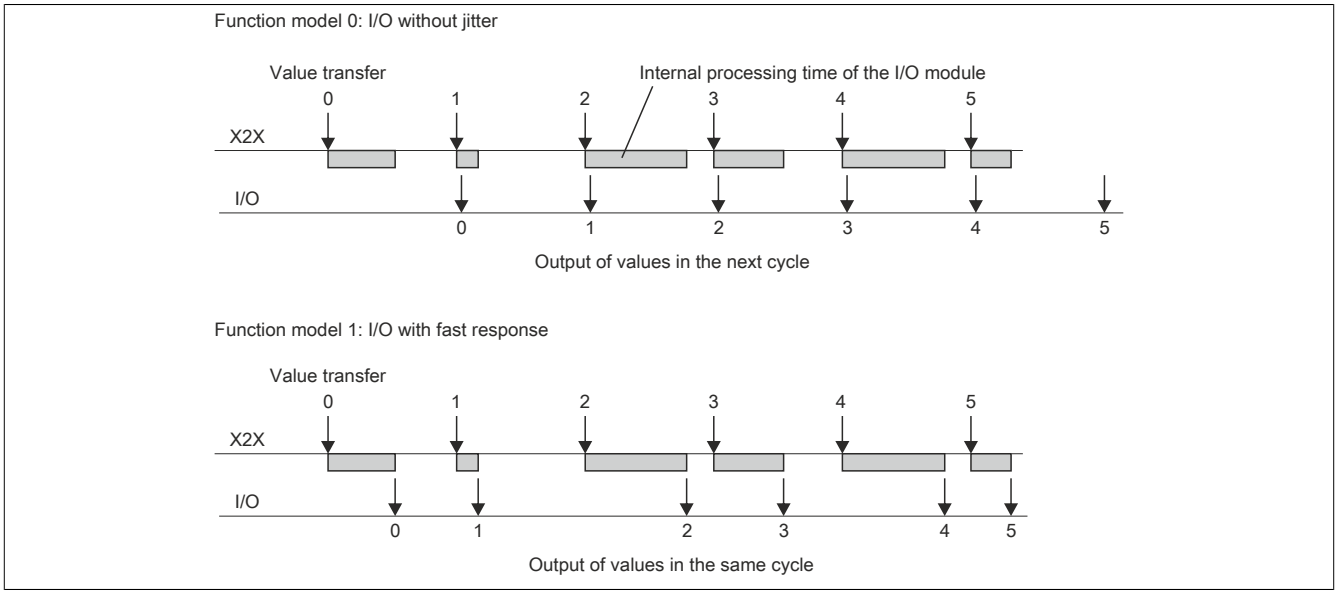
Function model 0: I/O without jitter (standard)

Corrected values are output in the next cycle if the minimum cycle is ≥300 µs in order to reduce jitter to a minimum.

Function model 1: I/O with fast reaction

Corrected values are output in the same cycle if the minimum cycle is ≥300 µs (optimized reactions).

Comparison of the two function models



2.3.5 Register description

2.3.5.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 System user's manual.

2.3.5.2 Function model 0 - Standard and function model 1 - I/O with fast reaction

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
18	ConfigOutput01	USINT		•		•
Communication						
0	AnalogOutput01	INT			•	
2	AnalogOutput02	INT			•	

2.3.5.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
18	-	ConfigOutput01 (channel type)	USINT		•		•
Communication							
0	0	AnalogOutput01	INT			•	
2	2	AnalogOutput02	INT			•	

1) The offset specifies the position of the register within the CAN object.

2.3.5.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

2.3.5.3.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

2.3.5.4 Analog outputs

The individual channels can be configured for either current or voltage signals. The type of signal is also determined by the terminals used.

2.3.5.4.1 Output values of the analog outputs

Name:
AnalogOutput01 to AnalogOutput02

These registers provide the standardized output values. Once a permitted value is received the module outputs the respective current or voltage.

Data type	Value	Information
INT	-32768 to 32767	Voltage signal -10 to 10 VDC
	0 to 32767	Current signal 0 to 20 mA
	0 to 32767	Current signal 4 to 20 mA[1)]

1) From upgrade version 1.0.2.0 or hardware revision "I0"

2.3.5.4.2 Setting the channel type

Name:
ConfigOutput01

This register can be used to set the channel type of the outputs.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Name	Value	Information
0	Channel 1	0	Voltage signal (bus controller default setting)
		1	Current signal, measurement range corresponding to bit 4
1	Channel 2	0	Voltage signal
		1	Current signal, measurement range corresponding to bit 5
2 - 3	Reserved	0	
4	Channel 1: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal
5	Channel 2: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal
6 - 7	Reserved	0	

2.3.5.5 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
250 µs

2.3.5.6 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time
300 µs

2.4 X20AO2632

2.4.1 General information

The module is equipped with 2 outputs with 16-bit (including sign) digital converter resolution. It is possible to select between the current and voltage signal using different terminals.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

- 2 analog outputs
- Either current or voltage signal possible
- 16-bit digital converter resolution
- NetTime timestamp: Switch-off time

NetTime timestamp for output

For many applications, not only the output value is important, but also the exact switching time. The module is equipped with a NetTime timestamp function for this that can define a switching time to the nearest microsecond.

The timestamp function is based on synchronized timers. The CPU can predefine output events and provide them with a timestamp. After transferring the respective data, including the exact time, the module executes the predefined action at the exactly defined time.

2.4.2 Order data

Order number	Short description	Figure
	Analog outputs	
X20AO2632	X20 analog output module, 2 outputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, NetTime function	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 109: X20AO2632 - Order data

2.4.3 Technical data

Order number	X20AO2632
Short description	
I/O module	2 analog outputs ±10 V or 0 to 20 mA
General information	
B&R ID code	0x1BA4
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Channel type	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	1.1 W
Rev. ≥B0	
Bus	0.01 W
Internal I/O	1.2 W
Rev. <B0	
Bus	0.01 W
Internal I/O	1.6 W
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
KC	Yes
EAC	Yes
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
DNV GL	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
LR	ENV1
Analog outputs	
Output	±10 V or 0 to 20 mA, via different terminal connections
Digital converter resolution	16-bit
Digital converter resolution	
Voltage	±15-bit
Current	15-bit
Conversion time	50 µs for all outputs
Settling time on output change over entire range	500 µs (Rev. <H0: 1 ms)
Switch on/off behavior	Internal enable relay for booting
Max. error at 25°C	
Gain	0.045% [1]
Offset	0.025% [2]
Voltage	
Gain	0.045% [1]
Offset	0.025% [2]
Current	
Gain	0.09% [1]
Offset	0.045% [2]
Output protection	Short circuit protection
Output format	
Voltage	INT 0x8000 - 0x7FFF / 1 LSB = 0x0001 = 305.176 µV
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 610.352 nA
Load per channel	
Voltage	Max. ±10 mA, load ≥1 kΩ
Current	Load max. 600 Ω (Rev. ≥ J0); 500 Ω (Rev. < J0)
Short-circuit proof	Current limiting ±40 mA
Output filter	1st-order low pass / cutoff frequency 10 kHz
Max. gain drift	0.015 %/°C [1]
Max. gain drift	
Voltage	0.015 %/°C [1]
Current	0.02 %/°C [1]
Max. offset drift	0.013 %/°C [2]
Max. offset drift	
Voltage	0.013 %/°C [2]
Current	0.013 %/°C [2]

Table 110: X20AO2632 - Technical data

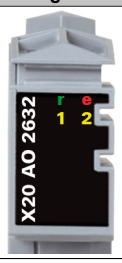
Order number	X20AO2632
Error caused by load change	
Voltage	Max. 0.11%, from 10 MΩ → 1 kΩ, resistive
Current	Max. 0.5%, from 1 Ω → 600 Ω, resistive
Nonlinearity	<0.007% 3)
Insulation voltage between channel and bus	500 V_{eff}
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Pitch	$12.5^{+0.2}$ mm

Table 110: X20AO2632 - Technical data

1) Based on the current output value.
2) Based on the entire output range.
3) Based on the output range.

2.4.4 LED status indicators

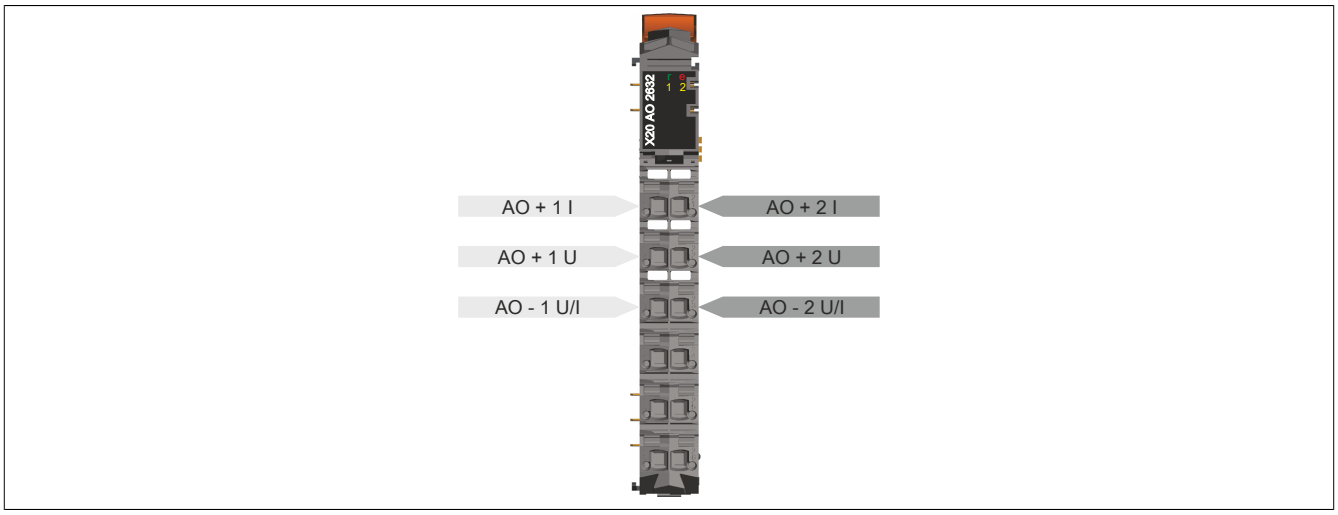
For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 system user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)1)
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	1 - 2	Orange	Off	Value = 0
			On	Value ≠ 0

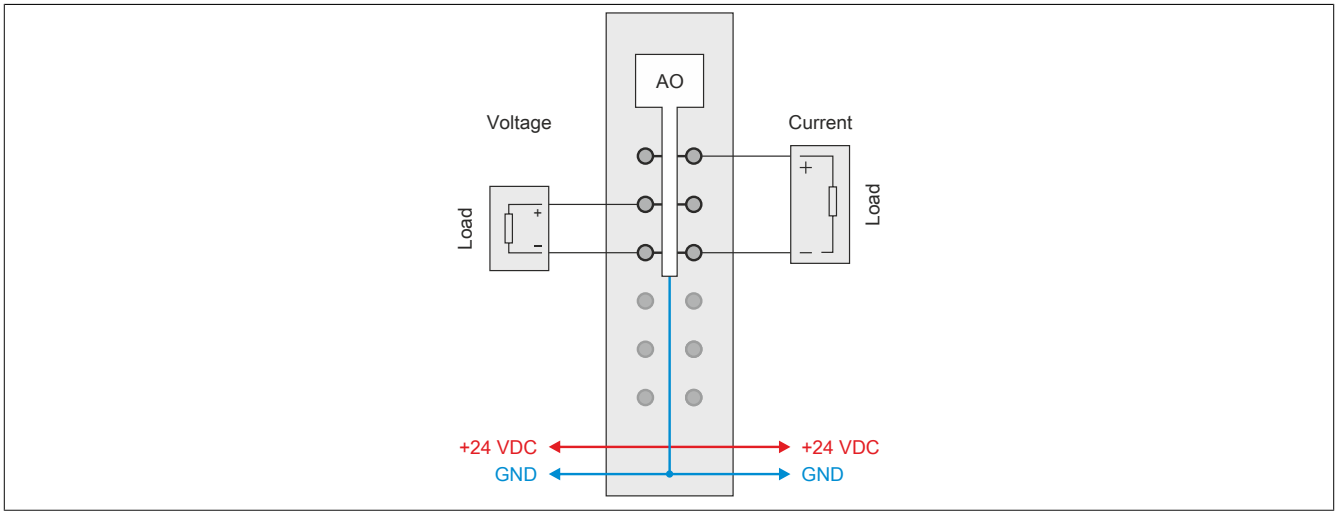
1) Depending on the configuration, a firmware update can take up to several minutes.

2.4.5 Pinout

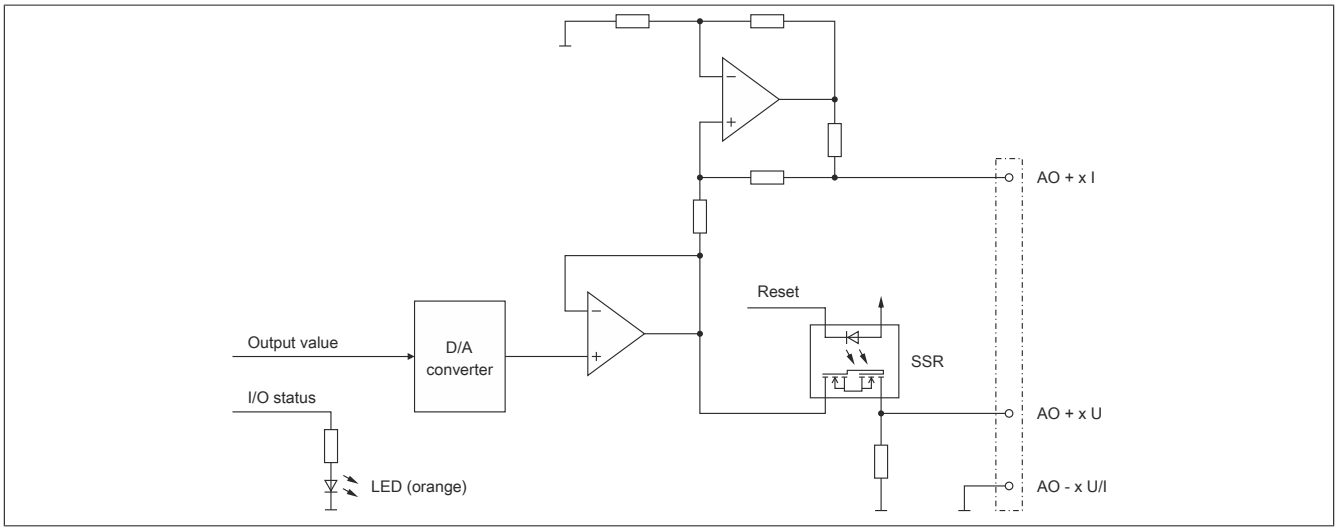
The individual channels can be configured for either current or voltage signals. The type of signal is also determined by the terminals used.



2.4.6 Connection example



2.4.7 Output circuit diagram



2.4.8 Register description

2.4.8.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 system user's manual.

2.4.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog output - Configuration						
0	ConfigOutput01 (channel type)	UINT				•
594 598	Cfo_Channel01TimeMode Cfo_Channel02TimeMode	UINT				•
Analog output - Communication						
2 4	AnalogOutput01 AnalogOutput02	INT			•	
457	SDCLifeCount	SINT	•			
802 810	ValidationTimer01 ValidationTimer02	INT			•	
804 812	ValidationTimer01 ValidationTimer02	DINT			•	
833	Enabling/disabling the output channels	USINT	•		•	
	AnalogOutput01Enable, ~Readback	Bit 0				
	AnalogOutput02Enable, ~Readback	Bit 1				
835	Checking the output values	USINT	•			
	AnalogOutput01OK	Bit 0				
	AnalogOutput02OK	Bit 1				

2.4.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog output - Configuration							
0	-	ConfigOutput01 (channel type)	UINT				•
Analog output - Communication							
2 4	0 2	AnalogOutput01 AnalogOutput02	INT			•	

1) The offset specifies the position of the register within the CAN object.

2.4.8.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

2.4.8.3.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

2.4.8.4 General information

The module provides 2 analog outputs. Each channel can output a voltage range of ±10 V or a current range of 0 to 20 mA.

The module also has a time-based watchdog monitor. The user can activate this feature channel-by-channel as needed.

2.4.8.5 Analog output - Configuration

Each channel is configured independently. The user can also define an optional time-based monitor. To make this possible, 2 watchdog timers were implemented, which can be assigned to the outputs.

2.4.8.5.1 Setting the channel type

Name:
ConfigOutput01

This register can be used to set the channel type of the outputs.

Each channel is capable of handling either current or voltage signals. The type of signal is determined by the terminal connections used. Since current and voltage require different adjustment values, it is also necessary to configure the desired type of output signal. The following output signals can be set:

- ±10 V voltage signal
- 0 to 20 mA current signal

Data type	Values	Bus controller default setting
UINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0 - 7	Reserved	0	
8	Channel 1	0	Voltage signal (bus controller default setting)
		1	Current signal
9	Channel 2	0	Voltage signal (bus controller default setting)
		1	Current signal
10 - 15	Reserved	0	

2.4.8.5.2 Configuring the time-based watchdog monitor

Name:
Cfo_Channel01TimeMode to Cfo_Channel02TimeMode

This register is used to activate or configure the time-based watchdog monitor for the analog output channels.

Possibilities per channel:

- Validation timer data type: General choice 16 or 32 bit
- Validation window: The maximum value can be further limited within the data type.
- Timer allocation: A separate timer is available for each channel. However, all channels can be configured with the same validation timer, whereby the same settings must be made for the data type and window in the TimeMode registers.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 4	Max. validation time	00000	Disabled
		00001	2 µs
		00010	4 µs
		00011	8 µs
		...	...
		11111	2,147,483,648 µs (~35 min)
5 - 7	Reserved	0	
8	Timer allocation	0	ValidationTimer01 (default for channel 1)
		1	ValidationTimer02 (default for channel 2)
9 - 14	Reserved	0	
15	Time format	0	16-bit
		1	32-bit

2.4.8.6 Analog output - Communication

In standard mode, the module's outputs are enabled. Based on the configuration and AnalogOutput value, they output the corresponding current or voltage.

If the application requires time-controlled monitoring of the outputs, a validation timer can be assigned to each channel. The validation timer register assigns a validity period to the current output value. If validation is enabled, the module compares the validation time and the NetTime of the X2X Link. If the transmitted validity period is exceeded, the module switches off the channel and resets the output. State "Safety shutdown" is only exited again when a new valid validation time has been transmitted. If enabled, the module reports back which state it is currently in via the error state bit of the channel.

If the value of the validation timer is incremented in each task cycle, the valid validation time will be calculated as follows:

NetTime of the X2X Link master (to which the module is connected)	
+	Timespan for transferring data from the X2X Link master to the CPU (higher-level system)
+	Cycle time of task class (including tolerance)
+	Timespan for transferring the data from the CPU to the module
+	Timespan allowed by the application (e.g. for tolerating failure of an X2X Link cycle)
=	Valid validation time

The AnalogOutputEnableByte is enabled during time-based monitoring. If the timer expires prematurely, the corresponding bit in the AnalogOutputOkayByte is reset and the output drops out. This provides an easy way to achieve a defined state.

2.4.8.6.1 Output values of the analog outputs

Name:
AnalogOutput01 to AnalogOutput02

These registers provide the standardized output values. Once a permitted value is received, the module outputs the respective current or voltage.

Information:

The value "0" disables the channel status LED.

Data type	Value	
INT	-32767 to 32767	Voltage
	0 to 32767	Current

2.4.8.6.2 SDC counter register

Name:
SDCLifeCount

The 8-bit counter register is needed for the SDC software package. It is incremented with the system clock to allow the SDC to check the validity of the data frame.

Data type	Values
SINT	-128 to 127

2.4.8.6.3 Transfer of the timestamp

Name:
ValidationTimer01 to ValidationTimer02

When an output is being monitored, these registers must provide the timestamp which, when reached, will cause the output to shut down automatically. The values must be provided as signed 2-byte or 4-byte values.

For additional information about NetTime and timestamps, see "NetTime Technology" on page 730.

Data type	Values [µs]	
INT	-32768 to 32767	NetTime timestamp of the current output value
DINT	-2,147,483,648 to 2,147,483,647	NetTime timestamp of the current output value

2.4.8.6.4 Enabling/disabling the output channels

Name:
AnalogOutput01Enable to AnalogOutput02Enable
AnalogOutput01EnableReadback to AnalogOutput02EnableReadback

The "OutputEnable" byte is only needed for the channels with activated time-based monitoring. The individual bits are used to enable/disable the respective channels. To receive reliable feedback about the current state of the module, the byte was also implemented so that it can be read cyclically.

Data type	Value
USINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0	AnalogOutput01Enable AnalogOutput01EnableReadback	0	Output deactivated
		1	Output activated
1	AnalogOutput02Enable AnalogOutput02EnableReadback	0	Output deactivated
		1	Output activated
2 - 7	Reserved	0	

2.4.8.6.5 Checking the output values

Name:
AnalogOutput01OK to AnalogOutput02OK

These registers are only needed for channels with activated time-based monitoring. The individual bits report whether the respective channel is actually generating the required voltage or current.

Data type	Value
USINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0	AnalogOutput01OK	0	Electrical signal deactivated
		1	Electrical signal activated
1	AnalogOutput02OK	0	Electrical signal deactivated
		1	Electrical signal activated
2 - 7	Reserved	0	

2.4.8.7 NetTime Technology

NetTime refers to the ability to precisely synchronize and transfer system times between individual components of the controller or network (CPU, I/O modules, X2X Link, POWERLINK, etc.).

This allows the moment that events occur to be determined system-wide with microsecond precision. Upcoming events can also be executed precisely at a specified moment.

2.4.8.7.1 Time information

Various time information is available in the controller or on the network:

- System time (on the PLC, Automation PC, etc.)
- X2X Link time (for each X2X Link network)
- POWERLINK time (for each POWERLINK network)
- Time data points of I/O modules

The NetTime is based on 32-bit counters, which are increased with microsecond resolution. The sign of the time information changes after 35 min, 47 s, 483 ms and 648 µs; an overflow occurs after 71 min, 34 s, 967 ms and 296 µs.

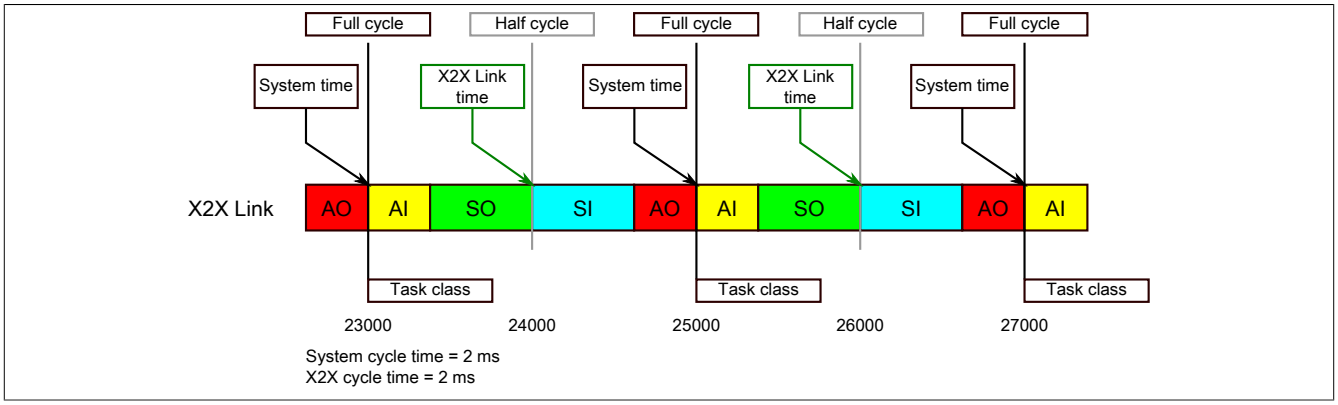
The initialization of the times is based on the system time during the startup of the X2X Link, the I/O modules or the POWERLINK interface.

Current time information in the application can also be determined via library AsIOTime.

2.4.8.7.1.1 PLC/Controller data points

The NetTime I/O data points of the PLC or the controller are latched to each system clock and made available.

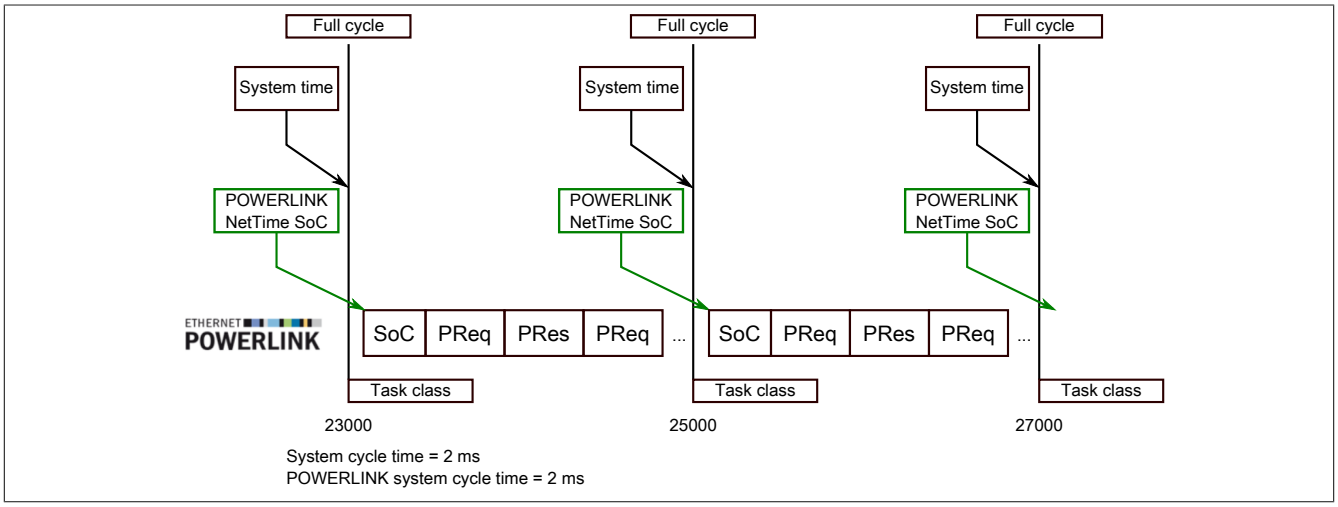
2.4.8.7.1.2 X2X Link reference moment



The reference moment on the X2X Link network is always calculated at the half cycle of the X2X Link cycle. This results in a difference between the system time and the X2X Link reference moment when the reference time is read out.

In the example above, this results in a difference of 1 ms, i.e. if the system time and X2X Link reference moment are compared at time 25000 in the task, then the system time returns the value 25000 and the X2X Link reference moment returns the value 24000.

2.4.8.7.1.3 POWERLINK - Reference time point

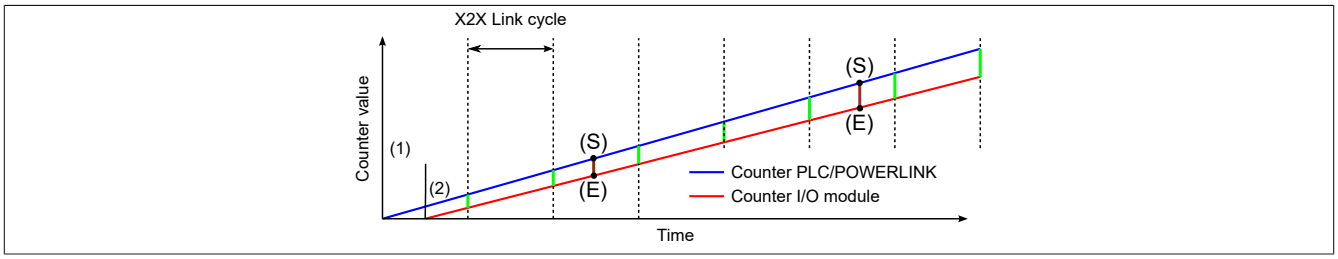


The reference time point on the POWERLINK network is always calculated at the start of cycle (SoC) of the POWERLINK network. The SoC starts 20 µs after the system clock due to the system. This results in the following difference between the system time and the POWERLINK reference time:

POWERLINK reference time = System time - POWERLINK cycle time + 20 µs.

In the example above, this means a difference of 1980 µs, i.e. if the system time and POWERLINK reference time are compared at time 25000 in the task, then the system time returns the value 25000 and the POWERLINK reference time returns the value 23020.

2.4.8.7.1.4 Synchronization of system time/POWERLINK time and I/O module



At startup, the internal counters for the PLC/POWERLINK (1) and the I/O module (2) start at different times and increase the values with microsecond resolution.

At the beginning of each X2X Link cycle, the PLC or the POWERLINK network sends time information to the I/O module. The I/O module compares this time information with the module's internal time and forms a difference (green line) between the two times and stores it.

When a NetTime event (E) occurs, the internal module time is read out and corrected with the stored difference value (brown line). This means that the exact system moment (S) of an event can always be determined, even if the counters are not absolutely synchronous.

Note

The deviation from the clock signal is strongly exaggerated in the picture as a red line.

2.4.8.7.2 Timestamp functions

NetTime-capable modules provide various timestamp functions depending on the scope of functions. If a timestamp event occurs, the module immediately saves the current NetTime. After the respective data is transferred to the CPU, including this precise moment, the CPU can then evaluate the data using its own NetTime (or system time), if necessary.

2.4.8.7.2.1 Time-based inputs

NetTime Technology can be used to determine the exact moment of a rising edge at an input. The rising and falling edges can also be detected and the duration between 2 events can be determined.

Information:

The determined moment always lies in the past.

2.4.8.7.2.2 Time-based outputs

NetTime Technology can be used to specify the exact moment of a rising edge on an output. The rising and falling edges can also be specified and a pulse pattern generated from them.

Information:

The specified time must always be in the future, and the set X2X Link cycle time must be taken into account for the definition of the moment.

2.4.8.7.2.3 Time-based measurements

NetTime Technology can be used to determine the exact moment of a measurement that has taken place. Both the starting and end moment of the measurement can be transmitted.

2.4.8.8 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

2.4.8.9 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time
200 µs

2.5 X20(c)AO4622

2.5.1 General information

2.5.1.1 Other applicable documents

For additional and supplementary information, see the following documents.

Other applicable documents

Document name	Title
MAX20	X20 System user's manual
MAEMV	Installation / EMC guide

2.5.1.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, method 4, exposure 21 days

2.5.1.2.1 Starting temperature

The starting temperature describes the minimum permissible ambient temperature in a voltage-free state at the time the coated module is switched on. This is permitted to be as low as -40°C. During operation, the conditions as specified in the technical data continue to apply.

Information:

It is important to absolutely ensure that there is no forced cooling by air currents in the closed control cabinet, e.g. due to the use of a fan or ventilation slots.

2.5.1.3 Order data

Order number	Short description	Figure
	Analog outputs	
X20AO4622	X20 analog output module, 4 outputs, 10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution	
X20cAO4622	X20 analog output module, coated, 4 outputs, 10 V or 0 to 20 mA / 4 to 20 mA, 13-bit converter resolution	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 111: X20AO4622, X20cAO4622 - Order data

2.5.1.4 Module description

The module is equipped with 4 outputs with 13-bit (including sign) digital converter resolution. It is possible to select between the current and voltage signal using different terminals.

Functions:

- Analog outputs

Analog outputs

The module is equipped with analog outputs with a configurable current and/or voltage signal.

2.5.2 Technical description

2.5.2.1 Technical data

Order number	X20AO4622	X20cAO4622
Short description		
I/O module	4 analog outputs ±10 V or 0 to 20 mA / 4 to 20 mA [1]	4 analog outputs ±10 V or 0 to 20 mA / 4 to 20 mA
General information		
B&R ID code	0x1BA3	0xE212
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using LED status indicator and software	
Channel type	Yes, using software	
Power consumption		
Bus	0.01 W	
Internal I/O	1.8 W (Rev. ≥ J0), 2.2 W (Rev. < J0)	1.8 W
Additional power dissipation caused by actuators (resistive) [W]	-	
Certifications		
CE	Yes	
UKCA	Yes	
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X	
UL	cULus E115267 Industrial control equipment	
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5	
DNV	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)	
LR	ENV1	
KR	Yes	
ABS	Yes	
BV	**EC33B** Temperature: 5 - 55°C Vibration: 4 g EMC: Bridge and open deck	
EAC	Yes	
KC	Yes	-
Analog outputs		
Output	±10 V or 0 to 20 mA / 4 to 20 mA, via different terminals [1]	±10 V or 0 to 20 mA / 4 to 20 mA, via different terminals
Max. output current	10 mA at voltage >5 V 15 mA at voltage <5 V	
Digital converter resolution		
Voltage	±12-bit	
Current	12-bit	
Conversion time	300 µs for all outputs	
Settling time on output change over entire range	500 µs	
Switch on/off behavior	Internal enable relay for startup	
Max. error		
Gain	0.08% [2]	-
Offset	0.05% [3]	-
Voltage		
Gain	0.08% [2]	
Offset	0.05% [3]	
Current		
Gain	0.09% [2]	
Offset	0.05% [3]	
Output protection	Short-circuit proof	
Output format		
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0008 = 2.441 mV	
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0008 = 4.883 µA	
Load per channel		
Voltage	Max. ±10 mA, load ≥1 kΩ	
Current	Load max. 600 Ω (Rev. ≥ J0), 500 Ω (Rev. < J0)	Max. load is 600 Ω
Short-circuit proof	Current limiting ±40 mA	
Output filter	First-order low-pass filter / cutoff frequency 10 kHz	
Max. gain drift	0.015%/°C [2]	-

Table 112: X20AO4622, X20cAO4622 - Technical data

Order number	X20AO4622	X20cAO4622
Max. gain drift		
Voltage	0.015%/°C [2]	
Current	0.02 %/°C [2]	
Max. offset drift	0.032%/°C [3]	-
Max. offset drift		
Voltage	0.032%/°C [3]	
Current	0.032%/°C [3]	
Error caused by load change		
Voltage	Max. 0.11%, from 10 MΩ → 1 kΩ, resistive	
Current	Max. 0.5%, from 1 Ω → 600 Ω, resistive	
Nonlinearity	<0.007% [3]	<0.005% [4]
Insulation voltage between channel and bus	500 V_{eff}	
Electrical properties		
Electrical isolation	Channel isolated from bus Channel not isolated from channel	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation elevation above sea level		
0 to 2000 m	No limitation	
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
Degree of protection per EN 60529	IP20	
Ambient conditions		
Temperature		
Operation		
Horizontal mounting orientation	-25 to 60°C (Rev. ≥ J0), 0 to 55°C (Rev. < J0)	-25 to 60°C
Vertical mounting orientation	-25 to 50°C (Rev. ≥ J0), 0 to 50°C (Rev. < J0)	-25 to 50°C
Derating	See section "Derating".	
Starting temperature	-	Yes, -40°C
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical properties		
Note	Order 1x terminal block X20TB12 separately. Order 1x bus module X20BM11 separately.	Order 1x terminal block X20TB12 separately. Order 1x bus module X20cBM11 separately.
Pitch	12.5$^{+0.2}$ mm	

Table 112: X20AO4622, X20cAO4622 - Technical data

1) 4 to 20 mA: Starting with upgrade version 1.0.2.0 and hardware revision "I0"
2) Based on the current output value.
3) Based on the entire output range.
4) Based on the output range.

2.5.2.2 LED status indicators

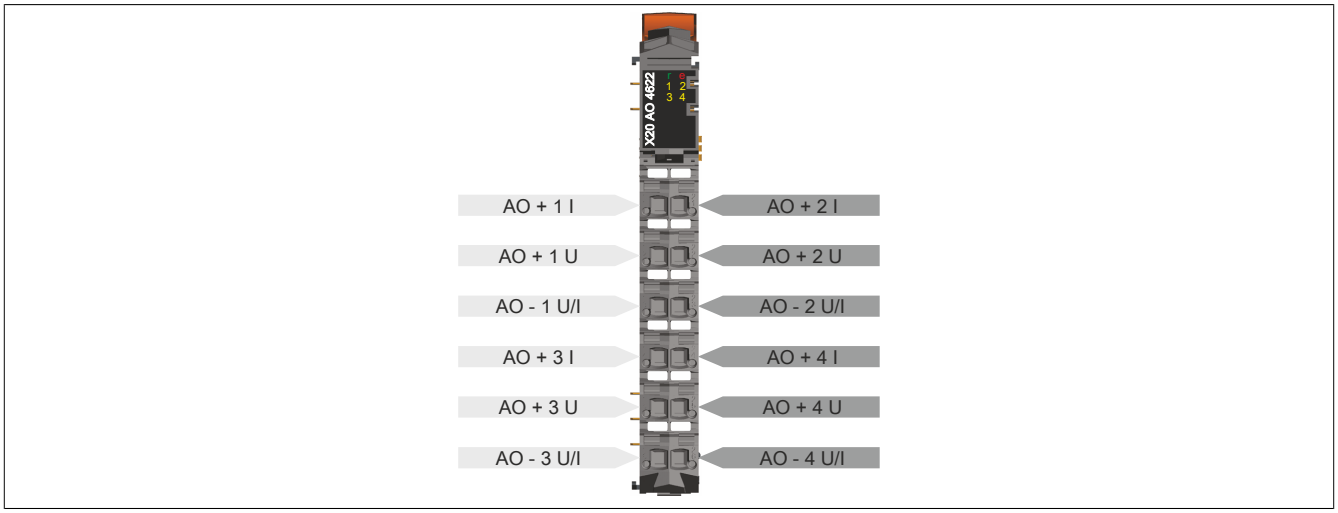
For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 System user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	e + r	Red on / Green single flash		Invalid firmware
	1 - 4	Orange	Off	Value = 0
			On	Value ≠ 0

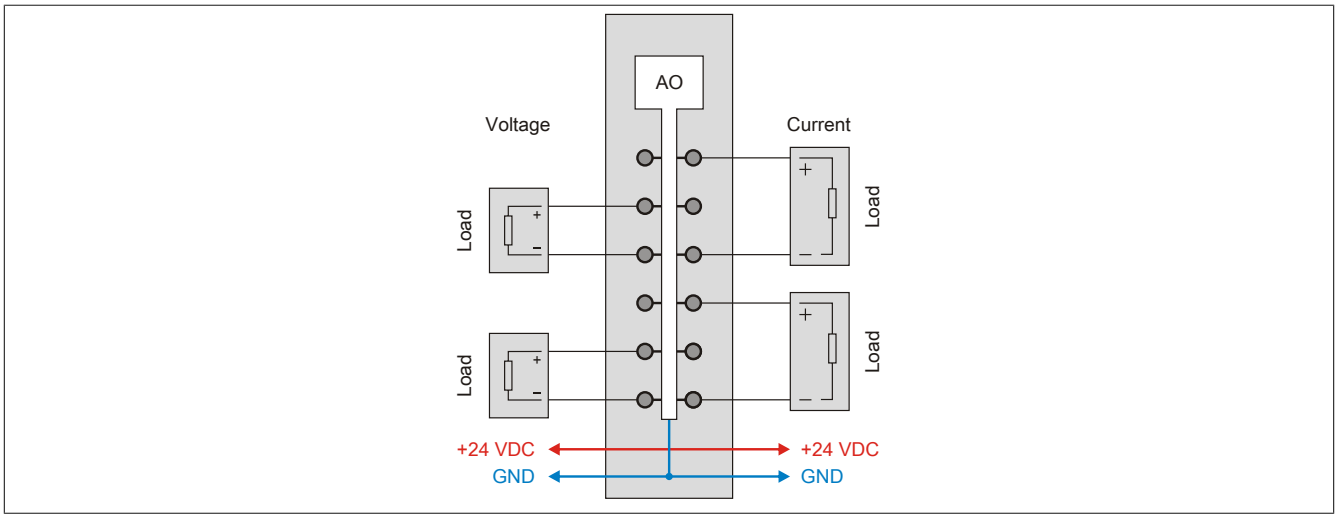
1) Depending on the configuration, a firmware update can take up to several minutes.

2.5.2.3 Pinout

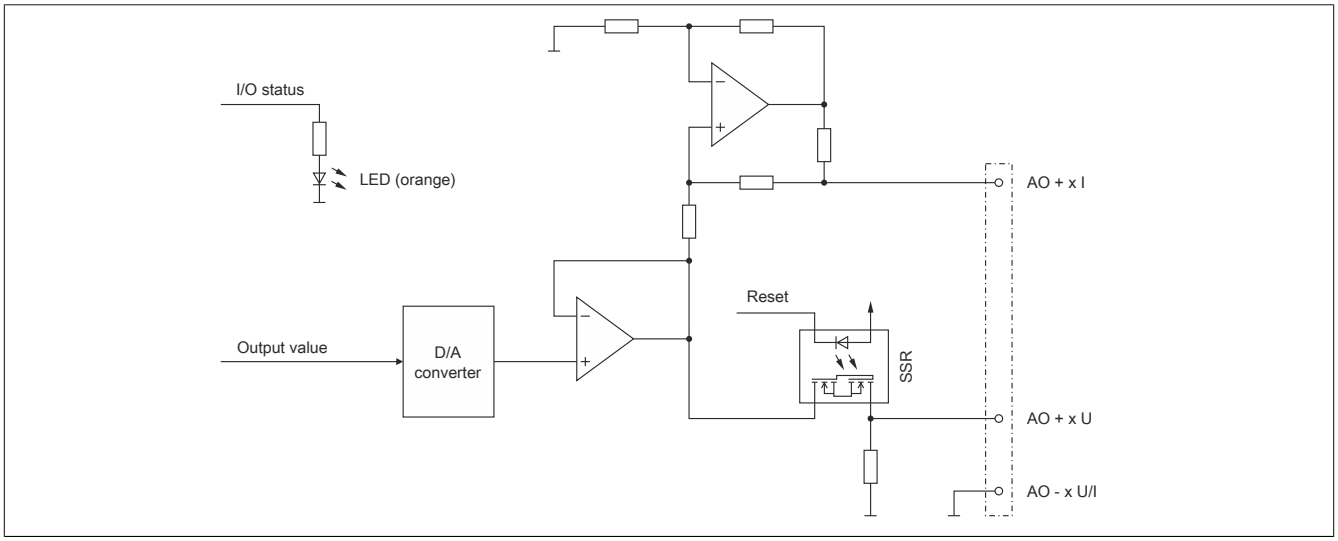
The individual channels can be configured for either current or voltage signals. The type of signal is also determined by the terminals used.



2.5.2.4 Connection example



2.5.2.5 Output circuit diagram

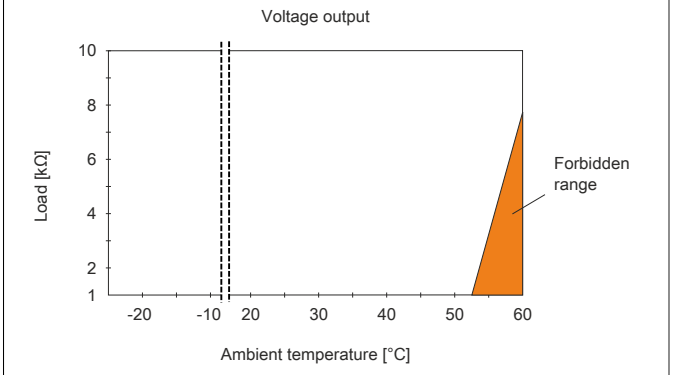
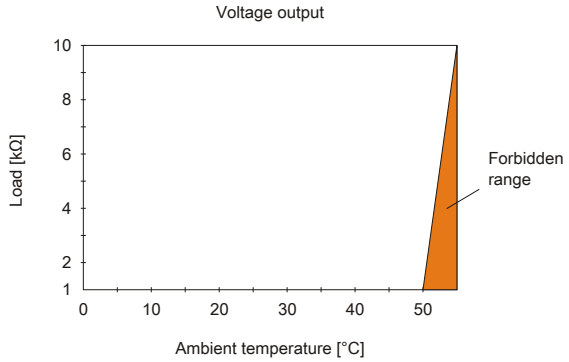
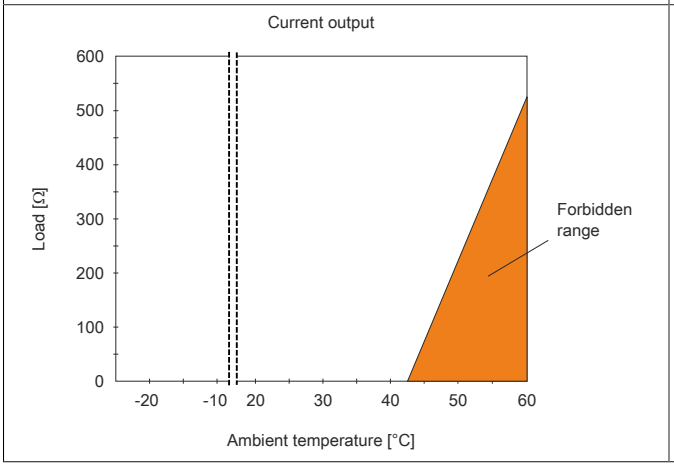
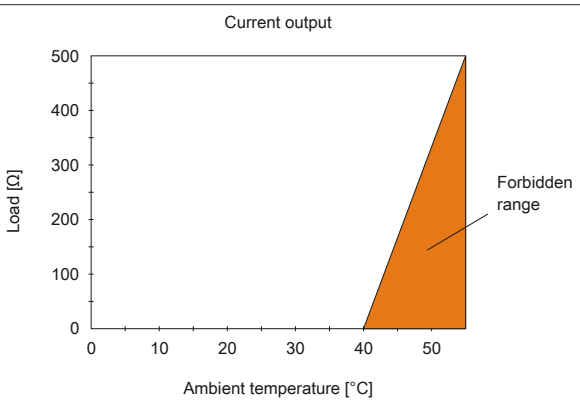


2.5.2.6 Derating

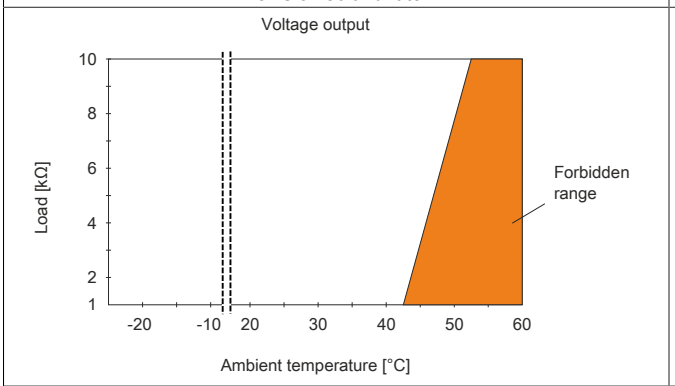
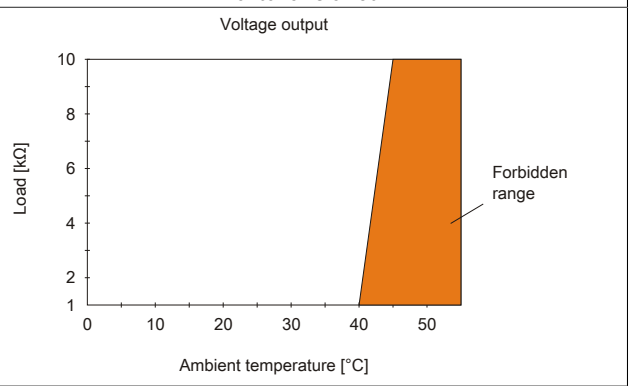
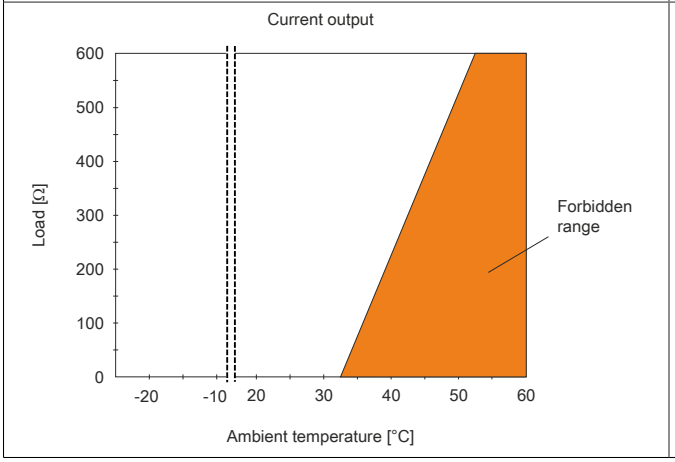
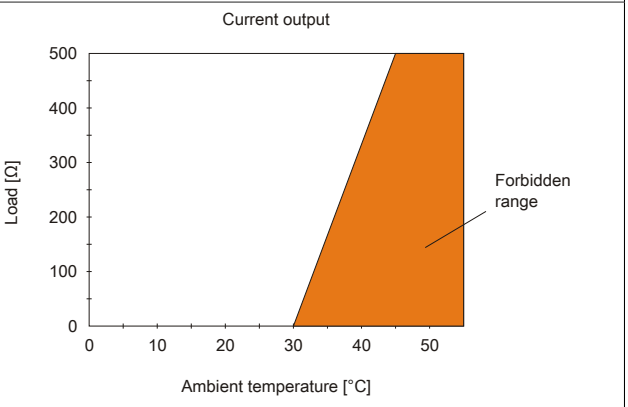
To ensure proper operation, the following points must be taken into account:

- The derating values listed below must be taken into account.
- In mixed operation with one current output, the mean value of both derating curves must be applied.
- In mixed operation with 2 or 3 current outputs, the derating of the current outputs must be applied.

Horizontal mounting orientation

Revision J0 and later	Prior to revision J0
	
	

Vertical mounting orientation

Revision J0 and later	Prior to revision J0
	
	

2.5.3 Function description

2.5.3.1 Analog outputs

The module is equipped with 4 analog outputs.

The individual channels are designed for current and voltage signals. The differentiation is made by different terminal connections; because of different adjustment values for current and voltage, the output signal must be selected. The following output signals can be set:

- ±10 V voltage signal
- 0 to 20 mA current signal
- 4 to 20 mA current signal

Information:

The register is described in "Setting the channel type" on page 742.

2.5.4 Commissioning

2.5.4.1 Optimizing the transfer of analog values

The appropriate function model must be selected for optimal transfer of analog values.

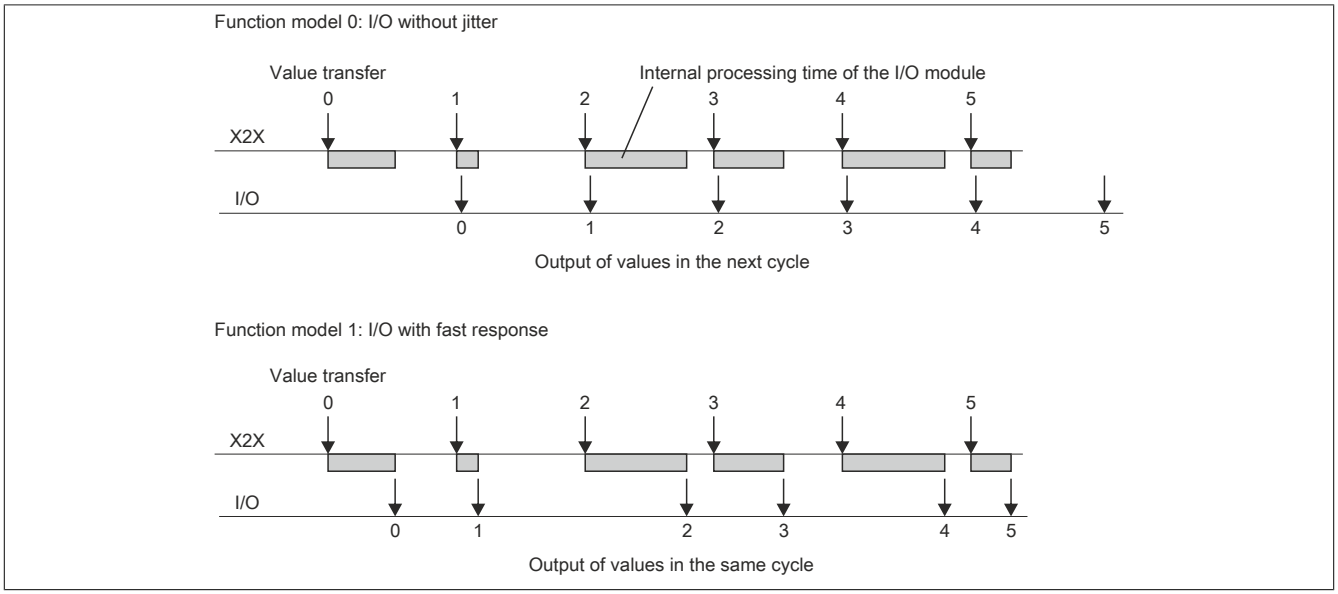
Function model 0: I/O without jitter (standard)

With a minimum cycle of ≥400 µs, the corrected values are output in the next cycle. This reduces jitter to a minimum.

Function model 1: I/O with fast response

With a minimum cycle of ≥400 µs, the corrected values are output in the same cycle (optimized response).

The two function models compared



2.5.5 Register description

2.5.5.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 System user's manual.

2.5.5.2 Function model 0 - Standard and function model 1 - I/O with fast response

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration						
18	ConfigOutput01 (channel type)	USINT		•		•
Analog signal - Communication						
0	AnalogOutput01	INT			•	
2	AnalogOutput02	INT			•	
4	AnalogOutput03	INT			•	
6	AnalogOutput04	INT			•	

2.5.5.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Analog signal - Configuration							
18	-	ConfigOutput01 (channel type)	USINT		•		•
Analog signal - Communication							
0	0	AnalogOutput01	INT			•	
2	2	AnalogOutput02	INT			•	
4	4	AnalogOutput03	INT			•	
6	6	AnalogOutput04	INT			•	

1) The offset specifies the position of the register within the CAN object.

2.5.5.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

2.5.5.3.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

2.5.5.4 Analog outputs

The individual channels can be configured for either current or voltage signals. The type of signal is also determined by the terminals used.

2.5.5.4.1 Output values of the analog output

Name:
AnalogOutput01 to AnalogOutput04

The normalized output values are specified via these registers. After a permissible value is transferred, the module outputs the corresponding current or voltage.

Data type	Values	Information
INT	-32768 to 32767	Voltage signal -10 to 10 VDC
	0 to 32767	Current signal 0 to 20 mA
	0 to 32767	Current signal 4 to 20 mA[1)]

1) Starting with upgrade version 1.0.2.0 and hardware revision "I0"

2.5.5.4.2 Setting the channel type

Name:
ConfigOutput01

The channel type of the outputs can be defined in this register.

Data type	Values	Bus controller default setting
USINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0	Channel 1	0	Voltage signal (bus controller default setting)
		1	Current signal, measurement range corresponding to bit 4
...		...	
3	Channel 4	0	Voltage signal
		1	Current signal, measurement range corresponding to bit 7
4	Channel 1: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal
...		...	
7	Channel 4: Current measurement range	0	0 to 20 mA current signal
		1	4 to 20 mA current signal

2.5.5.5 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
250 µs

2.5.5.6 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time
400 µs

2.6 X20(c)AO4632

2.6.1 General information

The module is equipped with 4 outputs with 16-bit (including sign) digital converter resolution. It is possible to select between the current and voltage signal using different terminals.

- 4 analog outputs
- Either current or voltage signal possible
- 16-bit digital converter resolution

2.6.2 Coated modules

Coated modules are X20 modules with a protective coating for the electronics component. This coating protects X20c modules from condensation and corrosive gases.
The modules' electronics are fully compatible with the corresponding X20 modules.

For simplification purposes, only images and module IDs of uncoated modules are used in this data sheet.

The coating has been certified according to the following standards:

- Condensation: BMW GS 95011-4, 2x 1 cycle
- Corrosive gas: EN 60068-2-60, method 4, exposure 21 days

2.6.2.1 -40°C starting temperature

The starting temperature describes the minimum permissible ambient temperature when the power is switched off at the time the coated module is switched on. This is permitted to be as low as -40°C. During operation, the conditions as specified in the technical data continue to apply.

Information:

It is important to absolutely ensure that there is no forced cooling by air currents in a closed control cabinet, for example using a fan or ventilation slots.

2.6.3 Order data

Order number	Short description	Figure
	Analog outputs	
X20AO4632	X20 analog output module, 4 outputs, ±10 V or 0 to 20 mA, 16-bit converter resolution	
X20cAO4632	X20 analog output module, coated, 4 outputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, NetTime function	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
X20cBM11	X20 bus module, coated, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 113: X20AO4632, X20cAO4632 - Order data

2.6.4 Technical data

Order number	X20AO4632	X20cAO4632
Short description		
I/O module	4 analog outputs ±10 V or 0 to 20 mA	
General information		
B&R ID code	0x1BA5	0xD575
Status indicators	I/O function per channel, operating state, module status	
Diagnostics		
Module run/error	Yes, using LED status indicator and software	Yes, using status LED and software
Channel type	Yes, using software	
Power consumption		
Bus	0.01 W	
Internal I/O	1.8 W (Rev. ≥ J0), 2.2 W (Rev. < J0)	1.8 W
Additional power dissipation caused by actuators (resistive) [W]	-	
Certifications		
CE	Yes	
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X	
UL	cULus E115267 Industrial control equipment	
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5	
DNV GL	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)	
LR	ENV1	
KR	Yes	
EAC	Yes	
KC	Yes	-
Analog outputs		
Output	±10 V or 0 to 20 mA, via different terminal connections	
Digital converter resolution		
Voltage	±15-bit	
Current	15-bit	
Conversion time	50 µs for all outputs	
Settling time on output change over entire range	500 µs	
Switch on/off behavior	Internal enable relay for startup	Internal enable relay for booting
Max. error		
Gain	0.04% [1]	-
Offset	0.022% [2]	-
Voltage		
Gain	0.04% [1]	
Offset	0.022% [2]	
Current		
Gain	0.09% [1]	
Offset	0.045% [2]	
Output protection	Short-circuit proof	Short circuit protection
Output format		
Voltage	INT 0x8001 - 0x7FFF / 1 LSB = 0x0001 = 305.176 µV	
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 610.352 nA	
Load per channel		
Voltage	Max. ±10 mA, load ≥1 kΩ	Max. ±10 mA, load ≥1 kΩ
Current	Load max. 600 Ω (Rev. ≥ J0), 500 Ω (Rev. < J0)	Max. load is 600 Ω
Short-circuit proof	Current limiting ±40 mA	
Output filter	First-order low-pass filter / cutoff frequency 10 kHz	1st-order low pass / cutoff frequency 10 kHz
Max. gain drift	0.01 %/°C [1]	-
Max. gain drift		
Voltage	0.01 %/°C [1]	
Current	0.02%/°C [1]	0.02 %/°C [1]
Max. offset drift	0.012%/°C [2]	-
Max. offset drift		
Voltage	0.012%/°C [2]	0.012 %/°C [2]
Current	0.012%/°C [2]	0.012 %/°C [2]
Error caused by load change		
Voltage	Max. 0.11%, from 10 MΩ → 1 kΩ, resistive	
Current	Max. 0.5%, from 1 Ω → 600 Ω, resistive	
Nonlinearity	<0.005% [3]	
Isolation voltage between channel and bus	500 V_{eff}	

Table 114: X20AO4632, X20cAO4632 - Technical data

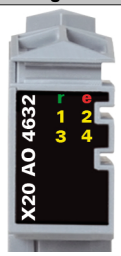
Order number	X20AO4632	X20cAO4632
Electrical properties		
Electrical isolation	Channel isolated from bus Channel not isolated from channel	
Operating conditions		
Mounting orientation		
Horizontal	Yes	
Vertical	Yes	
Installation elevation above sea level		
0 to 2000 m	No limitation	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m	
Degree of protection per EN 60529	IP20	
Ambient conditions		
Temperature		
Operation		
Horizontal mounting orientation	-25 to 60°C (Rev. ≥ J0), 0 to 55°C (Rev. < J0)	-25 to 60°C
Vertical mounting orientation	-25 to 50°C (Rev. ≥ J0), 0 to 50°C (Rev. < J0)	-25 to 50°C
Derating	See section "Derating".	See section "Derating"
Storage	-40 to 85°C	
Transport	-40 to 85°C	
Relative humidity		
Operation	5 to 95%, non-condensing	Up to 100%, condensing
Storage	5 to 95%, non-condensing	
Transport	5 to 95%, non-condensing	
Mechanical properties		
Note	Order 1x terminal block X20TB12 separately. Order 1x bus module X20BM11 separately.	Order 1x X20TB12 terminal block separately Order 1x X20cBM11 bus module separately
Pitch	12.5 $^{+0.2}$ mm	12.5$^{+0.2}$ mm

Table 114: X20AO4632, X20cAO4632 - Technical data

1) Based on the current output value.
2) Based on the entire output range.
3) Based on the output range.

2.6.5 LED status indicators

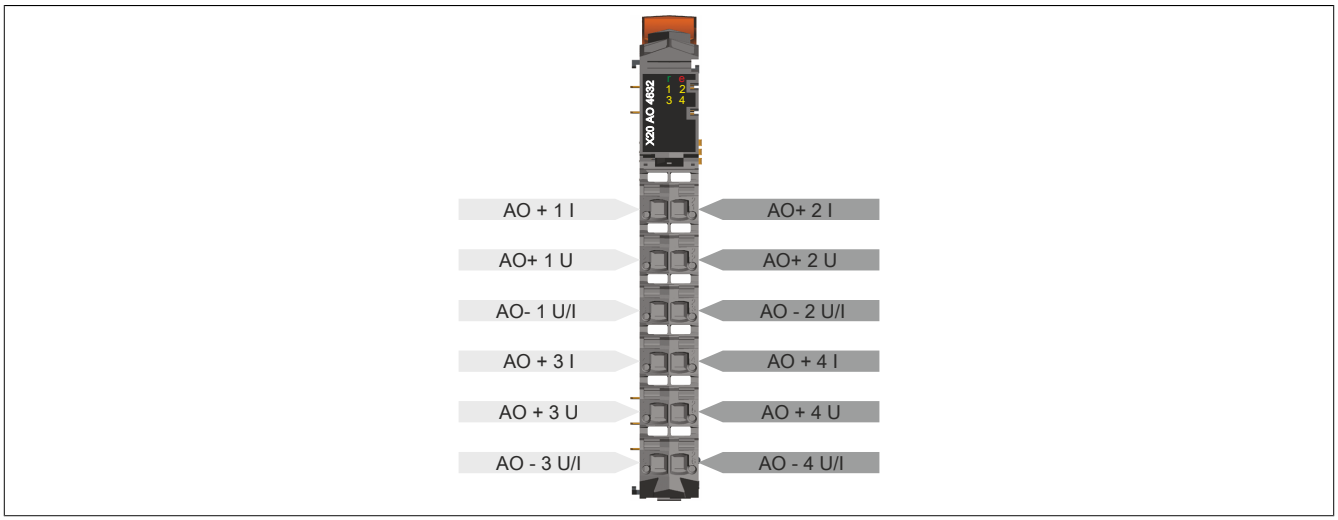
For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 system user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	1 - 4	Orange	Off	Value = 0
			On	Value ≠ 0

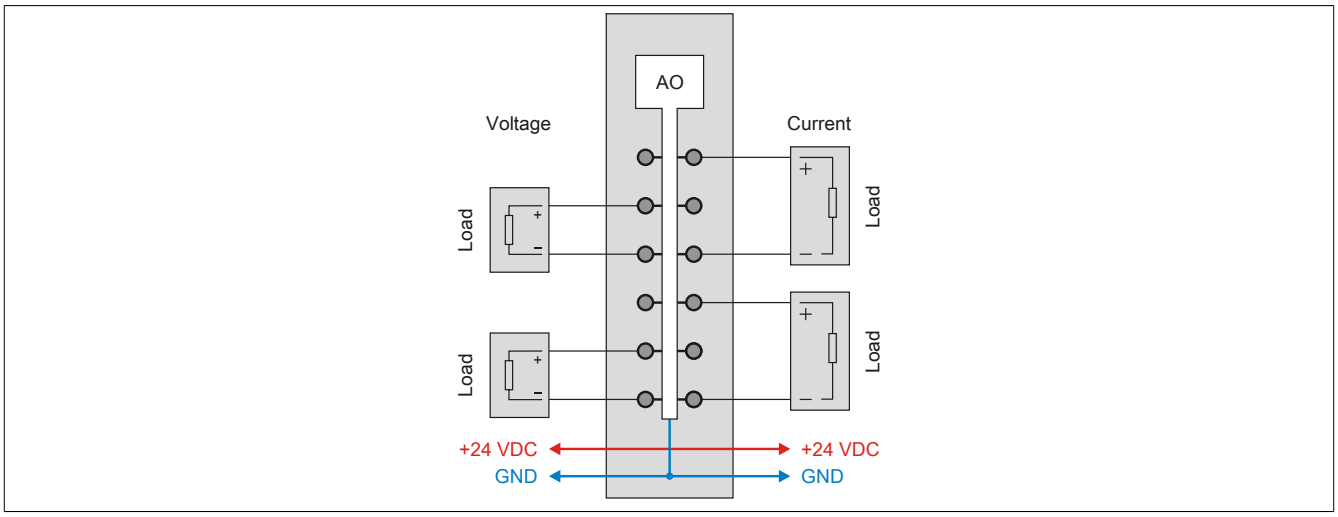
1) Depending on the configuration, a firmware update can take up to several minutes.

2.6.6 Pinout

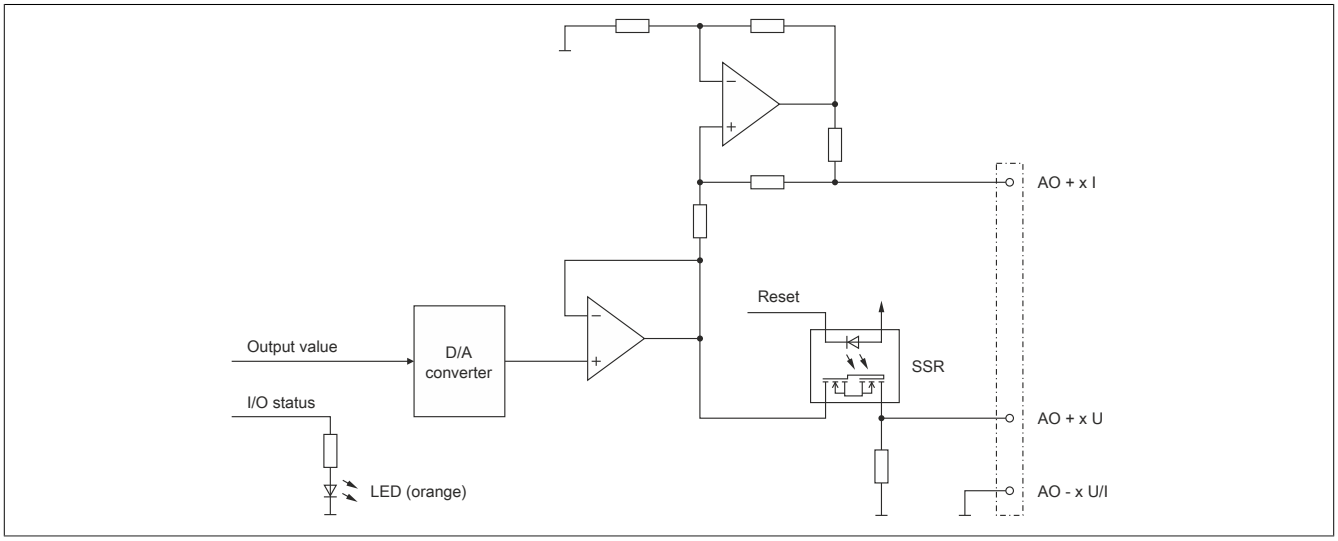
The individual channels can be configured for either current or voltage signals. The type of signal is also determined by the terminals used.



2.6.7 Connection example



2.6.8 Output circuit diagram

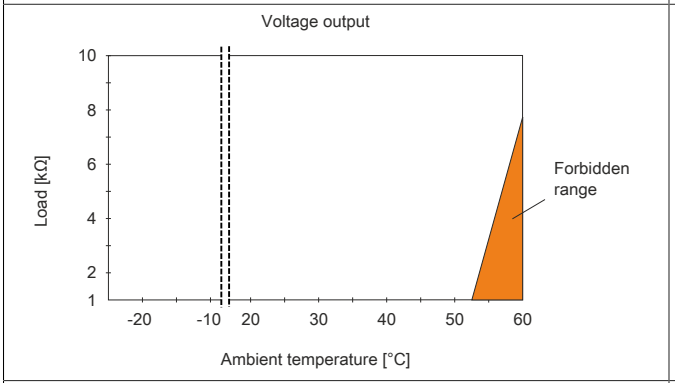
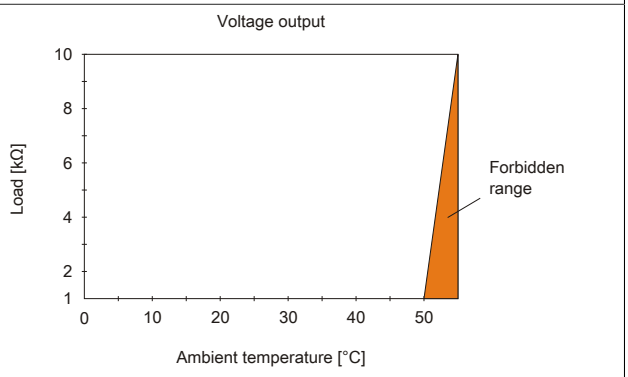
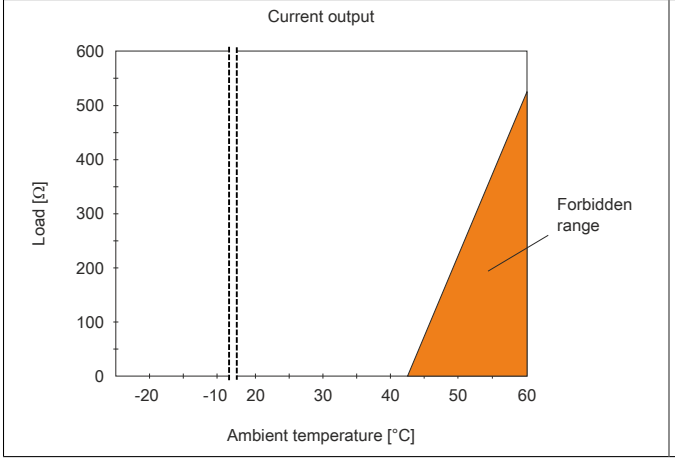
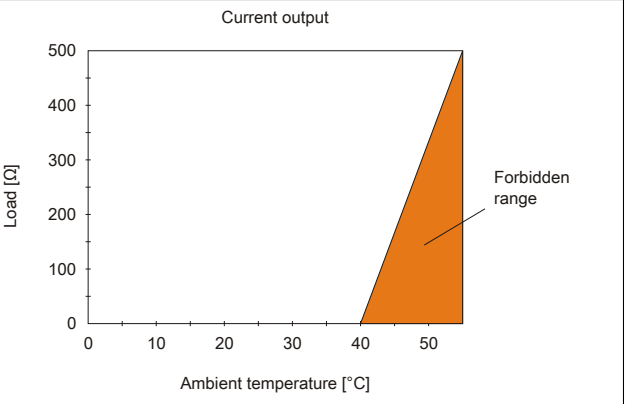


2.6.9 Derating

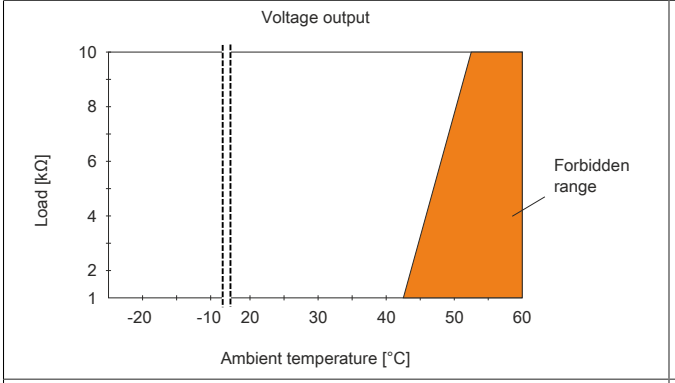
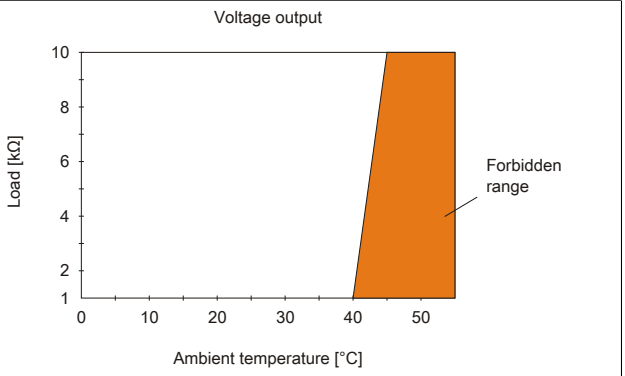
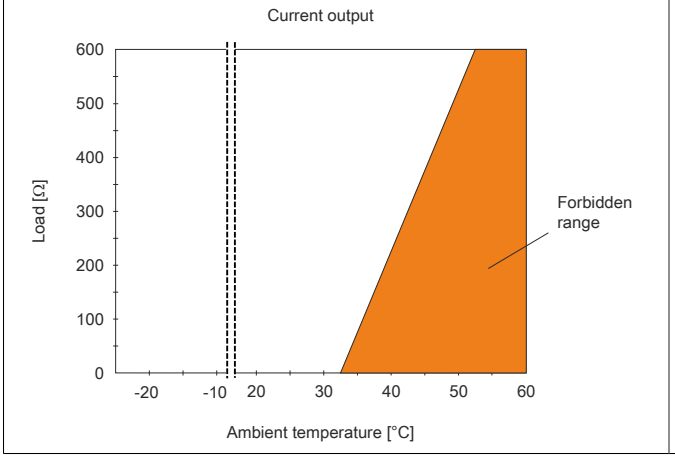
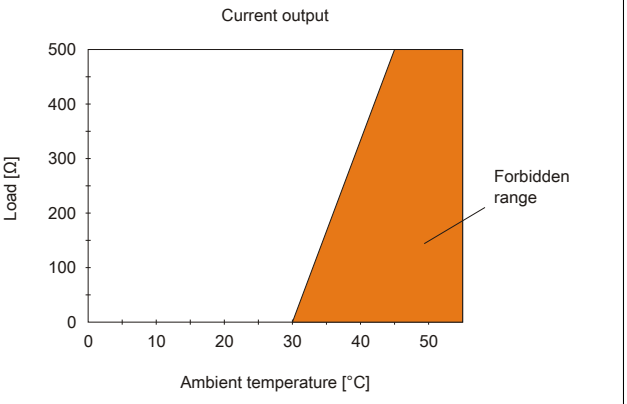
To ensure proper operation, the following points must be taken into account:

- The derating values listed below must be taken into account.
- In mixed operation with one current output, the mean value of both derating curves must be applied.
- In mixed operation with 2 or 3 current outputs, the derating of the current outputs must be applied.

Horizontal mounting orientation

Revision J0 and later	Prior to revision J0
	
	

Vertical mounting orientation

Revision J0 and later	Prior to revision J0
	
	

2.6.10 Register description

2.6.10.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 system user's manual.

2.6.10.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration						
0	ConfigOutput01 (channel type)	UINT				•
Analog signal - Communication						
Index * 2	AnalogOutput0N (Index N = 1 to 4)	INT			•	
10 + Index * 4	AnalogOutputDelayed0N (Index N = 0 to 3)	INT			•	
12	OutputDelayConfig00	UINT			•	
18	OutputDelayConfig01	UINT			•	
14	AnalogOutputLatchTime00	UINT	•			
22	AnalogOutputLatchTime01	UINT	•			
20	Error	UINT	•			

2.6.10.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog signal - Configuration							
0	-	ConfigOutput01 (channel type)	UINT				•
Analog signal - Communication							
10 + Index * 4	Index * 2 - 2	AnalogOutput0N (Index N = 1 to 4)	INT			•	

1) The offset specifies the position of the register within the CAN object.

2.6.10.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

2.6.10.3.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

2.6.10.4 Analog output - Configuration

2.6.10.4.1 Setting the channel type

Name:
ConfigOutput01

This register can be used to set the channel type of the outputs.

Each channel is capable of handling either current or voltage signals. The type of signal is determined by the terminal connections used. Since current and voltage require different adjustment values, it is also necessary to configure the desired type of output signal. The following output signals can be set:

- ±10 V voltage signal
- 0 to 20 mA current signal

Data type	Values	Bus controller default setting
UINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0 - 7	Reserved	0	
8	Channel 1	0	Voltage signal (bus controller default setting)
		1	Current signal
...		...	
11	Channel 4	0	Voltage signal (bus controller default setting)
		1	Current signal
12 - 15	Reserved	0	

2.6.10.5 Analog output - Configuration

2.6.10.5.1 Output values of the analog outputs

Name:
AnalogOutput01 to AnalogOutput04

These registers provide the standardized output values. Once a permitted value is received, the module outputs the respective current or voltage.

Information:

The value "0" disables the channel status LED.

Data type	Value	
INT	-32767 to 32767	Voltage
	0 to 32767	Current

2.6.10.5.2 Value for delayed output

Name:
AnalogOutputDelayed00 to AnalogOutputDelayed03

These registers contain the values with which the analog outputs are overwritten after the delay configured with "OutputDelayConfig0x" on page 750 has expired.

Data type	Value	Output Signal
INT	-32768 to 32767	Voltage signal -10 VDC to 10 VDC
	0 to 32767	Current signal 0 mA to 20 mA

2.6.10.5.3 Configuration of the output delay

Name:
OutputDelayConfig00 to OutputDelayConfig01

2 configurations independent from each other can be created using these registers.

The delay time after which "AnalogOutputDelay0x" on page 749 should overwrite the channel can be configured using bits 0 to 13. Using bits 14 and 15, the channel is determined for which the configuration is valid.

Each channel can only be overwritten once. No additional channel can be overwritten while the respective time is running.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 13	Delay time for the selected channel	x	Time in µs
14 - 15	Channel	00	Analog output 01
		01	Analog output 02
		10	Analog output 03
		11	Analog output 04

2.6.10.5.4 Delay time for the output value

Name:
AnalogOutputLatchTime00 to AnalogOutputLatchTime01

These registers can be used to read when the respective overwrite value was actually written on the output.

Data type	Value
UINT	Actual delay time

2.6.10.5.5 Error register for counter

Name:
Error

There are some limitations because 2 timers are used. This register is available to the user for reporting these potential errors.
The error bits are deleted as soon as a valid state is reset.

Data type	Values
UINT	See the bit structure.

Bit structure:

Bit	Description	Value	Information
0	Analog output 01	0	OK
		1	Has already been overwritten
...		...	
3	Analog output 04	0	OK
		1	Has already been overwritten
4	Timer 01	0	OK
		1	Already in use
5	Timer 02	0	OK
		1	Already in use
6	Timer 01 and 02	0	OK
		1	Both timers refer to the same channel number
7 - 15	Reserved	-	

2.6.10.6 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

2.6.10.7 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time
200 µs

2.7 X20AO4632-1

2.7.1 General information

The module is equipped with 4 outputs with 16-bit (including sign) digital converter resolution. It is possible to select between the current and voltage signal using different terminals.

- 4 analog outputs
- Either current or voltage signal possible
- Extended signal range
- 16-bit digital converter resolution
- NetTime timestamp: Switch-off time

NetTime timestamp for output

For many applications, not only the output value is important, but also the exact switching time. The module is equipped with a NetTime timestamp function for this that can define a switching time to the nearest microsecond.

The timestamp function is based on synchronized timers. The controller can predefine output events and provide them with a timestamp. After transferring the respective data, including the exact time, the module executes the predefined action at the exactly defined time.

2.7.1.1 Other applicable documents

For additional and supplementary information, see the following documents.

Other applicable documents

Document name	Title
MAX20	X20 System user's manual
MAEMV	Installation / EMC guide

2.7.2 Order data

Order number	Short description	Figure
	Analog outputs	
X20AO4632-1	X20 analog output module, 4 outputs, ±11 V or 0 to 22 mA, 16-bit converter resolution, NetTime function	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 115: X20AO4632-1 - Order data

2.7.3 Technical description

2.7.3.1 Technical data

Order number	X20AO4632-1
Short description	
I/O module	4 analog outputs ±11 V or 0 to 22 mA
General information	
B&R ID code	0xC36F
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using LED status indicator and software
Channel type	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	2.15 W
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
UKCA	Yes
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
DNV	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
LR	ENV1
KR	Yes
ABS	Yes
EAC	Yes
KC	Yes
Analog outputs	
Output	±11 V or 0 to 22 mA, via different terminal connections
Digital converter resolution	
Voltage	±15-bit
Current	15-bit
Conversion time	50 µs for all outputs
Settling time on output change over entire range	500 µs
Switch on/off behavior	Internal enable relay for startup
Max. error	
Voltage	
Gain	0.05% 1)
Offset	0.015% 2)
Current	
Gain	0.08% 1)
Offset	0.05% 2)
Output protection	Short-circuit proof
Output format	
Voltage	INT 0x8000 - 0x7FFF / 1 LSB = 0x0001 = 335.693 µV
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 671.386 nA
Load per channel	
Voltage	Max. ±11 mA, load ≥1 kΩ
Current	Max. load is 600 Ω
Short-circuit proof	Current limiting ±40 mA
Output filter	First-order low-pass filter / cutoff frequency 10 kHz
Max. gain drift	
Voltage	0.008 %/°C 1)
Current	0.011%/°C 1)
Max. offset drift	
Voltage	0.003 %/°C 2)
Current	0.008 %/°C 2)
Error caused by load change	
Voltage	Max. 0.1%, from 10 MΩ → 1 kΩ, resistive
Current	Max. 0.5%, from 1 Ω → 600 Ω, resistive
Nonlinearity	<0.007% 2)
Insulation voltage between channel and bus	500 V_{eff}

Table 116: X20AO4632-1 - Technical data

Order number	X20AO4632-1
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitation
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	See section "Derating".
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x terminal block X20TB12 separately. Order 1x bus module X20BM11 separately.
Pitch	12.5$^{+0.2}$ mm

Table 116: X20AO4632-1 - Technical data

1) Based on the current output value.
2) Based on the entire output range.

2.7.3.2 LED status indicators

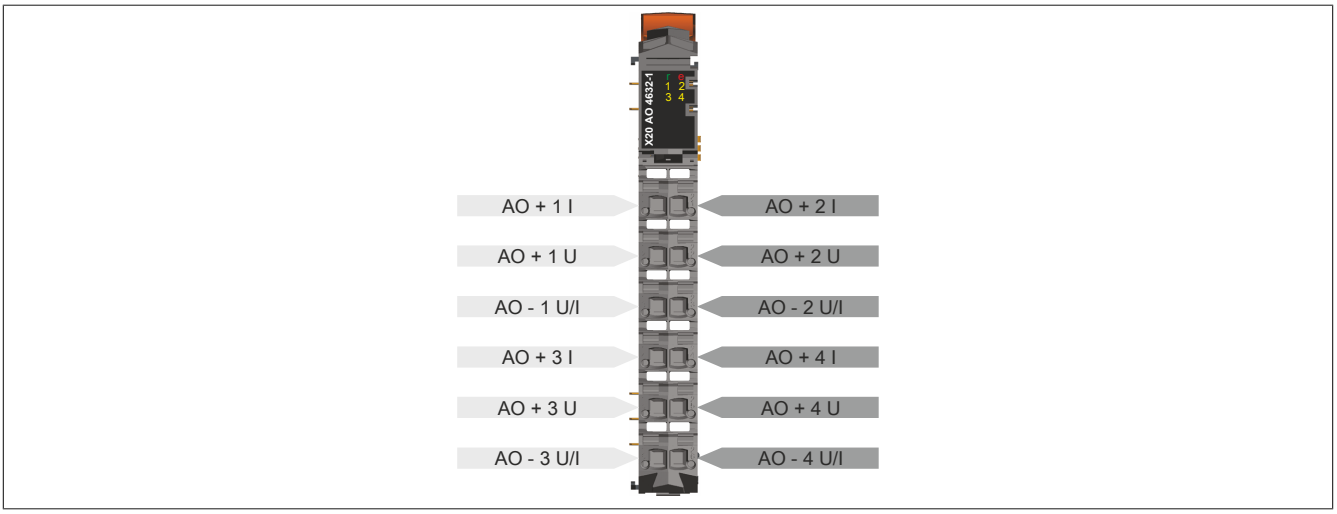
For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 System user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	1 - 4	Orange	Off	Value = 0
			On	Value ≠ 0

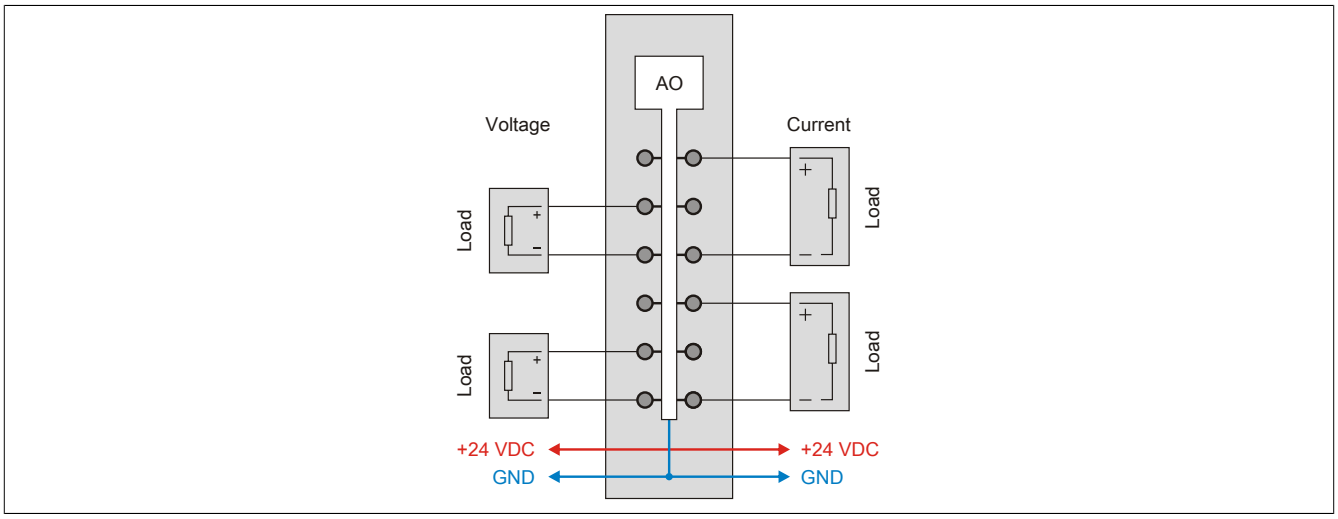
1) Depending on the configuration, a firmware update can take up to several minutes.

2.7.3.3 Pinout

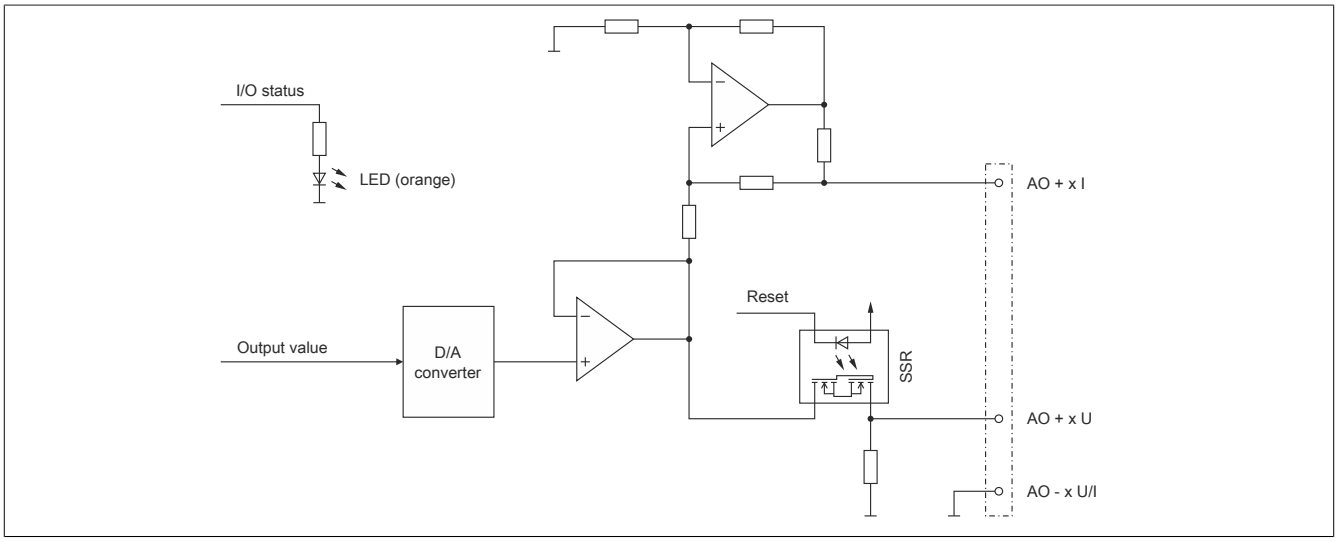
The individual channels can be configured for either current or voltage signals. The type of signal is also determined by the terminals used.



2.7.3.4 Connection example



2.7.3.5 Output circuit diagram



2.7.3.6 Derating

To ensure proper operation, the following items must be taken into consideration:

- The following derating listings must be taken into consideration
- For mixed operation with one current output, the average of both derating curves should be used
- For mixed operation with 2 or 3 current outputs, the derating for the current outputs should be used

Horizontal installation

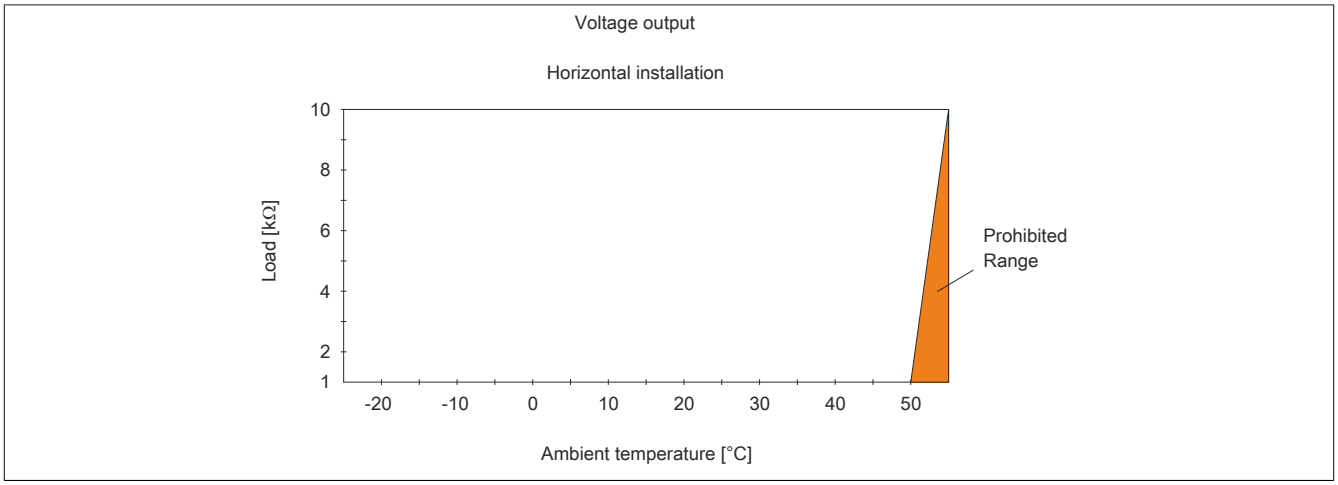


Figure 101: Derating the load with a voltage output and horizontal mounting

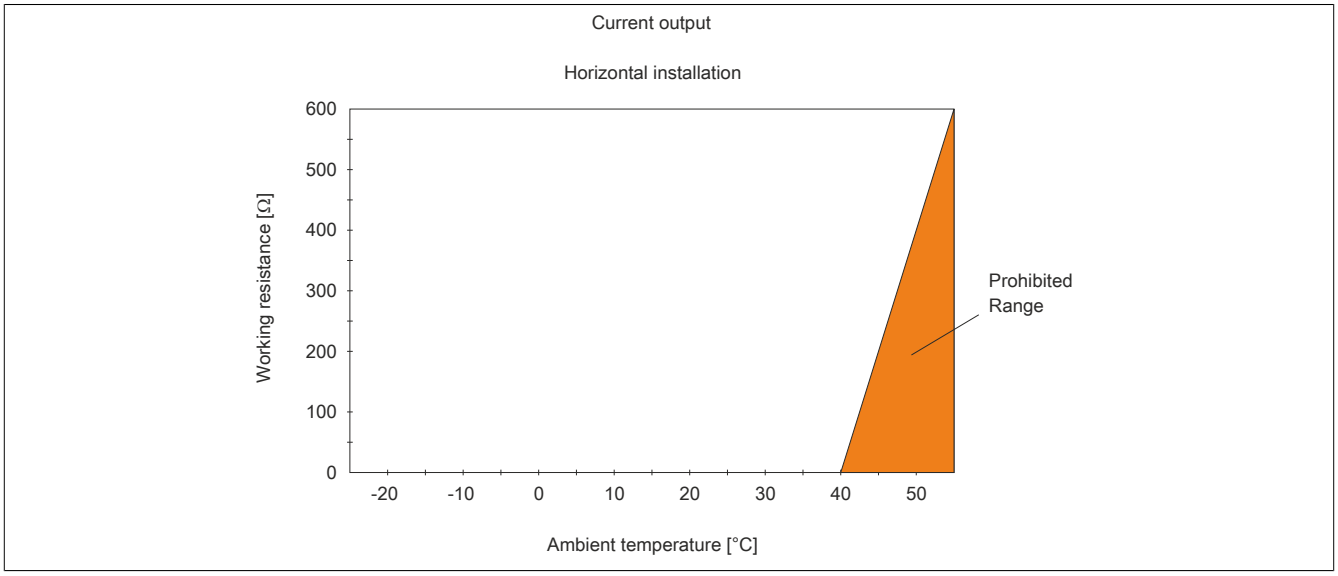


Figure 102: Derating the load with a current output and horizontal mounting

Vertical installation

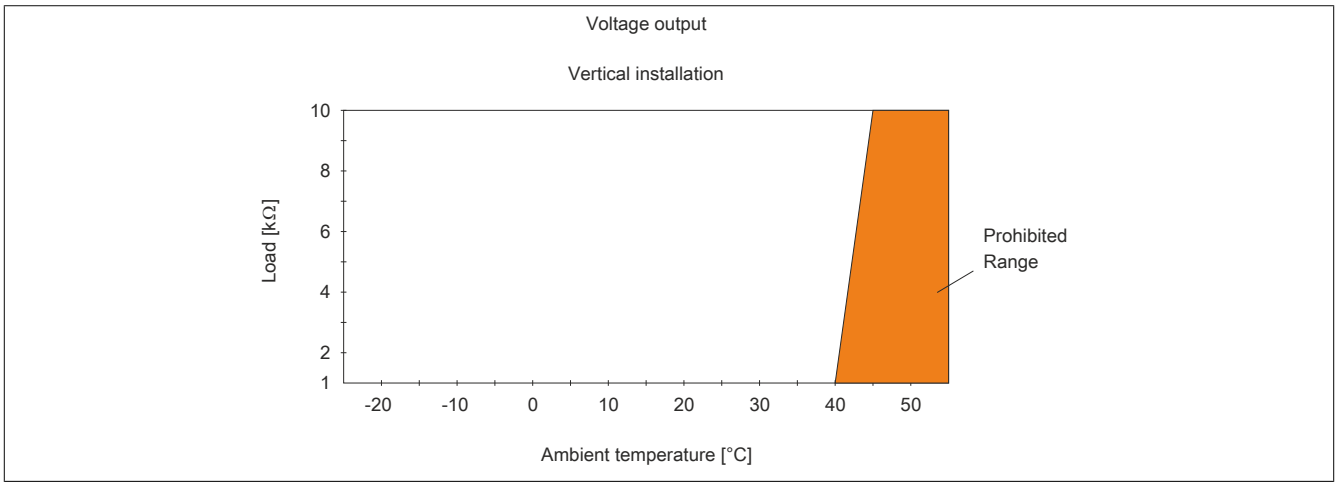


Figure 103: Derating the load with a voltage output and vertical mounting

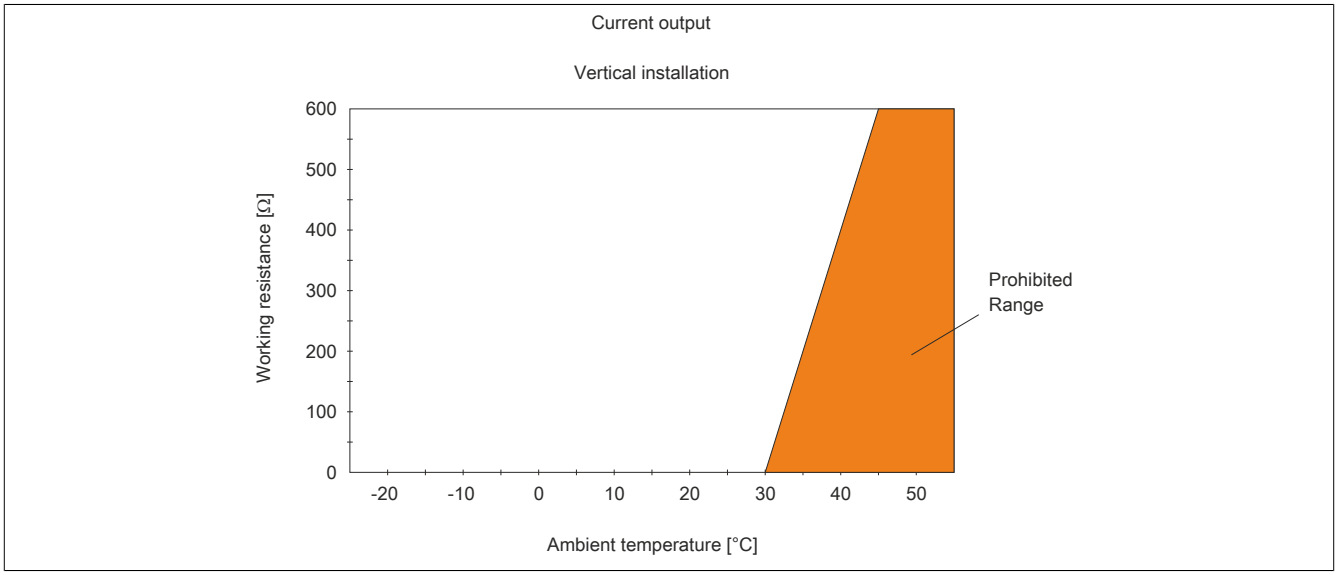


Figure 104: Derating the load with a current output and vertical mounting

2.7.4 Register description

2.7.4.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 System user's manual.

2.7.4.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog output - Configuration						
0	ConfigOutput01 (channel type)	UINT				•
590 + Index*4	Cfo_Channel0NTimeMode (Index N = 1 to 4)	UINT				•
Analog output - Communication						
Index * 2	AnalogOutput0N (Index N = 1 to 4)	INT			•	
457	SDCLifeCount	SINT	•			
794 + Index*8	ValidationTimer0N (Index N = 1 to 4)	INT			•	
796 + Index*8	ValidationTimer0N (Index N = 1 to 4)	DINT			•	
833	Enabling/disabling the output channels	USINT	•		•	
	AnalogOutput01Enable, ~Readback	Bit 0				
	...	...				
	AnalogOutput04Enable, ~Readback	Bit 3				
835	Checking the output values	USINT	•			
	AnalogOutput01OK	Bit 0				
	...	...				
	AnalogOutput04OK	Bit 3				

2.7.4.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog output - Configuration							
0	-	ConfigOutput01 (channel type)	UINT				•
Analog output - Communication							
10 + Index * 4	Index * 2 - 2	AnalogOutput0N (Index N = 1 to 4)	INT			•	

1) The offset specifies the position of the register within the CAN object.

2.7.4.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

2.7.4.3.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

2.7.4.4 General information

The module provides 4 analog outputs. Each channel can output a voltage range of ±11 V or a current range of 0 to 22 mA.

The module also has a time-based watchdog monitor. The user can activate this feature on a channel-by-channel basis as needed.

2.7.4.5 Analog output - Configuration

Each channel is configured independently. The user can also define an optional time-based monitor. To make this possible, 4 watchdog timers were implemented, which can be assigned to the outputs.

2.7.4.5.1 Setting the channel type

Name:
ConfigOutput01

This register can be used to set the channel type of the outputs.

Each channel is capable of handling either current or voltage signals. The type of signal is determined by the terminal connections used. Since current and voltage require different adjustment values, it is also necessary to configure the desired type of output signal. The following output signals can be set:

- ±11 V voltage signal
- 0 to 22 mA current signal

Data type	Values	Bus controller default setting
UINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0 - 7	Reserved	0	
8	Channel 1	0	Voltage signal (bus controller default setting)
		1	Current signal
...		...	
11	Channel 4	0	Voltage signal (bus controller default setting)
		1	Current signal
12 - 15	Reserved	0	

2.7.4.5.2 Configuring the time-based watchdog monitor

Name:
Cfo_Channel01TimeMode to Cfo_Channel04TimeMode

This register is used to activate or configure the time-based watchdog monitor for the analog output channels.

Possibilities per channel:

- Validation timer data type: General choice 16 or 32 bit
- Validation window: The maximum value can be further limited within the data type.
- Timer allocation: A separate timer is available for each channel. However, all channels can be configured with the same validation timer, whereby the same settings must be made for the data type and window in the TimeMode registers.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 4	Max. validation time	00000	Disabled
		00001	2 µs
		00010	4 µs
		00011	8 µs
		...	...
		11111	2,147,483,648 µs (~35 min)
5 - 7	Reserved	0	
8 - 9	Timer allocation	00	ValidationTimer01 (default for channel 1)
		01	ValidationTimer02 (default for channel 2)
		10	ValidationTimer03 (default for channel 3)
		11	ValidationTimer04 (default for channel 4)
10 - 14	Reserved	0	
15	Time format	0	16-bit
		1	32-bit

2.7.4.6 Analog output - Communication

In standard mode, the module's outputs are enabled. Based on the configuration and AnalogOutput value, they output the corresponding current or voltage.

If the application requires time-controlled monitoring of the outputs, a validation timer can be assigned to each channel. The validation timer register assigns a validity period to the current output value. If validation is enabled, the module compares the validation time and the NetTime of the X2X Link. If the transmitted validity period is exceeded, the module switches off the channel and resets the output. State "Safety shutdown" is only exited again when a new valid validation time has been transmitted. If enabled, the module reports back which state it is currently in via the error state bit of the channel.

If the value of the validation timer is incremented in each task cycle, the valid validation time will be calculated as follows:

NetTime of the X2X Link master (to which the module is connected)	
+	Time span for transferring data from the X2X Link master to the controller (higher-level system)
+	Cycle time of task class (including tolerance)
+	Time span for transferring data from the controller to the module
+	Time span allowed by the application, e.g. to tolerate the failure of an X2X Link cycle
=	Valid validation time

The AnalogOutputEnableByte is enabled during time-based monitoring. If the timer expires prematurely, the corresponding bit in the AnalogOutputOkayByte is reset and the output drops out. This provides an easy way to achieve a defined state.

2.7.4.6.1 Output values of the analog outputs

Name:
AnalogOutput01 to AnalogOutput04

These registers provide the standardized output values. Once a permitted value is received, the module outputs the respective current or voltage.

Information:

The value "0" disables the channel status LED.

Data type	Value	
INT	-32767 to 32767	Voltage
	0 to 32767	Current

2.7.4.6.2 SDC counter register

Name:
SDCLifeCount

The 8-bit counter register is needed for the SDC software package. It is incremented with the system clock to allow the SDC to check the validity of the data frame.

Data type	Values
SINT	-128 to 127

2.7.4.6.3 Transfer of the timestamp

Name:
ValidationTimer01 to ValidationTimer04

When an output is being monitored, these registers must provide the timestamp which, when reached, will cause the output to shut down automatically. The values must be provided as signed 2-byte or 4-byte values.

For additional information about NetTime and timestamps, see "NetTime Technology" on page 762.

Data type	Values [µs]	
INT	-32768 to 32767	NetTime timestamp of the current output value
DINT	-2,147,483,648 to 2,147,483,647	NetTime timestamp of the current output value

2.7.4.6.4 Enabling/disabling the output channels

Name:
AnalogOutput01Enable to AnalogOutput04Enable
AnalogOutput01EnableReadback to AnalogOutput04EnableReadback

Bye "OutputEnable" is only needed for the channels with enabled time control. The individual bits are used to switch the respective channels on/off. In order to obtain reliable feedback about the current module state, the byte has been additionally implemented as cyclically readable.

Data type	Value
USINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0	AnalogOutput01Enable AnalogOutput01EnableReadback	0	Output deactivated
		1	Output activated
...		...	
3	AnalogOutput04Enable AnalogOutput04EnableReadback	0	Output deactivated
		1	Output activated
4 - 7	Reserved	0	

2.7.4.6.5 Checking the output values

Name:
AnalogOutput01OK to AnalogOutput04OK

These registers are only needed for channels with activated time-based monitoring. The individual bits report whether the respective channel is actually generating the required voltage or current.

Data type	Value
USINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0	AnalogOutput01OK	0	Electrical signal deactivated
		1	Electrical signal activated
...		...	
3	AnalogOutput04OK	0	Electrical signal deactivated
		1	Electrical signal activated
4 - 7	Reserved	0	

2.7.4.7 NetTime Technology

NetTime refers to the ability to precisely synchronize and transfer system times between individual components of the controller or network (controller, I/O modules, X2X Link, POWERLINK, etc.).

This allows the moment that events occur to be determined system-wide with microsecond precision. Upcoming events can also be executed precisely at a specified moment.

2.7.4.7.1 Time information

Various time information is available in the controller or on the network:

- System time (on the PLC, Automation PC, etc.)
- X2X Link time (for each X2X Link network)
- POWERLINK time (for each POWERLINK network)
- Time data points of I/O modules

The NetTime is based on 32-bit counters, which are increased with microsecond resolution. The sign of the time information changes after 35 min, 47 s, 483 ms and 648 µs; an overflow occurs after 71 min, 34 s, 967 ms and 296 µs.

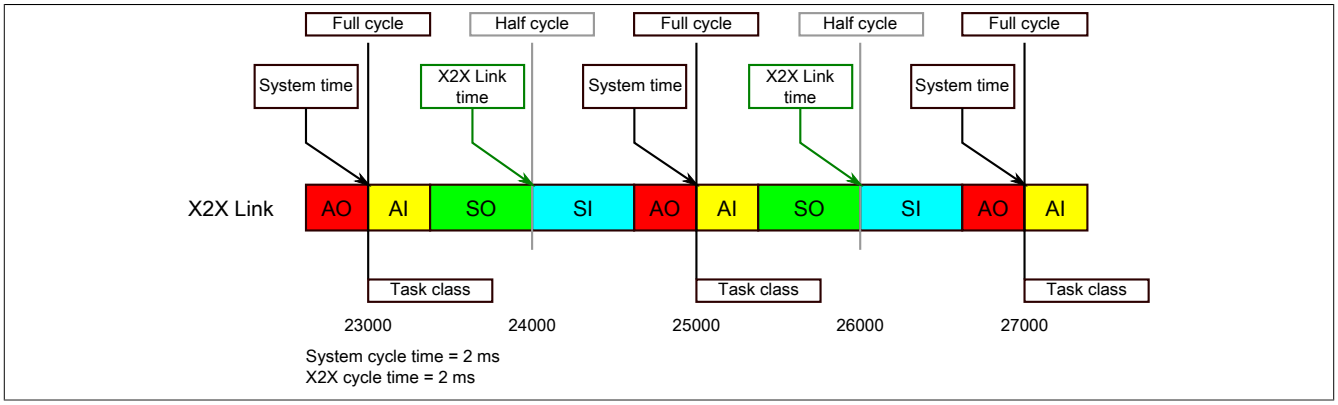
The initialization of the times is based on the system time during the startup of the X2X Link, the I/O modules or the POWERLINK interface.

Current time information in the application can also be determined via library AsIOTime.

2.7.4.7.1.1 Controller data points

The NetTime I/O data points of the controller are latched to each system clock and made available.

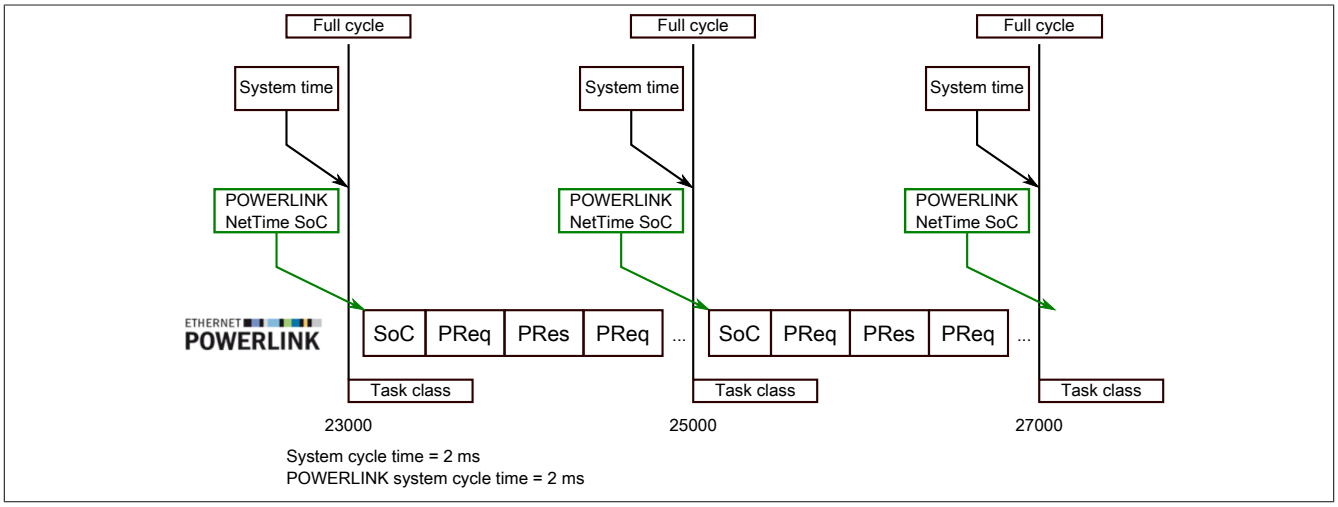
2.7.4.7.1.2 X2X Link - Reference time point



The reference time point on the X2X Link network is always calculated at the half cycle of the X2X Link cycle. This results in a difference between the system time and the X2X Link reference time point when the reference time is read out.

In the example above, this results in a difference of 1 ms, i.e. if the system time and X2X Link reference time are compared at time 25000 in the task, then the system time returns the value 25000 and the X2X Link reference time returns the value 24000.

2.7.4.7.1.3 POWERLINK - Reference time point

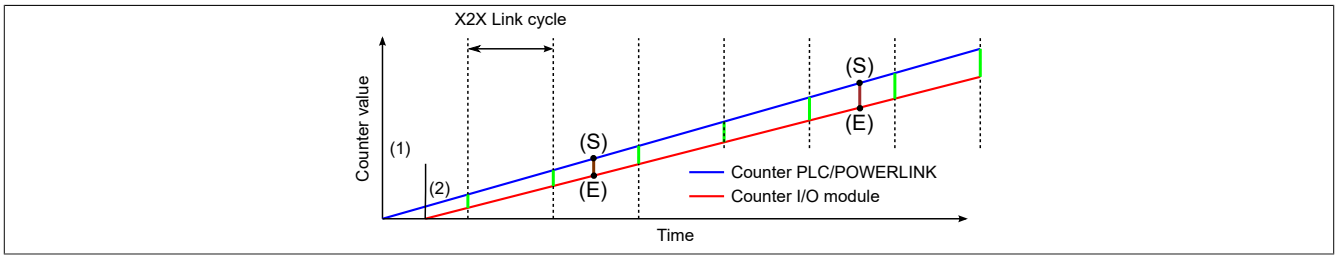


The reference time point on the POWERLINK network is always calculated at the start of cycle (SoC) of the POWERLINK network. The SoC starts 20 µs after the system clock due to the system. This results in the following difference between the system time and the POWERLINK reference time:

POWERLINK reference time = System time - POWERLINK cycle time + 20 µs.

In the example above, this means a difference of 1980 µs, i.e. if the system time and POWERLINK reference time are compared at time 25000 in the task, then the system time returns the value 25000 and the POWERLINK reference time returns the value 23020.

2.7.4.7.1.4 Synchronization of system time/POWERLINK time and I/O module



At startup, the internal counters for the controller/POWERLINK (1) and the I/O module (2) start at different times and increase the values with microsecond resolution.

At the beginning of each X2X Link cycle, the controller or POWERLINK network sends time information to the I/O module. The I/O module compares this time information with the module's internal time and forms a difference (green line) between the two times and stores it.

When a NetTime event (E) occurs, the internal module time is read out and corrected with the stored difference value (brown line). This means that the exact system moment (S) of an event can always be determined, even if the counters are not absolutely synchronous.

Note

The deviation from the clock signal is strongly exaggerated in the picture as a red line.

2.7.4.7.2 Timestamp functions

NetTime-capable modules provide various timestamp functions depending on the scope of functions. If a timestamp event occurs, the module immediately saves the current NetTime. After the respective data is transferred to the controller, including this precise moment, the controller can then evaluate the data using its own NetTime (or system time), if necessary.

2.7.4.7.2.1 Time-based inputs

NetTime Technology can be used to determine the exact moment of a rising edge at an input. The rising and falling edges can also be detected and the duration between 2 events can be determined.

Information:

The determined moment always lies in the past.

2.7.4.7.2.2 Time-based outputs

NetTime Technology can be used to specify the exact moment of a rising edge on an output. The rising and falling edges can also be specified and a pulse pattern generated from them.

Information:

The specified time must always be in the future, and the set X2X Link cycle time must be taken into account for the definition of the moment.

2.7.4.7.2.3 Time-based measurements

NetTime Technology can be used to determine the exact moment of a measurement that has taken place. Both the starting and end moment of the measurement can be transmitted.

2.7.4.8 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

2.7.4.9 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time
200 µs

2.8 X20AO4635

2.8.1 General information

The module is equipped with 4 outputs with 16-bit (including sign) digital converter resolution. It is possible to select between the current and voltage signal using different terminals.

- 4 analog outputs
- Either current or voltage signal possible
- 16-bit digital converter resolution
- Low temperature drift

2.8.2 Order data

Order number	Short description	Figure
	Analog outputs	
X20AO4635	X20 analog output module, 4 outputs, ±10 V or 0 to 20 mA, 16-bit converter resolution, low temperature drift	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 117: X20AO4635 - Order data

2.8.3 Technical data

Order number	X20AO4635
Short description	
I/O module	4 analog outputs, ±10 V or 0 to 20 mA, low temperature drift
General information	
B&R ID code	0xA7FE
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Channel type	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	1.5 W
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
KC	Yes
EAC	Yes
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
DNV GL	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
LR	ENV1
KR	Yes
Analog outputs	
Output	±10 V or 0 to 20 mA, via different terminal connections
Digital converter resolution	
Voltage	±15-bit
Current	15-bit
Conversion time	50 µs for all outputs
Settling time for output changes over entire range	500 µs
Switch on/off behavior	Internal enable relay for booting
Max. error at 25°C	
Gain	0.04% [1]
Offset	0.022% [2]
Output protection	Short circuit protection
Output format	
Voltage	INT 0x8000 - 0x7FFF / 1 LSB = 0x0001 = 305.176 µV
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 610.352 nA
Load per channel	
Voltage	Max. ±10 mA, load ≥ 1 kΩ
Current	Max. load is 500 Ω
Short-circuit proof	Current limiting ±40 mA
Output filter	1st-order low pass / cutoff frequency 10 kHz
Error caused by load change	
Voltage	Max. 0.02%, from 10 MΩ → 1 kΩ, resistive
Current	Max. 0.5%, from 1 Ω → 500 Ω, resistive
Nonlinearity	<0.005%
Isolation voltage between channel and bus	500 V_{eff}
Signal	
0 to 20 mA	
Max. gain drift	0.01 %/°C [1]
Max. offset drift	0.012 %/°C [2]
±10 V	
Max. gain drift	0.0025 %/°C [1]
Max. offset drift	0.001 %/°C [2]
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes

Table 118: X20AO4635 - Technical data

Order number	X20AO4635
Installation elevation above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 55°C
Vertical mounting orientation	-25 to 50°C
Derating	See section "Module operation"
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Spacing	$12.5^{+0.2}$ mm

Table 118: X20AO4635 - Technical data

1) Based on the current output value.
2) Based on the entire output range.

2.8.4 LED status indicators

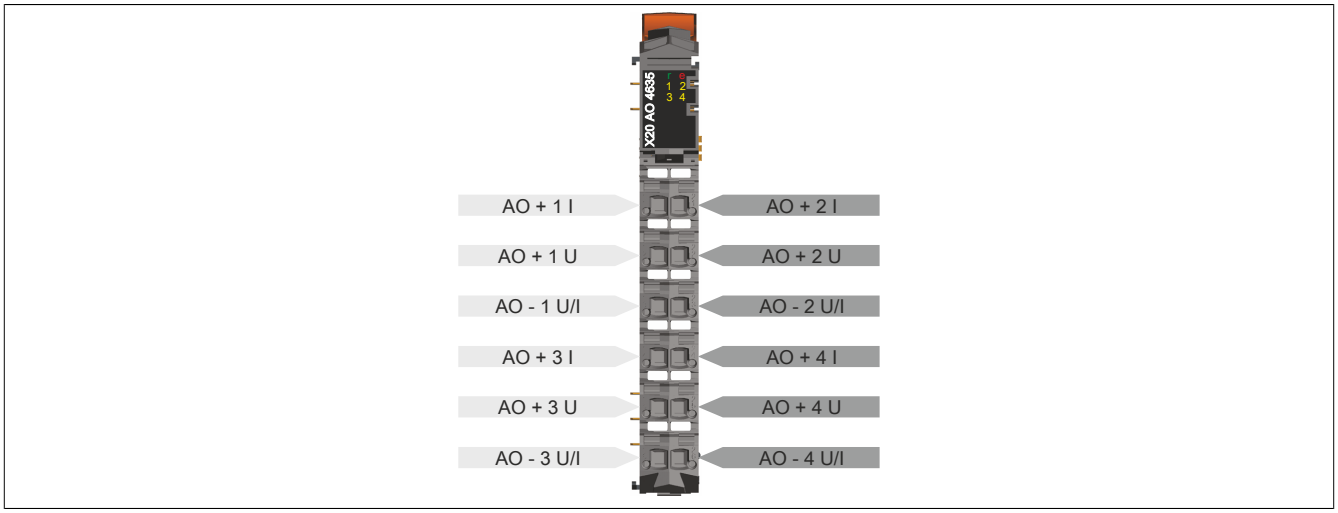
For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 system user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	1 - 4	Orange	Off	Value = 0
			On	Value ≠ 0

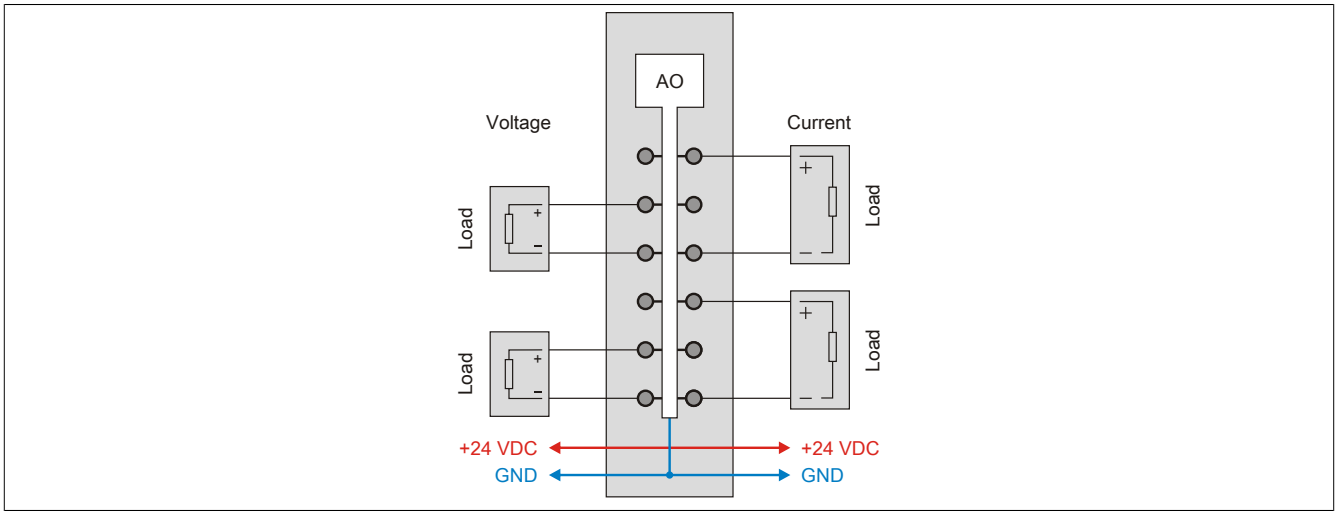
1) Depending on the configuration, a firmware update can take up to several minutes.

2.8.5 Pinout

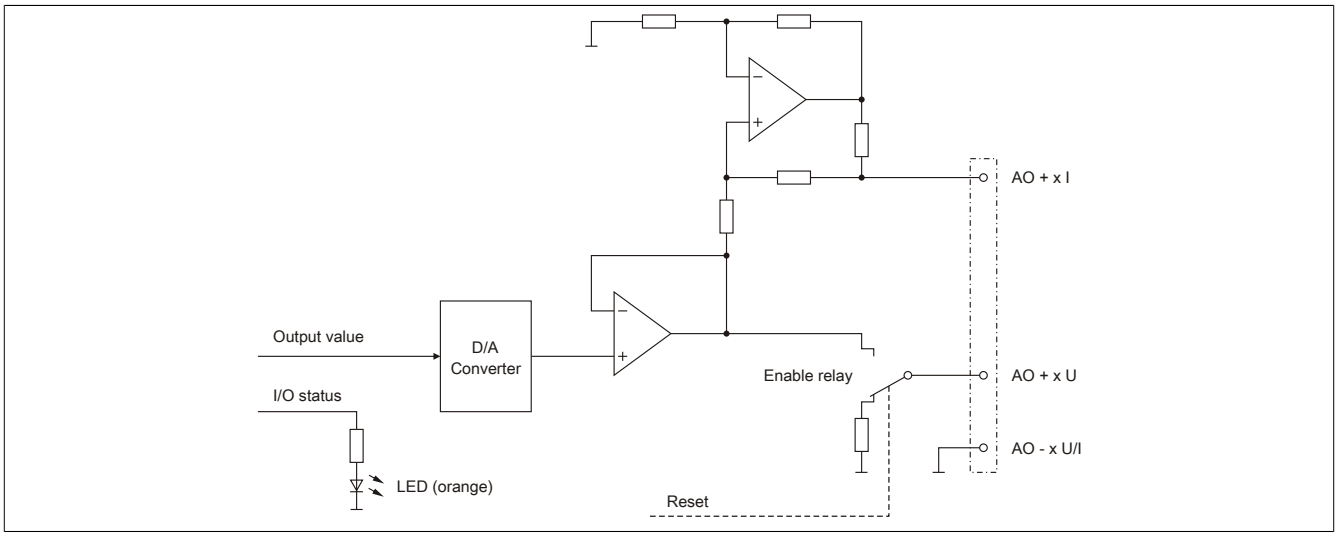
The individual channels can be configured for either current or voltage signals. The type of signal is also determined by the terminals used.



2.8.6 Connection example



2.8.7 Output circuit diagram



2.8.8 Module operation

To ensure proper operation, the following items must be taken into consideration:

- The following derating listings must be taken into consideration
- For mixed operation with one current output, the average of both derating curves should be used
- For mixed operation with 2 or 3 current outputs, the derating for the current outputs should be used

Horizontal installation

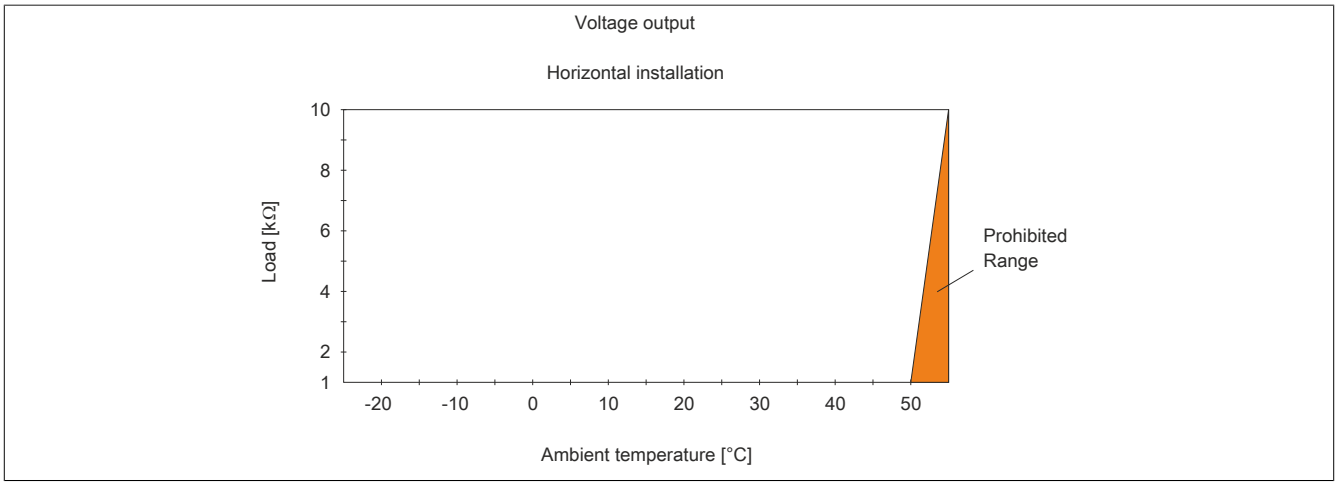
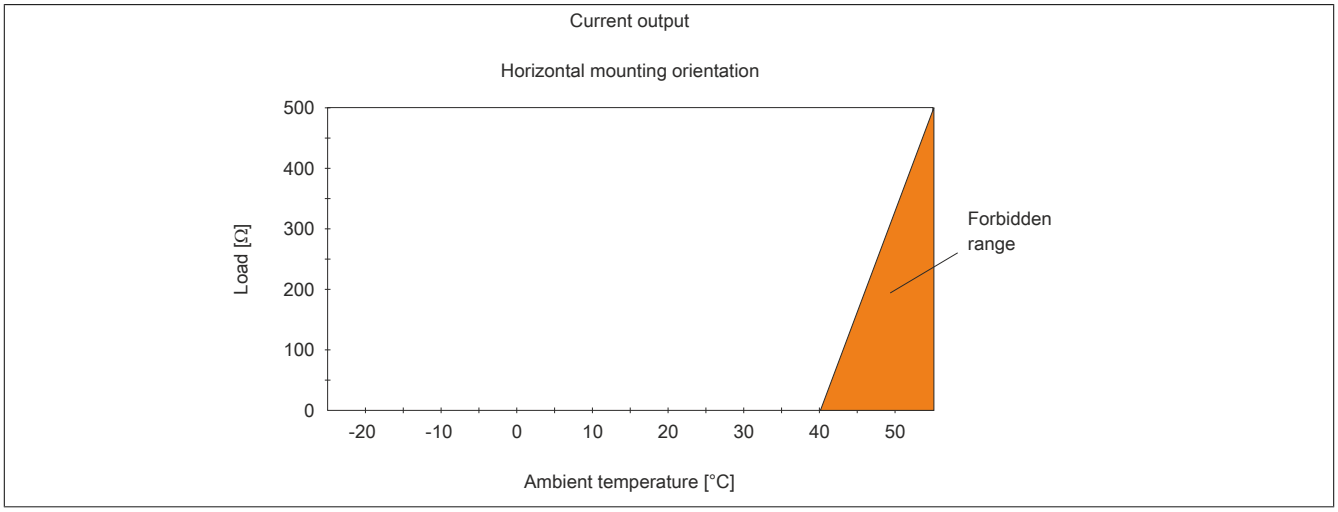


Figure 105: Derating the load with a voltage output and horizontal mounting



Vertical installation

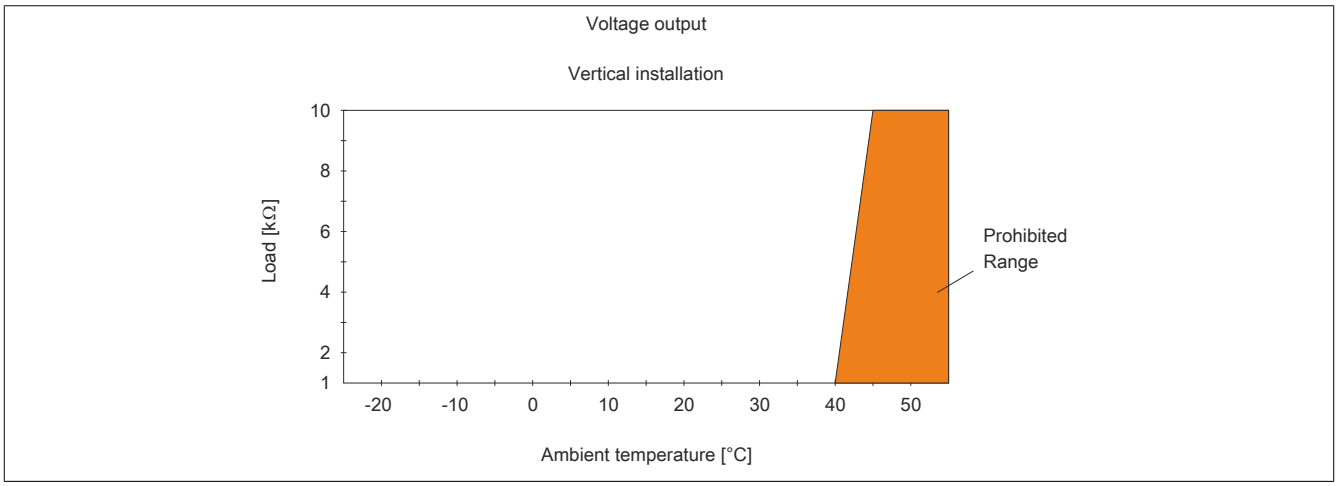
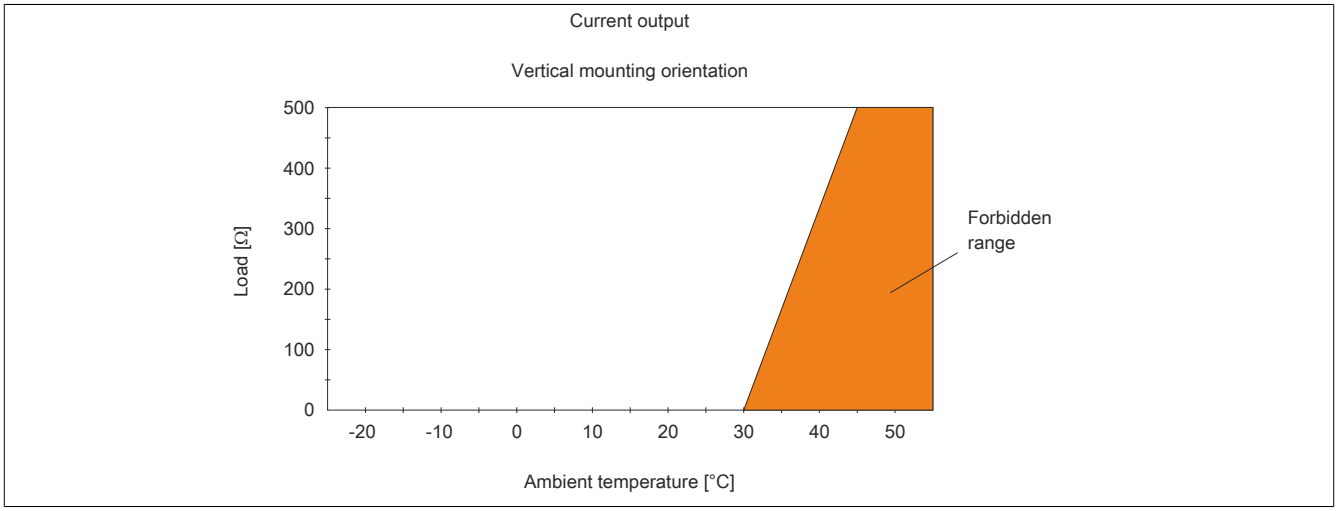


Figure 106: Derating the load with a voltage output and vertical mounting



2.8.9 Register description

2.8.9.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 system user's manual.

2.8.9.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration						
0	ConfigOutput01 (channel type)	UINT				•
Communication						
2	AnalogOutput01	INT			•	
4	AnalogOutput02	INT			•	
6	AnalogOutput03	INT			•	
8	AnalogOutput04	INT			•	

2.8.9.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Configuration							
0	-	ConfigOutput01 (channel type)	UINT				•
Communication							
2	0	AnalogOutput01	INT			•	
4	2	AnalogOutput02	INT			•	
6	4	AnalogOutput03	INT			•	
8	6	AnalogOutput04	INT			•	

1) The offset specifies the position of the register within the CAN object.

2.8.9.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

2.8.9.3.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

2.8.9.4 Analog outputs

The individual channels can be configured for either current or voltage signals. The type of signal is also determined by the terminals used.

2.8.9.4.1 Output values of the analog outputs

Name:
AnalogOutput01 to AnalogOutput04

These registers provide the standardized output values. Once a permitted value is received, the module outputs the respective current or voltage.

Information:

The value "0" disables the channel status LED.

Data type	Value	
INT	-32767 to 32767	Voltage
	0 to 32767	Current

2.8.9.4.2 Setting the channel type

Name:
ConfigOutput01

This register can be used to set the channel type of the outputs.

Each channel is capable of handling either current or voltage signals. The type of signal is determined by the terminal connections used. Since current and voltage require different adjustment values, it is also necessary to configure the desired type of output signal. The following output signals can be set:

- ±10 V voltage signal
- 0 to 20 mA current signal

Data type	Values	Bus controller default setting
UINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0 - 7	Reserved	0	
8	Channel 1	0	Voltage signal (bus controller default setting)
		1	Current signal
...		...	
11	Channel 4	0	Voltage signal (bus controller default setting)
		1	Current signal
12 - 15	Reserved	0	

2.8.9.5 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

2.8.9.6 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time
200 µs

2.9 For reference only

Information:

The data sheets in this section are for reference only when the modules are already in use.

2.9.1 X20AO2632-1

2.9.1.1 General information

The module is equipped with 2 outputs with 16-bit (including sign) digital converter resolution. It is possible to select between the current and voltage signal using different terminals.

This module is designed for X20 6-pin terminal blocks. If needed (e.g. for logistical reasons), the 12-pin terminal block can also be used.

- 2 analog outputs
- Either current or voltage signal possible
- Extended signal range
- 16-bit digital converter resolution
- NetTime timestamp: Switch-off time

NetTime timestamp for output

For many applications, not only the output value is important, but also the exact switching time. The module is equipped with a NetTime timestamp function for this that can define a switching time to the nearest microsecond.

The timestamp function is based on synchronized timers. The CPU can predefine output events and provide them with a timestamp. After transferring the respective data, including the exact time, the module executes the predefined action at the exactly defined time.

2.9.1.2 Order data

Order number	Short description	Figure
	Analog outputs	
X20AO2632-1	X20 analog output module, 2 outputs, ±11 V or 0 to 22 mA, 16-bit converter resolution, NetTime function	
	Required accessories	
	Bus modules	
X20BM11	X20 bus module, 24 VDC keyed, internal I/O power supply connected through	
X20BM15	X20 bus module, with node number switch, 24 VDC keyed, internal I/O power supply connected through	
	Terminal blocks	
X20TB06	X20 terminal block, 6-pin, 24 VDC keyed	
X20TB12	X20 terminal block, 12-pin, 24 VDC keyed	

Table 119: X20AO2632-1 - Order data

2.9.1.3 Technical data

Order number	X20AO2632-1
Short description	
I/O module	2 analog outputs ±11 V or 0 to 22 mA
General information	
B&R ID code	0xC36E
Status indicators	I/O function per channel, operating state, module status
Diagnostics	
Module run/error	Yes, using status LED and software
Channel type	Yes, using software
Power consumption	
Bus	0.01 W
Internal I/O	1.25 W
Additional power dissipation caused by actuators (resistive) [W]	-
Certifications	
CE	Yes
KC	Yes
EAC	Yes
UL	cULus E115267 Industrial control equipment
HazLoc	cCSAus 244665 Process control equipment for hazardous locations Class I, Division 2, Groups ABCD, T5
ATEX	Zone 2, II 3G Ex nA nC IIA T5 Gc IP20, Ta (see X20 user's manual) FTZÚ 09 ATEX 0083X
DNV GL	Temperature: **B** (0 - 55°C) Humidity: **B** (up to 100%) Vibration: **B** (4 g) EMC: **B** (bridge and open deck)
LR	ENV1
Analog outputs	
Output	±11 V or 0 to 22 mA, via different terminal connections
Digital converter resolution	
Voltage	±15-bit
Current	15-bit
Conversion time	50 µs for all outputs
Settling time on output change over entire range	500 µs
Switch on/off behavior	Internal enable relay for booting
Max. error at 25°C	
Voltage	
Gain	0.05% 1)
Offset	0.015% 2)
Current	
Gain	0.08% 1)
Offset	0.05% 2)
Output protection	Short circuit protection
Output format	
Voltage	INT 0x8000 - 0x7FFF / 1 LSB = 0x0001 = 335.693 µV
Current	INT 0x0000 - 0x7FFF / 1 LSB = 0x0001 = 671.386 nA
Load per channel	
Voltage	Max. ±11 mA, load ≥1 kΩ
Current	Max. load is 600 Ω
Short-circuit proof	Current limiting ±40 mA
Output filter	1st-order low pass / cutoff frequency 10 kHz
Max. gain drift	
Voltage	0.008 %/°C 1)
Current	0.011 %/°C 1)
Max. offset drift	
Voltage	0.003 %/°C 2)
Current	0.008 %/°C 2)
Error caused by load change	
Voltage	Max. 0.1%, from 10 MΩ → 1 kΩ, resistive
Current	Max. 0.5%, from 1 Ω → 600 Ω, resistive
Nonlinearity	<0.007% 3)
Insulation voltage between channel and bus	500 V_{eff}
Electrical properties	
Electrical isolation	Channel isolated from bus Channel not isolated from channel

Table 120: X20AO2632-1 - Technical data

Order number	X20AO2632-1
Operating conditions	
Mounting orientation	
Horizontal	Yes
Vertical	Yes
Installation elevation above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
Degree of protection per EN 60529	IP20
Ambient conditions	
Temperature	
Operation	
Horizontal mounting orientation	-25 to 60°C
Vertical mounting orientation	-25 to 50°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Relative humidity	
Operation	5 to 95%, non-condensing
Storage	5 to 95%, non-condensing
Transport	5 to 95%, non-condensing
Mechanical properties	
Note	Order 1x X20TB06 or X20TB12 terminal block separately Order 1x X20BM11 bus module separately
Pitch	12.5$^{+0.2}$ mm

Table 120: X20AO2632-1 - Technical data

1) Based on the current output value.
2) Based on the entire output range.
3) Based on the output range.

2.9.1.4 LED status indicators

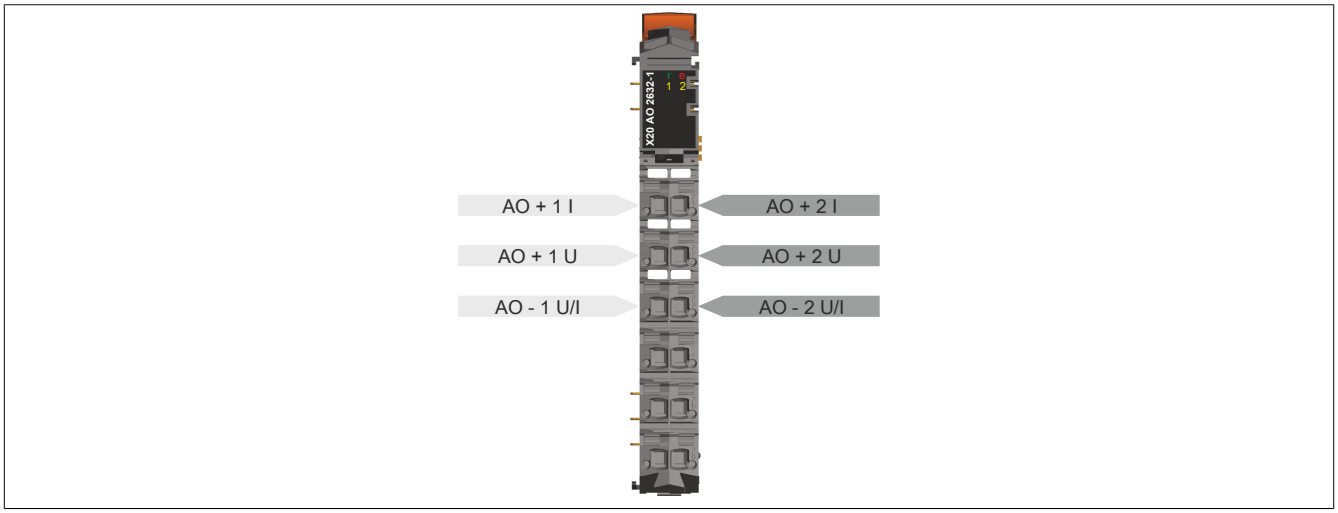
For a description of the various operating modes, see section "Additional information - Diagnostic LEDs" in the X20 system user's manual.

Figure	LED	Color	Status	Description
	r	Green	Off	No power to module
			Single flash	RESET mode
			Double flash	BOOT mode (during firmware update)[1)]
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	e	Red	Off	No power to module or everything OK
			On	Error or reset status
	1 - 2	Orange	Off	Value = 0
			On	Value ≠ 0

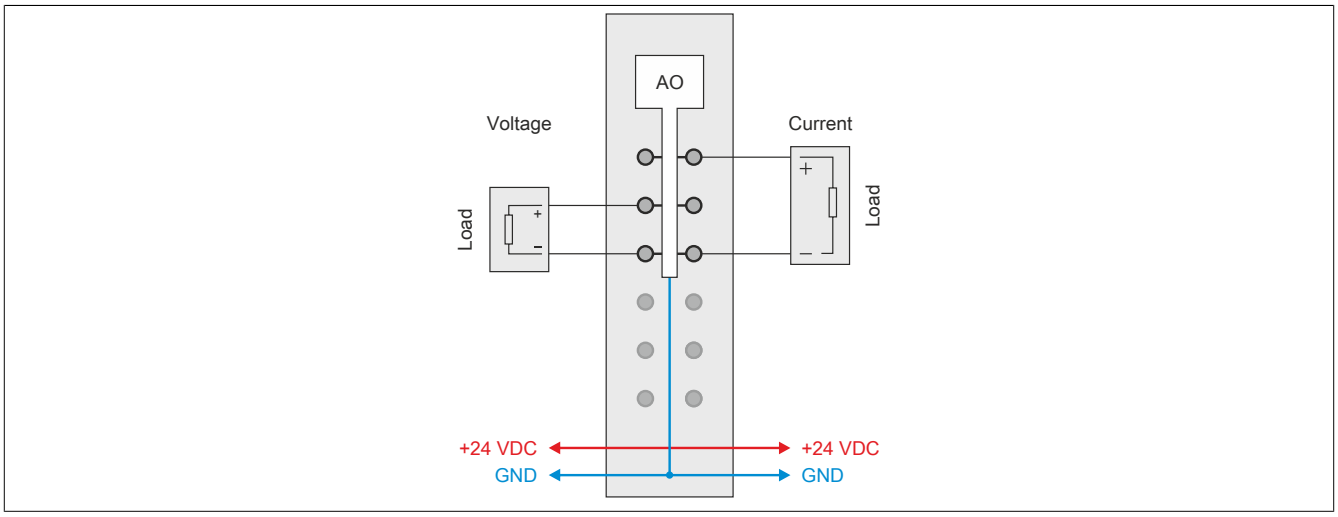
1) Depending on the configuration, a firmware update can take up to several minutes.

2.9.1.5 Pinout

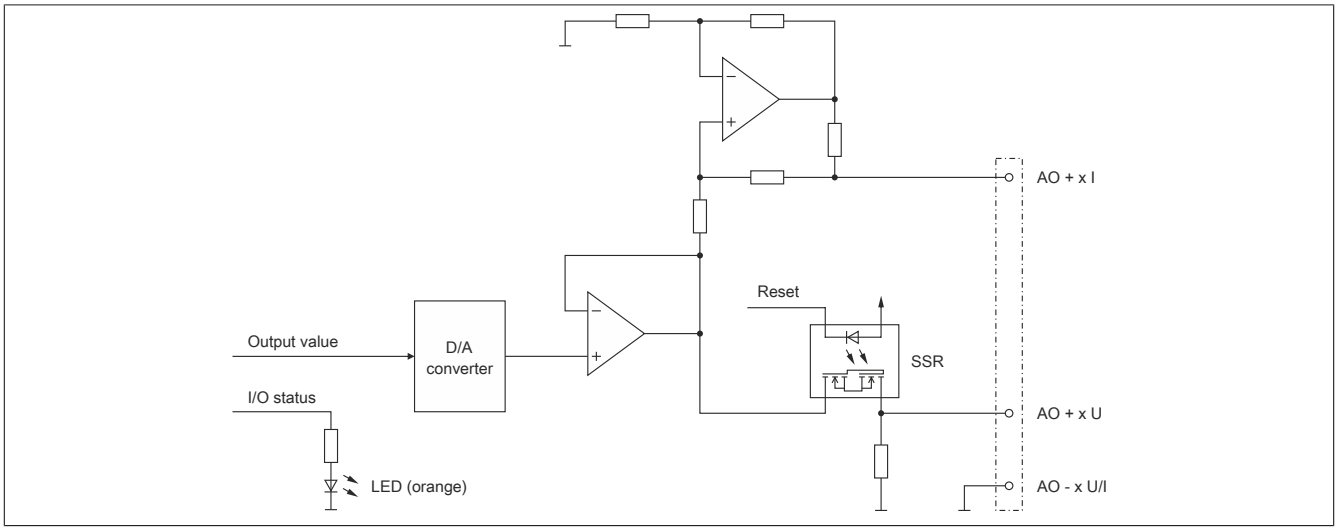
The individual channels can be configured for either current or voltage signals. The type of signal is also determined by the terminals used.



2.9.1.6 Connection example



2.9.1.7 Output circuit diagram



2.9.1.8 Register description

2.9.1.8.1 General data points

In addition to the registers described in the register description, the module has additional general data points. These are not module-specific but contain general information such as serial number and hardware variant.

General data points are described in section "Additional information - General data points" in the X20 system user's manual.

2.9.1.8.2 Function model 0 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog output - Configuration						
0	ConfigOutput01 (channel type)	UINT				•
594 598	Cfo_Channel01TimeMode Cfo_Channel02TimeMode	UINT				•
Analog output - Communication						
2 4	AnalogOutput01 AnalogOutput02	INT			•	
457	SDCLifeCount	SINT	•			
802 810	ValidationTimer01 ValidationTimer02	INT			•	
804 812	ValidationTimer01 ValidationTimer02	DINT			•	
833	Enabling/disabling the output channels	USINT	•		•	
	AnalogOutput01Enable, ~Readback	Bit 0				
	AnalogOutput02Enable, ~Readback	Bit 1				
835	Checking the output values	USINT	•			
	AnalogOutput01OK	Bit 0				
	AnalogOutput02OK	Bit 1				

2.9.1.8.3 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Non-cyclic	Cyclic	Non-cyclic
Analog output - Configuration							
0	-	ConfigOutput01 (channel type)	UINT				•
Analog output - Communication							
2 4	0 2	AnalogOutput01 AnalogOutput02	INT			•	

1) The offset specifies the position of the register within the CAN object.

2.9.1.8.3.1 Using the module on the bus controller

Function model 254 "Bus controller" is used by default only by non-configurable bus controllers. All other bus controllers can use other registers and functions depending on the fieldbus used.

For detailed information, see section "Additional information - Using I/O modules on the bus controller" in the X20 user's manual (version 3.50 or later).

2.9.1.8.3.2 CAN I/O bus controller

The module occupies 1 analog logical slot on CAN I/O.

2.9.1.8.4 General information

The module provides 2 analog outputs. Each channel can output a voltage range of ±11 V or a current range of 0 to 22 mA.

The module also has a time-based watchdog monitor. The user can activate this feature channel-by-channel as needed.

2.9.1.8.5 Analog output - Configuration

Each channel is configured independently. The user can also define an optional time-based monitor. To make this possible, 2 watchdog timers were implemented, which can be assigned to the outputs.

2.9.1.8.5.1 Setting the channel type

Name:
ConfigOutput01

This register can be used to set the channel type of the outputs.

Each channel is capable of handling either current or voltage signals. The type of signal is determined by the terminal connections used. Since current and voltage require different adjustment values, it is also necessary to configure the desired type of output signal. The following output signals can be set:

- ±11 V voltage signal
- 0 to 22 mA current signal

Data type	Values	Bus controller default setting
UINT	See the bit structure.	0

Bit structure:

Bit	Description	Value	Information
0 - 7	Reserved	0	
8	Channel 1	0	Voltage signal (bus controller default setting)
		1	Current signal
9	Channel 2	0	Voltage signal (bus controller default setting)
		1	Current signal
10 - 15	Reserved	0	

2.9.1.8.5.2 Configuring the time-based watchdog monitor

Name:
Cfo_Channel01TimeMode to Cfo_Channel02TimeMode

This register is used to activate or configure the time-based watchdog monitor for the analog output channels.

Possibilities per channel:

- Validation timer data type: General choice 16 or 32 bit
- Validation window: The maximum value can be further limited within the data type.
- Timer allocation: A separate timer is available for each channel. However, all channels can be configured with the same validation timer, whereby the same settings must be made for the data type and window in the TimeMode registers.

Data type	Values
USINT	See the bit structure.

Bit structure:

Bit	Name	Value	Information
0 - 4	Max. validation time	00000	Disabled
		00001	2 µs
		00010	4 µs
		00011	8 µs
		...	...
		11111	2,147,483,648 µs (~35 min)
5 - 7	Reserved	0	
8	Timer allocation	0	ValidationTimer01 (default for channel 1)
		1	ValidationTimer02 (default for channel 2)
9 - 14	Reserved	0	
15	Time format	0	16-bit
		1	32-bit

2.9.1.8.6 Analog output - Communication

In standard mode, the module's outputs are enabled. Based on the configuration and AnalogOutput value, they output the corresponding current or voltage.

If the application requires time-controlled monitoring of the outputs, a validation timer can be assigned to each channel. The validation timer register assigns a validity period to the current output value. If validation is enabled, the module compares the validation time and the NetTime of the X2X Link. If the transmitted validity period is exceeded, the module switches off the channel and resets the output. State "Safety shutdown" is only exited again when a new valid validation time has been transmitted. If enabled, the module reports back which state it is currently in via the error state bit of the channel.

If the value of the validation timer is incremented in each task cycle, the valid validation time will be calculated as follows:

NetTime of the X2X Link master (to which the module is connected)	
+	Timespan for transferring data from the X2X Link master to the CPU (higher-level system)
+	Cycle time of task class (including tolerance)
+	Timespan for transferring the data from the CPU to the module
+	Timespan allowed by the application (e.g. for tolerating failure of an X2X Link cycle)
=	Valid validation time

The AnalogOutputEnableByte is enabled during time-based monitoring. If the timer expires prematurely, the corresponding bit in the AnalogOutputOkayByte is reset and the output drops out. This provides an easy way to achieve a defined state.

2.9.1.8.6.1 Output values of the analog outputs

Name:
AnalogOutput01 to AnalogOutput02

These registers provide the standardized output values. Once a permitted value is received, the module outputs the respective current or voltage.

> **Information:**
>
> **The value "0" disables the channel status LED.**

Data type	Value	
INT	-32767 to 32767	Voltage
	0 to 32767	Current

2.9.1.8.6.2 SDC counter register

Name:
SDCLifeCount

The 8-bit counter register is needed for the SDC software package. It is incremented with the system clock to allow the SDC to check the validity of the data frame.

Data type	Values
SINT	-128 to 127

2.9.1.8.6.3 Transfer of the timestamp

Name:
ValidationTimer01 to ValidationTimer02

When an output is being monitored, these registers must provide the timestamp which, when reached, will cause the output to shut down automatically. The values must be provided as signed 2-byte or 4-byte values.

For additional information about NetTime and timestamps, see "NetTime Technology" on page 782.

Data type	Values [µs]	
INT	-32768 to 32767	NetTime timestamp of the current output value
DINT	-2,147,483,648 to 2,147,483,647	NetTime timestamp of the current output value

2.9.1.8.6.4 Enabling/disabling the output channels

Name:
AnalogOutput01Enable to AnalogOutput02Enable
AnalogOutput01EnableReadback to AnalogOutput02EnableReadback

The "OutputEnable" byte is only needed for the channels with activated time-based monitoring. The individual bits are used to enable/disable the respective channels. To receive reliable feedback about the current state of the module, the byte was also implemented so that it can be read cyclically.

Data type	Value
USINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0	AnalogOutput01Enable AnalogOutput01EnableReadback	0	Output deactivated
		1	Output activated
1	AnalogOutput02Enable AnalogOutput02EnableReadback	0	Output deactivated
		1	Output activated
2 - 7	Reserved	0	

2.9.1.8.6.5 Checking the output values

Name:
AnalogOutput01OK to AnalogOutput02OK

These registers are only needed for channels with activated time-based monitoring. The individual bits report whether the respective channel is actually generating the required voltage or current.

Data type	Value
USINT	See bit structure

Bit structure:

Bit	Name	Value	Information
0	AnalogOutput01OK	0	Electrical signal deactivated
		1	Electrical signal activated
1	AnalogOutput02OK	0	Electrical signal deactivated
		1	Electrical signal activated
2 - 7	Reserved	0	

2.9.1.8.7 NetTime Technology

NetTime refers to the ability to precisely synchronize and transfer system times between individual components of the controller or network (CPU, I/O modules, X2X Link, POWERLINK, etc.).

This allows the moment that events occur to be determined system-wide with microsecond precision. Upcoming events can also be executed precisely at a specified moment.

NetTime TECHNOLOGY

2.9.1.8.7.1 Time information

Various time information is available in the controller or on the network:

- System time (on the PLC, Automation PC, etc.)
- X2X Link time (for each X2X Link network)
- POWERLINK time (for each POWERLINK network)
- Time data points of I/O modules

The NetTime is based on 32-bit counters, which are increased with microsecond resolution. The sign of the time information changes after 35 min, 47 s, 483 ms and 648 µs; an overflow occurs after 71 min, 34 s, 967 ms and 296 µs.

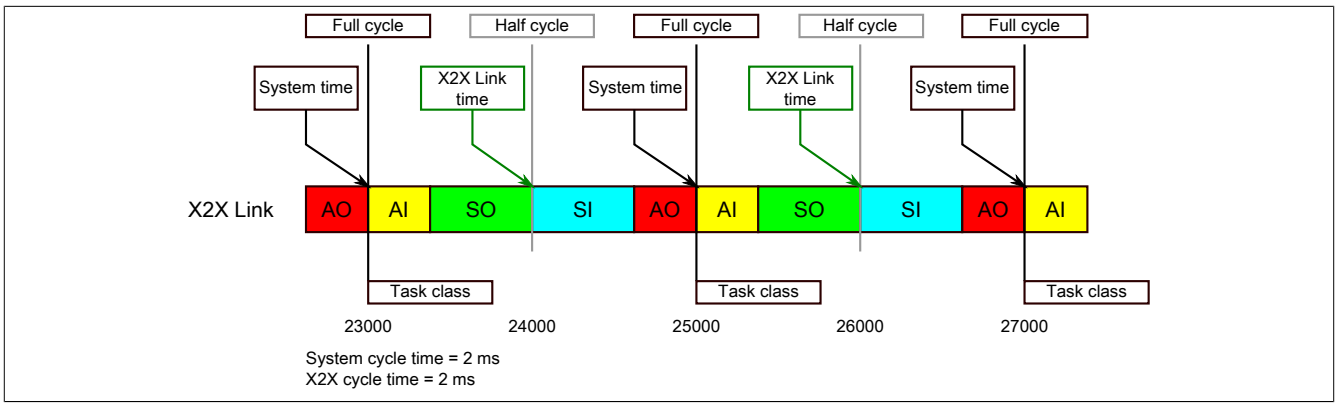
The initialization of the times is based on the system time during the startup of the X2X Link, the I/O modules or the POWERLINK interface.

Current time information in the application can also be determined via library AsIOTime.

PLC/Controller data points

The NetTime I/O data points of the PLC or the controller are latched to each system clock and made available.

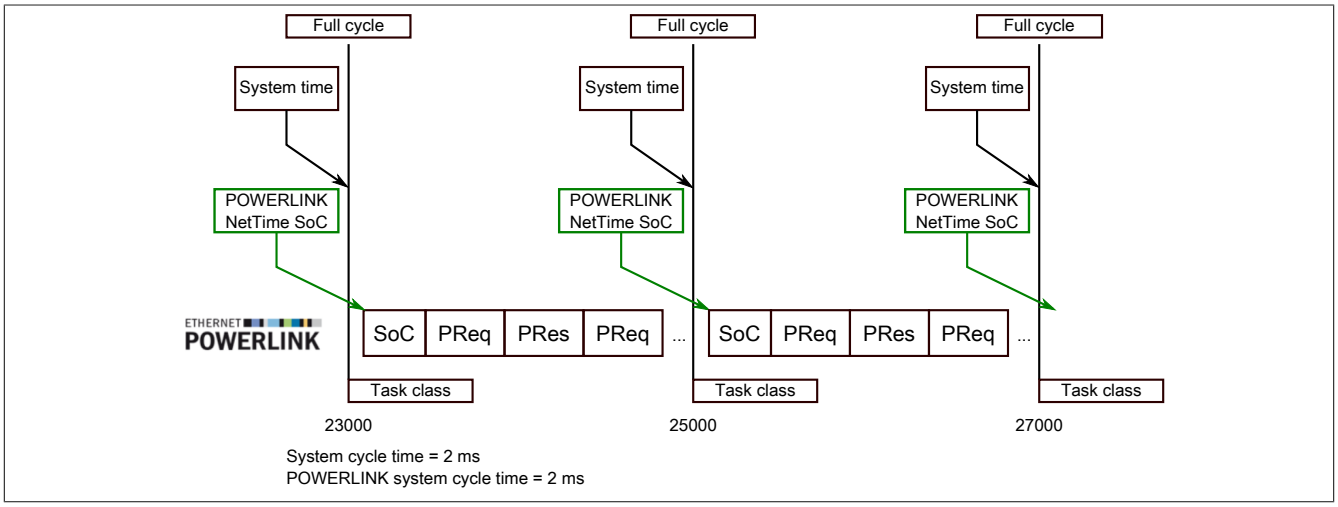
X2X Link reference moment



The reference moment on the X2X Link network is always calculated at the half cycle of the X2X Link cycle. This results in a difference between the system time and the X2X Link reference moment when the reference time is read out.

In the example above, this results in a difference of 1 ms, i.e. if the system time and X2X Link reference moment are compared at time 25000 in the task, then the system time returns the value 25000 and the X2X Link reference moment returns the value 24000.

POWERLINK - Reference time point

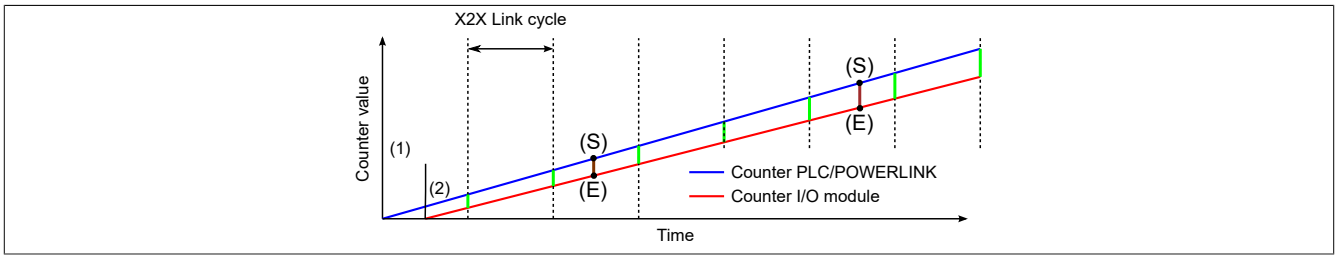


The reference time point on the POWERLINK network is always calculated at the start of cycle (SoC) of the POWERLINK network. The SoC starts 20 µs after the system clock due to the system. This results in the following difference between the system time and the POWERLINK reference time:

POWERLINK reference time = System time - POWERLINK cycle time + 20 µs.

In the example above, this means a difference of 1980 µs, i.e. if the system time and POWERLINK reference time are compared at time 25000 in the task, then the system time returns the value 25000 and the POWERLINK reference time returns the value 23020.

Synchronization of system time/POWERLINK time and I/O module



At startup, the internal counters for the PLC/POWERLINK (1) and the I/O module (2) start at different times and increase the values with microsecond resolution.

At the beginning of each X2X Link cycle, the PLC or the POWERLINK network sends time information to the I/O module. The I/O module compares this time information with the module's internal time and forms a difference (green line) between the two times and stores it.

When a NetTime event (E) occurs, the internal module time is read out and corrected with the stored difference value (brown line). This means that the exact system moment (S) of an event can always be determined, even if the counters are not absolutely synchronous.

Note

The deviation from the clock signal is strongly exaggerated in the picture as a red line.

2.9.1.8.7.2 Timestamp functions

NetTime-capable modules provide various timestamp functions depending on the scope of functions. If a timestamp event occurs, the module immediately saves the current NetTime. After the respective data is transferred to the CPU, including this precise moment, the CPU can then evaluate the data using its own NetTime (or system time), if necessary.

Time-based inputs

NetTime Technology can be used to determine the exact moment of a rising edge at an input. The rising and falling edges can also be detected and the duration between 2 events can be determined.

> **Information:**
>
> **The determined moment always lies in the past.**

Time-based outputs

NetTime Technology can be used to specify the exact moment of a rising edge on an output. The rising and falling edges can also be specified and a pulse pattern generated from them.

> **Information:**
>
> **The specified time must always be in the future, and the set X2X Link cycle time must be taken into account for the definition of the moment.**

Time-based measurements

NetTime Technology can be used to determine the exact moment of a measurement that has taken place. Both the starting and end moment of the measurement can be transmitted.

2.9.1.8.8 Minimum cycle time

The minimum cycle time specifies how far the bus cycle can be reduced without communication errors occurring. It is important to note that very fast cycles reduce the idle time available for handling monitoring, diagnostics and acyclic commands.

Minimum cycle time
200 µs

2.9.1.8.9 Minimum I/O update time

The minimum I/O update time specifies how far the bus cycle can be reduced so that an I/O update is performed in each cycle.

Minimum I/O update time
200 µs