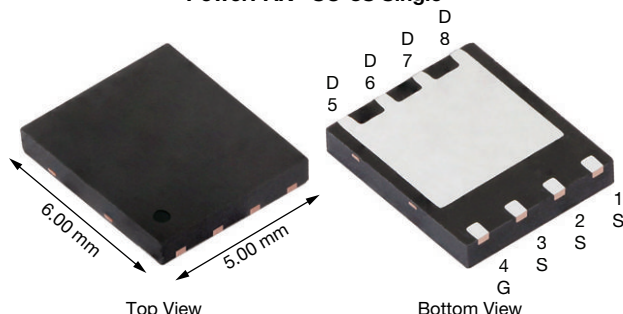


N-Channel 30 V (D-S) MOSFET

PowerPAK® SO-8S Single



FEATURES

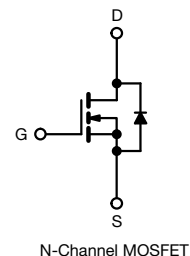
- TrenchFET® Gen IV power MOSFET
- Very low $R_{DS(on)}$ x Q_g figure-of-merit (FOM)
- 100 % R_g and UIS tested
- Enhance power dissipation and lower R_{thJC}
- Leadership $R_{DS(on)}$ minimizes power loss from conduction
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous rectification
- DC/DC converters
- OR-ing and hot swap switch
- Battery management



PRODUCT SUMMARY	
V_{DS} (V)	30
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.00040
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.00068
Q_g typ. (nC)	84
I_D (A) ^a	680
Configuration	Single

ORDERING INFORMATION

Package	PowerPAK SO-8S
Lead (Pb)-free and halogen-free	SiRS4300DP-T1-RE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage	V_{DS}	30	V
Gate-source voltage	V_{GS}	+20, -16	V
Continuous drain current ($T_J = 150$ °C)	$T_C = 25$ °C	680	A
	$T_C = 70$ °C	544	
	$T_A = 25$ °C	117 ^{b, c}	
	$T_A = 70$ °C	94 ^{b, c}	
Pulsed drain current ($t = 100$ μ s)	I_{DM}	800	A
Continuous source-drain diode current	$T_C = 25$ °C	252	A
	$T_A = 25$ °C	7.6 ^{b, c}	
Single pulse avalanche current	I_{AS}	77	mJ
Single pulse avalanche energy	E_{AS}	300	
Maximum power dissipation	$T_C = 25$ °C	278	W
	$T_C = 70$ °C	178	
	$T_A = 25$ °C	8.3 ^{b, c}	
	$T_A = 70$ °C	5.3 ^{b, c}	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^c		260	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^{b, f}	R_{thJA}	10	15	°C/W
Maximum junction-to-case (drain)	R_{thJC}	0.30	0.45	

Notes

- $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 45 °C/W



SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	30	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	I _D = 10 mA	-	18.1	-	mV/°C
V _{GS(th)} temperature coefficient	ΔV _{GS(th)} /T _J	I _D = 250 μA	-	-6.2	-	
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1	-	2.2	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = +20, -16 V	-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V	-	-	1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 55 °C	-	-	10	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A	-	0.00033	0.00040	Ω
		V _{GS} = 4.5 V, I _D = 20 A	-	0.00054	0.00068	
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 40 A	-	185	-	S
Dynamic ^b						
Input capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	-	11 710	-	pF
Output capacitance	C _{oss}		-	5000	-	
Reverse transfer capacitance	C _{rss}		-	305	-	
Total gate charge	Q _g	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 20 A	-	180	270	nC
		V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 20 A	-	84	126	
Gate-source charge	Q _{gs}		-	40	-	
Gate-drain charge	Q _{gd}		-	18	-	
Output charge	Q _{oss}	V _{DS} = 15 V, V _{GS} = 0 V	-	141	-	Ω
Gate resistance	R _g	f = 1 MHz	0.28	1.4	2.8	
Turn-on delay time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω, I _D ≅ 10 A, V _{GEN} = 10 V, R _g = 1 Ω	-	18	35	ns
Rise time	t _r		-	12	25	
Turn-off delay time	t _{d(off)}		-	70	140	
Fall time	t _f		-	16	35	
Turn-on delay time	t _{d(on)}	V _{DD} = 15 V, R _L = 1.5 Ω, I _D ≅ 10 A, V _{GEN} = 4.5 V, R _g = 1 Ω	-	87	175	
Rise time	t _r		-	130	260	
Turn-off delay time	t _{d(off)}		-	65	130	
Fall time	t _f		-	31	60	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	252	A
Pulse diode forward current	I _{SM}		-	-	800	
Body diode voltage	V _{SD}	I _S = 10 A, V _{GS} = 0 V	-	0.70	1.1	V
Body diode reverse recovery time	t _{rr}	I _F = 10 A, di/dt = 100 A/μs, T _J = 25 °C	-	83	165	ns
Body diode reverse recovery charge	Q _{rr}		-	190	380	nC
Reverse recovery fall time	t _a		-	48	-	ns
Reverse recovery rise time	t _b		-	35	-	

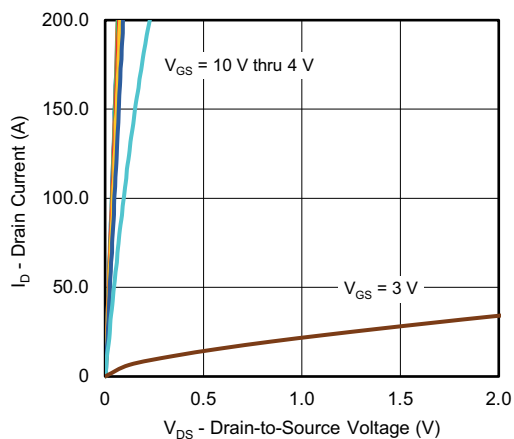
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

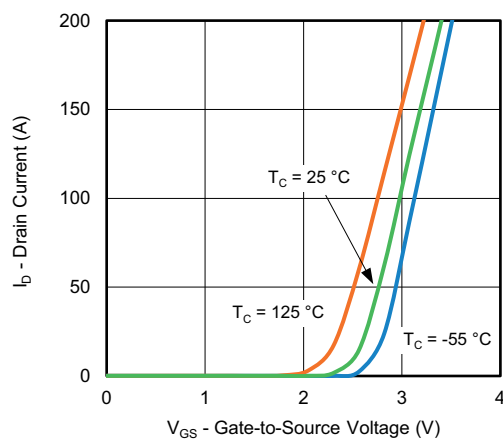
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



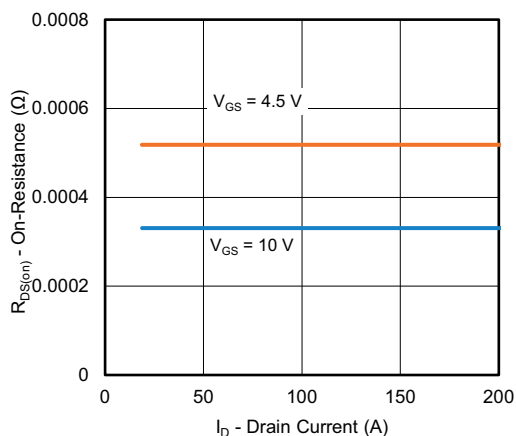
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



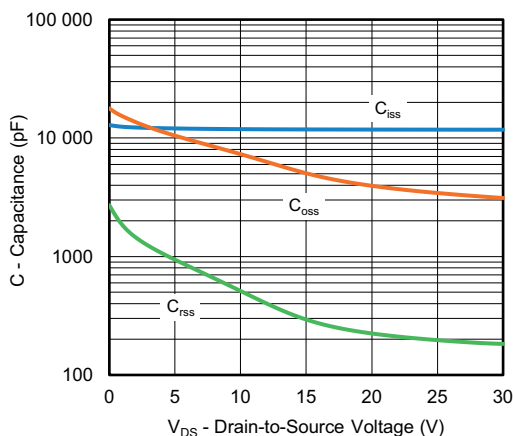
Output Characteristics



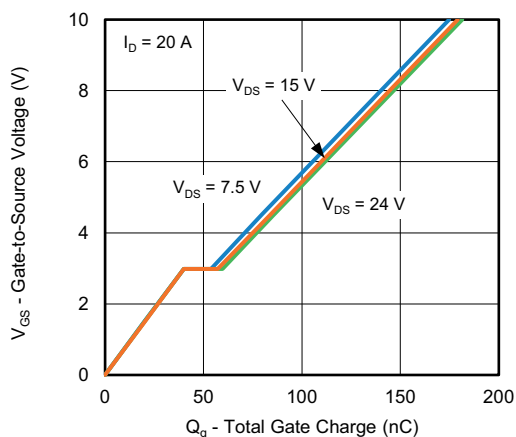
Transfer Characteristics



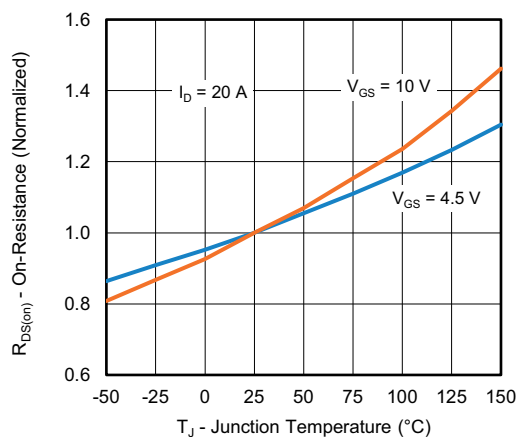
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



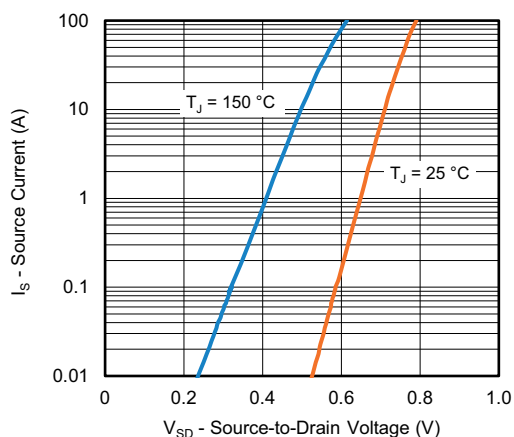
Gate Charge



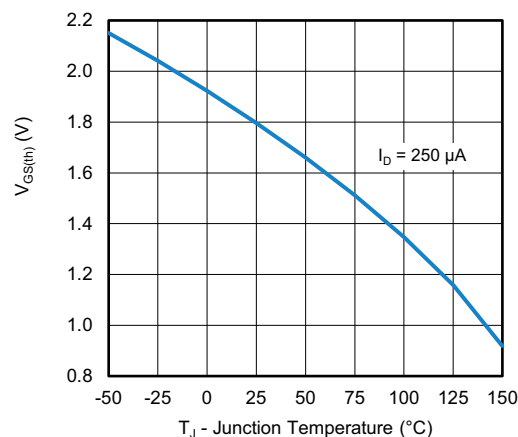
On-Resistance vs. Junction Temperature



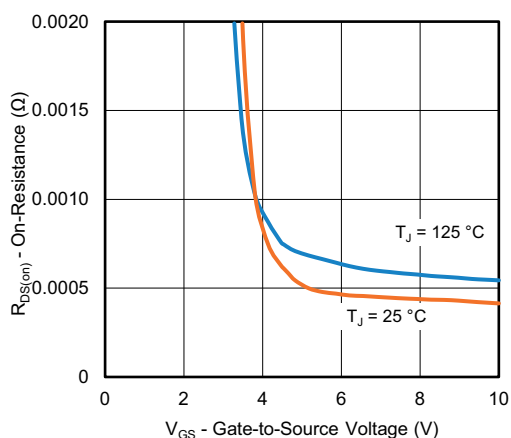
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



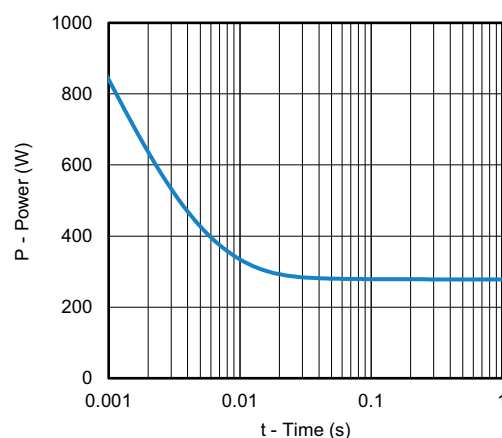
Source-Drain Diode Forward Voltage



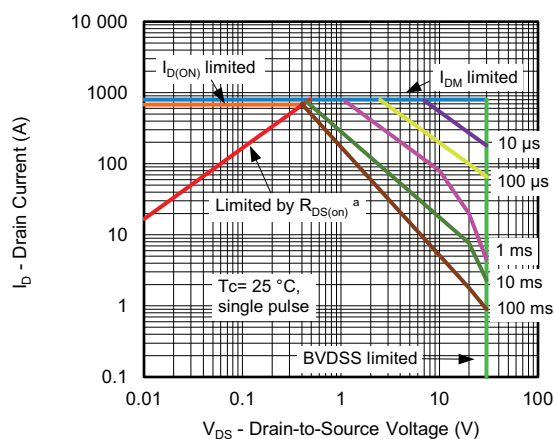
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Case



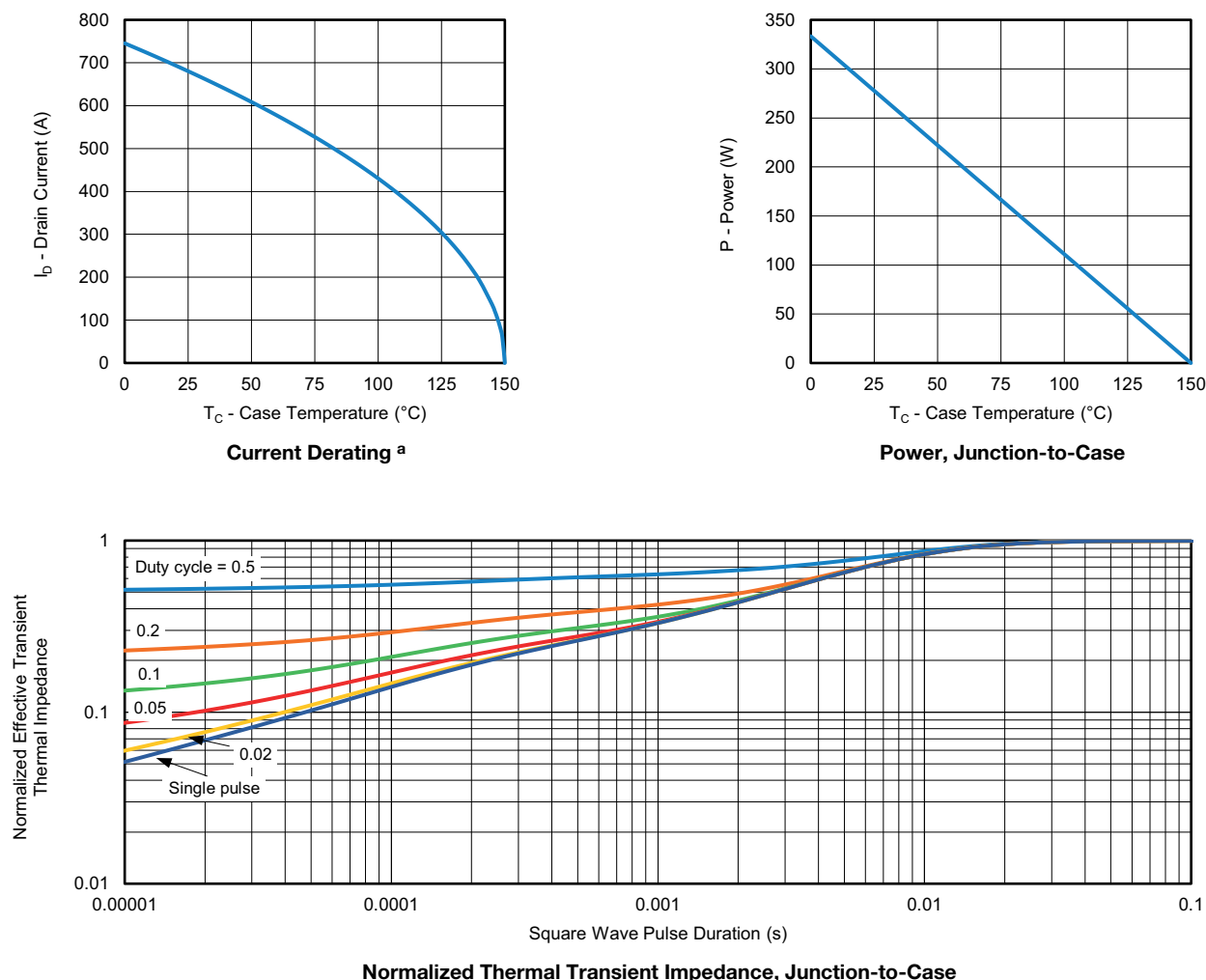
Safe Operating Area, Junction-to-Case

Note

a. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



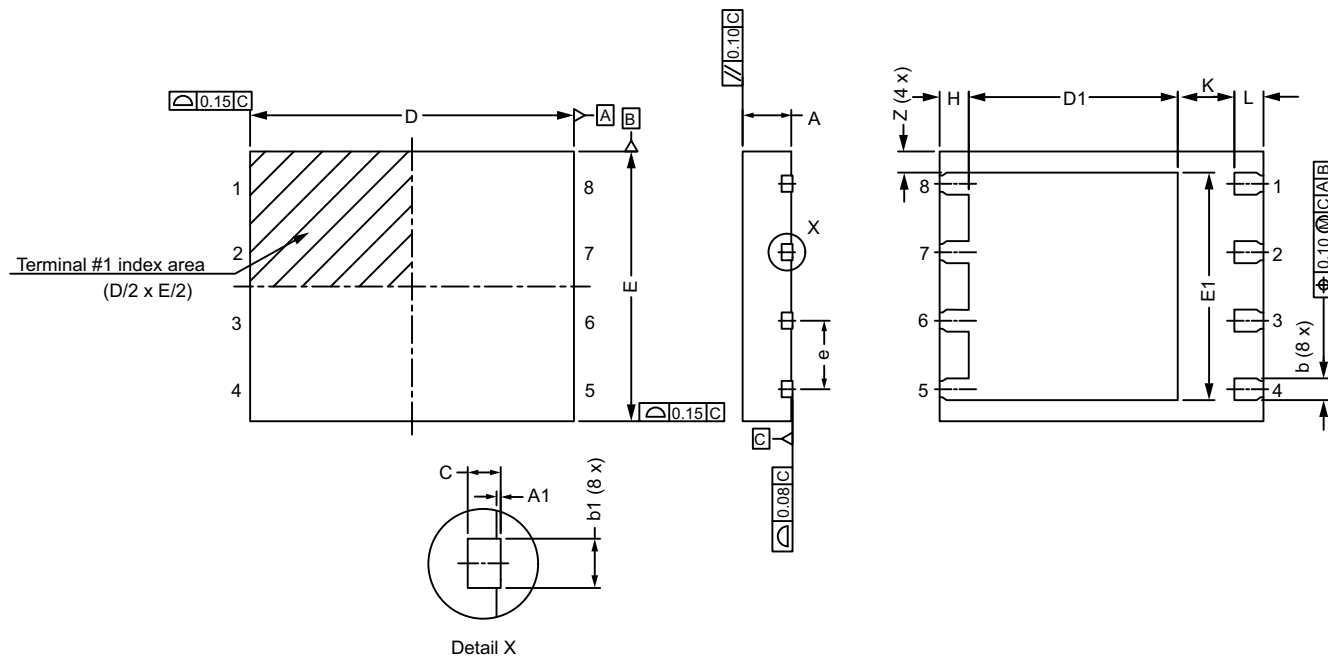
Note

- a. The power dissipation P_D is based on $T_J \text{ max.} = 150^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

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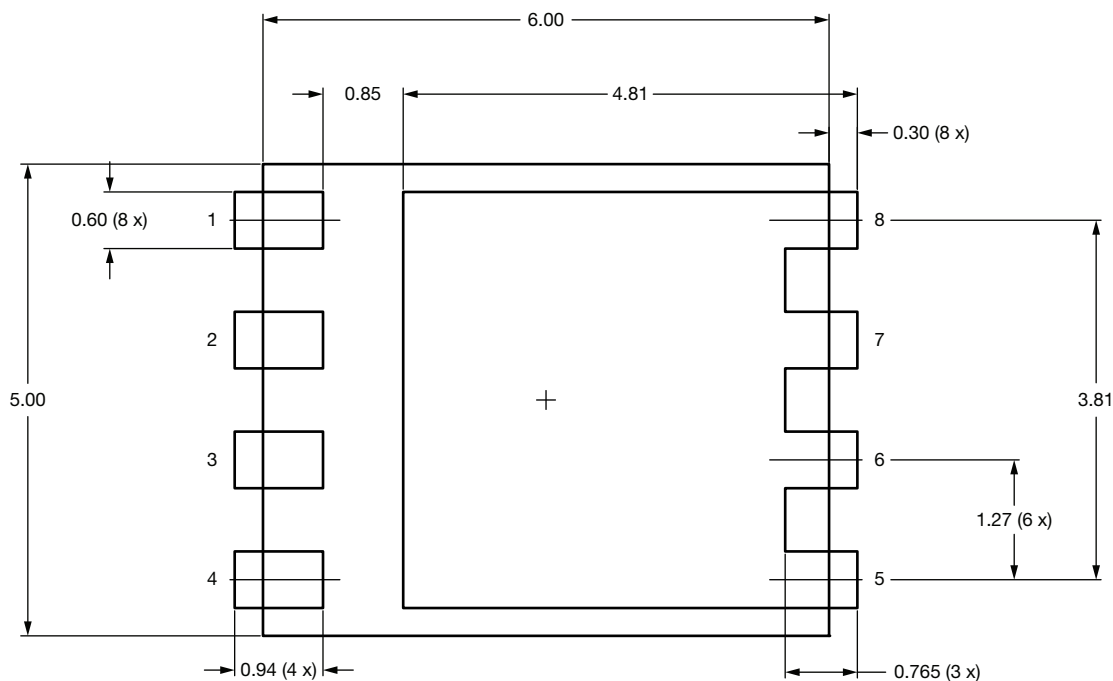
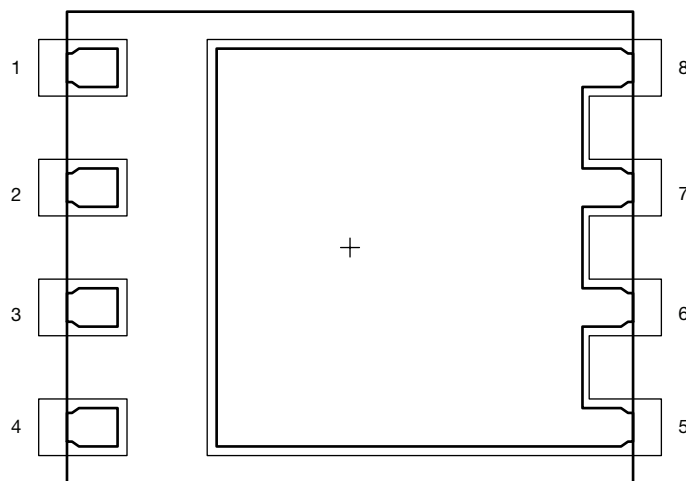


PowerPAK® SO-8S BWL



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.85	0.90	0.95	0.033	0.035	0.037
A1	-	-	0.05	-	-	0.002
b	0.31	0.41	0.51	0.012	0.016	0.020
b1	0.20	0.30	0.40	0.008	0.012	0.016
c	0.20 ref.			0.008 ref.		
D	5.90	6.00	6.10	0.232	0.236	0.240
D1	3.78	3.88	3.98	0.149	0.153	0.157
E	4.90	5.00	5.10	0.193	0.197	0.201
E1	4.12	4.22	4.32	0.162	0.166	0.170
e	1.27 BSC			0.050 BSC		
H	0.44	0.54	0.64	0.017	0.021	0.025
K	1.05 ref.			0.041 ref.		
L	0.44	0.54	0.64	0.017	0.021	0.025
Z	0.39 ref.			0.015 ref.		
ECN: C20-0936-Rev. A, 03-Aug-2020						
DWG: 6082						

Recommended Land Pattern PowerPAK® SO-8S BWL





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