mXT1066TD 1.0.AB

maXTouch 1066-node Touchscreen Controller

maXTouch® Adaptive Sensing Touchscreen Technology

- Up to 41 X (transmit) lines and 26 Y (receive) lines for use by a touchscreen
- A maximum of 1066 nodes can be allocated to the touch sensor
- Touchscreen size of 12.4 inches (16:10 aspect ratio), assuming a sensor electrode pitch of 6.5 mm. Other sizes are possible with different electrode pitches and appropriate sensor material
- Multiple touch support with up to 16 concurrent touches tracked in real time
- Dual-boot OS support for Microsoft® Windows® and Android™

Touch Sensor Technology

- Discrete/out-cell support including glass and PET film-based sensors
- On-cell/touch-on display support including TFT, LCD (ITPS, IPS) and OLED
- Synchronization with display refresh timing capability
- Support for standard (for example, Diamond) and proprietary sensor patterns (review of designs by Microchip or a Microchip-qualified touch sensor module partner is recommended)

Front Panel Material

- Works with PET or glass, including curved profiles (configuration and stack-up to be approved by Microchip or a Microchip-qualified touch sensor module partner)
- 10 mm glass (or 5 mm PMMA) with bare finger (dependent on screen size, touch size, configuration and stack-up)
- 6 mm glass (or 3 mm PMMA) with multi-finger 5 mm glove (2.7 mm PMMA equivalent) (dependent on screen size, touch size, configuration and stack-up)

Touch Performance

- Moisture/Water Compensation
  - No false touch with condensation or water drop up to 22 mm diameter
  - One-finger tracking with condensation or water drop up to 22 mm diameter
- Mutual capacitance and self capacitance measurements supported for robust touch detection
- P2P mutual capacitance measurements supported for extra sensitive multi-touch sensing
- Noise suppression technology to combat ambient, charger, and power-line noise
  - Up to 240 V_{PP} between 1 Hz and 1 kHz sinusoidal waveform
  - Up to 20 V_{PP} between 1 kHz and 1 MHz sinusoidal waveform
- Stylus Support
  - Supports passive stylus with 1.5 mm contact diameter, subject to configuration, stack-up, and sensor design
- Scan Speed
  - Typical report rate for 10 touches ≥85 Hz (subject to configuration)
  - Initial touch latency <20 ms for first touch from idle (subject to configuration)
  - Configurable to allow for power and speed optimization
- Touch panel failure detection
  - Automatic touch sensor diagnostics during run time to support the implementation of safety critical features
  - Diagnostics reported using dedicated output pin or by standard Object Protocol messages
  - Configurable test limits

Enhanced Algorithms

- Lens bending algorithms to remove display noise
- Touch suppression algorithms to remove unintentional large touches, such as palm
- Palm Recovery Algorithm for quick restoration to normal state

Product Data Store Area

- Up to 60 bytes of user-defined data can be stored during production

Power Saving

- Programmable timeout for automatic transition from Active to Idle state
- Pipelined analog sensing detection and digital processing to optimize system power efficiency

Application Interfaces

- I^2C interface with support for Standard mode (up to 100 kHz), Fast mode (up to 400 kHz), Fast-mode Plus (up to 1 MHz), High Speed mode (up to 3.4 MHz)
- HID-I^2C interface for Microsoft Windows 8.x and later versions
- Interrupt to indicate when a message is available
- Additional SPI Debug Interface to read the raw data for tuning and debugging purposes

Power Supply

- Digital (Vdd) 3.3V nominal
- Digital I/O (VddIO) 1.8V nominal to 3.3V nominal
- Analog (AVdd) 3.3V nominal
- High voltage internal X line drive (XVdd) 6.6V or 9.9V with internal voltage pump

Packages

- 114-ball UFBGA 7 × 5 × 0.65 mm, 0.5 mm pitch, High Density Interconnect
- 117-ball UFBGA 9.5 × 7 × 0.65 mm, 0.65 mm pitch, non-HDI package

Operating Temperature

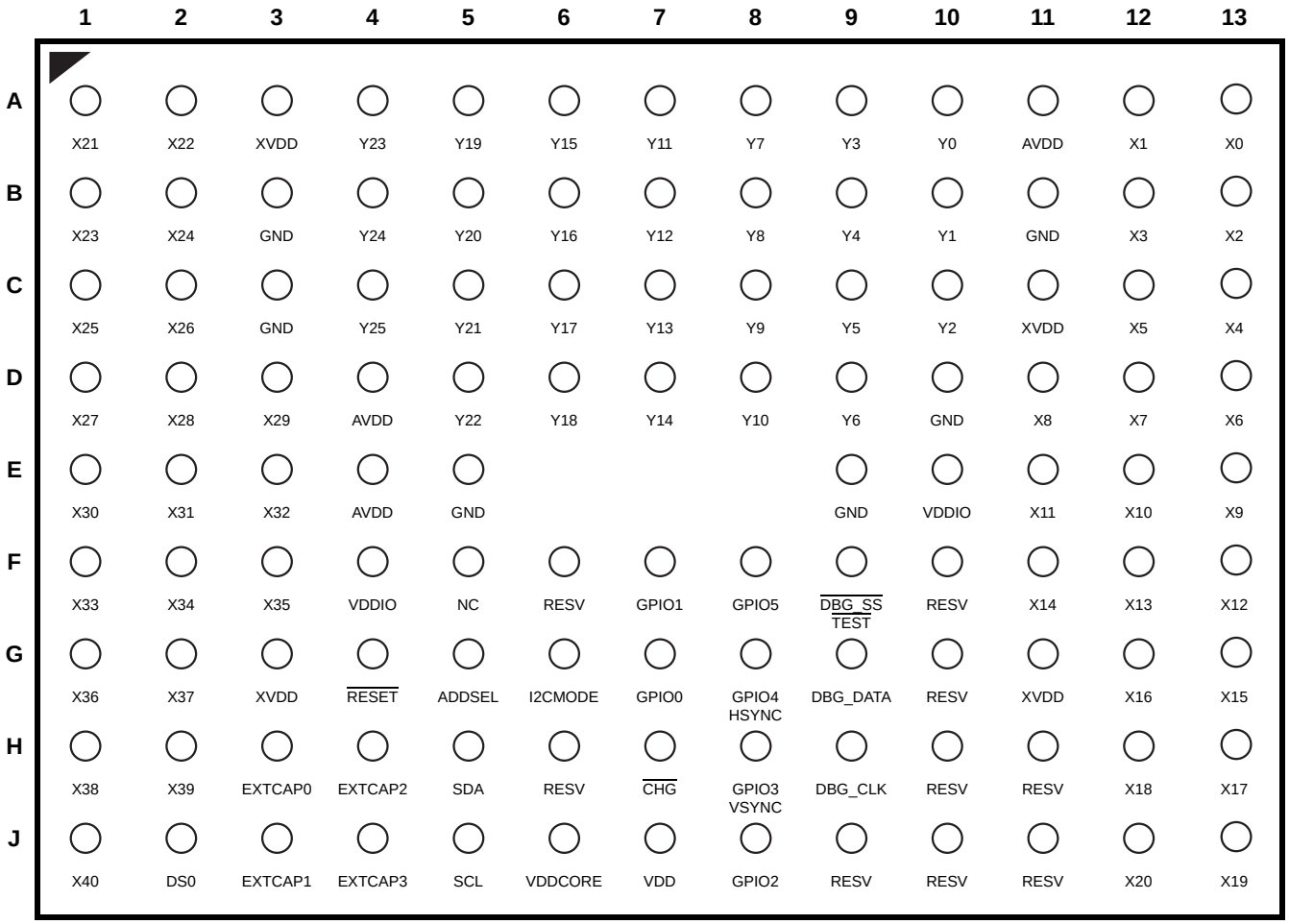
- –40°C to +85°C

Design Services

- Review of device configuration, stack-up and sensor patterns
- Custom firmware versions can be considered
- Contact your Microchip representative for more information

PIN CONFIGURATION

114-ball UFBGA



	1	2	3	4	5	6	7	8	9	10	11	12	13
A	X21	X22	XVDD	Y23	Y19	Y15	Y11	Y7	Y3	Y0	AVDD	X1	X0
B	X23	X24	GND	Y24	Y20	Y16	Y12	Y8	Y4	Y1	GND	X3	X2
C	X25	X26	GND	Y25	Y21	Y17	Y13	Y9	Y5	Y2	XVDD	X5	X4
D	X27	X28	X29	AVDD	Y22	Y18	Y14	Y10	Y6	GND	X8	X7	X6
E	X30	X31	X32	AVDD	GND				GND	VDDIO	X11	X10	X9
F	X33	X34	X35	VDDIO	NC	RESV	GPIO1	GPIO5	$\overline{\text{DBG\_SS}}$ $\overline{\text{TEST}}$	RESV	X14	X13	X12
G	X36	X37	XVDD	$\overline{\text{RESET}}$	ADDSEL	I2CMODE	GPIO0	GPIO4 HSYNC	DBG_DATA	RESV	XVDD	X16	X15
H	X38	X39	EXTCAP0	EXTCAP2	SDA	RESV	$\overline{\text{CHG}}$	GPIO3 VSYNC	DBG_CLK	RESV	RESV	X18	X17
J	X40	DS0	EXTCAP1	EXTCAP3	SCL	VDDCORE	VDD	GPIO2	RESV	RESV	RESV	X20	X19

Top View

TABLE 0-1: PIN LISTING – 114-BALL UFBGA

Ball	Name	Type	Supply	Description	If Unused...
A1	X21	S	XVdd	X line connection	Leave open
A2	X22	S	XVdd	X line connection	Leave open
A3	XVDD	P	–	X line drive power (internally generated). WARNING: The device may be permanently damaged if this pin is shorted to ground or high current is drawn from it.	–
A4	Y23	S	AVdd	Y line connection	Leave open
A5	Y19	S	AVdd	Y line connection	Leave open
A6	Y15	S	AVdd	Y line connection	Leave open
A7	Y11	S	AVdd	Y line connection	Leave open
A8	Y7	S	AVdd	Y line connection	Leave open
A9	Y3	S	AVdd	Y line connection	Leave open
A10	Y0	S	AVdd	Y line connection	Leave open
A11	AVDD	P	–	Analog power	–
A12	X1	S	XVdd	X line connection	Leave open
A13	X0	S	XVdd	X line connection	Leave open
B1	X23	S	XVdd	X line connection	Leave open
B2	X24	S	XVdd	Y line connection	Leave open
B3	GND	P	–	Ground	–
B4	Y24	S	AVdd	Y line connection	Leave open
B5	Y20	S	AVdd	Y line connection	Leave open
B6	Y16	S	AVdd	Y line connection	Leave open
B7	Y12	S	AVdd	Y line connection	Leave open
B8	Y8	S	AVdd	Y line connection	Leave open
B9	Y4	S	AVdd	Y line connection	Leave open
B10	Y1	S	AVdd	Y line connection	Leave open
B11	GND	P	–	Ground	–
B12	X3	S	XVdd	X line connection	Leave open
B13	X2	S	XVdd	X line connection	Leave open
C1	X25	S	XVdd	X line connection	Leave open
C2	X26	S	XVdd	X line connection	Leave open
C3	GND	P	–	Ground	–
C4	Y25	S	AVdd	Y line connection	Leave open
C5	Y21	S	AVdd	Y line connection	Leave open
C6	Y17	S	AVdd	Y line connection	Leave open
C7	Y13	S	AVdd	Y line connection	Leave open
C8	Y9	S	AVdd	Y line connection	Leave open
C9	Y5	S	AVdd	Y line connection	Leave open
C10	Y2	S	AVdd	Y line connection	Leave open
C11	XVDD	P	–	X line drive power (internally generated). WARNING: The device may be permanently damaged if this pin is shorted to ground or high current is drawn from it.	–

TABLE 0-1: PIN LISTING – 114-BALL UFBGA (CONTINUED)

Ball	Name	Type	Supply	Description	If Unused...
C12	X5	S	XVdd	X line connection	Leave open
C13	X4	S	XVdd	X line connection	Leave open
D1	X27	S	XVdd	X line connection	Leave open
D2	X28	S	XVdd	X line connection	Leave open
D3	X29	S	XVdd	X line connection	Leave open
D4	AVDD	P	–	Analog power	–
D5	Y22	S	AVdd	Y line connection	Leave open
D6	Y18	S	AVdd	Y line connection	Leave open
D7	Y14	S	AVdd	Y line connection	Leave open
D8	Y10	S	AVdd	Y line connection	Leave open
D9	Y6	S	AVdd	Y line connection	Leave open
D10	GND	P	–	Ground	–
D11	X8	S	XVdd	X line connection	Leave open
D12	X7	S	XVdd	X line connection	Leave open
D13	X6	S	XVdd	X line connection	Leave open
E1	X30	S	XVdd	X line connection	Leave open
E2	X31	S	XVdd	X line connection	Leave open
E3	X32	S	XVdd	X line connection	Leave open
E4	AVDD	P	–	Analog power	–
E5	GND	P	–	Ground	–
E9	GND	P	–	Ground	–
E10	VDDIO	P	–	Digital power	–
E11	X11	S	XVdd	X line connection	Leave open
E12	X10	S	XVdd	X line connection	Leave open
E13	X9	S	XVdd	X line connection	Leave open
F1	X33	S	XVdd	X line connection	Leave open
F2	X34	S	XVdd	X line connection	Leave open
F3	X35	S	XVdd	X line connection	Leave open
F4	VDDIO	P	–	Digital power	–
F5	NC	–	–	–	–
F6	RESV	–	–	Reserved; do not connect	Leave open
F7	GPIO1	I/O	VddIO	General purpose IO; see Section 2.3.9 “GPIO Pins”	Connect to GND
F8	GPIO5	I/O	VddIO	General purpose IO; see Section 2.3.9 “GPIO Pins”	Connect to GND
F9	$\overline{\text{DBG\_SS}}$	O	VddIO	Primary Debug SS line. Pull up to VddIO; see Section 2.3.10 “SPI Debug Interface”	Connect to test point Pull up to VddIO
	$\overline{\text{TEST}}$	–		Reserved for factory use; pull up to VddIO	
F10	RESV	–	–	Reserved; do not connect	Leave open
F11	X14	S	XVdd	X line connection	Leave open
F12	X13	S	XVdd	X line connection	Leave open
F13	X12	S	XVdd	X line connection	Leave open
G1	X36	S	XVdd	X line connection	Leave open

TABLE 0-1: PIN LISTING – 114-BALL UFBGA (CONTINUED)

Ball	Name	Type	Supply	Description	If Unused...
G2	X37	S	XVdd	X line connection	Leave open
G3	XVDD	P	–	X line drive power (internally generated). WARNING: The device may be permanently damaged if this pin is shorted to ground or high current is drawn from it.	–
G4	$\overline{\text{RESET}}$	I	VddIO	Reset low. Connection to host system is recommended	Pull up to VddIO
G5	ADDSEL	I	VddIO	I^2C address select; see Section 7.2 "I^2C Address Selection – ADDSEL Pin"	–
G6	I2CMODE	I	VddIO	Selects I^2C mode; see Section 7.1 "I^2C Mode Selection – I2CMODE Pin"	–
G7	GPIO0	I/O	VddIO	General purpose IO; see Section 2.3.9 "GPIO Pins"	Connect to GND
G8	GPIO4	I/O	VddIO	General purpose IO; see Section 2.3.9 "GPIO Pins"	Input: connect to GND Output: leave open
	HSYNC	I		External pulse synchronization	
G9	DBG_DATA	O	VddIO	Debug data; see Section 2.3.10 "SPI Debug Interface"	Leave open
G10	RESV	–	–	Reserved; do not connect	Leave open
G11	XVDD	P	–	X line drive power (internally generated). WARNING: The device may be permanently damaged if this pin is shorted to ground or high current is drawn from it.	–
G12	X16	S	XVdd	X line connection	Leave open
G13	X15	S	XVdd	X line connection	Leave open
H1	X38	S	XVdd	X line connection	Leave open
H2	X39	S	XVdd	X line connection	Leave open
H3	EXTCAP0	P	–	Connect to EXTCAP1 via capacitor; see Section 2.3.5 "XVdd"	Leave open
H4	EXTCAP2	P	–	Connect to EXTCAP3 via capacitor; see Section 2.3.5 "XVdd"	Leave open
H5	SDA	OD	VddIO	Serial interface data	Leave open
H6	RESV	–	VddIO	Reserved for factory use	Connect to GND
H7	$\overline{\text{CHG}}$	OD	VddIO	State change interrupt Note: Briefly set (~100 ms) as an input after power-up/reset for diagnostic purposes	Pull up to VddIO
H8	GPIO3	I/O	VddIO	General purpose IO; see Section 2.3.9 "GPIO Pins"	Input: connect to GND Output: leave open
	VSYNC	I		External frame synchronization	
H9	DBG_CLK	O	VddIO	Debug clock; see Section 2.3.10 "SPI Debug Interface"	Leave open
H10	RESV	–	–	Reserved; do not connect	Leave open
H11	RESV	–	–	Reserved; do not connect	Leave open
H12	X18	S	XVdd	X line connection	Leave open
H13	X17	S	XVdd	X line connection	Leave open
J1	X40	S	XVdd	X line connection	Leave open
J2	DS0	O	AVdd	Driven Shield signal; used as guard track between X/Y signals and ground	Leave open
J3	EXTCAP1	P	–	Connect to EXTCAP0 via capacitor; see Section 2.3.5 "XVdd"	Leave open

TABLE 0-1: PIN LISTING – 114-BALL UFBGA (CONTINUED)

Ball	Name	Type	Supply	Description	If Unused...
J4	EXTCAP3	P	–	Connect to EXTCAP2 via capacitor; see Section 2.3.5 “XVdd”	Leave open
J5	SCL	OD	VddIO	Serial clock input	Leave open
J6	VDDCORE	P	–	Digital core power	–
J7	VDD	P	–	Digital power	–
J8	GPIO2	I/O	VddIO	General purpose IO; see Section 2.3.9 “GPIO Pins”	Connect to GND
J9	RESV	–	–	Reserved; do not connect	Leave open
J10	RESV	–	–	Reserved; do not connect	Leave open
J11	RESV	–	–	Reserved; do not connect	Leave open
J12	X20	S	XVdd	X line connection	Leave open
J13	X19	S	XVdd	X line connection	Leave open

Key:

I	Input only	O	Output only	I/O	Input or output
OD	Open drain output	P	Ground or power	S	Sense pin

117-ball UFBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	X21	X22	XVDD	Y23	Y19	Y15	Y11	Y7	Y3	Y0	AVDD	X1	X0
B	X23	X24	GND	Y24	Y20	Y16	Y12	Y8	Y4	Y1	GND	X3	X2
C	X25	X26	GND	Y25	Y21	Y17	Y13	Y9	Y5	Y2	XVDD	X5	X4
D	X27	X28	X29	AVDD	Y22	Y18	Y14	Y10	Y6	GND	X8	X7	X6
E	X30	X31	X32	AVDD	GND	VDDCORE	VDD	GND	VDDIO	XVDD	X11	X10	X9
F	X33	X34	X35	VDDIO	NC	$\overline{\text{CHG}}$	GPIO3 VSYNC	DBG_DATA	$\overline{\text{DBG\_SS}}$ $\overline{\text{TEST}}$	RESV	X14	X13	X12
G	X36	X37	XVDD	$\overline{\text{RESET}}$	ADDSEL	RESV	GPIO2	DBG_CLK	RESV	RESV	RESV	X16	X15
H	X38	X39	EXTCAP0	EXTCAP2	SDA	I2CMODE	GPIO1	GPIO5	RESV	RESV	RESV	X18	X17
J	X40	DS0	EXTCAP1	EXTCAP3	SCL	RESV	GPIO0	GPIO4 HSYNC	RESV	RESV	RESV	X20	X19

Top View

TABLE 0-2: PIN LISTING – 117-BALL UFBGA

Ball	Name	Type	Supply	Description	If Unused...
A1	X21	S	XVdd	X line connection	Leave open
A2	X22	S	XVdd	X line connection	Leave open
A3	XVDD	P	–	X line drive power (internally generated). WARNING: The device may be permanently damaged if this pin is shorted to ground or high current is drawn from it.	–
A4	Y23	S	AVdd	Y line connection	Leave open
A5	Y19	S	AVdd	Y line connection	Leave open
A6	Y15	S	AVdd	Y line connection	Leave open
A7	Y11	S	AVdd	Y line connection	Leave open
A8	Y7	S	AVdd	Y line connection	Leave open
A9	Y3	S	AVdd	Y line connection	Leave open
A10	Y0	S	AVdd	Y line connection	Leave open
A11	AVDD	P	–	Analog power	–
A12	X1	S	XVdd	X line connection	Leave open
A13	X0	S	XVdd	X line connection	Leave open
B1	X23	S	XVdd	X line connection	Leave open
B2	X24	S	XVdd	Y line connection	Leave open
B3	GND	P	–	Ground	–
B4	Y24	S	AVdd	Y line connection	Leave open
B5	Y20	S	AVdd	Y line connection	Leave open
B6	Y16	S	AVdd	Y line connection	Leave open
B7	Y12	S	AVdd	Y line connection	Leave open
B8	Y8	S	AVdd	Y line connection	Leave open
B9	Y4	S	AVdd	Y line connection	Leave open
B10	Y1	S	AVdd	Y line connection	Leave open
B11	GND	P	–	Ground	–
B12	X3	S	XVdd	X line connection	Leave open
B13	X2	S	XVdd	X line connection	Leave open
C1	X25	S	XVdd	X line connection	Leave open
C2	X26	S	XVdd	X line connection	Leave open
C3	GND	P	–	Ground	–
C4	Y25	S	AVdd	Y line connection	Leave open
C5	Y21	S	AVdd	Y line connection	Leave open
C6	Y17	S	AVdd	Y line connection	Leave open
C7	Y13	S	AVdd	Y line connection	Leave open
C8	Y9	S	AVdd	Y line connection	Leave open
C9	Y5	S	AVdd	Y line connection	Leave open
C10	Y2	S	AVdd	Y line connection	Leave open
C11	XVDD	P	–	X line drive power (internally generated). WARNING: The device may be permanently damaged if this pin is shorted to ground or high current is drawn from it.	–

TABLE 0-2: PIN LISTING – 117-BALL UFBGA (CONTINUED)

Ball	Name	Type	Supply	Description	If Unused...
C12	X5	S	XVdd	X line connection	Leave open
C13	X4	S	XVdd	X line connection	Leave open
D1	X27	S	XVdd	X line connection	Leave open
D2	X28	S	XVdd	X line connection	Leave open
D3	X29	S	XVdd	X line connection	Leave open
D4	AVDD	P	–	Analog power	–
D5	Y22	S	AVdd	Y line connection	Leave open
D6	Y18	S	AVdd	Y line connection	Leave open
D7	Y14	S	AVdd	Y line connection	Leave open
D8	Y10	S	AVdd	Y line connection	Leave open
D9	Y6	S	AVdd	Y line connection	Leave open
D10	GND	P	–	Ground	–
D11	X8	S	XVdd	X line connection	Leave open
D12	X7	S	XVdd	X line connection	Leave open
D13	X6	S	XVdd	X line connection	Leave open
E1	X30	S	XVdd	X line connection	Leave open
E2	X31	S	XVdd	X line connection	Leave open
E3	X32	S	XVdd	X line connection	Leave open
E4	AVDD	P	–	Analog power	–
E5	GND	P	–	Ground	–
E6	VDDCORE	P	–	Digital core power	–
E7	VDD	P	–	Digital power	–
E8	GND	P	–	Ground	–
E9	VDDIO	P	–	Digital power	–
E10	XVDD	P	–	X line drive power (internally generated). WARNING: The device may be permanently damaged if this pin is shorted to ground or high current is drawn from it.	–
E11	X11	S	XVdd	X line connection	Leave open
E12	X10	S	XVdd	X line connection	Leave open
E13	X9	S	XVdd	X line connection	Leave open
F1	X33	S	XVdd	X line connection	Leave open
F2	X34	S	XVdd	X line connection	Leave open
F3	X35	S	XVdd	X line connection	Leave open
F4	VDDIO	P	–	Digital power	–
F5	NC	–	–	No connection	–
F6	$\overline{\text{CHG}}$	OD	VddIO	Change line interrupt	Pull up to VddIO
F7	GPIO3	I/O	VddIO	General purpose IO; see Section 2.3.9 “GPIO Pins”	Input: connect to GND Output: leave open
	VSYNC	I		External frame synchronization	
F8	DBG_DATA	O	VddIO	Debug data; see Section 2.3.10 “SPI Debug Interface”	Leave open
F9	$\overline{\text{DBG\_SS}}$	O	VddIO	Primary Debug SS line. Pull up to VddIO; see Section 2.3.10 “SPI Debug Interface”	Connect to test point Pull up to VddIO
	$\overline{\text{TEST}}$	–		Reserved for factory use; pull up to VddIO	

TABLE 0-2: PIN LISTING – 117-BALL UFBGA (CONTINUED)

Ball	Name	Type	Supply	Description	If Unused...
F10	RESV	–	–	Reserved; do not connect	Leave open
F11	X14	S	XVdd	X line connection	Leave open
F12	X13	S	XVdd	X line connection	Leave open
F13	X12	S	XVdd	X line connection	Leave open
G1	X36	S	XVdd	X line connection	Leave open
G2	X37	S	XVdd	X line connection	Leave open
G3	XVDD	P	–	X line drive power (internally generated). WARNING: The device may be permanently damaged if this pin is shorted to ground or high current is drawn from it.	–
G4	$\overline{\text{RESET}}$	I	VddIO	Reset low. Connection to host system is recommended	Pull up to VddIO
G5	ADDSEL	I	VddIO	I^2C address select; see Section 7.2 “I^2C Address Selection – ADDSEL Pin”	–
G6	RESV	–	–	Reserved; do not connect	Leave open
G7	GPIO2	I/O	VddIO	General purpose IO; see Section 2.3.9 “GPIO Pins”	Connect to GND
G8	DBG_CLK	O	VddIO	Debug clock; see Section 2.3.10 “SPI Debug Interface”	Leave open
G9	RESV	–	–	Reserved; do not connect	Leave open
G10	RESV	–	–	Reserved; do not connect	Leave open
G11	RESV	–	–	Reserved; do not connect	Leave open
G12	X16	S	XVdd	X line connection	Leave open
G13	X15	S	XVdd	X line connection	Leave open
H1	X38	S	XVdd	X line connection	Leave open
H2	X39	S	XVdd	X line connection	Leave open
H3	EXTCAP0	P	–	Connect to EXTCAP1 via capacitor; see Section 2.3.5 “XVdd”	Leave open
H4	EXTCAP2	P	–	Connect to EXTCAP3 via capacitor; see Section 2.3.5 “XVdd”	Leave open
H5	SDA	OD	VddIO	Serial interface data	Leave open
H6	I2CMODE	I	VddIO	Selects I^2C mode; see Section 7.1 “I^2C Mode Selection – I2CMODE Pin”	–
H7	GPIO1	I/O	VddIO	General purpose IO; see Section 2.3.9 “GPIO Pins”	Connect to GND
H8	GPIO5	I/O	VddIO	General purpose IO; see Section 2.3.9 “GPIO Pins”	Connect to GND
H9	RESV	–	–	Reserved; do not connect	Leave open
H10	RESV	–	–	Reserved; do not connect	Leave open
H11	RESV	–	–	Reserved; do not connect	Leave open
H12	X18	S	XVdd	X line connection	Leave open
H13	X17	S	XVdd	X line connection	Leave open
J1	X40	S	XVdd	X line connection	Leave open
J2	DS0	O	AVdd	Driven Shield signal; used as guard track between X/Y signals and ground	Leave open
J3	EXTCAP1	P	–	Connect to EXTCAP0 via capacitor; see Section 2.3.5 “XVdd”	Leave open
J4	EXTCAP3	P	–	Connect to EXTCAP2 via capacitor; see Section 2.3.5 “XVdd”	Leave open

TABLE 0-2: PIN LISTING – 117-BALL UFBGA (CONTINUED)

Ball	Name	Type	Supply	Description	If Unused...
J5	SCL	OD	VddIO	Serial clock input	Leave open
J6	RESV	–	VddIO	Reserved for factory use	Connect to GND
J7	GPIO0	I/O	VddIO	General purpose IO; see Section 2.3.9 “GPIO Pins”	Connect to GND
J8	GPIO4	I/O	VddIO	General purpose IO; see Section 2.3.9 “GPIO Pins”	Input: connect to GND Output: leave open
	HSYNC	I		External pulse synchronization	
J9	RESV	–	–	Reserved; do not connect	Leave open
J10	RESV	–	–	Reserved; do not connect	Leave open
J11	RESV	–	–	Reserved; do not connect	Leave open
J12	X20	S	XVdd	X line connection	Leave open
J13	X19	S	XVdd	X line connection	Leave open

Key:

I	Input only	O	Output only	I/O	Input or output
OD	Open drain output	P	Ground or power	S	Sense pin

TABLE OF CONTENTS

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Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; **http://www.microchip.com**
- Your local Microchip sales office (see last page)

When contacting Microchip, please specify which device, revision of silicon and data sheet (include literature number) you are using.

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Register on our web site at **http://www.microchip.com** to receive the most current information on all of our products.

1.0 OVERVIEW OF MXT1066TD

The Microchip maXTouch family of touch controllers brings industry-leading capacitive touch performance to customer applications. The mXT1066TD features the latest generation of Microchip adaptive sensing technology that utilizes a hybrid mutual and self capacitive sensing system in order to deliver unparalleled touch features and a robust user experience.

- **Patented capacitive sensing method** – The mXT1066TD uses a unique charge-transfer acquisition engine to implement Microchip's patented capacitive sensing method. Coupled with a state-of-the-art CPU, the entire touchscreen sensing solution can measure, classify and track a number of individual finger touches with a high degree of accuracy in the shortest response time.
- **Capacitive Touch Engine (CTE)** – The mXT1066TD features an acquisition engine that uses an optimal measurement approach to ensure almost complete immunity from parasitic capacitance on the receiver input lines. The engine includes sufficient dynamic range to cope with anticipated touchscreen self and mutual capacitances, which allows great flexibility for use with the Microchip proprietary sensor pattern designs. One- and two-layer ITO sensors are possible using glass or PET substrates.
- **Touch detection** – The mXT1066TD allows for both mutual and self capacitance measurements, with the self capacitance measurements being used to augment the mutual capacitance measurements to produce reliable touch information.

  When self capacitance measurements are enabled, touch classification is achieved using both mutual and self capacitance touch data. This has the advantage that both types of measurement systems can work together to detect touches under a wide variety of circumstances.

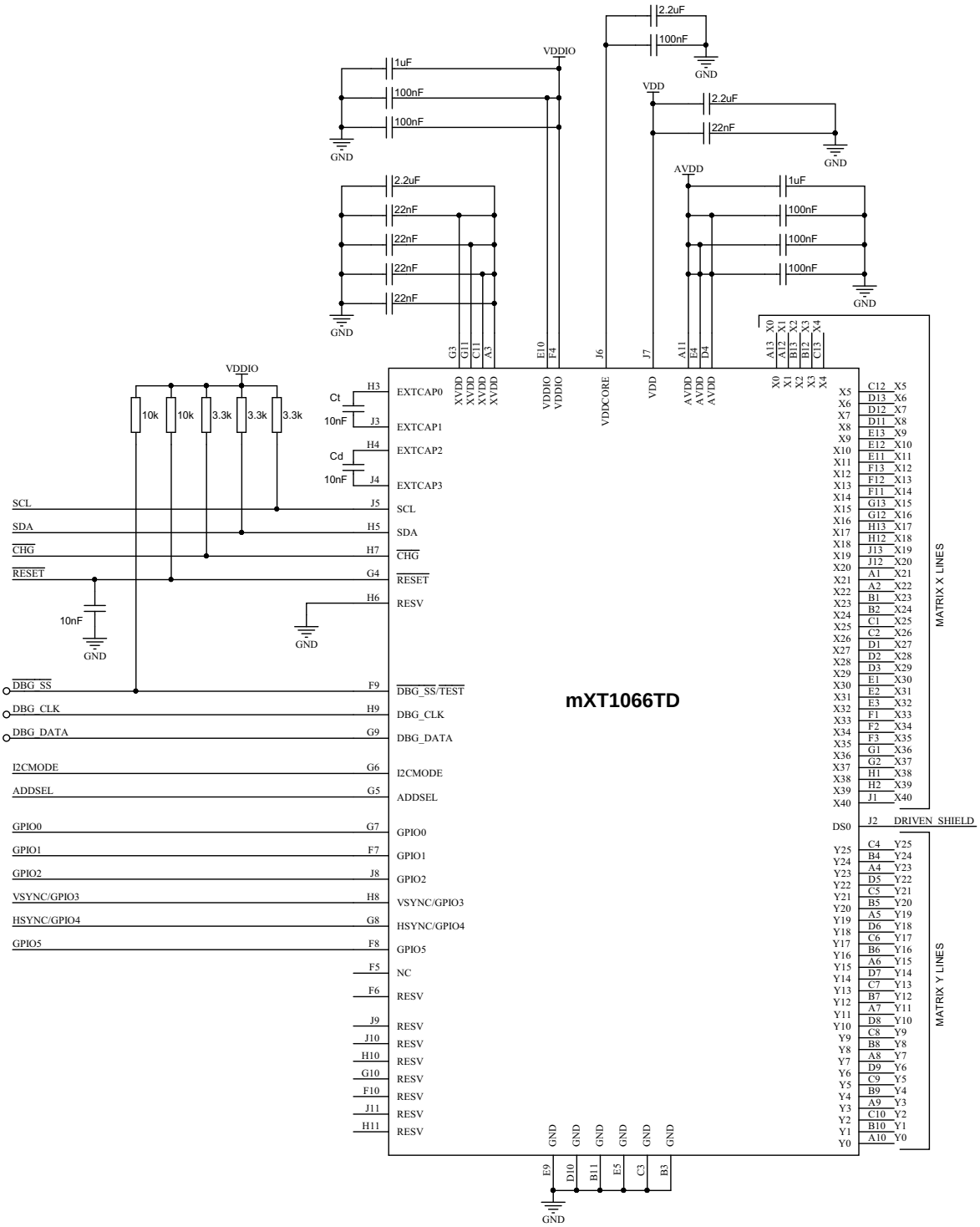
  The system may be configured for different types of default measurements in both idle and active modes. For example, the device may be configured for Mutual Capacitance Touch as the default in active mode and Self Capacitance Touch as the default in idle mode. Note that other types of scans (such as P2P mutual capacitance scans and other types of self capacitance scans) may also be made depending on configuration.

  Mutual capacitance touch data is used wherever possible to classify touches as this has a greater resolution than self capacitance measurements and provides positional information on touches. For this reason, multiple touches can only be determined by mutual capacitance touch data. In Self Capacitance Touch Default mode, if the self capacitance touch processing detects multiple touches, touchscreen processing is skipped until mutual capacitance touch data is available.

  Self capacitance and P2P mutual capacitance measurements allow for the detection of touches in extreme scenarios, such as thick glove touches, when mutual capacitance touch detection alone may miss touches.
- **Display Noise Cancellation** – A combination of analog circuitry, hardware noise processing, and firmware combats display noise without requiring additional listening channels or synchronization to display timing. This enables the use of shieldless touch sensor stacks, including touch-on-lens.
- **Noise filtering** – Hardware noise processing in the capacitive touch engine provides enhanced autonomous filtering and allows a broad range of noise profiles to be handled. The result is good performance in the presence of LCD noise.
- **Processing power** – The main CPU has two companion microsequencer coprocessors under its control consuming low power. This system allows the signal acquisition, preprocessing and postprocessing to be partitioned in an efficient and flexible way.
- **Interpreting user intention** – The Microchip hybrid mutual and self capacitance method provides unambiguous multitouch performance. Algorithms in the mXT1066TD provide optimized touchscreen position filtering for the smooth tracking of touches, responding to a user's intended touches while preventing false touches triggered by ambient noise, conductive material on the sensor surface, such as moisture, or unintentional touches from the user's resting palm or fingers.

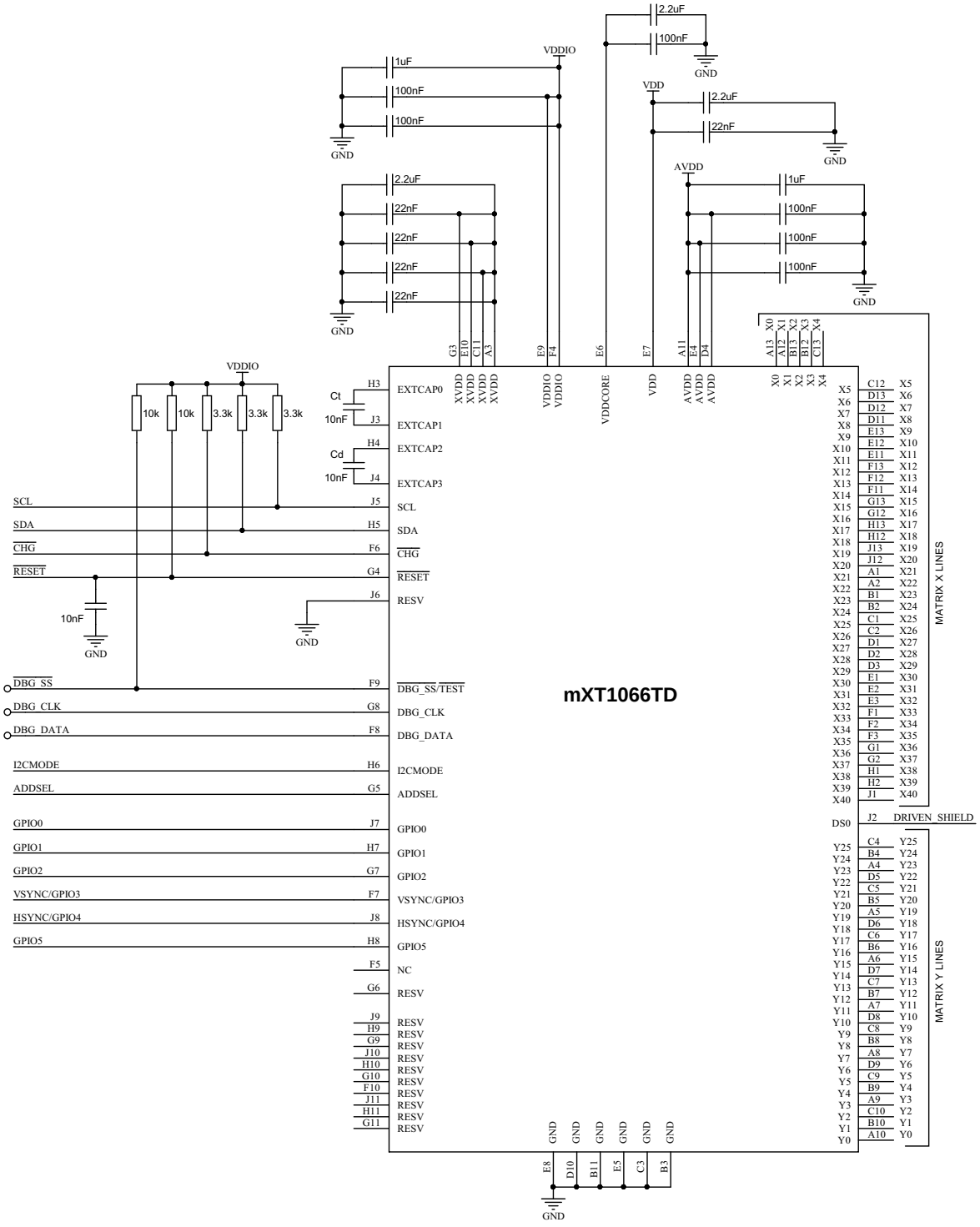
2.0 SCHEMATICS

2.1 UFBGA 114 Balls



See Section 2.3 “Schematic Notes”

2.2 UFBGA 117 Balls



See Section 2.3 “Schematic Notes”

2.3 Schematic Notes

2.3.1 POWER SUPPLY

The sense and I/O pins are supplied by the power rails on the device as listed in Table 2-1. This information is also indicated in "Pin configuration".

TABLE 2-1: POWER SUPPLY FOR SENSE AND I/O PINS

Power Supply	Pins
XVdd	X sense pins
AVdd	Y sense pins, DS0
VddIO	$\overline{\text{RESET}}$, $\overline{\text{CHG}}$ SDA, SCL, ADDSEL, I2CMODE, DBG_CLK, DBG_DATA, $\overline{\text{DBG\_SS}}$/$\overline{\text{TEST}}$ VSYNC/GPIO3, HSYNC/GPIO4, GPIO*n*

2.3.2 DECOUPLING CAPACITORS

All decoupling capacitors must be X7R or X5R and placed less than 5 mm away from the pins for which they act as bypass capacitors. Pins of the same type can share a capacitor provided no pin is more than 10 mm from the capacitor.

The schematics on the previous pages show the capacitors required. The parallel combination of capacitors is recommended to give high and low frequency filtering, which is beneficial if the voltage regulators are likely to be some distance from the device (for example, If an active tail design is used). Note that this requires that the voltage regulator supplies for AVdd, Vdd and VddIO are clean and noise free. It also assumes that the track length between the capacitors and on-board power supplies is less than 50 mm.

The number of base capacitors can be reduced if the pinout configuration means that sharing a bypass capacitor is possible (subject to the distance between the pins satisfying the conditions above and there being no routing difficulties).

2.3.3 PULL-UP RESISTORS

The pull-up resistors shown in the schematics are suggested typical values and may be modified to meet the requirements of an individual customer design.

This applies, in particular, to the pull-up resistors on the I^2C SDA and SCL lines (shown on the schematic), as the values of these resistors depend on the speed of the I^2C interface. See Section 13.9 "I2C Specification" for details.

Note that if a VddIO supply at the low end of the allowable range is used, the I^2C pull-up resistor values may need to be reduced.

2.3.4 VDDCORE

VddCore is internally generated from the Vdd power supply. To guarantee stability of the internal voltage regulator, one or more external decoupling capacitors are required.

2.3.5 XVDD

XVdd power can be supplied either as high voltage (using an internal voltage tripler) or as low voltage (using an internal voltage doubler). The operating mode should be chosen according to the final application.

To operate in voltage tripler mode, the voltage pump requires two external capacitors:

- EXTCAP2 must be connected to EXTCAP3 via a capacitor (Cd).
- EXTCAP0 must be connected to EXTCAP1 via a capacitor (Ct).

To operate in voltage doubler mode, the voltage pump requires one external capacitor:

- EXTCAP2 must be connected to EXTCAP3 via a capacitor (Cd).
- EXTCAP0 and EXTCAP1 can be left unconnected.

Capacitors Cd and Ct should each provide a capacitance of 10 nF. The capacitors must be placed as close as possible to the EXTCAP*n* pins.

2.3.6 DRIVEN SHIELD LINE

The driven shield line (DS0) should be used to shield the X/Y sense lines. Specifically, it acts as a driven shield in self capacitance operation. See Section 10.4 "Driven Shield Line" for more details.

2.3.7 MULTIPLE FUNCTION PINS

Some pins may have multiple functions. In this case, only one function can be chosen and the circuit should be designed accordingly.

2.3.8 VSYNC AND HSYNC PIN

The mXT1066TD has two synchronization pins: VSYNC for frame synchronization and HSYNC for pulse synchronization.

2.3.9 GPIO PINS

The mXT1066TD has 6 GPIO pins. The pins can be set to be either an input or an output, as required, using the GPIO Configuration T19 object.

If a GPIO pin is unused, it can be left unconnected externally as long as it is given a defined state by the GPIO Configuration T19 object.

By default the GPIO pins are set to be inputs so if a pin is not used, and is left configured as an input, it should be connected to GND through a resistor. Alternatively, the internal pull-up resistor should be enabled (in the GPIO Configuration T19 object) to pull up the pin.

Alternatively, the GPIO pin can be set as an output low using the GPIO Configuration T19 object and left open. This second option avoids any problems should the pin accidentally be configured as output high at a later date.

If the GPIO Configuration T19 object is not enabled for use, the GPIO pins cannot be used for GPIO purposes, although any alternative function can still be used.

Some GPIO pins have alternative functions. If an alternative function is used then this takes precedence over the GPIO function and the pin cannot be used as a GPIO pin. In particular:

- GPIO3 cannot be used if the VSYNC function is in use.
- GPIO4 cannot be used if the HSYNC function is in use.

2.3.10 SPI DEBUG INTERFACE

The DBG_CLK, DBG_DATA and $\overline{\text{DBG\_SS}}$ lines form the SPI Debug Interface. These pins should be routed to test points on all designs, such that they can be connected to external hardware during system development and for debug purposes. See also Section 12.1 “SPI Debug Interface”.

3.0 TOUCHSCREEN BASICS

3.1 Sensor Construction

A touchscreen is usually constructed from a number of transparent electrodes. These are typically on a glass or plastic substrate. They can also be made using non-transparent electrodes, such as copper or carbon. Electrodes are constructed from Indium Tin Oxide (ITO) or metal mesh. Thicker electrodes yield lower levels of resistance (perhaps tens to hundreds of Ω/square) at the expense of reduced optical clarity. Lower levels of resistance are generally more compatible with capacitive sensing. Thinner electrodes lead to higher levels of resistance (perhaps hundreds of Ω/square) with some of the best optical characteristics.

Interconnecting tracks in ITO can cause problems. The excessive RC time constants formed between the resistance of the track and the capacitance of the electrode to ground can inhibit the capacitive sensing function. In such cases, the tracks should be replaced by screen printed conductive inks (non-transparent) outside the touchscreen viewing area.

3.2 Electrode Configuration

The specific electrode designs used in Microchip touchscreens are the subject of various patents and patent applications. Further information is available on request.

The device supports various configurations of electrodes as summarized in Section 4.0 “Sensor Layout”.

3.3 Scanning Sequence

All nodes are scanned in sequence by the device. Where possible, there is a parallelism in the scanning sequence to improve overall response time. The nodes are scanned by measuring capacitive changes at the intersections formed between the first drive (X) line and all the receive (Y) lines. Then the intersections between the next drive line and all the receive lines are scanned, and so on, until all X and Y combinations have been measured.

The device can be configured in various ways. It is possible to disable some nodes so that they are not scanned at all. This can be used to improve overall scanning time.

3.4 Touchscreen Sensitivity

3.4.1 ADJUSTMENT

Sensitivity of touchscreens can vary across the extents of the electrode pattern due to natural differences in the parasitic capacitance of the interconnections, control chip, and so on. An important factor in the uniformity of sensitivity is the electrode design itself. It is a natural consequence of a touchscreen pattern that the edges form a discontinuity and hence tend to have a different sensitivity. The electrodes at the edges do not have a neighboring electrode on one side and this affects the electric field distribution in that region.

A sensitivity adjustment is available for the whole touchscreen. This adjustment is a basic algorithmic threshold that defines when a node is considered to have enough signal change to qualify as being in detect.

3.4.2 MECHANICAL STACKUP

The mechanical stackup refers to the arrangement of material layers that exist above and below a touchscreen. The arrangement of the touchscreen in relation to other parts of the mechanical stackup has an effect on the overall sensitivity of the screen. The maXTouch technology has an excellent ability to operate in the presence of ground planes close to the sensor. The sensitivity of the maXTouch technology is attributed more to the interaction of the electric fields between the transmitting (X) and receiving (Y) electrodes than to the surface area of these electrodes. For this reason, stray capacitance on the X or Y electrodes does not strongly reduce sensitivity.

Front panel dielectric material has a direct bearing on sensitivity. Plastic front panels are usually suitable up to about 5 mm, and glass up to about 10 mm (dependent upon the screen size and layout). The thicker the front panel, the lower the signal-to-noise ratio of the measured capacitive changes and hence the lower the resolution of the touchscreen. In general, glass front panels are near optimal because they conduct electric fields almost twice as easily as plastic panels.

NOTE	Care should be taken using ultra-thin glass panels as retransmission effects can occur, which can significantly degrade performance.

4.0 SENSOR LAYOUT

NOTE	The specific electrode designs used in Microchip touchscreens may be the subject of various patents and patent applications. Further information is available on request.

4.1 Electrodes

The device supports various configurations of touch electrodes as summarized below:

- Touchscreen: 1 touchscreen panel occupies a rectangular matrix of up to 41 X × 26 Y lines maximum (subject to other configurations).

4.2 Sensor Matrix Layout

When designing the physical layout of the touch panel, the following rules must be obeyed:

- **General layout rules:**
  - The Multiple Touch Touchscreen T100 object should be a regular rectangular shape in terms of the lines it uses.
- **Additional layout rules for Multiple Touch Touchscreen T100:**
  - The Multiple Touch Touchscreen T100 object ***must*** start at (X0, Y0)
  - The touchscreen must contain a minimum of 3 X lines for mutual capacitance measurements. If Dual X Drive is enabled for use in the Noise Suppression T72 object, the minimum is 4 X lines.
  - If self capacitance measurements are enabled in the Acquisition Configuration T8 object, the touchscreen must contain a minimum of 6 X lines. Note, however, that X31 must be included within the sensor matrix if the driven shield is used (see Section 4.4 “Driven Shield Line”), which means an effective minimum of 32 X lines.
  - The touchscreen must contain a minimum of 3 Y lines for mutual capacitance measurements.

4.3 Screen Size

Table 4-1 lists some typical screen size and electrode pitch combinations to achieve various aspect ratios.

TABLE 4-1: TYPICAL SCREEN SIZES

Aspect Ratio	Matrix Size	Node Count	Screen Diagonal (Inches)			
			3.8 mm Pitch (2)	5 mm Pitch	6 mm Pitch	6.5 mm Pitch
16:10	X = 41, Y = 26	1066	7.26	9.56	11.47	12.42
16:9	X = 41, Y = 23	943	7.03	9.25	11.1	12.03
4:3	X = 35, Y = 26	910	6.52	8.58	10.3	11.16

Note 1: The figures given in the table are for a Touchscreen and show the largest node count possible to achieve the desired aspect ratio.

2: Recommended sensor pitch for 1.5 mm passive stylus tip diameter.

4.4 Driven Shield Line

A driven shield trace is recommended to run between the groups of X tracks and the groups of Y tracks, as well as between the combined group of X/Y tracks and Ground. See Section 10.4 “Driven Shield Line” for more information.

NOTE	X31 is connected internally to the driven shield line (DS0). The driven shield does not function if X31 is not used for self capacitance measurements. X31 must therefore be included within the sensor matrix if the driven shield is used.

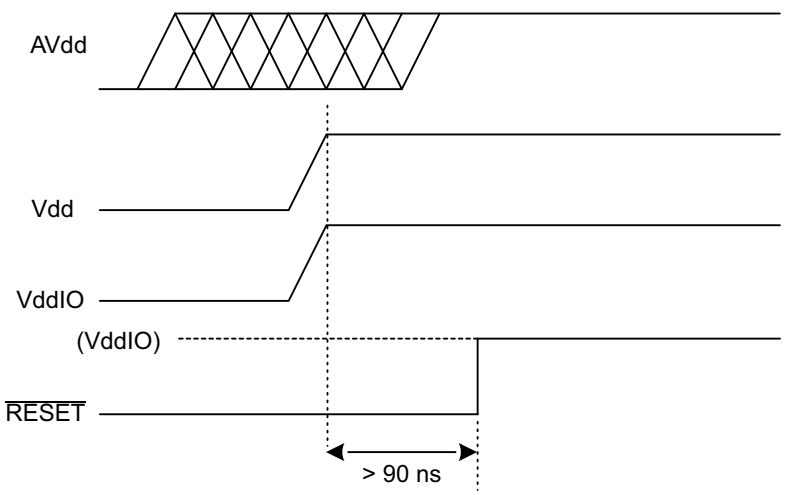
5.0 POWER-UP / RESET REQUIREMENTS

5.1 Power-on Reset

There is an internal Power-on Reset (POR) in the device.

If an external reset is to be used the device must be held in RESET (active low) while the digital (Vdd), analog (AVdd) and digital I/O (VddIO) power supplies are powering up. The supplies must have reached their nominal values before the RESET signal is deasserted (that is, goes high). This is shown in Figure 5-1. See Section 13.2 “Recommended Operating Conditions” for nominal values for the power supplies to the device.

FIGURE 5-1: POWER SEQUENCING ON THE MXT1066TD



Note: When using external RESET at power-up, VddIO must not be enabled after Vdd

It is recommended that customer designs include the capability for the host to control all the maXTouch power supplies and pull the RESET line low.

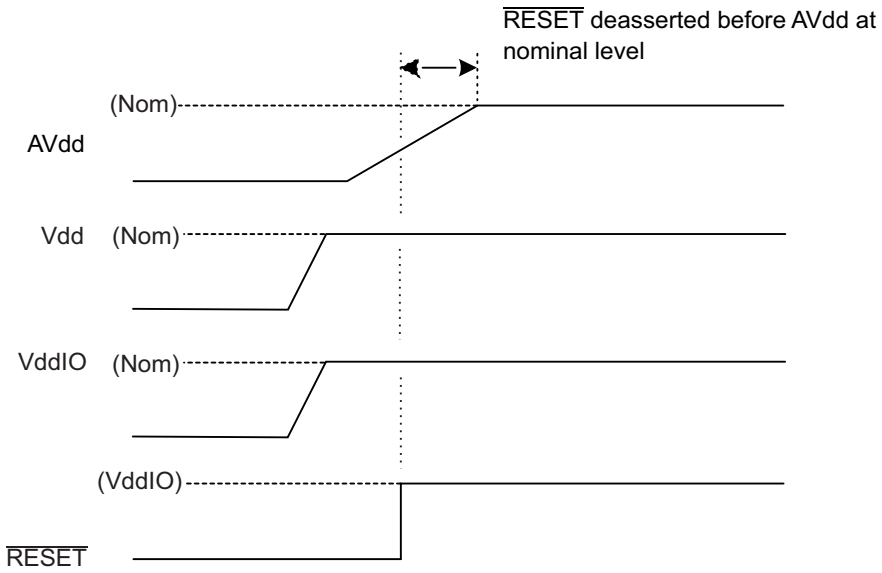
After power-up, the device typically takes 97 ms before it is ready to start communications.

NOTE	Device initialization will not complete until after all the power supplies are present. If any power supply is not present, internal initialization stalls and the device will not communicate with the host.

If the RESET line is released before the AVdd supply has reached its nominal voltage (see Figure 5-2), then some additional operations need to be carried out by the host. There are two options open to the host controller:

- Start the part in Deep Sleep mode and then send the command sequence to set the cycle time to wake the part and allow it to run normally. Note that in this case a calibration command is also needed.
- Send a RESET command.

FIGURE 5-2: POWER SEQUENCING ON THE MXT1066TD – LATE RISE ON AVDD



The RESET pin can be used to reset the device whenever necessary. The RESET pin must be asserted low for at least 90 ns to cause a reset. After the host has released the RESET pin, the device typically takes 92 ms before it is ready to start communications. It is recommended to connect the RESET pin to a host controller to allow the host to initiate a full hardware reset without requiring the mXT1066TD to be powered down.

WARNING	The device should be reset only by using the RESET line. If an attempt is made to reset by removing the power from the device without also sending the signal lines low, power will be drawn from the communication and I/O lines and the device will not reset correctly.

Make sure that any lines connected to the device are below or equal to Vdd during power-up and power-down. For example, if RESET is supplied from a different power domain to the VDDIO pin, make sure that it is held low when Vdd is off. If this is not done, the RESET signal could parasitically couple power via the RESET pin into the Vdd supply.

NOTE	The voltage level on the RESET pin of the device must never exceed VddIO (digital supply voltage).

A software RESET command (using the Command Processor T6 object) can be used to reset the chip. A software reset typically takes 116 ms before it is ready to start communications. After the chip has finished it asserts the CHG line to signal to the host that a message is available. The reset flag is set in the Command Processor T6 object message data to indicate to the host that it has just completed a reset cycle. This bit can be used by the host to detect any unexpected brownout events. This allows the host to take any necessary corrective actions, such as reconfiguration.

NOTE	The CHG line is briefly set (~100 ms) as an input during power-up or reset. It is therefore particularly important that the line should be allowed to float high via the CHG line pull-up resistor during this period. It should never be driven by the host (see Section 13.5.3 “Reset Timings”).

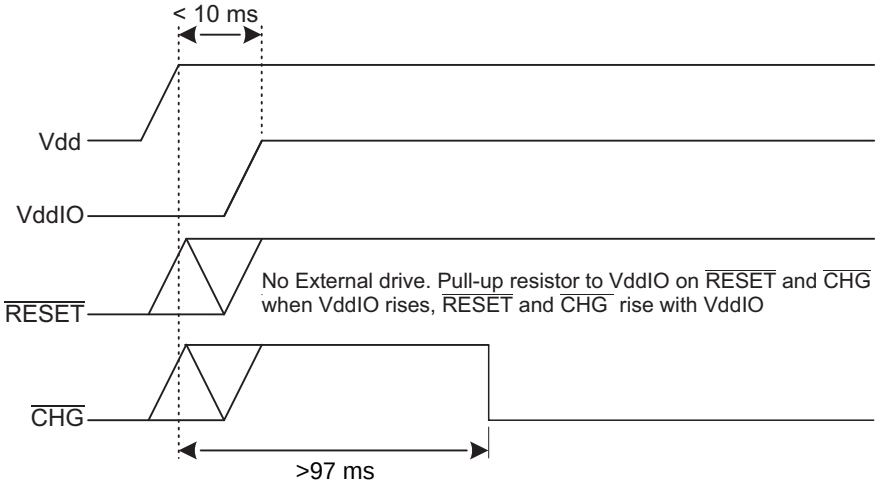
At power-on, the device performs a self-test routine (using the Self Test T25 object) to check for shorts that might cause damage to the device.

5.2 Power-up and Reset Sequence – VddIO Enabled after Vdd

The power-up sequence that can be used in applications where VddIO must be powered up after Vdd, is shown in Figure 5-3.

In this case the communication interface to the maXTouch device is not driven by the host system. The RESET and CHG pins are connected to VddIO using suitable pull-up resistors. Vdd is powered up, followed by VddIO, no more than 10 ms after Vdd. Due to the pull-up resistors, RESET and CHG will rise with VddIO. The internal POR system ensures reliable boot up of the device and the CHG line will go low approximately 97 ms after Vdd to notify the host that the device is ready to start communication.

FIGURE 5-3: POWER-UP SEQUENCE



5.3 Power-up and Initialization

The device uses a number of different power domains for optimum performance and contains circuitry to interface internal signals crossing between the different domains. There is also circuitry to ensure that the device interface logic will be initialized correctly as the device powers on. Note, however, that this does not negate specific instructions elsewhere in this section about the order that the different supplies should power up. Also, as previously mentioned, RESET should be held low until after all power rails are stable. In addition, the device will not initialize until all the voltage rails have powered up and are present.

If one domain loses power, however (for example, due to a fault or an ESD event), the device should be power-cycled to ensure that the interface logic is once again initialized. It is therefore recommended that customer designs include the capability for the host to control all the maXTouch power supplies and pull the RESET line low.

5.4 Summary

The power-up and reset requirements for the maXTouch devices are summarized in Table 5-1.

TABLE 5-1: POWER-UP AND RESET REQUIREMENTS

Condition	External RESET	VddIO Delay (After Vdd)	AVdd Power-Up	Comments
1	Low at Power-up	0 ms	Before RESET is released	If AVdd bring-up is delayed, then additional actions will be required by the host (see Section 5.1 “Power-on Reset”)
2	Not driven	<10 ms	Before VddIO	

6.0 DETAILED OPERATION

6.1 Touch Detection

The mXT1066TD allows for both mutual and self capacitance measurements, with the self capacitance measurements being used to augment the mutual capacitance measurements to produce reliable touch information.

When self capacitance measurements are enabled, touch classification is achieved using both mutual and self capacitance touch data. This has the advantage that both types of measurement systems can work together to detect touches under a wide variety of circumstances.

Mutual capacitance touch data is used wherever possible to classify touches as this has greater granularity than self capacitance measurements and provides positional information on touches.

Self capacitance measurements, on the other hand, allow for the detection of single touches in extreme cases, such as single thick glove touches, when touches can only be detected by self capacitance data and may be missed by mutual capacitance touch detection.

6.2 Operational Modes

The device operates in two modes: **Active** (touch detected) and **Idle** (no touches detected). Both modes operate as a series of burst cycles. Each cycle consists of a short burst (during which measurements are taken) followed by an inactive sleep period. The difference between these modes is the length of the cycles. Those in idle mode typically have longer sleep periods. The cycle length is configured using the IDLEACQINT and ACTVACQINT settings in the Power Configuration T7. In addition, an *Active to Idle Timeout* setting is provided.

6.3 Detection Integrator

The device features a touch detection integration mechanism. This acts to confirm a detection in a robust fashion. A counter is incremented each time a touch has exceeded its threshold and has remained above the threshold for the current acquisition. When this counter reaches a preset limit the sensor is finally declared to be touched. If, on any acquisition, the signal is not seen to exceed the threshold level, the counter is cleared and the process has to start from the beginning.

The detection integrator is configured using the appropriate touch objects (Multiple Touch Touchscreen T100).

6.4 Sensor Acquisition

The charge time for mutual capacitance measurements is set using the Acquisition Configuration T8 object. The device combines a number of factors together to arrive at the total acquisition time for one drive line (that is, one X line for mutual capacitance acquisitions or one axis for self capacitance acquisitions).

The following constraints apply on the mXT1066TD:

- The per X line mutual capacitance touch measurement and the per axis self capacitance measurement must not exceed 2 ms. Furthermore, the total acquisition time for the sensor as a whole must not exceed 250 ms. In the event of a timeout, a SIGERR may be reported.
- The high and low pulse periods must not exceed 37.26 µs each. This means that the maximum possible burst period is 74.52 µs (that is, a minimum frequency of 13.42 kHz). In addition, the burst period must not be less than 4 µs (that is, a maximum frequency of 250 kHz).

Unpredictable system behavior might occur if any of the above constraints are not met.

Care should be taken to configure all the objects that can affect the measurement timing so that these limits are not exceeded.

6.5 Calibration

Calibration is the process by which a sensor chip assesses the background capacitance on each node. Calibration occurs in a variety of circumstances, for example:

- When determined by the mutual capacitance recalibration process, as controlled by the Acquisition Configuration T8 object
- When determined by the self capacitance recalibration process, as controlled by the Self Capacitance Configuration T111 object
- When the Retransmission Compensation T80 object detects calibrated-in moisture has been removed

- Following a Self Capacitance Global Configuration T109 Tune command
- When the host issues a recalibrate command
- When certain configuration settings are changed

6.6 Digital Filtering and Noise Suppression

The mXT1066TD supports on-chip filtering of the acquisition data received from the sensor. Specifically, the Noise Suppression T72 object provides an algorithm to suppress the effects of noise (for example, from a noisy charger plugged into the user's product). This algorithm can automatically adjust some of the acquisition parameters on-the-fly to filter the Analog-to-Digital Conversions (ADCs) received from the sensor.

Additional noise suppression is provided by the Self Capacitance Noise Suppression T108 object. Similar in both design and configuration to the Noise Suppression T72 object, the Self Capacitance Noise Suppression T108 object is the noise suppression interface for self capacitance touch measurements.

Noise suppression is triggered when a noise source is detected.

- The host driver code can indicate when a noise source is present.
- The noise suppression is also triggered based on the noise levels detected using internal line measurements.The Noise Suppression T72 and Self Capacitance Noise Suppression T108 object selects the appropriate controls to suppress the noise present in the system.

6.7 Shieldless Support and Display Noise Suppression

The mXT1066TD can support shieldless sensor design even with a noisy LCD.

The Optimal Integration feature is not filtering as such, but enables the user to use a shorter integration window. The integration window optimizes the amount of charge collected against the amount of noise collected, to ensure an optimal SNR. This feature also benefits the system in the presence of an external noise source. This feature is configured using the Shieldless T56 object.

Display noise suppression allows the device to overcome display noise simultaneously with external noise. This feature is based on filtering provided by the Lens Bending T65 object (see Section 6.10 "Lens Bending").

6.8 Retransmission Compensation

The device can limit the undesirable effects on the mutual capacitance touch signals caused by poor device coupling to ground, such as poor sensitivity and touch break-up. This is achieved using the Retransmission Compensation T80 object. This object can be configured to allow the touchscreen to compensate for signal degradation due to these undesirable effects. If self capacitance measurements are also scheduled, the Retransmission Compensation T80 object will use the resultant data to enhance the compensation process.

The Retransmission Compensation T80 object is also capable of compensating for water presence on the sensor if self capacitance measurements are scheduled. In this case, both mutual capacitance and self capacitance measurements are used to detect moisture and then, once moisture is detected, self capacitance measurements are used to detect single touches in the presence of moisture.

6.9 Grip Suppression

The device has grip suppression functionality to suppress false detections from a user's grip.

Mutual capacitance grip suppression works by specifying a boundary around a touchscreen, within which touches can be suppressed whilst still allowing touches in the center of the touchscreen. This ensures that an accidental hand touch on the edge is suppressed while still allowing a "real" (finger) touch towards the center of the screen. Mutual capacitance grip suppression is configured using the Grip Suppression T40 object.

Self Capacitance grip suppression works by looking for characteristic shapes in the self capacitance measurement along the touchscreen boundary, and thereby distinguishing between a grip and a touch further into the sensor. Self capacitance grip suppression is configured using the Self Capacitance Grip Suppression T112 object.

6.10 Lens Bending

The device supports algorithms to eliminate disturbances from the measured signal.

When the sensor suffers from the screen deformation (lens bending) the signal values acquired by normal procedure are corrupted by the disturbance component (bend). The amount of bend depends on:

- The mechanical and electrical characteristics of the sensor
- The amount and location of the force applied by the user touch to the sensor

The Lens Bending T65 object measures the bend component and compensates for any distortion caused by the bend. As the bend component is primarily influenced by the user touch force, it can be used as a secondary source to identify the presence of a touch. The additional benefit of the Lens Bending T65 object is that it will eliminate LCD noise as well.

6.11 Glove Detection

The device has glove detection algorithms that process the measurement data received from the touchscreen classifying touches as potential gloved touches.

The Glove Detection T78 object is used to detect glove touches. In Normal Mode the Glove Detection T78 object applies vigorous glove classification to small signal touches to minimize the effect of unintentional hovering finger reporting. Once a gloved touch is found, the Glove Detection T78 object enters Glove Confidence Mode. In this mode the device expects the user to be wearing gloves so the classification process is much less stringent.

6.12 Stylus Support

The mXT1066TD allows for the particular characteristics of passive stylus touches, whilst still allowing conventional finger touches to be detected. The touch sensitivity and threshold controls for stylus touches are configured separately from those for conventional finger touches so that both types of touches can be accommodated.

Stylus support ensures that the small touch area of a stylus registers as a touch, as this would otherwise be considered too small for the touchscreen. Additionally, there are controls to distinguish a stylus touch from an unwanted approaching finger (such as on the hand holding the stylus).

Passive stylus touches are configured by the Passive Stylus T47 object. There is one instance of the Passive Stylus T47 object for each Multiple Touch Touchscreen T100 object present on the device.

6.13 Unintentional Touch Suppression

The Touch Suppression T42 object provides a mechanism to suppress false detections from unintentional touches from a large body area, such as from a face, ear or palm. The Touch Suppression T42 object also provides Maximum Touch Suppression to suppress all touches if more than a specified number of touches has been detected.

7.0 HOST COMMUNICATIONS

Communication between the mXT1066TD and the host is achieved using one of the following interfaces:

- I²C (see Section 8.0 “I2C Communications”)
- HID-I²C (see Section 9.0 “HID-I²C Communications”)

Either host interface can be used, depending on the needs of the user’s project, but only one interface can be used in any one design.

7.1 I²C Mode Selection – I2CMODE Pin

The selection of the I²C or the HID-I²C mode is determined by connecting the I2CMODE pin according to Table 7-1.

TABLE 7-1: I²C MODE SELECTION

I2CMODE	Interface Selected
Connected to GND	HID-I²C
Pulled up to VddIO (1)	I²C

Note 1: Requires an external pull-up resistor

7.2 I²C Address Selection – ADDSEL Pin

The I²C address is selected by connecting the ADDSEL pin according to Table 7-2.

TABLE 7-2: I²C ADDRESS SELECTION

ADDSEL	I²C Address
Connected to GND	0x4A
Pulled up to VddIO (1)	0x4B

Note 1: Requires an external pull-up resistor.

8.0 I²C COMMUNICATIONS

Communication with the device can be carried out over the I²C interface.

The I²C interface is used in conjunction with the $\overline{\text{CHG}}$ line. The $\overline{\text{CHG}}$ line going active signifies that a new data packet is available. This provides an interrupt-style interface and allows the device to present data packets when internal changes have occurred. See Section 8.5 “CHG Line” for more information.

See Section 7.0 “Host Communications” for information on selecting I²C mode.

8.1 I²C Addresses

The device supports two I²C device addresses that are selected using the ADDSEL line at startup. The two I²C device addresses are 0x4A and 0x4B. The selection of the address (and the communication mode) is described in Section 7.2 “I²C Address Selection – ADDSEL Pin”.

The I²C address is shifted left to form the SLA+W or SLA+R address when transmitted over the I²C interface, as shown in Table 8-1.

TABLE 8-1: FORMAT OF SLA+W/SLA+R

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address: 0x4A or 0x4B							Read/write

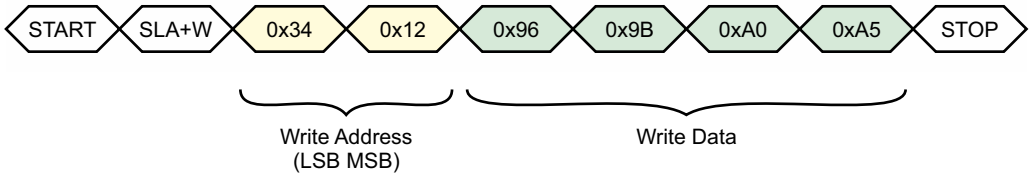
8.2 Writing To the Device

An I²C WRITE cycle consists of the following bytes:

START	1 bit	I²C START condition
SLA+W	1 byte	I²C address of the device (see Section 8.1 “I2C Addresses”)
Address (LSByte, MSByte)	2 bytes	Address of the location at which the data writing starts. This address is stored as the address pointer.
Data	0 or more bytes	The actual data to be written. The data is written to the device, starting at the location of the address pointer. The address pointer returns to its starting value when the I²C STOP condition is detected.
CRC (optional)	1 byte	An optional 8-bit CRC that includes all the bytes that have been sent, including the two address bytes, but not the SLA+W byte. If the device detects an error in the CRC during a write transfer, a COMSERR fault is reported by the Command Processor T6 object. See Section 8.3 “I²C Writes in Checksum Mode” for more details
STOP	1 bit	I²C STOP condition

Figure 8-1 shows an example of writing four bytes of data to contiguous addresses starting at 0x1234.

FIGURE 8-1: EXAMPLE OF A FOUR-BYTE WRITE STARTING AT ADDRESS 0x1234

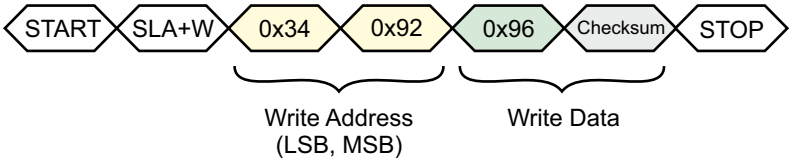


8.3 I²C Writes in Checksum Mode

In I²C checksum mode an 8-bit CRC is added to all I²C writes. The CRC is sent at the end of the data write as the last byte before the STOP condition. All the bytes sent are included in the CRC, including the two address bytes. Any command or data sent to the device is processed even if the CRC fails.

To indicate that a checksum is to be sent in the write, the most significant bit of the MSByte of the write address is set to 1. For example, the I²C command shown in Figure 8-2 writes a value of 150 (0x96) to address 0x1234 with a checksum. The address is changed to 0x**9**234 to indicate checksum mode.

FIGURE 8-2: EXAMPLE OF A WRITE TO ADDRESS 0x1234 WITH A CHECKSUM



8.4 Reading From the Device

Two I²C bus activities must take place to read from the device. The first activity is an I²C write to set the address pointer (LSByte then MSByte). The second activity is the actual I²C read to receive the data. The address pointer returns to its starting value when the read cycle NACK or STOP is detected.

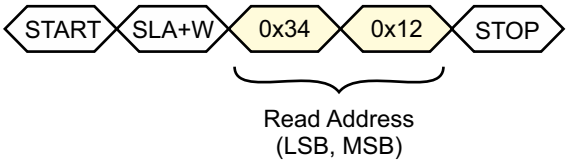
It is not necessary to set the address pointer before every read. The address pointer is updated automatically after every read operation. The address pointer will be correct if the reads occur in order. In particular, when reading multiple messages from the Message Processor T5 object, the address pointer is automatically reset to the address of the Message Processor T5 object, in order to allow continuous reads (see Section 8.4.2 “Reading Status Messages with DMA”).

The WRITE and READ cycles consist of a START condition followed by the I²C address of the device (SLA+W or SLA+R respectively).

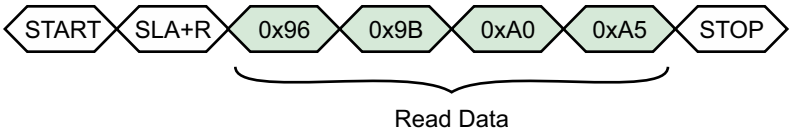
Figure 8-3 shows the I²C commands to read four bytes starting at address 0x1234.

FIGURE 8-3: EXAMPLE OF A FOUR-BYTE READ STARTING AT ADDRESS 0x1234

Set Address Pointer



Read Data



NOTE	At least one data byte must be read during an I²C READ transaction; it is illegal to abort the transaction with an I²C STOP condition without reading any data.

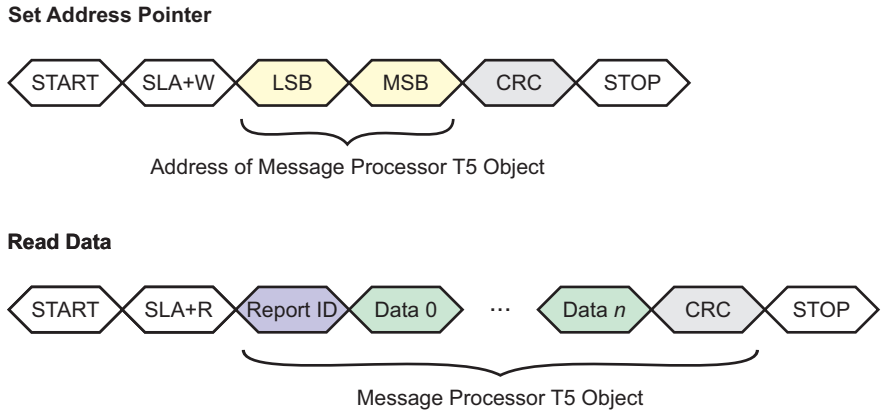
8.4.1 READING A MESSAGE FROM THE MESSAGE PROCESSOR T5 OBJECT

An I²C read of the Message Processor T5 object contains the following bytes:

START	1 bit	I²C START condition
SLA+R	1 byte	I²C address of the device (see Section 8.1 “I2C Addresses”)
Report ID	1 byte	Message report ID
Data	1 or more bytes	The message data (size = size of Message Processor T5 MESSAGE field)
CRC (optional)	1 byte	An 8-bit CRC (if requested) for the Message Processor T5 report ID and message data See Section 8.3 “I²C Writes in Checksum Mode” for more details on how to request a checksum
STOP	1 bit	I²C STOP condition

Figure 8-4 shows an example read from the Message Processor T5 object. To read multiple messages using Direct Memory Access, see Section 8.4.2 “Reading Status Messages with DMA”.

FIGURE 8-4: EXAMPLE READ FROM MESSAGE PROCESSOR T5 WITH A CHECKSUM



8.4.2 READING STATUS MESSAGES WITH DMA

The device facilitates the easy reading of multiple messages using a single continuous read operation. This allows the host hardware to use a Direct Memory Access (DMA) controller for the fast reading of messages, as follows:

1. The host uses a write operation to set the address pointer to the start of the Message Count T44 object, if necessary. Note that the STOP condition at the end of the read resets the address pointer to its initial location, so it may already be pointing at the Message Count T44 object following a previous message read. If a checksum is required on each message, the most significant bit of the MSByte of the read address must be set to 1.
2. The host starts the read operation of the message by sending a START condition.
3. The host reads the Message Count T44 object (one byte) to retrieve a count of the pending messages.
4. The host calculates the number of bytes to read by multiplying the message count by the size of the Message Processor T5 object. Note that the host should have already read the size of the Message Processor T5 object in its initialization code.

   Note that the size of the Message Processor T5 object as recorded in the Object Table includes a checksum byte. If a checksum has not been requested, one byte should be deducted from the size of the object. That is: number of bytes = count × (size – 1).
5. The host reads the calculated number of message bytes. It is important that the host does *not* send a STOP condition during the message reads, as this will terminate the continuous read operation and reset the address pointer. No START and STOP conditions must be sent between the messages.
6. The host sends a STOP condition at the end of the read operation after the last message has been read. The NACK condition immediately before the STOP condition resets the address pointer to the start of the Message Count T44 object.

Figure 8-5 shows an example of using a continuous read operation to read three messages from the device without a checksum. Figure 8-6 shows the same example with a checksum.

FIGURE 8-5: CONTINUOUS MESSAGE READ EXAMPLE – NO CHECKSUM

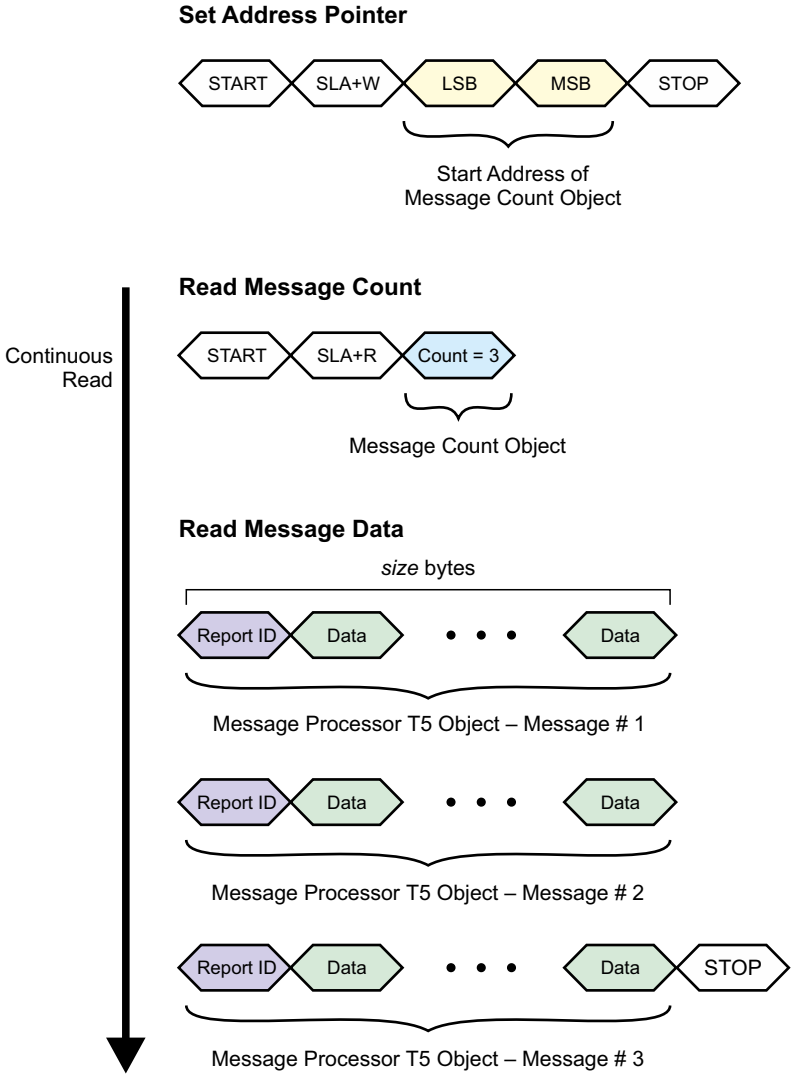
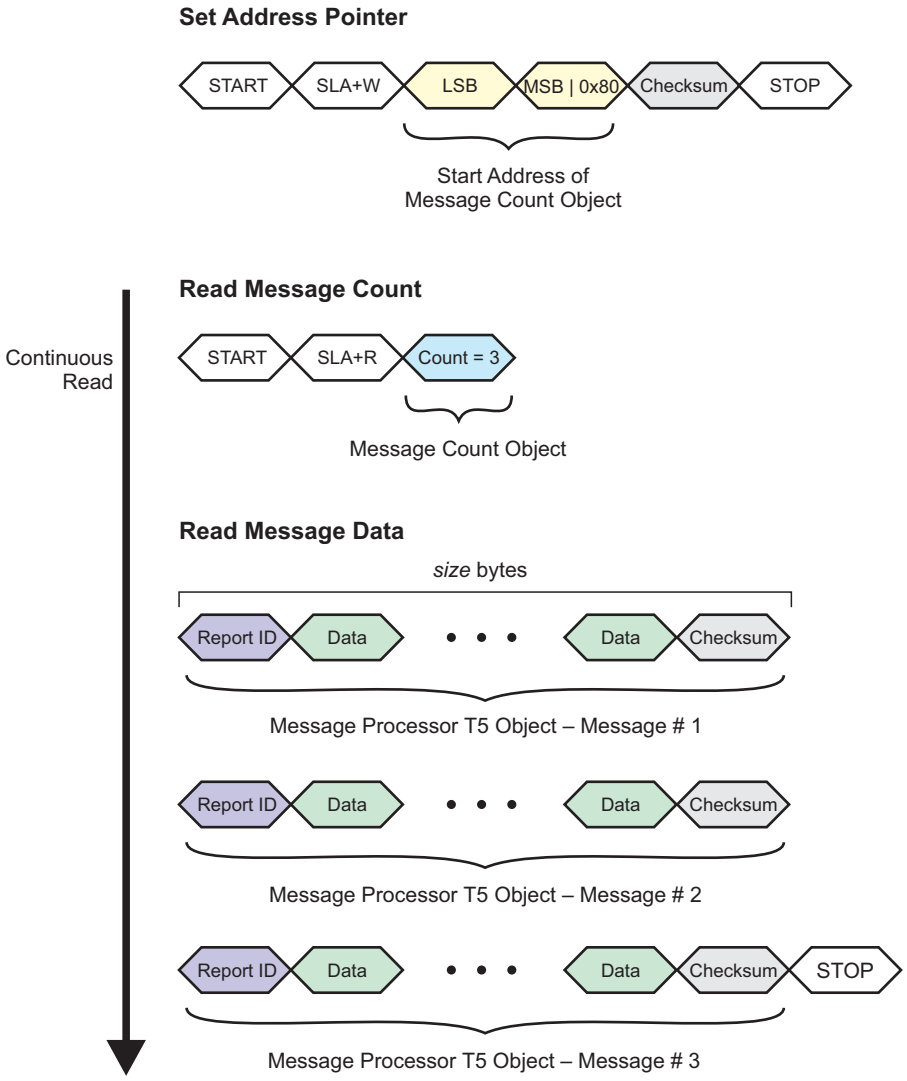


FIGURE 8-6: CONTINUOUS MESSAGE READ EXAMPLE – I²C CHECKSUM MODE



8.5 $\overline{\text{CHG}}$ Line

The $\overline{\text{CHG}}$ line is an active-low, open-drain output that is used to alert the host that a new message is available in the Message Processor T5 object. This provides the host with an interrupt-style interface with the potential for fast response times. It reduces the need for wasteful I²C communications.

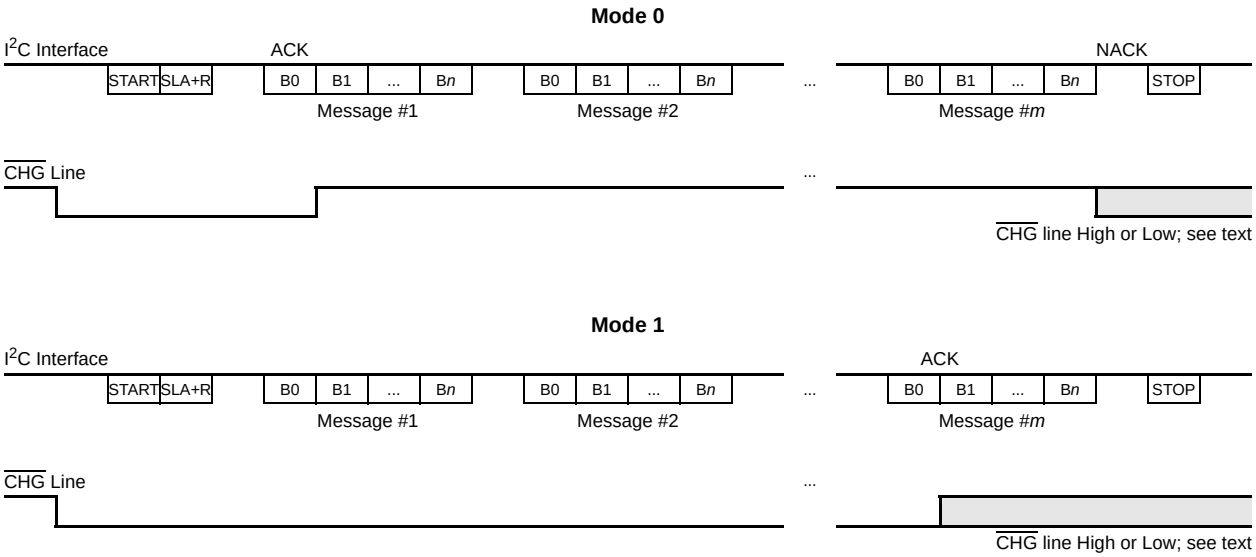
NOTE	The host should always use the $\overline{\text{CHG}}$ line as an indication that a message is ready to be read from the Message Processor T5 object; the host should never poll the device for messages.

The $\overline{\text{CHG}}$ line should always be configured as an input on the host during normal usage. This is particularly important after power-up or reset (see Section 5.0 “Power-up / Reset Requirements”).

A pull-up resistor is required to VddIO (see Section 2.0 “Schematics”).

The $\overline{\text{CHG}}$ line operates in two modes when it is used with I²C communications, as defined by the Communications Configuration T18 object.

FIGURE 8-7: $\overline{\text{CHG}}$ LINE MODES FOR I²C-COMPATIBLE TRANSFERS



In Mode 0 (edge-triggered operation):

1. The $\overline{\text{CHG}}$ line goes low to indicate that a message is present.
2. The $\overline{\text{CHG}}$ line goes high when the first byte of the first message (that is, its report ID) has been sent and acknowledged (ACK sent) and the next byte has been prepared in the buffer.
3. The STOP condition at the end of an I²C transfer causes the $\overline{\text{CHG}}$ line to stay high if there are no more messages. Otherwise the $\overline{\text{CHG}}$ line goes low to indicate a further message.

Note that Mode 0 also allows the host to continually read messages by simply continuing to read bytes back without issuing a STOP condition. Message reading should end when a report ID of 255 (“invalid message”) is received. Alternatively the host ends the transfer by sending a NACK after receiving the last byte of a message, followed by a STOP condition. If there is another message present, the $\overline{\text{CHG}}$ line goes low again, as in step 1. In this mode the state of the $\overline{\text{CHG}}$ line does not need to be checked during the I²C read.

In Mode 1 (level-triggered operation):

1. The $\overline{\text{CHG}}$ line goes low to indicate that a message is present.
2. The $\overline{\text{CHG}}$ line remains low while there are further messages to be sent after the current message.
3. The $\overline{\text{CHG}}$ line goes high again only once the first byte of the last message (that is, its report ID) has been sent and acknowledged (ACK sent) and the next byte has been prepared in the output buffer.

Mode 1 allows the host to continually read the messages until the $\overline{\text{CHG}}$ line goes high, and the state of the $\overline{\text{CHG}}$ line determines whether or not the host should continue receiving messages from the device.

NOTE	The state of the $\overline{\text{CHG}}$ line should be checked only between messages and not between the bytes of a message. The precise point at which the $\overline{\text{CHG}}$ line changes state cannot be predicted and so the state of the $\overline{\text{CHG}}$ line cannot be guaranteed between bytes.

The Communications Configuration T18 object can be used to configure the behavior of the $\overline{\text{CHG}}$ line. In addition to the $\overline{\text{CHG}}$ line operation modes described above, this object allows direct control over the state of the $\overline{\text{CHG}}$ line.

8.6 SDA and SCL

The I²C bus transmits data and clock with SDA and SCL, respectively. These are open-drain. The device can only drive these lines low or leave them open. The termination resistors (Rp) pull the line up to VddIO if no I²C device is pulling it down.

The termination resistors should be chosen so that the rise times on SDA and SCL meet the I²C specifications for the interface speed being used, bearing in mind other loads on the bus. For best latency performance, it is recommended that no other devices share the I²C bus with the maXTouch controller.

8.7 Clock Stretching

The device supports clock stretching in accordance with the I^2C specification. It may also instigate a clock stretch if a communications event happens during a period when the device is busy internally. The maximum clock stretch is 2 ms and typically less than 350 µs.

The device has an internal bus monitor that can reset the internal I^2C hardware if either SDA or SCL is stuck low for more than 200 ms. This means that if a prolonged clock stretch of more than 200 ms is seen by the device, then any ongoing transfers with the device may be corrupted.

The bus monitor is enabled or disabled using the Communications Configuration T18 object.

9.0 HID-I²C COMMUNICATIONS

The device is an HID-I²C device presenting two Top-level Collections (TLCs):

- **Generic HID-I²C** – Provides a generic HID-I²C interface that allows the host to communicate with the device using the object-based protocol (OBP).
- **Digitizer HID-I²C** – Supplies touch information to the host. This interface is supported by Microsoft Windows without the need for additional software.

See Section 7.0 “Host Communications” for information on selecting HID-I²C mode.

Other features are identical to standard I²C communication described in Section 8.0 “I2C Communications”.

Refer to the Microsoft HID-I²C documentation, *HID Over I²C Protocol Specification – Device Side*, for information on the HID-I²C specification.

9.1 I²C Addresses

See Section 8.1 “I2C Addresses”.

9.2 Device Specification

The device is compliant with HID-I²C specification V1.0. It has the specification shown in Table 9-1.

TABLE 9-1: DEVICE SPECIFICATION

Parameter	Value
Vendor ID	0x03EB (Microchip)
Product ID	0x2189 (mXT1066TD)
Version ID	A 16-bit number representing the firmware version and build number
HID Descriptor Address	0x0000

9.3 HID Descriptor

The host should read the HID descriptor on initialization to ascertain the key attribute of the HID device. These include the report description and the report ID to be used for communication with the HID device. The HID descriptor address is 0x0000.

Note that the host driver must not make any assumptions about the report packet formats, data locations or report IDs. These must be read from the HID descriptor as they may change in future versions of the firmware.

For more information on how to read the HID descriptor, refer to the Microsoft HID-I²C documentation.

9.4 HID-I²C Report IDs

Table 9-2 describes the HID-I²C report IDs used in reports sent to the host.

NOTE	The term HID-I²C report ID should not be confused with the term report Id as used in the Object Protocol; the two are entirely different concepts. Refer to the *mXT1066TD 1.0 Protocol Guide* for more information on the use of Object Protocol report IDs.

TABLE 9-2: HID-I²C REPORT IDS

Top-level Collection	Report ID	Description
Generic HID-I²C	0x06	Object Protocol (OBP) command and response (see Section 9.5 “Generic HID-I²C TLC”)

TABLE 9-2: HID-I²C REPORT IDS (CONTINUED)

Top-level Collection	Report ID	Description
Digitizer HID-I²C	0x01	Touch report (see Section 9.6.1 “Touch Report”)
	0x02	Maximum Touches (Surface Contacts) report (see Section 9.6.3 “Maximum Touches Report”)
	0x05	Touch Hardware Quality Assurance (THQA) report (see Section 9.6.4 “Touch Hardware Quality Assurance (THQA) Report”)

9.5 Generic HID-I²C TLC

The Generic HID-I²C TLC supports an input report for receiving data from the device and an output report for sending data to the device.

Commands are sent by the host using the output reports. Responses from the device are sent using input reports.

Supported commands are:

- Read/Write Memory Map
- Send Auto-return Messages

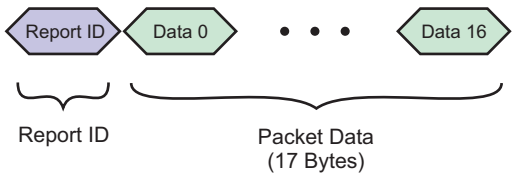
The HID-I²C report ID used is that for Object Protocol commands and responses; see Table 9-2 for the value.

9.5.1 READ/WRITE MEMORY MAP COMMAND

This command is used to carry out a write/read operation on the memory map of the device.

The data packet for a read/write command consists of 18 bytes, made up of a 1-byte HID-I²C report ID followed by 17 bytes of data (see Figure 9-1).

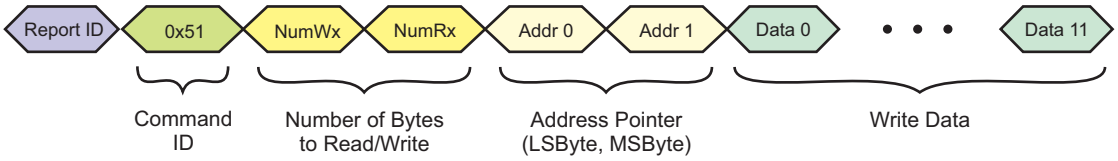
FIGURE 9-1: READ/WRITE MEMORY MAP – GENERIC PACKET FORMAT



9.5.1.1 Command and Response Packets

The command packet has the generic format given in Figure 9-2. The following sections give examples on using the command to write to the memory map and to read from the memory map.

FIGURE 9-2: READ/WRITE MEMORY MAP – COMMAND PACKET FORMAT



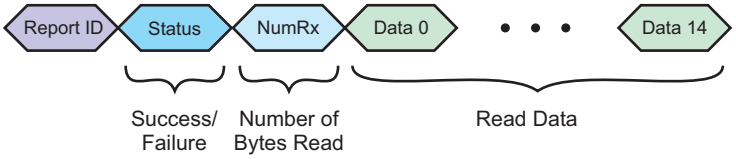
In Figure 9-2:

- **Rpt ID** is the HID-I²C report ID used for Object Protocol commands and responses (see Table 9-2).
- **Command ID** is the command ID for the write/read operation (0x51)
- **NumWx** is the number of data bytes to write to the memory map (may be zero). If the address pointer is being sent, this must include the size of the address pointer.
- **NumRx** is the number of data bytes to read from the memory map (may be zero).
- **Addr 0** and **Addr 1** form the address pointer to the memory map (where necessary; may be zero if not needed). This is typically an address of an object within the device.

- **Data 0** to **Data 11** are the bytes of data to be written (in the case of a write). Note that data locations beyond the number specified by NumWx will be ignored.

The response packet has the generic format given in Figure 9-3.

FIGURE 9-3: READ/WRITE MEMORY MAP – RESPONSE PACKET FORMAT



In Figure 9-3:

- **Rpt ID** is the HID-I^{2}C report ID used for Object Protocol commands and responses (see Table 9-2 on page 36).
- **Status** indicates the result of the command:
  - 0x00 = read and write completed; read data returned
  - 0x04 = write completed; no read data requested
- **NumRx** is the number of bytes following that have been read from the memory map (in the case of a read). This will be the same value as NumRx in the command packet.
- **Data 0** to **Data 14** are the data bytes read from the memory map.

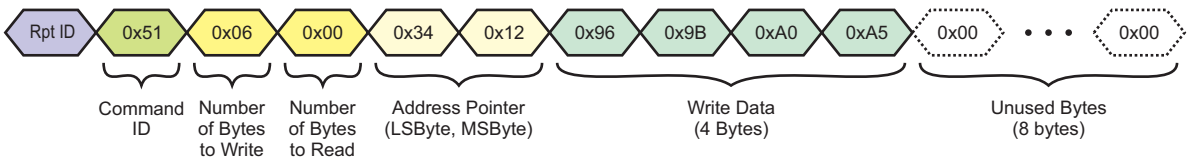
9.5.1.2 Writing To the Device

A write operation cycle to the device consists of sending a packet that contains six header bytes. These specify the HID-I^{2}C report ID, the Command ID, the number of bytes to read, the number of bytes to write, and the 16-bit address pointer.

Subsequent bytes in a multi-byte transfer form the actual data. These are written to the location of the address pointer, location of the address pointer +1, location of the address pointer + 2, and so on.

Figure 9-4 shows an example command packet to write four bytes of data to contiguous addresses starting at 0x1234.

FIGURE 9-4: EXAMPLE OF A FOUR-BYTE WRITE COMMAND STARTING AT ADDRESS 0x1234

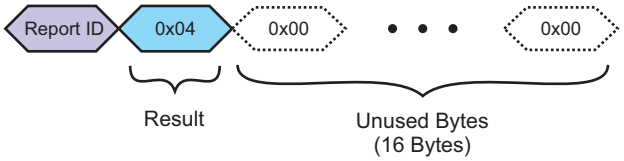


In Figure 9-4:

- **Rpt ID** is the HID-I^{2}C report ID used for Object Protocol commands and responses (see Table 9-2 on page 36).
- **Number of Bytes to Read** is set to zero as this is a write-only operation.
- **Number of Bytes to Write** is six (that is, four data bytes plus the two address pointer bytes).

Figure 9-5 shows the response to this command. In this case, the result status returned is 0x04 (that is, the write operation was completed but no read data was requested). Note that the report ID will be the same one used in the command packet.

FIGURE 9-5: RESPONSE TO EXAMPLE FOUR-BYTE WRITE

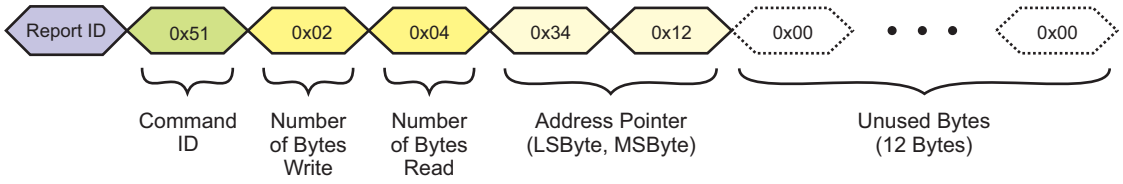


9.5.1.3 Reading From the Device

A read operation consists of sending a packet that contains the six header bytes only and no write data.

Figure 9-6 shows an example command packet to read four bytes starting at address 0x1234. Note that the address pointer is included in the number of bytes to write, so the number of bytes to write is set to 2 as there are no other data bytes to be written.

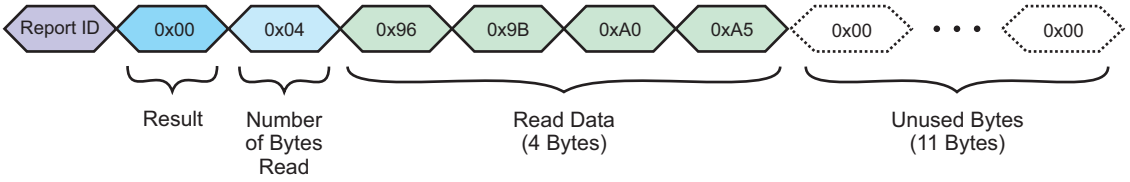
FIGURE 9-6: EXAMPLE OF A FOUR-BYTE READ COMMAND STARTING AT ADDRESS 0x1234



It is not necessary to set the address pointer before every read. The address pointer is updated automatically after every read operation, so the address pointer will be correct if the reads occur in order.

Figure 9-7 shows the response to this command. The result status returned is 0x00 (that is the write operation was completed and the data was returned). The number of bytes returned will be the same as the number requested (4 in this case).

FIGURE 9-7: RESPONSE TO EXAMPLE FOUR-BYTE READ

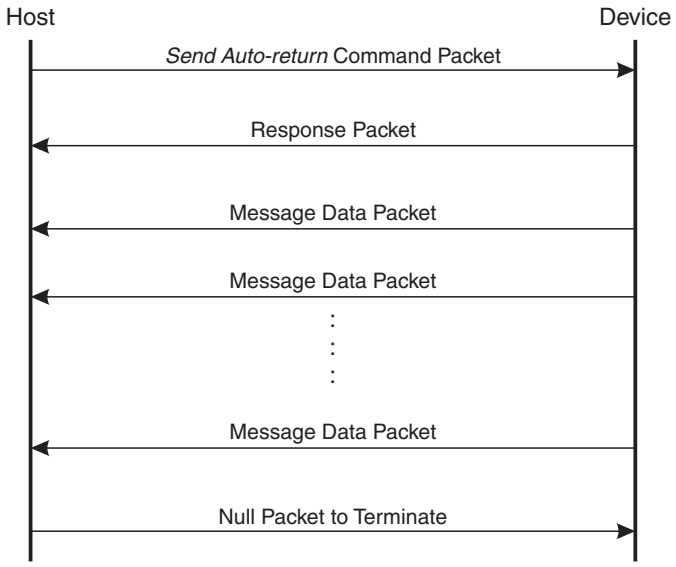


9.5.2 SEND AUTO-RETURN COMMAND

With this command the device can be configured to return new messages from the Message Processor T5 object autonomously.

The packet sequence to do this is shown in Figure 9-8.

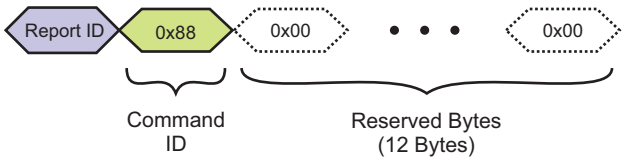
FIGURE 9-8: SEND AUTO-RETURN – PACKET SEQUENCE



The data packet for Send Auto-return commands consists of 14 bytes, made up of a 1-byte HID-I^{2}C report ID followed by 13 bytes of data. Note that this is different to the packet for standard read/write operations described in Section 9.5.1 “Read/Write Memory Map Command”.

The command packet has the format given in Figure 9-9.

FIGURE 9-9: SEND AUTO-RETURN – COMMAND PACKET FORMAT



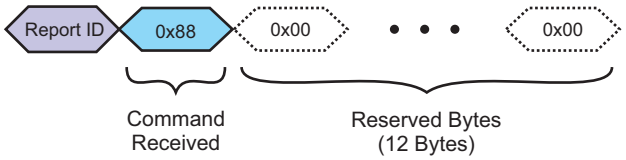
In Figure 9-9:

- **Rpt ID** is the HID-I^{2}C report ID used for Object Protocol commands and responses (see Table 9-2 on page 36).
- **Command ID** is the command ID for the Send Auto-return command (0x88)
- **Reserved Bytes** are reserved bytes with a value of 0x00.

Note that with this command, the command packet does not include an address pointer as the device already knows the address of the Message Processor T5 object.

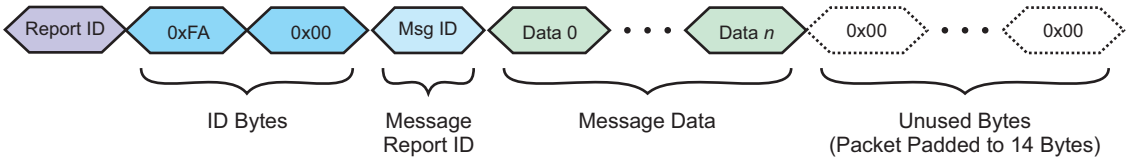
The response packet has the format given in Figure 9-10.

FIGURE 9-10: SEND AUTO-RETURN – RESPONSE PACKET FORMAT



Once the device has responded to the command, it starts sending message data. Each time a message is generated in the Message Processor T5 object, the device automatically sends a message packet to the host with the data. The message packets have the format given in Figure 9-11.

FIGURE 9-11: SEND AUTO-RETURN – MESSAGE PACKET FORMAT

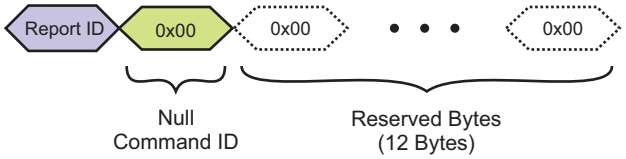


In Figure 9-11:

- **Rpt ID** is the HID-I^{2}C report ID used for Object Protocol commands and responses (see Table 9-2 on page 36).
- **ID Bytes** identify the packet as an auto-return message packet.
- **Message Report ID** is the report ID returned by the Message Processor T5 object. Note that this is the report ID used in the Object Protocol and should not be confused with the HID-I^{2}C report ID. Refer to the *mXT1066TD 1.0 Protocol Guide* for more information on the use of Object Protocol report IDs.
- **Message Data** bytes are the bytes of data returned by the Message Processor T5 object. The size of the data depends on the source object for which this is the message data. Any unused bytes are padded with zeros. Refer to the *mXT1066TD 1.0 Protocol Guide* for more information on the messages from the various objects.

To stop the sending of the messages, the host can send a null command packet. This consists of two bytes: the HID-I^{2}C report ID for Object Protocol commands and responses (see Table 9-2 on page 36) and a null command byte of 0x00 (see Figure 9-12).

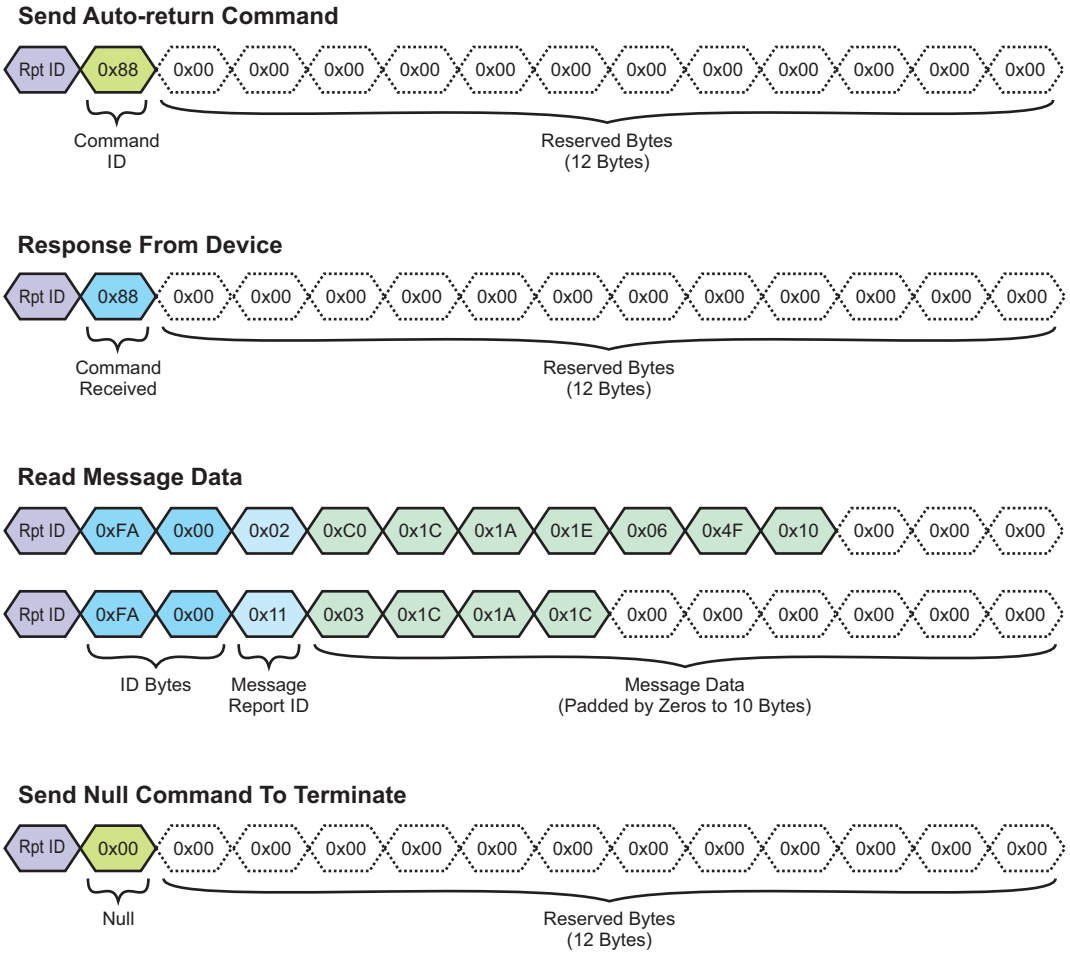
FIGURE 9-12: SEND AUTO-RETURN – NULL COMMAND PACKET FORMAT



Note that any standard read or write operation will also terminate any currently enabled auto-return mode (see Section 9.5.1 “Read/Write Memory Map Command”).

Figure 9-13 shows an example sequence of packets to receive messages from the Message Processor T5 object using the Send Auto-return command.

FIGURE 9-13: SEND AUTO-RETURN – EXAMPLE SEQUENCE



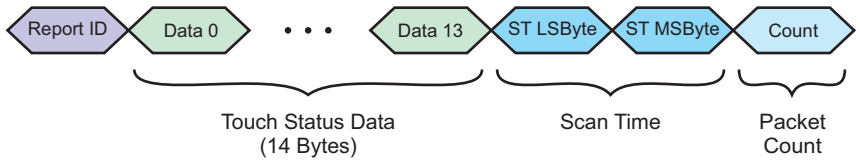
9.6 Digitizer HID-I²C

This is a digitizer class HID.

9.6.1 TOUCH REPORT

The format of a Touch report is shown in Figure 9.6.2. Each Touch report is 18 bytes long and contains the data for one touch.

9.6.2 TOUCH REPORT PACKET FORMAT

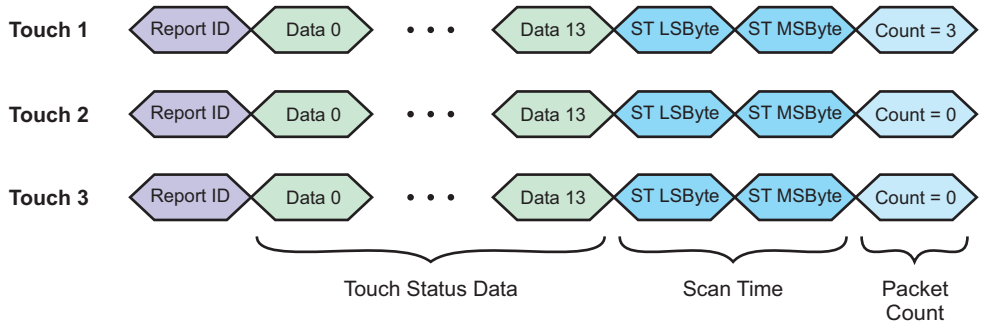


In Figure 9.6.2:

- **Rpt ID** is the HID-I²C report ID used for Touch reports (see Table 9-2 on page 36).
- **Touch** is the data for the touch.
- **Scan Time** is the Timestamp for the report packet
- **Count** is used to identify the report packets for current active touches that are to be reported as a single package. The Count in the first packet for the first touch is set to the number of active touches to be sent in one package (that is, the number of packets). Subsequent packets for subsequent active touches have a Count of 0.

An example of the Touch report packets for 3 active touches is shown in Figure 9-14.

FIGURE 9-14: EXAMPLE TOUCH REPORT PACKETS FOR 3 ACTIVE TOUCHES



Each input report consists of a HID-I²C report ID followed by 17 bytes that describe the status of one active touch. The input report format depends on the geometry calculation control (TCHGEOMEN) of the Digitizer HID Configuration T43 object. Table 9-3 and Table 9-4 give the detailed format of a touch report packet.

TABLE 9-3: TOUCH REPORT FORMAT WHEN TCHGEOMEN = 1

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	HID-I²C Touch Report ID							
1	Reserved							Status
2	Touch ID							
3	Touch X Position LSByte (first touch)							
4	Reserved				Touch X Position MSBits (first touch)			
5	Touch Center X Position LSByte (first touch)							
6	Reserved				Touch Center X Position MSBits (first touch)			
7	Touch Y Position LSByte (first touch)							
8	Reserved				Touch Y Position MSBits (first touch)			
9	Touch Center Y Position LSByte (first touch)							
10	Reserved				Touch Center Y Position MSBits (first touch)			

TABLE 9-3: TOUCH REPORT FORMAT WHEN TCHGEOMEN = 1 (CONTINUED)

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
11	Touch Width							
12	Reserved							
13	Touch Height							
14	Reserved							
15	Scan Time LSByte							
16	Scan Time MSByte							
17	Packet Count							

TABLE 9-4: TOUCH REPORT FORMAT WHEN TCHGEOMEN = 0

Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	HID-I^{2}C Touch Report ID							
1	Reserved							Status
2	Touch ID							
3	Touch X Position LSByte (first touch)							
4	Reserved				Touch X Position MSBits (first touch)			
5	Reserved							
6	Reserved							
7	Touch Y Position LSByte (first touch)							
8	Reserved				Touch Y Position MSBits (first touch)			
9	Reserved							
10	Reserved							
11	Reserved							
12	Reserved							
13	Reserved							
14	Reserved							
15	Scan Time LSByte							
16	Scan Time MSByte							
17	Packet Count							

- Byte 0:
  The HID-I^{2}C report ID (see Table 9-2 on page 36 for Touch reports).
- Byte 1:
  Status is the status of the touch detection. This bit is set to 1 if touch is detected, and set to 0, if no touches are detected.
- Byte 2:
  Touch ID identifies the touch for which this is a status report (starting from 0).
- Bytes 3 to 10:
  X and Y positions identify the touch position. These are scaled to 12-bit resolution. This means that the upper four bits of the MSByte will always be zero. Bytes 5, 6, 9 and 10 are reserved when TCHGEOMEN field is set to 0.
- Byte 11:
  Touch Width reports the width of the detected touch when TCHGEOMEN is set to 1.
  Reserved when TCHGEOMEN is set to 0
- Byte 13:
  Touch Height reports the height of the detected touch when TCHGEOMEN is set to 1.
  Reserved when TCHGEOMEN is set to 0
- Byte 15 to 16:
  Scan Time is the timestamp associated with the current report packet (10 kHz resolution).
- Byte 17:
  Count is the number of active touches to be sent in one package, for the first touch only. Subsequent packets for subsequent active touches have a Count of 0.

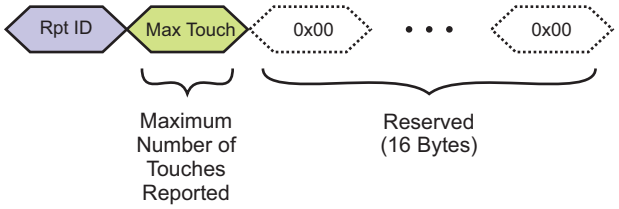
9.6.3 MAXIMUM TOUCHES REPORT

Read this report to receive the maximum number of touches (surface contacts) that can currently be reported.

Write this report to set the maximum number of touches to be reported.

The format of the Maximum Touches report packet is shown in Figure 9-15. Each Maximum Touch report is 18 bytes long and contains a single byte giving the maximum number of touches to be reported.

FIGURE 9-15: MAXIMUM TOUCHES REPORT FORMAT



In Figure 9-15:

- **Rpt ID** is the HID-I^{2}C report ID used for Maximum Touches reports (see Table 9-2 on page 36).
- **Max Touch** is the maximum number of touches to be reported by the device.

NOTE	The number of touches cannot be set to more than the maximum number of touches configured in the device by the Multiple Touch Touchscreen T100 object.

9.6.4 TOUCH HARDWARE QUALITY ASSURANCE (THQA) REPORT

The THQA data is reported to Microsoft Windows using the THQA report ID (see Table 9-2 on page 36 for the value). The content of this data is defined by Microsoft.

9.7 $\overline{\text{CHG}}$ Line

The $\overline{\text{CHG}}$ line is used to implement the HID-I^{2}C interrupt line. It provides a level triggered interrupt to the host to indicate when there is one or more reports to be read. The $\overline{\text{CHG}}$ line will be pulled low when a report is ready and will remain low as long as there are further reports to be read. Once the last report is read the $\overline{\text{CHG}}$ line will go high.

NOTE	In order to comply with the HID-I^{2}C specification, Communications Configuration T18 MODE should be set to 0.

9.8 SDA, SCL

Identical to standard I^{2}C operation. See Section 8.6 “SDA and SCL”.

9.9 Clock Stretching

Identical to standard I^{2}C operation. See Section 8.7 “Clock Stretching”.

9.10 Power Control

The mXT1066TD supports the use of the HID-I^{2}C *SET POWER* commands to put the device into a low power state

9.11 Microsoft Windows Compliance

The mXT1066TD has algorithms within the Multiple Touch Touchscreen T100 object specifically to ensure compliance with Microsoft Windows 8.x and later versions.

The device also supports Microsoft Touch Hardware Quality Assurance (THQA) in the Serial Data Command T68 object. Refer to the Microsoft whitepaper *How to Design and Test Multitouch Hardware Solutions for Windows 8*.

These, and other device features, may need specific tuning.

10.0 PCB DESIGN CONSIDERATIONS

10.1 Introduction

The following sections give the design considerations that should be adhered to when designing a PCB layout for use with the mXT1066TD. Of these, power supply and ground tracking considerations are the most critical.

By observing the following design rules, and with careful preparation for the PCB layout exercise, designers will be assured of a far better chance of success and a correctly functioning product.

10.2 Printed Circuit Board

Microchip recommends the use of a four-layer printed circuit board for mXT1066TD applications. This, together with careful layout, will ensure that the board meets relevant EMC requirements for both noise radiation and susceptibility, as laid down by the various national and international standards agencies.

10.2.1 PCB CLEANLINESS

Modern no-clean-flux is generally compatible with capacitive sensing circuits.

CAUTION!	If a PCB is reworked to correct soldering faults relating to any device, or to any associated traces or components, be sure that you fully understand the nature of the flux used during the rework process. Leakage currents from hygroscopic ionic residues can stop capacitive sensors from functioning. If you have any doubts, a thorough cleaning after rework may be the only safe option.

10.3 Power Supply

10.3.1 SUPPLY QUALITY

While the device has good Power Supply Rejection Ratio properties, poorly regulated and/or noisy power supplies can significantly reduce performance.

Particular care should be taken of the AVdd supply, as it supplies the sensitive analog stages in the device.

10.3.2 SUPPLY RAILS AND GROUND TRACKING

Power supply and clock distribution are the most critical parts of any board layout. Because of this, it is advisable that these be completed before any other tracking is undertaken. After these, supply decoupling, and analog and high speed digital signals should be addressed. Track widths for all signals, especially power rails should be kept as wide as possible in order to reduce inductance.

The Power and Ground planes themselves can form a useful capacitor. Flood filling for either or both of these supply rails, therefore, should be used where possible. It is important to ensure that there are no floating copper areas remaining on the board: all such areas should be connected to the ground plane. The flood filling should be done on the outside layers of the board.

10.3.3 POWER SUPPLY DECOUPLING

Decoupling capacitors should be fitted as specified in Section 2.3 “Schematic Notes”.

The decoupling capacitors must be placed as close as possible to the pin being decoupled. The traces from these capacitors to the respective device pins should be wide and take a straight route. They should be routed over a ground plane as much as possible. The capacitor ground pins should also be connected directly to a ground plane.

Surface mounting capacitors are preferred over wire-leaded types due to their lower ESR and ESL. It is often possible to fit these decoupling capacitors underneath and on the opposite side of the PCB to the digital ICs. This will provide the shortest tracking, and most effective decoupling possible.

10.3.4 VOLTAGE PUMP

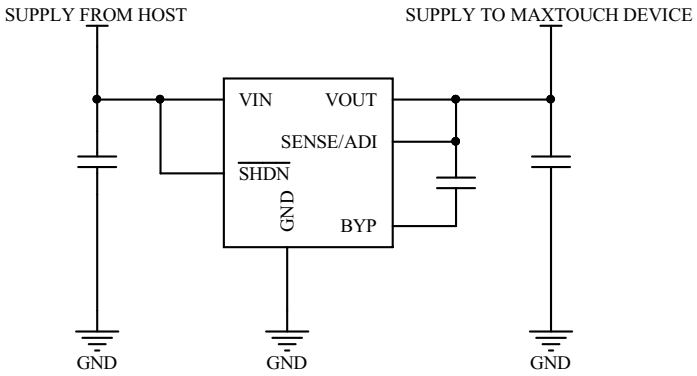
The traces for the voltage pump capacitors between EXTCAP2 and EXTCAP3 and between EXTCAP0 and EXTCAP1 (Cd and Ct on the schematic in Section 2.0 “Schematics”) should be kept as short and as wide as possible for best pump performance. They should also be routed as parallel and as close as possible to each other in order to reduce emissions, and ideally the traces should be the same length.

10.3.5 VOLTAGE REGULATORS

Each supply rail requires a Low Drop-Out (LDO) voltage regulator, although an LDO can be shared where supply rails share the same voltage level.

Figure 10-1 shows an example circuit for an LDO.

FIGURE 10-1: EXAMPLE LDO CIRCUIT



An LDO regulator should be chosen that provides adequate output capability, low noise, no-load stability, good load regulation and step response. The mXT1066TD has been qualified for use only with the Microchip LDOs listed in Table 10-1. However, some alternative LDOs with similar specifications are listed in Table 10-2. Microchip has not tested this maXTouch controller with any of these alternative LDOs. Microchip cannot guarantee the functionality or performance of this maXTouch controller with these or any other LDO besides those listed in Table 10-1.

NOTE	Microchip recommends that a minimum of a 1.0 µF ceramic, low ESR capacitor at the input and output of these devices is always used. The datasheet for the device should always be referred to when selecting capacitors and the typical recommended values, types and dielectrics adhered to.

TABLE 10-1: LDO REGULATORS – QUALIFIED FOR USE

Manufacturer	Device	Current Rating (mA)
Microchip Technology Inc.	MCP1824	300
Microchip Technology Inc.	MCP1824S	300
Microchip Technology Inc.	MAQ5300	300
Microchip Technology Inc.	MCP5504	300
Microchip Technology Inc.	MCP1725	500
Microchip Technology Inc.	MIC5514	300
Microchip Technology Inc.	MIC5323	300

TABLE 10-2: LDO REGULATORS – OTHER DEVICES

Manufacturer	Device	Current Rating (mA)
Analog Devices	ADP122/ADP123	300
Diodes Inc.	AP2125	300
Diodes Inc.	AP7335	300
Linear Technology	LT1763CS8-3.3	500
NXP	LD6836	300
Texas Instruments	LP3981	300

10.3.6 SINGLE SUPPLY OPERATION

When designing a PCB for an application using a single LDO, extra care should be taken to ensure short, low inductance traces between the supply and the touch controller supply input pins. Ideally, tracking for the individual supplies should be arranged in a star configuration, with the LDO at the junction of the star. This will ensure that supply current variations or noise in one supply rail will have minimum effect on the other supplies. In applications where a ground plane is not practical, this same star layout should also apply to the power supply ground returns.

Only regulators with a 300 mA or greater rating can be used in a single-supply design.

Refer to the following application note for more information:

- Application Note: MXTAN0208 – *Design Guide for PCB Layouts for maXTouch Touch Controllers*

10.3.7 MULTIPLE VOLTAGE REGULATOR SUPPLY

The AVdd supply stability is critical for the device because this supply interacts directly with the analog front end. If noise problems exist when using a single LDO regulator, Microchip recommends that AVdd is supplied by a regulator that is separate from the digital supply. This reduces the amount of noise injected into the sensitive, low signal level parts of the design.

10.4 Driven Shield Line

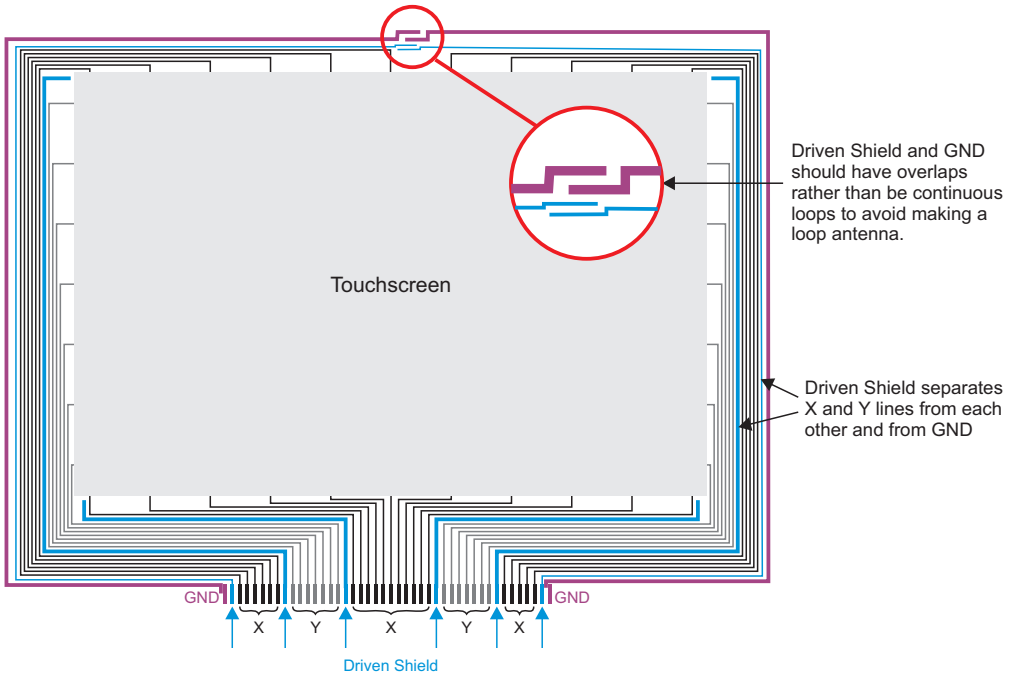
The driven shield line is used to provide a guard track around the touchscreen panel that serves as Ground in mutual capacitance operation and as a driven shield in self capacitance operation.

The guard track must be routed between the X and Y tracks, as well as between the X/Y tracks and Ground. It should be fairly wide to avoid X-to-Y coupling in mutual capacitance operation, as the guard track will act as Ground in this circumstance.

A guard track is also needed between any self capacitance X/Y lines and mutual capacitance only X/Y lines.

NOTE	DS0 is internally multiplexed to X31. X31 must be configured for use if DS0 is to be used (either as a driven shield for self capacitance measurements or as a Ground guard track in a mutual capacitance only design), otherwise DS0 cannot be used in the user's design.

FIGURE 10-2: EXAMPLE DRIVEN SHIELD ROUTING



NOTE: Sample touchscreen for illustrative purposes only. The number of X/Y lines available on any given device might differ from that shown here. Similarly, the routing of the X/Y lines shown should not be taken as indicative of any preferred layout and the user's layout may vary.

10.5 ESD Ground Routing

To avoid damage due to ESD strikes, the outermost track on the sensor should be an ESD ground (see Figure 10-2). Like the driven shield, this should completely surround the sensor but with an overlap at the top rather than forming a complete loop.

To avoid electromagnetic induction of currents into the driven shield trace, a minimum separation of 0.3 mm should be maintained between the ESD GND trace and the Driven Shield.

The ESD ground traces should be connected to a dedicated ground trace in the PCB, and routed such that ESD strike currents do not flow under or close to the touch controller or the connecting wiring between it and the touchscreen array. The ESD ground should be connected in to the main system ground at a star point at the main GND connection to the PCB.

See also:

- MXTAN0208 – *Design guide for PCB Layouts for maXTouch Touch Controllers*

10.6 Analog I/O

In general, tracking for the analog I/O signals from the device should be kept as short as possible. These normally go to a connector which interfaces directly to the touchscreen.

Ensure that adequate ground-planes are used. An analog ground plane should be used in addition to a digital one. Care should be taken to ensure that both ground planes are kept separate and are connected together only at the point of entry for the power to the PCB. This is usually at the input connector.

10.7 Component Placement and Tracking

It is important to orient all devices so that the tracking for important signals (such as power and clocks) are kept as short as possible.

10.7.1 DIGITAL SIGNALS

In general, when tracking digital signals, it is advisable to avoid sharp directional changes on sensitive signal tracks (such as analog I/O) and any clock or crystal tracking.

A good ground return path for all signals should be provided, where possible, to ensure that there are no discontinuities.

10.8 EMC and Other Observations

The following recommendations are not mandatory, but may help in situations where particularly difficult EMC or other problems are present:

- Try to keep as many signals as possible on the inside layers of the board. If suitable ground flood fills are used on the top and bottom layers, these will provide a good level of screening for noisy signals, both into and out of the PCB.
- Ensure that the on-board regulators have sufficient tracking around and underneath the devices to act as a heatsink. This heatsink will normally be connected to the 0 V or ground supply pin. Increasing the width of the copper tracking to any of the device pins will aid in removing heat. There should be no solder mask over the copper track underneath the body of the regulators.
- Ensure that the decoupling capacitors, especially high capacity ceramic type, have the requisite low ESR, ESL and good stability/temperature properties. Refer to the regulator manufacturer’s datasheet for more information.

11.0 GETTING STARTED WITH MXT1066TD

11.1 Establishing Contact

11.1.1 COMMUNICATION WITH THE HOST

The host can use any of the following interfaces to communicate with the device (See Section 7.0 “Host Communications”):

- I^2C interface (see Section 8.0 “I2C Communications”)
- HID-I^2C interface (see Section 9.0 “HID-I^2C Communications”)

11.1.2 POWER-UP SEQUENCE

The power-up sequence is as follows:

1. On power-up, the $\overline{\text{CHG}}$ line goes low to indicate that there is new data to be read from the device. If the $\overline{\text{CHG}}$ line does not go low within a suitable timeout (for example, 300 ms), there is a problem with the device.
2. Once the $\overline{\text{CHG}}$ line goes low, the host should attempt to read the first 7 bytes of memory from location 0x0000 to establish that the device is present and running following power-up. These bytes represent the ID Information portion of the Information Block and should be recorded by the host so it can read the Object Table (see Section 11.2 “Using the Object Protocol”).
3. The device performs a checksum on the configuration settings held in the non-volatile memory. If the checksum does not match a stored copy of the last checksum, then this indicates that the settings have become corrupted. The host should write a correct configuration to the device, and issue a Command Processor T6 Backup command, if the read checksum does not match the expected checksum, or if the configuration error bit in the message data from the Command Processor T6 object is set.

Once the device has been initialized, the host must perform the following initialization so that it can communicate with the device:

1. Read the start positions of all the objects in the device from the Object Table and build up a list of these addresses. Note that the number of elements was read by the host at start-up as part of the ID Information bytes.
2. Use the Object Table to calculate the report IDs so that messages from the device can be correctly interpreted.
3. Read any pending messages generated during the start-up process.

Refer to Application Note MXTAN0213, *Interfacing with maXTouch Touchscreen Controllers*, for more information.

11.2 Using the Object Protocol

The device has an object-based protocol that is used to communicate with the device. Typical communication includes configuring the device, sending commands to the device, and receiving messages from the device.

11.2.1 CLASSES OF OBJECTS

The mXT1066TD contains the following classes of objects:

- **Debug objects** – provide a raw data output method for development and testing.
- **General objects** – required for global configuration, transmitting messages and receiving commands.
- **Touch objects** – operate on measured signals from the touch sensor and report touch data.
- **Signal processing objects** – process data from other objects (typically signal filtering operations).
- **Support objects** – provide additional functionality on the device.

11.2.2 OBJECT INSTANCES

TABLE 11-1: OBJECTS ON THE MXT1066TD

Object	Description	Number of Instances	Usage
Debug Objects			
Diagnostic Debug T37	Allows access to diagnostic debug data to aid development.	1	Debug commands only; Read-only object. No configuration or tuning necessary. Not for use in production.

TABLE 11-1: OBJECTS ON THE MXT1066TD (CONTINUED)

Object	Description	Number of Instances	Usage
General Objects			
Message Processor T5	Handles the transmission of messages. This object holds a message in its memory space for the host to read.	1	No configuration necessary.
Command Processor T6	Performs a command when written to. Commands include reset, calibrate and backup settings.	1	No configuration necessary.
Power Configuration T7	Controls the sleep mode of the device. Power consumption can be lowered by controlling the acquisition frequency and the sleep time between acquisitions.	1	Must be configured before use.
Acquisition Configuration T8	Controls how the device takes each capacitive measurement.	1	Must be configured before use.
Touch Objects			
Multiple Touch Touchscreen T100	Creates a Touchscreen that supports the tracking of more than one touch.	1	Enable and configure as required.
Signal Processing Objects			
Grip Suppression T40	Suppresses false detections caused, for example, by the user gripping the edge of a touchscreen.	1	Enable and configure as required.
Touch Suppression T42	Suppresses false detections caused by unintentional large touches by the user.	1	Enable and configure as required.
Passive Stylus T47	Processes passive stylus input.	1	Enable and configure as required.
Shieldless T56	Allows a sensor to use true single-layer co-planar construction.	1	Enable and configure as required.
Lens Bending T65	Compensates for lens deformation (lens bending) by attempting to eliminate the disturbance signal from the reported deltas.	3	Enable and configure as required.
Noise Suppression T72	Performs various noise reduction techniques during sensor signal acquisition.	1	Enable and configure as required.
Glove Detection T78	Allows for the reporting of glove touches.	1	Enable and configure as required.
Retransmission Compensation T80	Limits the negative effects on touch signals caused by poor device coupling to ground or moisture on the sensor.	1	Enable and configure as required.
Self Capacitance Noise Suppression T108	Suppresses the effects of external noise within the context of self capacitance touch measurements.	1	Enable and configure as required.
Self Capacitance Grip Suppression T112	Allows touches to be reported from the self capacitance measurements while the device is being gripped.	1	Enable and configure as required.
Support Objects			
Communications Configuration T18	Configures additional communications behavior for the device.	1	Check and configure as necessary.
GPIO Configuration T19	Allows the host controller to configure and use the general purpose I/O pins on the device.	1	Enable and configure as required.
Self Test T25	Configures and performs self-test routines to find faults on a touch sensor.	1	Enable and configure as required.

TABLE 11-1: OBJECTS ON THE MXT1066TD (CONTINUED)

Object	Description	Number of Instances	Usage
User Data T38	Provides a data storage area for user data.	1	Configure as required.
Digitizer HID Configuration T43	Configures the Digitizer HID interface and the Descriptors associated with it.	1	Enable and configure as required.
Message Count T44	Provides a count of pending messages.	1	Read-only object.
CTE Configuration T46	Controls the capacitive touch engine for the device.	1	Must be configured.
Timer T61	Provides control of a timer.	6	Enable and configure as required.
Serial Data Command T68	Provides an interface for the host driver to deliver various data sets to the device.	1	Enable and configure as required.
Dynamic Configuration Controller T70	Allows rules to be defined that respond to system events.	20	Enable and configure as required.
Dynamic Configuration Container T71	Allows the storage of user configuration on the device that can be selected at runtime based on rules defined in the Dynamic Configuration Controller T70 object.	1	Configure if Dynamic Configuration Controller T70 is in use.
Auxiliary Touch Configuration T104	Allows the setting of self capacitance gain and thresholds for a particular measurement to generate auxiliary touch data for use by other objects.	1	Enable and configure if using self capacitance measurements
Self Capacitance Global Configuration T109	Provides configuration for self capacitance measurements employed on the device.	1	Check and configure as required (if using self capacitance measurements).
Self Capacitance Tuning Parameters T110	Provides configuration space for a generic set of settings for self capacitance measurements.	6	Use under the guidance of Microchip field engineers only.
Self Capacitance Configuration T111	Provides configuration for self capacitance measurements employed on the device.	2	Check and configure as required (if using self capacitance measurements).
Self Capacitance Measurement Configuration T113	Configures self capacitance measurements to generate data for use by other objects.	1	Enable and configure as required.

11.2.3 CONFIGURING AND TUNING THE DEVICE

The objects are designed such that a default value of zero in their fields is a “safe” value that typically disables functionality. The objects must be configured before use and the settings written to the non-volatile memory using the Command Processor T6 object.

Perform the following actions for each object:

1. Enable the object, if the object requires it.
2. Configure the fields in the object, as required.
3. Enable reporting, if the object supports messages, to receive messages from the object.

11.3 Writing to the Device

The following mechanisms can be used to write to the device:

- Using an I^2C write operation (see Section 8.2 “Writing To the Device”).
- Using the Generic HID-I^2C write operation (see Section 9.5.1.2 “Writing To the Device”).

Communication with the device is achieved by writing to the appropriate object:

- To send a command to the device, an appropriate command is written to the Command Processor T6 object.

- To configure the device, a configuration parameter is written to the appropriate object. For example, writing to the Power Configuration T7 configures the power consumption for the device and writing to the Multiple Touch Touchscreen T100 object sets up the touchscreen. Some objects are optional and need to be enabled before use.

IMPORTANT!	When the host issues any command within an object that results in a flash write to the device Non-Volatile Memory (NVM), that object should have its CTRL RPTEN bit set to 1, if it has one. This ensures that a message from the object writing to the NVM is generated at the completion of the process and an assertion of the $\overline{\text{CHG}}$ line is executed. The host must also ensure that the assertion of the $\overline{\text{CHG}}$ line refers to the expected object report ID before asserting the $\overline{\text{RESET}}$ line to perform a reset. Failure to follow this guidance may result in a corruption of device configuration area and the generation of a CFGERR.

11.4 Reading from the Device

Status information is stored in the Message Processor T5 object. This object can be read to receive any status information from the device.

The following mechanisms provide an interrupt-style interface for reading messages in the Message Processor T5 object:

- In I^2C mode, the $\overline{\text{CHG}}$ line is asserted whenever a new message is available in the Message Processor T5 object (see Section 8.5 “CHG Line”). See Section 8.4 “Reading From the Device” for information on the format of the I^2C read operation.
- When using the HID-I^2C interface, the interface provides an interrupt-driven interface that sends the messages automatically (see Section 9.5.1.3 “Reading From the Device”)

NOTE	The host should always wait to be notified of messages; the host should not poll the device for messages (either by polling the Message Processor T5 object or by polling the $\overline{\text{CHG}}$ line).

12.0 DEBUGGING AND TUNING

12.1 SPI Debug Interface

The SPI Debug Interface is used for tuning and debugging when running the system and allows the development engineer to use Microchip maXTouch Studio to read the real-time raw data. This uses the low-level debug port.

The SPI Debug Interface consists of the $\overline{\text{DBG\_SS}}$, DBG_CLK, and DBG_DATA lines. These lines should be routed to test points on all designs such that they can be connected to external hardware during system development. These lines should not be connected to power or GND. See Section 2.3.10 “SPI Debug Interface” for more details.

The SPI Debug Interface is enabled by the Command Processor T6 object and by default will be off.

NOTE	When the $\overline{\text{DBG\_SS}}$, DBG_CLK, and DBG_DATA lines are in use for debugging, any alternative function for the pins cannot be used. The touch controller will take care of the pin configuration.

12.2 Object-based Protocol

The device provides a mechanism for obtaining debug data for development and testing purposes by reading data from the Diagnostic Debug T37 object.

NOTE	The Diagnostic Debug T37 object is of most use for simple tuning purposes. When debugging a design, it is preferable to use the SPI Debug Interface, as this will have a much higher bandwidth and can provide real-time data.

12.3 Self Test

There is a Self Test T25 object that runs self-test routines in the device to find hardware faults on the sense lines and the electrodes. This object also performs an initial pin fault test on power-up to ensure that there is no pin short (X to Y, or X lines to power or GND) before the high-voltage supply is enabled inside the chip. A high-voltage short on the sense lines could damage the device.

In addition to one-off hardware tests, the Self Test T25 object can also provide continuous monitoring of the health of the device while it is in operation. A periodic test can be run at a user-specified interval and reports pass and/or fail messages (as determined by the device configuration). Reporting is achieved either by standard Self Test T25 object protocol messages or by a configurable hardware GPIO pin, configured using the GPIO Configuration T19 object.

13.0 SPECIFICATIONS

13.1 Absolute Maximum Specifications

Vdd	3.6V
VddIO	3.6V
AVdd	3.6V
Maximum continuous combined pin current, all GPIO*n* pins	60 mA
Voltage forced onto any pin	–0.3 V to Vdd/VddIO/AVdd + 0.3 V
Configuration parameters maximum writes	10,000
Maximum junction temperature	125°C

CAUTION! Stresses beyond those listed under *Absolute Maximum Specifications* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum specification conditions for extended periods may affect device reliability.

13.2 Recommended Operating Conditions

Operating temperature	–40°C to +85°C
Storage temperature	–60°C to +150°C
Vdd	3.3 V ±5%
VddIO	1.8 V to 3.3 V ±5%
AVdd	3.3 V ±5%
XVdd with internal voltage doubler	2 × Vdd
XVdd with internal voltage tripler	3 × Vdd
Temperature slew rate	10°C/min

13.2.1 DC CHARACTERISTICS

13.2.1.1 Analog Voltage Supply – AVdd

Parameter	Min	Typ	Max	Units	Notes
AVdd					
Operating limits	2.7	3.3	3.6	V	
Supply Rise Rate	–	–	0.036	V/µs	For example, for a 3.3 V rail, the voltage should take a minimum of 92 µs to rise

13.2.1.2 Digital Voltage Supply – VddIO, Vdd

Parameter	Min	Typ	Max	Units	Notes
VddIO					
Operating limits – Normal Voltage	2.97	3.3	3.6	V	
Operating limits – Low Voltage	1.62	1.8	1.98	V	
Supply Rise Rate	–	–	0.036	V/µs	For example, for a 3.3 V rail, the voltage should take a minimum of 92 µs to rise
Vdd					
Operating limits	3.0	3.3	3.47	V	
Supply Rise Rate	–	–	0.036	V/µs	For example, for a 3.3 V rail, the voltage should take a minimum of 92 µs to rise
Supply Fall Rate	–	–	0.05	V/µs	For example, for a 3.3 V rail, the voltage should take a minimum of 66 µs to fall

13.2.1.3 XVdd Voltage Supply – XVdd

Parameter	Min	Typ	Max	Units	Notes
XVdd					
Operating limits – voltage doubler enabled	–	2 × Vdd	–	V	
Operating limits – voltage tripler enabled	–	3 × Vdd	–	V	

13.2.2 POWER SUPPLY RIPPLE AND NOISE

Parameter	Min	Typ	Max	Units	Notes
Vdd	–	–	±50	mV	Across frequency range 1 Hz to 1 MHz
AVdd	–	–	±40	mV	Across frequency range 1 Hz to 1 MHz, with Noise Suppression enabled

13.3 Test Configuration

The configuration values listed below were used in the reference unit to validate the interfaces and derive the characterization data provided in the following sections.

TABLE 13-1: TEST CONFIGURATION

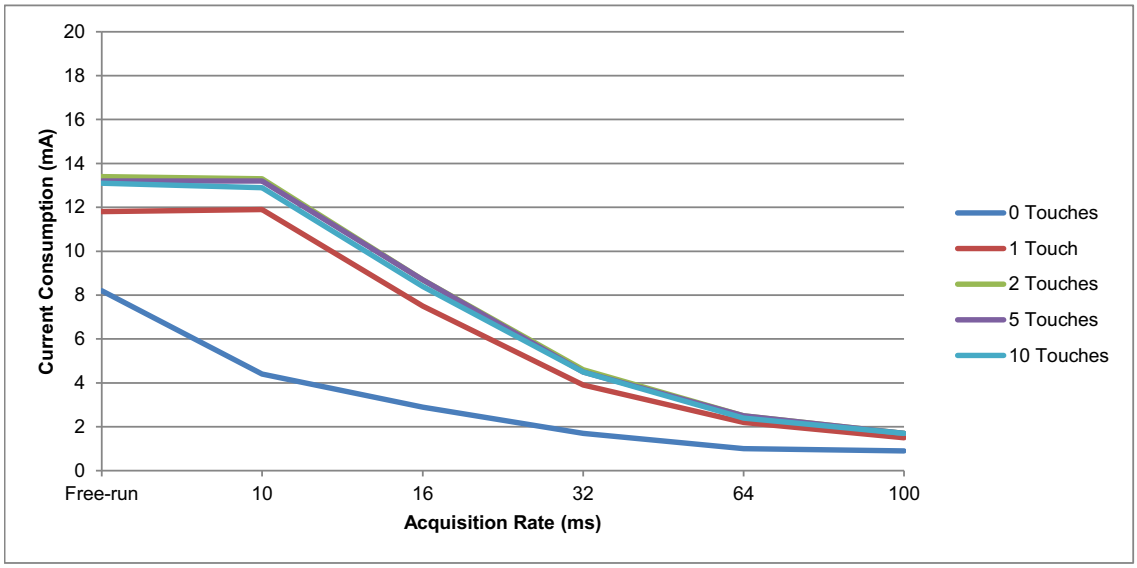
Object/Parameter	Description/Setting (Numbers in Decimal)
Power Configuration T7	
CFG2 DISPOWMON	0 (Power Monitor Enabled)
Acquisition Configuration T8	
CHRGTIME	38
MEASALLOW	11
Self Test T25	Object Enabled
CTE Configuration T46	Object Enabled
IDLESYNCSPERX	16
ACTVSYNCSPERX	16
Shieldless T56	Object Enabled
INTTIME	20
Lens Bending T65 Instance 0	Object Instance Enabled
Lens Bending T65 Instance 1	Object Instance Enabled
Lens Bending T65 Instance 2	Object Instance Enabled
Noise Suppression T72	Object Enabled
Glove Detection T78	Object Enabled
Retransmission Compensation T80	Object Enabled
Multiple Touch Touchscreen T100	Object Enabled
XSIZE	41
YSIZE	26
Auxiliary Touch Configuration T104	Object Enabled
Self Capacitance Noise Suppression T108	Object Enabled
Self Capacitance Configuration T111 Instance 0	
INTTIME	70
IDLESYNCSPERL	24
ACTVSYNCSPERL	24
Self Capacitance Configuration T111 Instance 1	
INTTIME	70
IDLESYNCSPERL	32
ACTVSYNCSPERL	32

13.4 Current Consumption

NOTE The characterization charts show typical values based on the configuration in Table 13-1. Actual power consumption in the user's application will depend on the circumstances of that particular project and will vary from that shown here. Further tuning will be required to achieve an optimal performance.

13.4.1 AVDD 3.3V

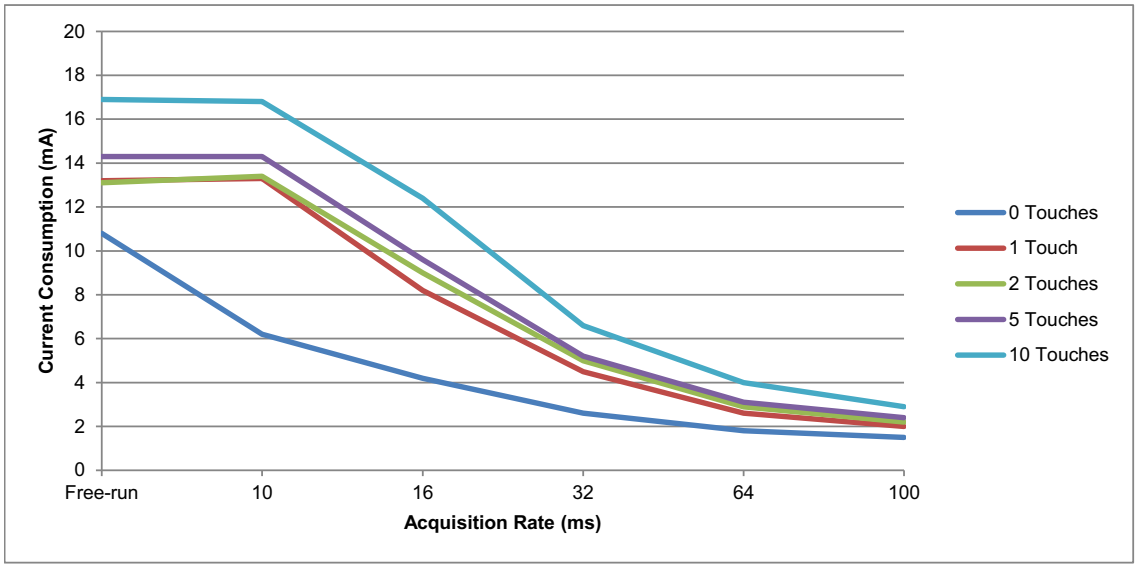
	Current Consumption (mA)				
Acquisition Rate (ms)	**0 Touches**	**1 Touch**	**2 Touches**	**5 Touches**	**10 Touches**
Free-run	8.2	11.8	13.4	13.2	13.1
10	4.4	11.9	13.3	13.2	12.9
16	2.9	7.5	8.7	8.7	8.4
32	1.7	3.9	4.6	4.5	4.5
64	1	2.2	2.5	2.5	2.4
100	0.9	1.5	1.7	1.7	1.7



NOTE These figures were obtained with the Power Monitor turned on. If the Power Monitor is disabled (Power Configuration T7 CFG2 DISPOWMON = 1), the current consumption is reduced by approximately 0.4 mA for AVdd.

13.4.2 VDD 3.3V

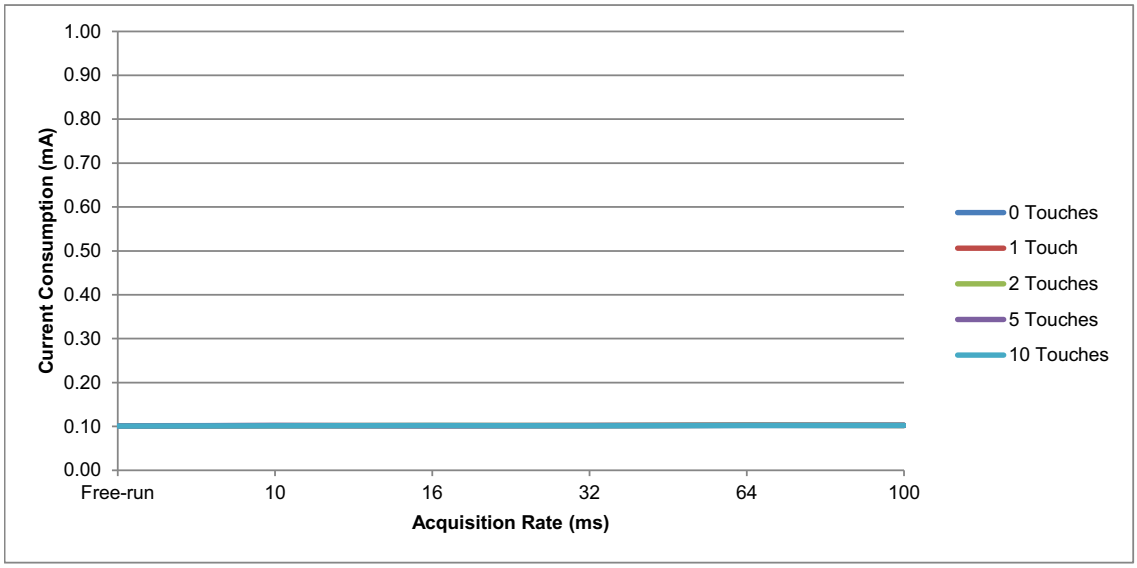
	Current Consumption (mA)				
Acquisition Rate (ms)	**0 Touches**	**1 Touch**	**2 Touches**	**5 Touches**	**10 Touches**
Free-run	10.8	13.2	13.1	14.3	16.9
10	6.2	13.3	13.4	14.3	16.8
16	4.2	8.2	9	9.6	12.4
32	2.6	4.5	5	5.2	6.6
64	1.8	2.6	2.9	3.1	4
100	1.5	2	2.2	2.4	2.9



NOTE These figures were obtained with the Power Monitor turned on. If the Power Monitor is disabled (Power Configuration T7 CFG2 DISPOWMON = 1), the current consumption is reduced by approximately 0.5 mA for Vdd.

13.4.3 VDDIO 1.8V

	Current Consumption (mA)				
Acquisition Rate (ms)	**0 Touches**	**1 Touch**	**2 Touches**	**5 Touches**	**10 Touches**
Free-run	0.10	0.10	0.10	0.10	0.10
10	0.10	0.10	0.10	0.10	0.10
16	0.10	0.10	0.10	0.10	0.10
32	0.10	0.10	0.10	0.10	0.10
64	0.10	0.10	0.10	0.10	0.10
100	0.10	0.10	0.10	0.10	0.10



NOTE These figures were obtained with the Power Monitor turned on. If the Power Monitor is disabled (Power Configuration T7 CFG2 DISPOWMON = 1), the current consumption is reduced by approximately 0.09 mA for VddIO.

13.4.4 DEEP SLEEP

T_A = 25°C

	Power Monitoring			
Parameter	**On**	**Off**	**Units**	**Notes**
Deep Sleep Current	1.09	0.19	mA	Vdd = 3.3V, AVdd = 3.3V, VddIO = 1.8V
Deep Sleep Power	3.45	0.62	mW	Vdd = 3.3V, AVdd = 3.3V

13.5 Timing Specifications

NOTE The figures below show typical values based on the test configuration. Actual timings in the user's application will depend on the circumstances of that particular project and will vary from those shown below. Further tuning will be required to achieve an optimal performance.

13.5.1 TOUCH LATENCY

Conditions: XSIZE = 41; YSIZE = 26; CHRGTIME = 38; IDLESYNCSPERX = 16; ACTVSYNCSPERX = 16;
T = ambient temperature; Finger center of screen; Reporting off (except T100); C_{pk} Process Capability Index calculation not applied

Idle Primary = Mutual Capacitance; Active Primary = Mutual Capacitance

	Pipelining Off			Pipelining On			
T100 TCHDIDOWN	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
3	34	38	43	34	39	44	ms
2	24	28	33	24	29	34	ms
1	15	19	24	15	19	24	ms
Disabled (DISTCHDIDOWN = 1)	6	11	16	4	11	17	ms

Idle Primary = Self Capacitance; Active Primary = Mutual Capacitance

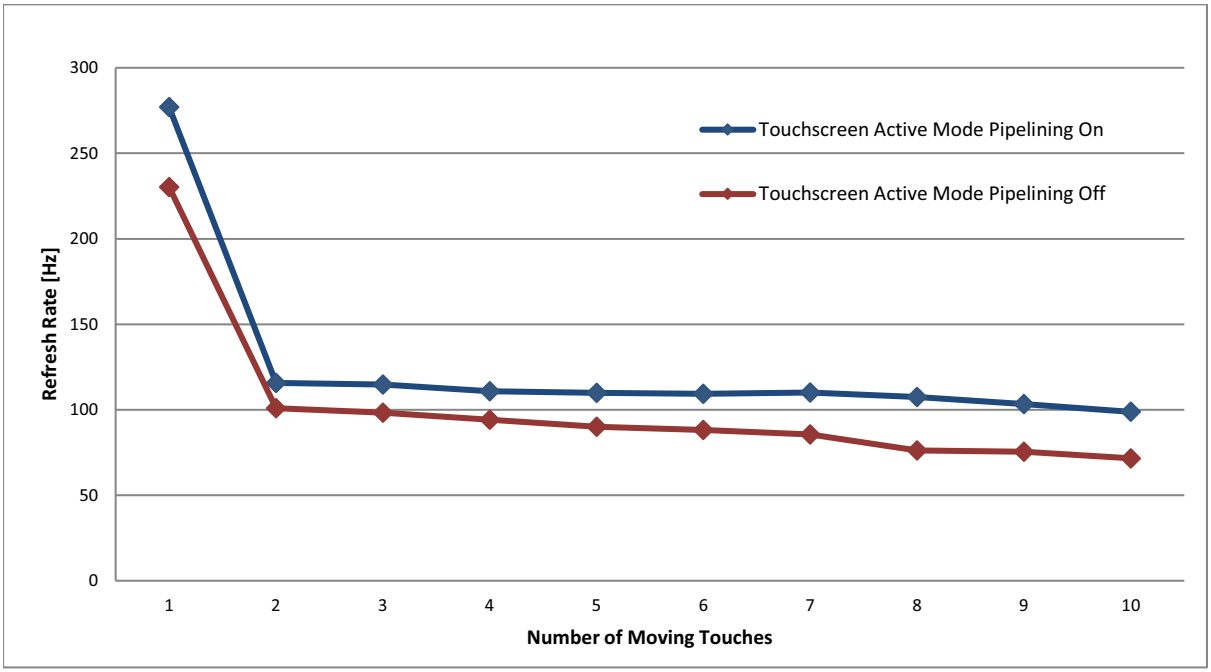
	Pipelining Off			Pipelining On			
T100 TCHDIDOWN	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
3	33	35	43	33	37	43	ms
2	23	26	33	24	27	34	ms
1	13	16	23	14	17	24	ms
Disabled (DISTCHDIDOWN = 1)	13	15	17	13	16	18	ms

Idle Primary = Self Capacitance; Active Primary = Self Capacitance

	Pipelining Off			Pipelining On			
T100 TCHDIDOWN	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
3	22	25	32	28	31	38	ms
2	18	21	28	24	27	34	ms
1	13	15	23	14	17	24	ms
Disabled (DISTCHDIDOWN = 1)	13	15	17	3	15	18	ms

13.5.2 REPORT RATE

Conditions: Touchscreen: XSIZE = 41; YSIZE = 26; CHRGTIME = 39; IDLESYNCSPERX = 16; ACTVSYNCSPERX = 16; T = ambient temperature



13.5.3 RESET TIMINGS

Parameter	Min	Typ	Max	Units	Notes
Power on to $\overline{\text{CHG}}$ line low	–	97	–	ms	Vdd supply for POR VddIO supply for external reset
Hardware reset to $\overline{\text{CHG}}$ line low	–	92	–	ms	
Software reset to $\overline{\text{CHG}}$ line low	–	116	–	ms	

Note 1: Any $\overline{\text{CHG}}$ line activity before the power-on or reset period has expired should be ignored by the host. Operation of this signal cannot be guaranteed before the power-on/reset periods have expired.

2: The mXT1066TD meets the requirements of Microsoft Windows 8.x and later versions.

13.6 Touch Accuracy and Repeatability

Parameter	Min	Typ	Max	Units	Notes
Linearity	–	±0.5	–	mm	Finger diameter 8 mm
Accuracy (across all areas of screen)	–	0.5	–	mm	Finger diameter 8 mm
Repeatability	–	±0.25	–	%	X axis with 12-bit resolution

13.7 Touchscreen Sensor Characteristics

Parameter	Description	Value
Cm	Mutual capacitance	Typical value is between 0.15 pF and 10 pF on a single node.
Cpx	Mutual capacitance load to X	Microchip recommends a maximum load of 300 pF on each X or Y line. (1)
	With Internal Voltage Pump	Maximum recommended load on each X line: (2) Cpx + (*num_Y* × Cm) < 125 pF
	With Internal Voltage Pump and Dual X	Maximum recommended load on each X line: (2) Cpx + (2 × *num_Y* × Cm) < 62.5 pF
Cpy	Mutual capacitance load to Y	Microchip recommends a maximum load of 300 pF on each X or Y line. (1)
Cpx	Self capacitance load to X	Microchip recommends a maximum load of 100 pF on each X or Y line. (1)
Cpy	Self capacitance load to Y	
ΔCpx	Self capacitance imbalance on X	Nominal value is 21 pF. Value increases by 1 pF for every 45 pF reduction in Cpx/Cpy (based on 100 pF load)
ΔCpy	Self capacitance imbalance on Y	
Cpds0	Self capacitance load to Driven Shield	Microchip recommends a maximum load of 100 pF on the Driven Shield line. (1)

Note 1: Please contact your Microchip representative for advice if you intend to use higher values.

2: *num_Y* = Number of active Y lines defined by Multiple Touch Touchscreen T100.

13.8 Input/Output Characteristics

Parameter	Description	Min	Typ	Max	Units	Notes
Input (All input pins connected to the VddIO power rail)						
Vil	Low input logic level	–0.3	–	0.3 × VddIO	V	VddIO = 1.8 V to Vdd
Vih	High input logic level	0.7 × VddIO	–	VddIO	V	VddIO = 1.8 V to Vdd
Iil	Input leakage current	–	–	1	µA	Pull-up resistors disabled
$\overline{\text{RESET}}$	Internal pull-up resistor	20	40	60	kΩ	
GPIOs	Internal pull-up/pull-down resistor					
Output (All output pins connected to the VddIO power rail)						
Vol	Low output voltage	0	–	0.2 × VddIO	V	VddIO = 1.8 V to Vdd Iol = –2 mA
Voh	High output voltage	0.8 × VddIO	–	VddIO	V	VddIO = 1.8 V to Vdd Ioh = 2 mA

13.9 I²C Specification

Parameter	Value
Addresses	0x4A or 0x4B
I²C specification (1)	Revision 6.0
Maximum bus speed (SCL) (2)	3.4 MHz
Standard Mode (3)	100 kHz
Fast Mode (3)	400 kHz
Fast Mode Plus (3)	1 MHz
High Speed Mode (3)	3.4 MHz

Note 1: More detailed information on I²C operation is available from www.nxp.com/documents/user_manual/UM10204.pdf.

2: In systems with heavily laden I²C lines, even with minimum pull-up resistor values, bus speed may be limited by capacitive loading to less than the theoretical maximum.

3: The values of pull-up resistors should be chosen to ensure SCL and SDA rise and fall times meet the I²C specification. The value required will depend on the amount of capacitance loading on the lines.

13.10 HID-I²C Specification

Parameter	Value
Vendor ID	0x03EB (Microchip)
Product ID	0x2189 (mXT1066TD)
HID-I²C specification	1.0

13.11 Thermal Packaging

13.11.1 THERMAL DATA

Parameter	Description	Typ	Unit	Condition	Package
θ_{JA}	Junction to ambient thermal resistance	55.0	°C/W	Still air	114-ball UFBGA 7 × 5 × 0.65 mm
θ_{JC}	Junction to case thermal resistance	7.0	°C/W		114-ball UFBGA 7 × 5 × 0.65 mm
θ_{JA}	Junction to ambient thermal resistance	47.0	°C/W	Still air	117-ball UFBGA 9.5 × 7 × 0.65 mm
θ_{JC}	Junction to case thermal resistance	7.5	°C/W		117-ball UFBGA 9.5 × 7 × 0.65 mm

13.11.2 JUNCTION TEMPERATURE

The maximum junction temperature allowed on this device is 125°C.

The average junction temperature in °C (T_J) for this device can be obtained from the following:

$$T_J = T_A + (P_D \times \theta_{JA})$$

If a cooling device is required, use this equation:

$$T_J = T_A + (P_D \times (\theta_{HEATSINK} + \theta_{JC}))$$

where:

- θ_{JA}= package thermal resistance, Junction to ambient (°C/W) (see Section 13.11.1 “Thermal Data”)
- θ_{JC} = package thermal resistance, Junction to case thermal resistance (°C/W) (see Section 13.11.1 “Thermal Data”)
- $\theta_{HEATSINK}$ = cooling device thermal resistance (°C/W), provided in the cooling device datasheet
- P_D = device power consumption (W)
- T_A is the ambient temperature (°C)

13.12 ESD Information

Parameter	Value	Reference Standard
Human Body Model (HBM)	±2000V	JEDEC JS–001
Charge Device Model (CDM)	±250V	JEDEC JS–001

13.13 Soldering Profile

Profile Feature	Green Package
Average Ramp-up Rate (217°C to Peak)	3°C/s max
Preheat Temperature 175°C ±25°C	150 – 200°C
Time Maintained Above 217°C	60 – 150 s
Time within 5°C of Actual Peak Temperature	30 s
Peak Temperature Range	260°C
Ramp down Rate	6°C/s max
Time 25°C to Peak Temperature	8 minutes max

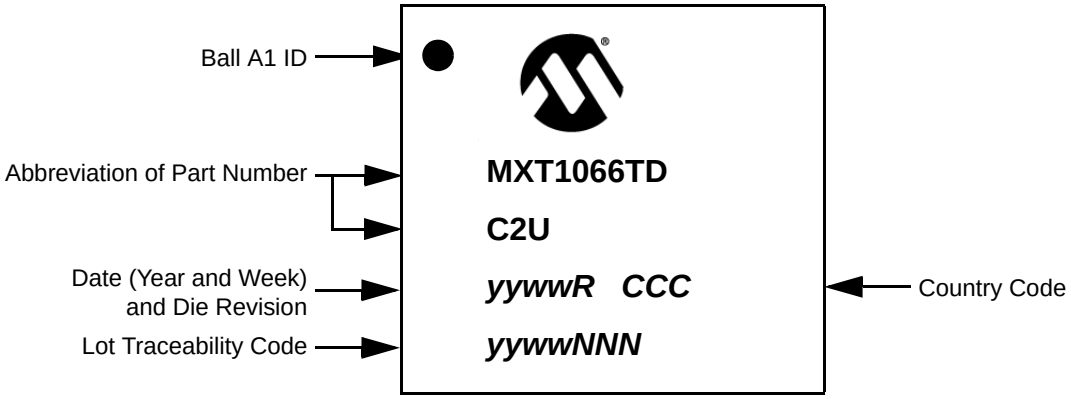
13.14 Moisture Sensitivity Level (MSL)

MSL Rating	Package Type(s)	Peak Body Temperature	Specifications
MSL3	114-ball UFBGA	260°C	IPC/JEDEC J-STD-020
MSL3	117-ball UFBGA	260°C	IPC/JEDEC J-STD-020

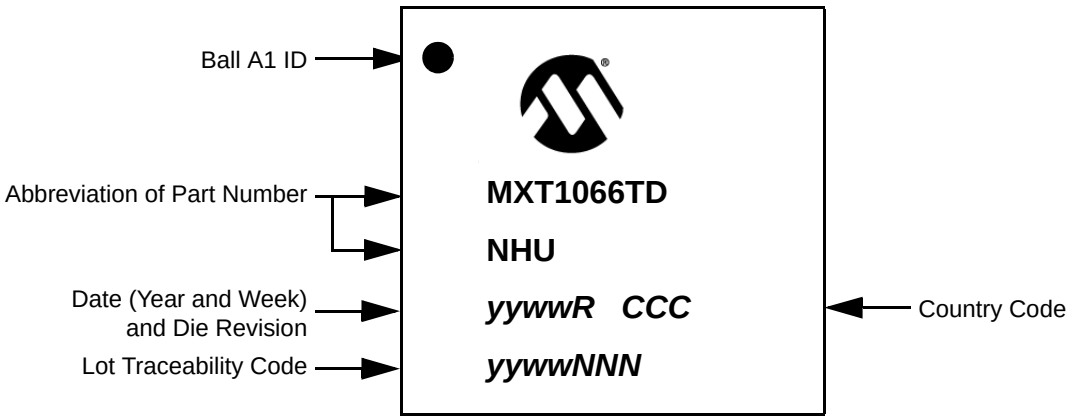
14.0 PACKAGING INFORMATION

14.1 Package Marking Information

14.1.1 114-BALL UFBGA



14.1.2 117-BALL UFBGA



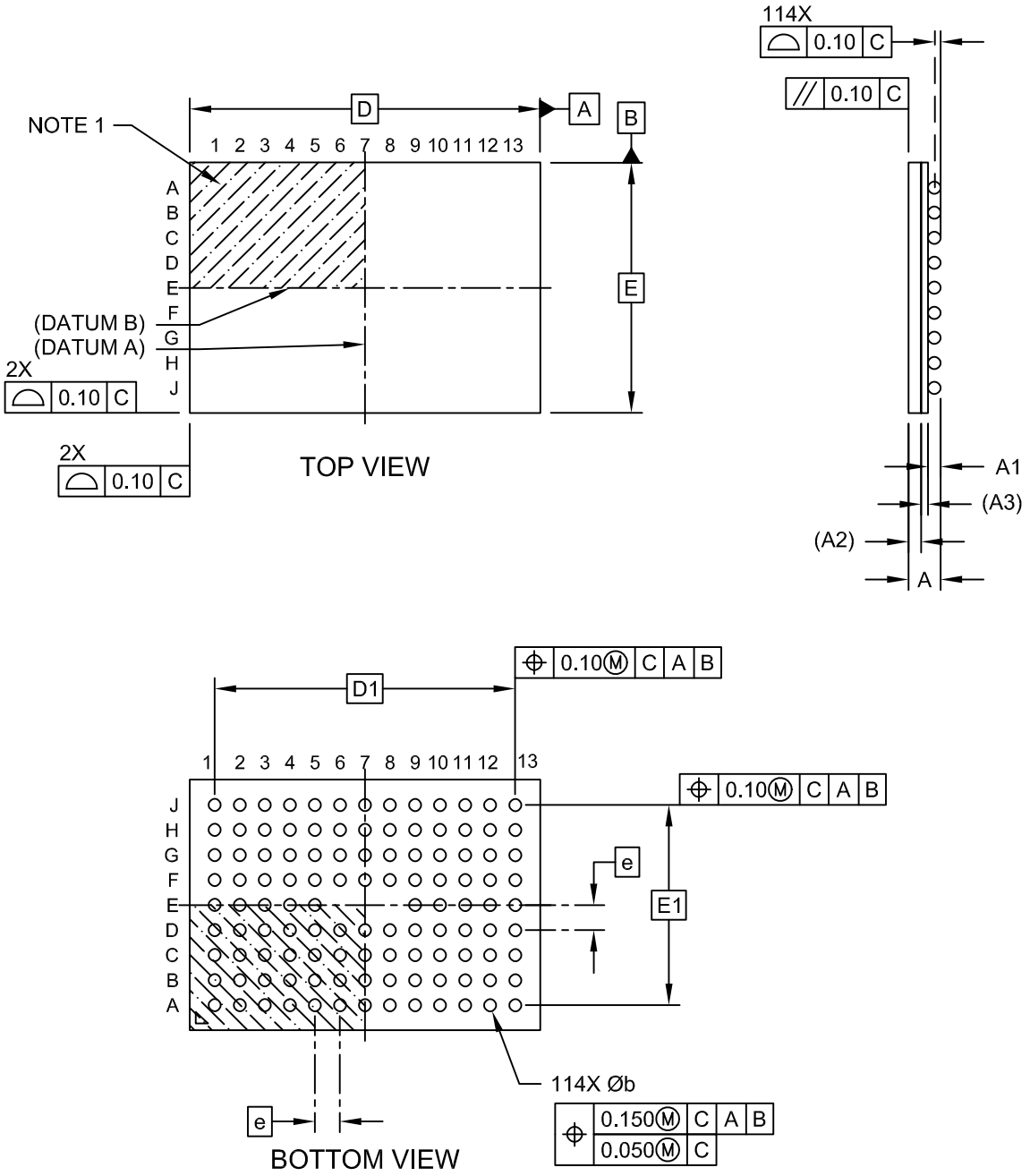
14.1.3 ORDERABLE PART NUMBERS

The product identification system for maXTouch devices is described in “Product Identification System”. That section also lists example part numbers for the device.

14.2 Package Details

114-Ball Ultra Thin Fine-Pitch Ball Grid Array Package (C2B) - 7x5x0.65 mm Body With 13x9 Array, 0.5 mm Pitch [UFBGA]; Atmel Legacy GPC CBJ

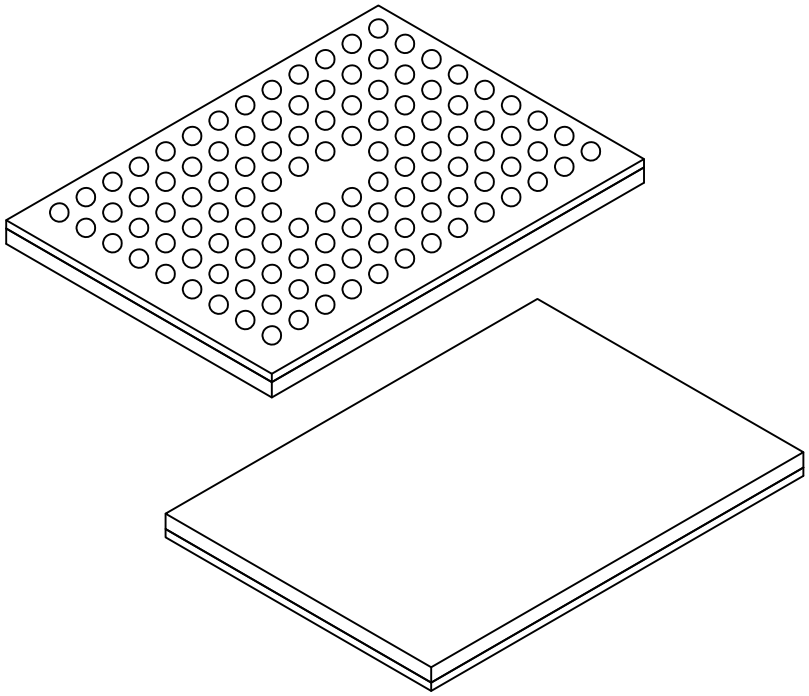
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21163 Rev A Sheet 1 of 2

114-Ball Ultra Thin Fine-Pitch Ball Grid Array Package (C2B) - 7x5x0.65 mm Body With 13x9 Array, 0.5 mm Pitch [UFBGA]; Atmel Legacy GPC CBJ

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		114	
Pitch	e		0.50 BSC	
Overall Height	A	-	-	0.65
Ball Height	A1	0.140	-	0.240
Mold Thickness	A2		0.250 REF	
Substrate Thickness	A3		0.136 REF	
Overall Length	D		7.00 BSC	
Ball Array Length	D1		6.00 BSC	
Overall Width	E		5.00 BSC	
Ball Array Width	E1		4.00 BSC	
Ball Width	b	0.200	-	0.300
Ball Diameter			0.250 REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

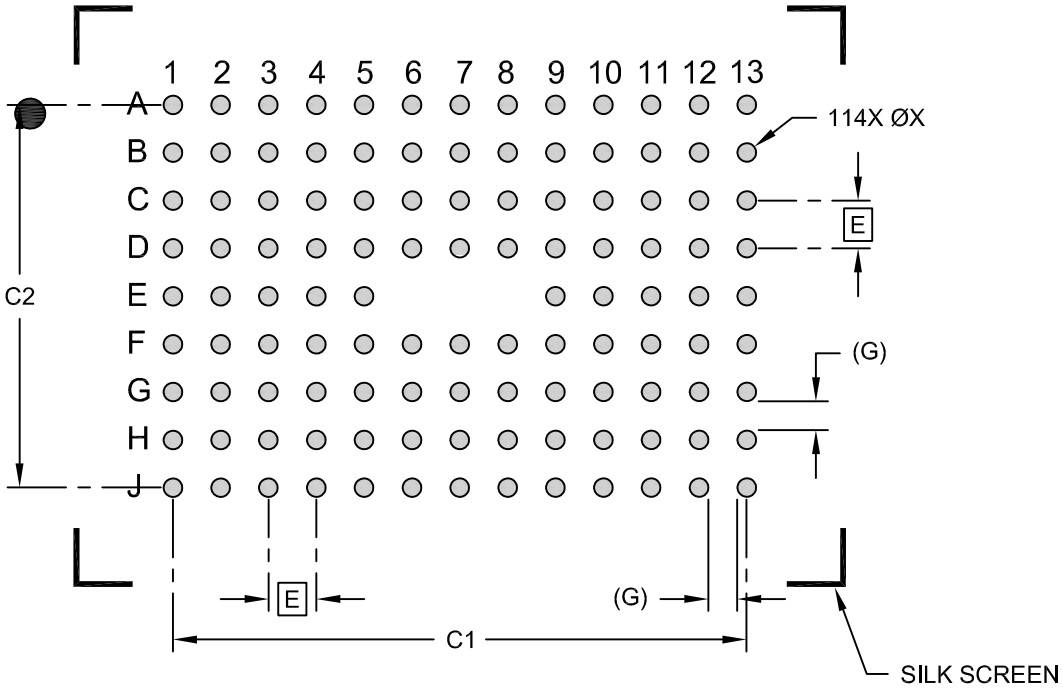
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21163 Rev A Sheet 2 of 2

114-Ball Ultra Thin Fine-Pitch Ball Grid Array Package (C2B) - 7x5x0.65 mm Body With 13x9 Array, 0.5 mm Pitch [UFBGA]; Atmel Legacy GPC CBJ

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Pad Diameter (X114)	X			0.20
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		4.00	
Column and Row Spacing	G	0.30 REF		

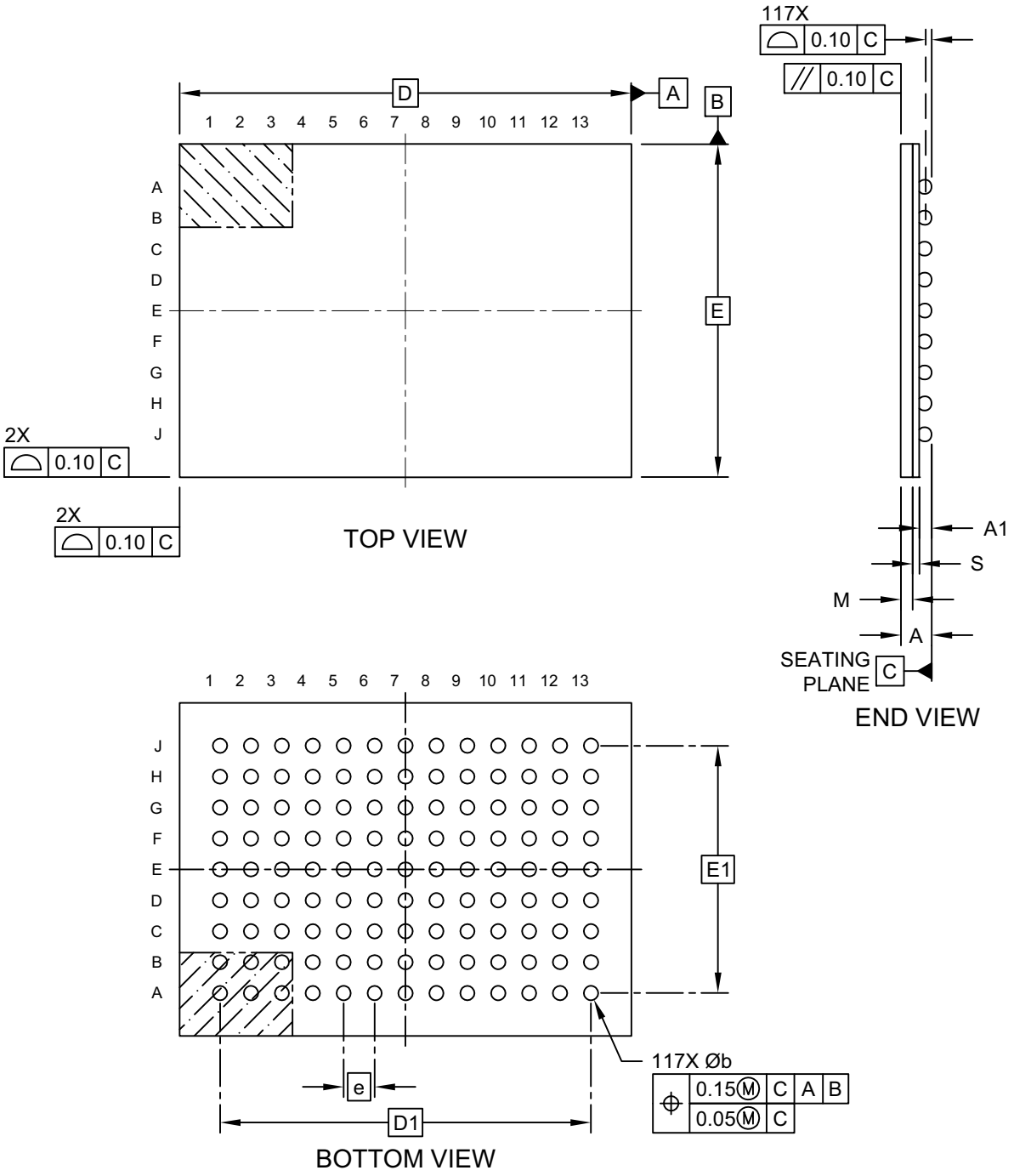
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-23163 Rev A

117-Ball Ultra Thin Fine-Pitch Ball Grid Array Package (C5B) - 9.5x7.0x0.65 mm Body [UFBGA]

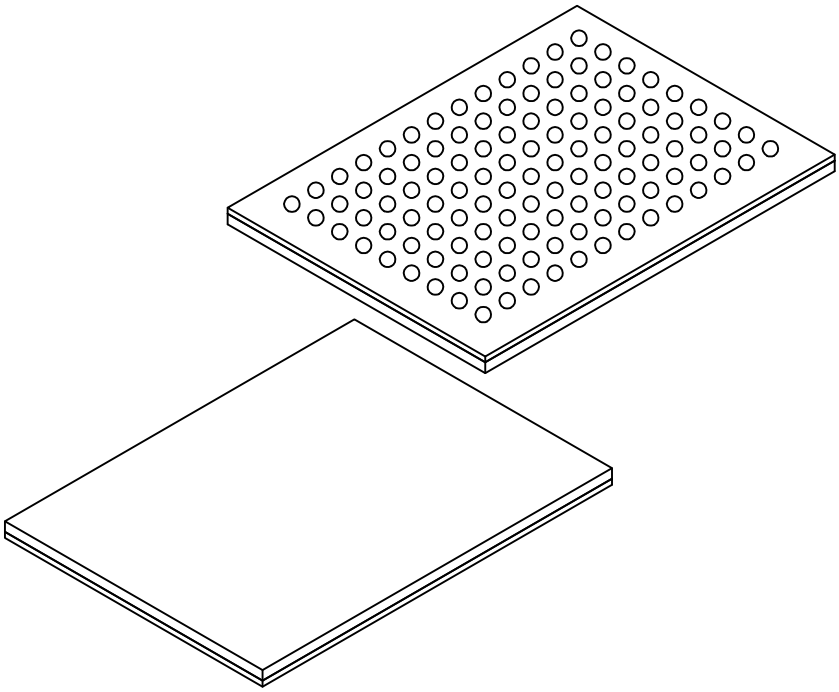
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-21166 Rev A Sheet 1 of 2

117-Ball Ultra Thin Fine-Pitch Ball Grid Array Package (C5B) - 9.5x7.0x0.65 mm Body [UFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		117	
Pitch	e		0.65 BSC	
Overall Height	A	–	–	0.65
Ball Height	A1	0.16	0.21	0.26
Mold Thickness	M		0.25 REF	
Substrate Thickness	S		0.136 REF	
Overall Length	D		9.50 BSC	
Ball Array Length	D1		7.80 BSC	
Overall Width	E		7.00 BSC	
Ball Array Width	E1		5.20 BSC	
Ball Diameter	b	0.25	0.30	0.35

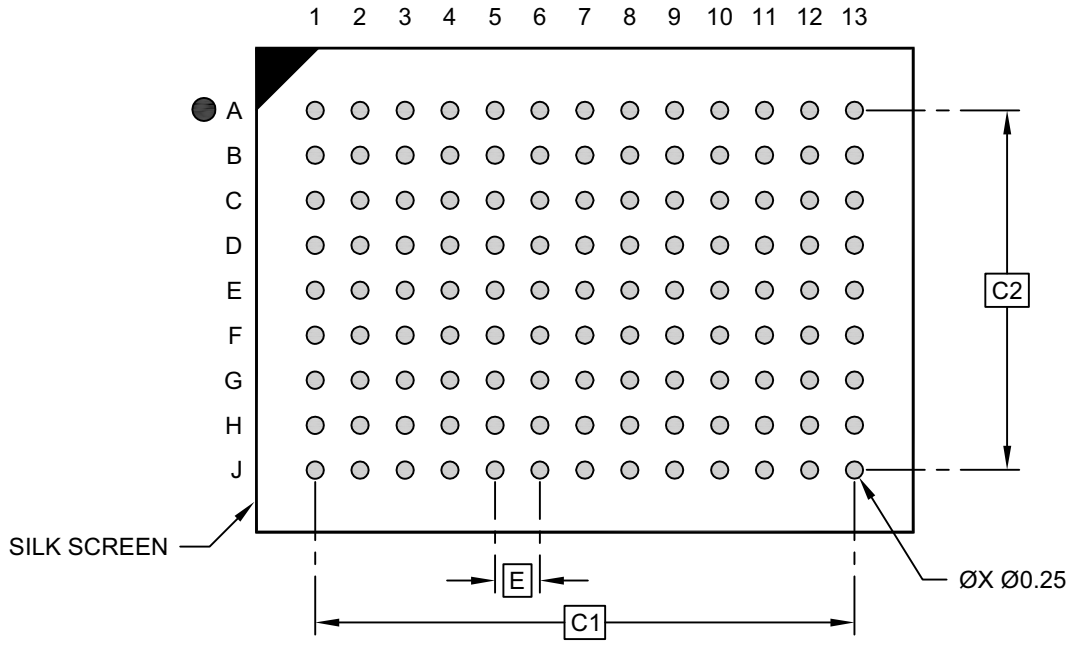
Notes:

1. Ball A1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21166 Rev A Sheet 2 of 2

117-Ball Ultra Thin Fine-Pitch Ball Grid Array Package (C5B) - 9.5x7.0x0.65 mm Body [UFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1	7.80 BSC		
Contact Pad Spacing	C2	5.20 BSC		
Contact Pad Width (Xnn)	X			0.25

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-23166 Rev A

APPENDIX A: ASSOCIATED DOCUMENTS

Microchip maXTouch Documents

The following documents are available by contacting your Microchip representative.

Touchscreen Design and PCB/FPCB Layout Guidelines

- Application Note: QTAN0054 – *Getting Started with maXTouch Touchscreen Designs*
- Application Note: MXTAN0208 – *Design Guide for PCB Layouts for maXTouch Touch Controllers*
- Application Note: QTAN0080 – *Touchscreens Sensor Design Guide*
- Application Note: AN2683 – *Edge Wiring for Self Capacitance maXTouch Touchscreens*

Configuring and Tuning the Device

- Application Note: MXTAN0213 – *Interfacing with maXTouch Touchscreen Controllers*

Tools

- *maXTouch Studio User Guide* (distributed as on-line help with maXTouch Studio)

External Documents

The following documents are not supplied by Microchip. To obtain any of the following documents, please contact the relevant organization.

I^2C Interface

- UM10204, *I^2C bus specification and user manual*, Rev. 6 — 4 April 2014
  Available from NXP: www.nxp.com/documents/user_manual/UM10204.pdf

APPENDIX B: REVISION HISTORY

Revision A (January 2021)

Initial edition for firmware revision 1.0.AB – Release

INDEX

PRODUCT IDENTIFICATION SYSTEM

The table below gives details on the product identification system for maXTouch devices. See "Orderable Part Numbers" below for example part numbers for the mXT1066TD.

To order or obtain information, for example on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–XXX	[X]	[X]	[XXX]
Device	Package	Temperature Range	Tape and Reel Option	Pattern

Device:	Base device name		
Package:	A	=	QFP (Plastic Quad Flatpack)
	CC	=	UFBGA (Ultra Thin Fine-pitch Ball Grid Array)
	C2	=	UFBGA (Ultra Thin Fine-pitch Ball Grid Array)
	NH	=	UFBGA (Ultra Thin Fine-pitch Ball Grid Array)
	C4	=	X1FBGA (Extra Thin Fine-pitch Ball Grid Array)
	MA	=	XQFN (Super Thin Quad Flat No Lead Sawn)
	MA5	=	XQFN (Super Thin Quad Flat No Lead Sawn)
Temperature Range:	U	=	–40°C to +85°C (Grade 3)
	T	=	–40°C to +85°C (Grade 3)
	B	=	–40°C to +105°C (Grade 2)
Tape and Reel Option:	*Blank*	=	Standard Packaging (Tube or Tray)
	R	=	Tape and Reel (1)
Pattern:	Extension, QTP, SQTP, Code or Special Requirements (Blank Otherwise)		

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. See "Orderable Part Numbers" below or check with your Microchip Sales Office for package availability with the Tape and Reel option.

Orderable Part Numbers

Orderable Part Number	Firmware Revision	Description
ATMXT1066TD-C2U002 (Supplied in trays)	1.0.AB	114-ball UFBGA 7 × 5 × 0.65 mm, RoHS compliant Industrial grade; not suitable for automotive characterization
ATMXT1066TD-C2UR002 (Supplied in tape and reel)		
ATMXT1066TD-NHU002 (Supplied in trays)	1.0.AB	117-ball UFBGA 9.5 × 7 × 0.65 mm, RoHS compliant Industrial grade; not suitable for automotive characterization
ATMXT1066TD-NHUR002 (Supplied in tape and reel)		

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- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

THE MAXTOUCH WEB SITE

Information on Microchip's maXTouch product line can be accessed via the microchip web site at www.microchip.com, This information is also available for direct access via a short-cut at www.maxtouch.com. The maXTouch web pages contain the following information:

- **Product Information** – Product specifications, brochures, datasheets, protocol guides
- **Tools and Software** – Evaluation kits, maXTouch Studio, software libraries for individual maXTouch touch controllers
- **Training and Support** – Generic application notes and training material for the maXTouch product range

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NOTES:

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