

TARGET188EB

User Manual

Contents

Revision History	3
Preface	5
The Manual	5
Name Conventions	5
Problem?	5
Contents - Packing List	5
Utility Disks	6
Anti-Static Handling	6
Electromagnetic Compatibility (EMC)	6
Packaging	6
Section 1. Introduction	7
Section 2. Getting Started	9
Equipment required	9
Installation	9
Section 3. Links and Options	11
Default Link Positions	11
User Configuration Record	14
Section 4. Using the TARGET188EB	15
Programmable Memory and I/O Map	15
Memory Map After Power-up/Reset	16
On-Board Control Registers	17
User Links and LEDs	18

Revision History

Manual Version/Issue	PCB	Comments	
A	V 1 Iss 1	961107	First release.
B	V1 Iss 1	961218	Edits to Appendix F. Circuit Diagrams.

© Copyright Arcom Control Systems Ltd. 1996

The choice of boards and systems is the responsibility of the buyer, and the use to which they are put cannot be the liability of Arcom Control Systems Ltd. However, Arcom's sales team is always available to assist you in making your decision.

Preface

The Manual

This manual details the operation and features of Arcom's TARGET188EB boards. It has been designed as both a guide to getting started with the TARGET188EB Development Kit and a reference for the hardware features of the board.

Name Conventions

Throughout this document an asterisk '*' suffix to a signal name denotes that a signal is active low (e.g. DATAACK*).

All numbers are in decimal unless otherwise indicated. Where a number is suffixed by 'h' the value is in hexadecimal format.

Problem?

If you have any problems finding information about this board, or the board fails to work, or something is missing, please contact Arcom Customer Support at our offices in Cambridge, UK.

If the engineers are busy please leave a message, or alternatively, send a facsimile message. Please state:

- Your name, telephone and facsimile numbers
- The time and date
- The product name
- The problem

Arcom Customer Support: Tel: 01223 412428
Fax: 01223 410457

For US callers: Tel: (816) 941 7025

For US callers: Fax: (816) 941 0343

Internet: support@arcom.co.uk
 sales@arcom.co.uk

Arcom Main Switchboard: Tel: 01223 411200
Fax: 01224 403400

Contents - Packing List

In your TARGET188EB Development Kit package you should have:

- A TARGET188EB in a sealed anti-static bag.
- A document titled 'TARGET188EB User Manual' (this document)
- An SVIF1 Development Interface Module
- A CAB-SVIF1 Development Interface Cable
- A high density 3 1/2" floppy disk titled 'TARGET188EB Monitor Disk'

Section 1. Introduction

TARGET188EB is a Eurocard sized target CPU board developed specifically for embedded applications offering the following features:

- Intel 188EB microprocessor running at 25MHz
- STEbus 8-bit expansion interface
- PC/104 8-bit expansion interface
- 128KB SRAM as standard, 256KB option available (8-bit wide access)
- 128KB socketed ROM on-board as standard (8-bit wide) with resident monitor software
- Socket for further 32/64/128/256KB ROM which may be 5V Flash EPROM
- Programmable memory and I/O maps
- Two 120KBaud (max.) RS232 serial communications ports (one Zilog 85230 SCC)
- Watchdog timer
- One TTL 8-bit digital output port
- One TTL 8-bit digital input port
- One TTL 8-bit digital input/output port
- Flexible hardware interrupt support
- Software development/download port (SVIF1 port)
- Two user links
- Two user LEDs and +5V power LED

The TARGET188EB is available as two variants:

Variant Name	Specification
TARGET188EB	STEbus Master and PC/104 Master 128k SRAM
TARGET188EB-H	STEbus Master and PC/104 Master 256k SRAM

This manual covers both variants.

The TARGET188EB is shipped with a software monitor blown into a 128K EPROM to allow simple exercising of the board and downloading application code. The 'remote' target portion of Arcom's SourceVIEW development software is also blown into the ROM. By using the board with the TARGET188EB Development Kit the user can develop and debug application software very quickly.

Section 2. Getting Started

This section is designed to familiarise the user with the features of the TARGET188EB and demonstrate the use of the monitor software.

Equipment required

- TARGET188EB Development Kit
- STEbus rack and backplane with power supply OR
- Power supply (+5V at 1A minimum) connected up to PL4 (see Appendix B. Connections)
- IBM PC/AT compatible computer running terminal emulation software

Installation & Monitor Startup

Refer to Target188EB Quickstart Manual for more comprehensive instructions with drawings.

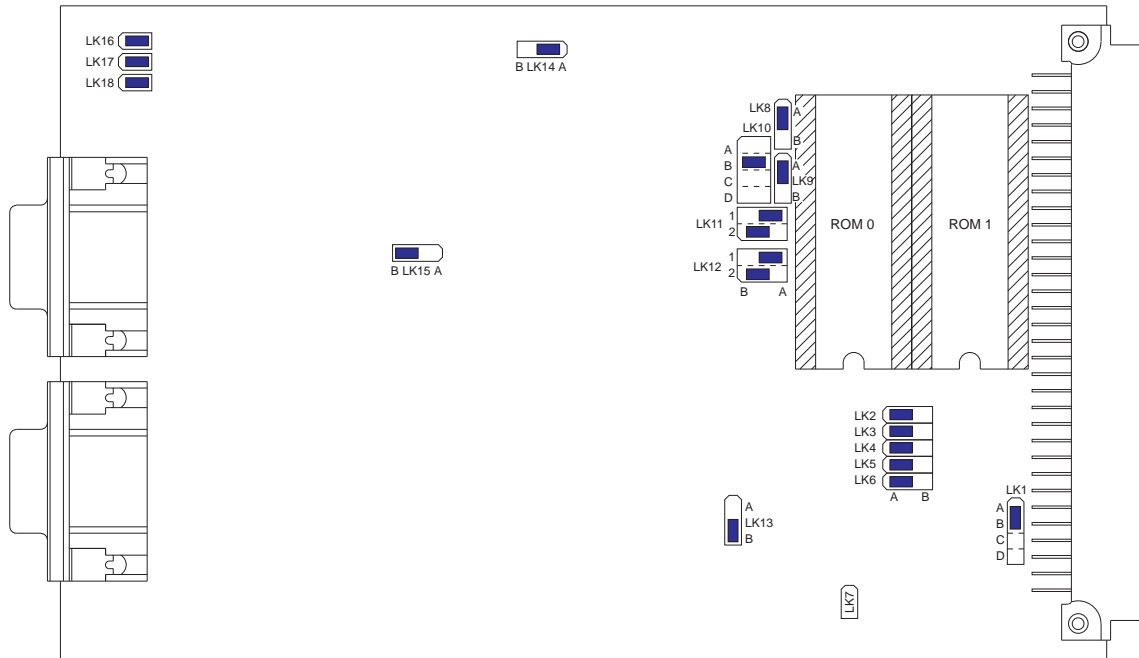
1. Ensure that the links on the TARGET188EB board are in their default configurations (see Section 3. Links and Options).
2. From the TARGET188EB Development Kit take the CAB-SVIF1 cable and plug the 10 way ribbon cable connector into the SVIF1 PL2 header.
3. Plug PL1 of the SVIF1 into PL2 (software development/download port) on the TARGET188EB. The body of the SVIF1 should lie over the TARGET188EB.
4. Align the TARGET188EB into the STEbus rack until it mates with one of the backplane connectors.

OR

5. Wire the +5V power supply cable to pin 2 of the PL4 screw terminal block and the 0V cable to either pin 5 or pin 6 of the terminal block.
6. Plug the 9 way D-type connector marked channel B on the CAB-SVIF1 cable into one of the COM ports on the PC/AT computer.
7. Configure the terminal emulation software on the PC/AT for communications via the appropriate COM port at 19200 Baud with 8 data bits, no parity and 1 stop bit. Set the protocol to 'none'.
8. Turn on the STEbus rack OR power supply - the surface mount power indicator LED on the TARGET188EB will illuminate.

Section 3. Links and Options

Default Link Positions



Note: A '+' next to a link position indicates the default shipping position.

LK1. STEbus SYSRST*

LK1	Function
+A	Board drives SYSRST* to backplane
B	Board receives SYSRST* from backplane
C	Board can be reset by push-button connected to PL3 only

LK2. INT3 source selection (1 link of 2)

LK2	Function
+A	PC/104 IRQ7 or STEbus TFRERR* (see LK13 also)
B	STEbus ATNRQ3*

LK3. INT2 source selection

LK3	Function
+A	PC/104 IRQ5
B	STEbus ATNRQ2*

LK4. INT0 source selection

LK4	Function
+A	PC/104 IRQ3
B	STEbus ATNRQ0*

LK12. ROM1 size selection - see also LK10 & LK11

LK12	1A	1B	2A	2B
EPROM size				
32K	omit	fit	X	X
64K	fit	omit	X	X
128K	fit	omit	omit	fit
256K	fit	omit	fit	omit

Note: Both EPROM's must be of the same size

LK13. INT3 source selection (2 link of 2)

LK13	Function
A	STEBus TFRERR*
+B	PC/104 IRQ7

LK14. Watchdog source selection

LK14	Function
+A	Watchdog strobe driven from BCLK (i.e. disabled)
B	Watchdog strobe driven from 188EB port 2 bit 3 (i.e. enabled)

LK15. Timer 1 source selection

LK15	Function
A	Timer1 source driven from Timer0 out (cascade)
+B	Timer1 source driven from external source

LK16. Run Mode Select

Selects whether the processor runs the monitor software or the users application code after a power-up or reset. Application code must be set to start running at C0000H (lowest EPROM memory address).

LK16	Function
Omit	Run application starting at memory address C0000H
+Fit	Run monitor software

LK17. User Link 1. - CPU port P2 bit 4

LK17	Function
Omit	CPU port P2 bit 4 reads as 1
+Fit	CPU port P2 bit 4 reads as 0

LK18. User Link 2. CPU port P2 bit 5

LK18	Function
Omit	CPU port P2 bit 5 reads as 1
+Fit	CPU port P2 bit 5 reads as 0

Section 4. Using the TARGET188EB

Programmable Memory and I/O Map

The TARGET188EB has a very flexible scheme for locating its on-board memory, peripherals and expansion busses in its memory and I/O maps. The 188EB processor has eight outputs called 'general chip selects', GCS0 to GCS7. These outputs may be programmed so that they become active over a range of memory or I/O addresses and can be used to activate devices connected to the 188EB. The table below shows how the chip selects are used on the TARGET188EB with the default address ranges programmed by the monitor after initialisation.

188EB Chip Select	TARGET188EB Chip Select Use	Default Address Range
GCS7	Accesses STEbus	not programmed or enabled
GCS6	Accesses STEbus	not programmed or enabled
GCS5	Accesses STEbus	not programmed or enabled
GCS4	Accesses STEbus	not programmed or enabled
GCS3	Parallel port	not programmed or enabled
GCS2	SVIF1 port	FC0C-FC0F
GCS1	85C230 SCC Interrupt acknowledge	not programmed or enabled
GCS0	85C230 SCC	not programmed or enabled

Chip selects GCS0, GCS1, GCS2 and GCS3 are activated for the address ranges indicated in the table to control CPU accesses to the on-board memory and peripherals.

Any CPU access to an address that is not covered by one of GCS0, GCS1, GCS2 or GCS3 is automatically directed to the PC/104 bus. Boards using the STEbus can access peripheral boards on both PC/104 and STEbus. The STEbus is the non-default expansion bus. As shown in the table above, 188EB chip selects GCS4, GCS5, GCS6 and GCS7 can be used to direct CPU accesses that would normally go into the PC/104 bus to access the STEbus expansion bus instead.

This example illustrates the use of GCS3 to GCS6. The monitor software sets the TARGET188EB up so that the memory area from 200000h(128k RAM) or 40000h(256k RAM) to 7FFFFh is directed to the PC/104 bus by default. The user has an STEbus memory board that exists in the memory address range 60000h to 6FFFFh. Any one of GCS4 to GCS7 may be programmed to cover 60000h to 6FFFFh and CPU accesses to any address in this range will then be diverted to the STEbus instead of the PC/104.

GCS4, GCS5, GCS6 and GCS7 can be programmed very flexibly to create multiple 'holes' in the PC/104 memory or I/O space that are directed to the STEbus.

Memory space between the bottom of ROM and the top of main RAM (location selected by LCS) will be automatically mapped to the PC/104 bus. GCS4-7 can be programmed to direct accesses to the STEbus.

Note: when running the monitor software on 256KB RAM variants of board the extra 128KB of RAM is not accessible until chip select LCS is re-programmed.

I/O Map

FFFFh	PC/104 STEbus (GCS4-7)
FC0Fh	SVIF1 Port
FC0Ch	
F8FFh	On-chip peripherals (interrupt controllers, timers, SCC)
F000h	
EFFFh	
0000h	PC/104 STEbus (GCS4-7)

On-Board Control Registers

SVIF1 Port Registers

The SVIF1 port takes up 4 bytes of I/O space. The default base address of the SVIF1 port under the monitor software is I/O FC0Ch.

A1	A0	Function
1	1	Channel A Data
1	0	Channel B Data
0	1	Channel A Control
0	0	Channel B Control

Bus Timeout Clear

A read from the I/O address range setup for chip select GCS3 (parallel port) will clear a bus timeout when address lines A0 and A1 are high.

Parallel I/O port

To use this onboard facility it is necessary to program GCS3 for the address range required.

There are three TTL 8-bit digital I/O ports covered by this chip select.

1 digital I/O port
1 digital input port
1 digital output port

To access the output port A1 and A0 must be '0'.

To access the input port A1 is a '0' A0 is a '1'.

To access the I/O port A1 is a '1' A0 is a '0'.

If a read occurs from the I/O address range set in GCS3 and A1 and A0 are '1' this will clear a bus time-out.

When using the I/O port as an input port firstly set the outputs to '1'.

STEBus Support

The TARGET188EB is compliant with the STEbus IEEE1000 specification.

PC/104 Support

The TARGET188EB is compliant with version 2.3 of the PC/104 specification. It supports memory and I/O reads and writes as a sole master to 8 bit PC/104 peripheral boards. It does not support DMA or other PC/104 masters in the same module stack.

Battery Back-up

The TARGET188EB supports battery backup of its main system SRAM via the +VSTBY line on the STEbus or via pin 1 of the power connector PL4.

Using the STEbus, a +5V source should be connected between +VSTBY (+ve terminal) and GND (-ve terminal) on the STEbus backplane.

Using the board as an SBC, a +5V source should be connected between pin 1 (+ve terminal) and pin 6 (-ve terminal) of PL4.

Battery backup current is approximately 140uA.

Section 5. Troubleshooting

Problem	Suggestions
<ul style="list-style-type: none"> • No sign-on screen on terminal when running with SVIF1 	<ul style="list-style-type: none"> • Check connections to correct COM port • Check links in default positions especially LK16 (should be fitted) • Check baud rate, stop bits and parity of terminal • Check power on board - red surface mount LED should be lit.
<ul style="list-style-type: none"> • Can't access STEbus peripheral board 	<ul style="list-style-type: none"> • Check that SYSRST* is being driven on power-up by one board only in the system • Check that SYSCLK is being driven by one board in the system • Check that STEbus address range being accessed is available off-board (is it covered by one of the on-board memory or general chip selects) • Check that at least one on chip selects GCS4-7 been set up to cover the required address range
<ul style="list-style-type: none"> • Can't access PC/104 peripheral board 	<ul style="list-style-type: none"> • Is the address range being accessed available to the PC/104 bus - is it covered by one of the on-board general chip selects • Is the PC/104 board correctly plugged onto the board

Appendix A. Specification

Microprocessor	Intel 80188EB
Speed	25MHz
Memory	Sockets to hold up to 512KB ROM (8-bits wide, two wait states) top 16KB occupied by monitor software. 5V Flash ROMs may be programmed on-board. 128KB or 256KB main system SRAM (8-bits wide, one wait state)
Peripherals	1 x 85230 SCC RS232 serial communications ports (120KBaud max.) with RX, TX, CTS, RTS, DSR, DTR, DCD and RI Arcom SVIF debug/development port Watchdog timer fixed at 1200ms generates CPU reset 3 counter/timers max counter interval 1s. Each counter can generate an interrupt on a shared interrupt line Two user LEDs Two user links plus run monitor/run application link Power monitor generates CPU reset if +5V supply drops below 4.62V +/- 0.12V. Reset button connector
Expansion	STEBus IEEE1000 compatible master mode PC/104 version 2.3 compatible, 8 bit only. DMA and MASTER* modes not supported
Temperature	Operating: 0 to 55°C Storage: 0 to 70°C
Humidity	10% to 80% RH (non-condensing)
Power	+5V @ 600mA typical +12V and -12V routed to PL1, PL4, PL6 and PL7 but not used on board
Battery	External +5V @ 140uA
Dimensions	160mm x 100mm
Weight	140g (TARGET188EB) 160g with 2x 128k EPROMs fitted
MTBF	320000 hours

Appendix B. Connections

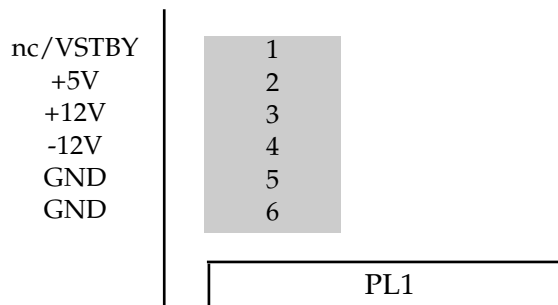
PL1. STEbus Connector

Standard 64way a&c row DIN41612 right angle PCB mount plug.
Pin-out in accordance with IEEE1000 specification.

PL1			
GND	a1	c1	GND
+5V	a2	c2	+5V
D0	a3	c3	D1
D2	a4	c4	D3
D4	a5	c5	D5
D6	a6	c6	D7
A0	a7	c7	GND
A2	a8	c8	A1
A4	a9	c9	A3
A6	a10	c10	A5
A8	a11	c11	A7
A10	a12	c12	A9
A12	a13	c13	A11
A14	a14	c14	A13
A16	a15	c15	A15
A18	a16	c16	A17
CM0	a17	c17	A19
CM2	a18	c18	CM1
ADRSTB*	a19	c19	GND
DATAACK*	a20	c20	DATSTB*
TRFERR*	a21	c21	GND
ATNRQ0*	a22	c22	SYSRST*
ATNRQ2*	a23	c23	ATNRQ1*
nc	a24	c24	ATNRQ3*
nc	a25	c25	nc
GND	a26	c26	nc
nc	a27	c27	nc
nc	a28	c28	nc
STECLK	a29	c29	+VSTBY
-12V	a30	c30	+12V
GND	a31	c31	+5V
GND	a32	c32	GND

PL4. External Power Connector

Phoenix MCV series two part combicon screw terminal connector. Pinout as:



PL7 . PC/104 Connectors

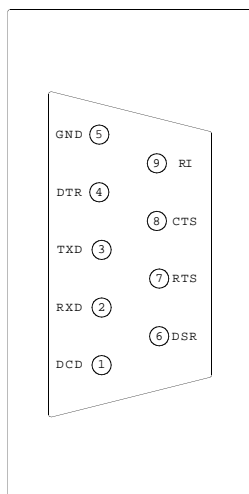
One 64 way non-stackthrough 0.1" grid socket connectors. Pinout and physical arrangement in accordance with PC/104 specification version 2.3.

PL7

nc	A1	B1	GND
D7	A2	B2	RESET
D6	A3	B3	+5
D5	A4	B4	nc
D4	A5	B5	nc
D3	A6	B6	nc
D2	A7	B7	-12
D1	A8	B8	ENDXFR*
D0	A9	B9	+12
IOCHRDY	A10	B10	nc
AEN (GND)	A11	B11	SMEMW*
A19	A12	B12	SMEMR*
A18	A13	B13	IOW*
A17	A14	B14	IOR*
A16	A15	B15	pull-up
A15	A16	B16	nc
A14	A17	B17	pull-up
A13	A18	B18	nc
A12	A19	B19	pull-up
A11	A20	B20	SYCLK
A10	A21	B21	IRQ7
A9	A22	B22	IRQ6
A8	A23	B23	IRQ5
A7	A24	B24	nc
A6	A25	B25	nc
A5	A26	B26	pull-up
A4	A27	B27	nc
A3	A28	B28	BALE
A2	A29	B29	+5
A1	A30	B30	OSC
A0	A31	B31	GND
GND	A32	B32	GND

PL8 and PL9. RS232 Serial Port connectors

Two 9-way D-type plugs. Pinout as:



Appendix C. Reference

The STEbus and the TARGET188EB

STEbus is a high reliability 8 bit backplane system, ideal for industrial I/O applications with powerful facilities for multi-processing and interrupt handling.

STEbus boards are classified as either bus masters or slaves. A bus master can initiate a bus transfer whereas a slave can only respond. Generally bus masters are CPU boards which access memory and I/O peripheral slave boards. Some slave boards do have on-board microprocessors.

STEbus master and slave boards may be placed in any slot in the STEbus backplane.

The TARGET188EB can act only as an STEbus master. It may not be used in multi-master systems as it does not have an arbiter necessary to arbitrate between multiple masters.

Only one board in an STEbus system should drive the 16MHz SYSCLK signal.

STEbus slaves are accessed simply by memory and I/O read and write commands from the processor. These generate address strobe (ADRSTB*), data strobe (DATSTB*), command modifier (CM2 to CM0), address and data signals to the STEbus. Slave boards that decode their address for a transfer respond with a DATAACK* signal when they have accepted or placed data on the STEbus. Slave boards should be configured to fit in the STEbus memory or I/O space available on the TARGET188EB. Note that if an STEbus slave has a non-movable address then the memory and I/O maps on the TARGET188EB are very flexible and may be re-configured using registers within the 188EB processor (see memory and I/O maps in Section 4. Using the TARGET188EB).

There are eight interrupt request lines on the STEbus, ATNRQ7* to ATNRQ0*. These are usually driven by slave boards to request action from a master. STEbus interrupt lines are level triggered and slave boards may share interrupt lines. The TARGET188EB can be configured to monitor ATNRQ3*, ATNRQ2*, ATNRQ1* and ATNRQ0*.

All transfers on the STEbus are monitored by bus timeout circuit that terminates any cycles that are longer than 8 μ . This is required because if no slave board responds to an STEbus cycle then the bus could stay in that bus cycle indefinitely, the bus timeout monitor prevents this. Bus timeouts on the TARGET188EB can optionally (link) generate an interrupt to the 188EB processor to indicate that a transfer problem took place.

Appendix D. Bibliography

Intel188EB Embedded Microprocessor Data Sheet

Intel Order No.: 272433-000

Intel188EB Embedded Microprocessor User's Manual

Intel Order No.: 270830-003

These may be ordered from these Intel literature centres:

tel: 1-800-548-4725 U.S. and Canada

tel: 708-296-9333 U.S. (from overseas)

tel: 44(0)1793-431155 Europe (U.K)

tel: 44(0)1792-421333 Germany

tel: 44(0)1793-421777 France

tel: 81(0)120-47-88-32 Japan (fax only)

IEEE Standard for an 8-bit Backplane Interface: STEbus
ANSI/IEEE 1000-1987

The Institute of Electrical and Electronic Engineers Inc.
345 East 47th Street
New York NY 10017
USA
ISBN 1-55937-002-5

PC/104 Specification, Version 2.2

PC/104 Consortium
P.O. Box 4303
Mountain View
CA 94040
USA

tel: 415-903-8304

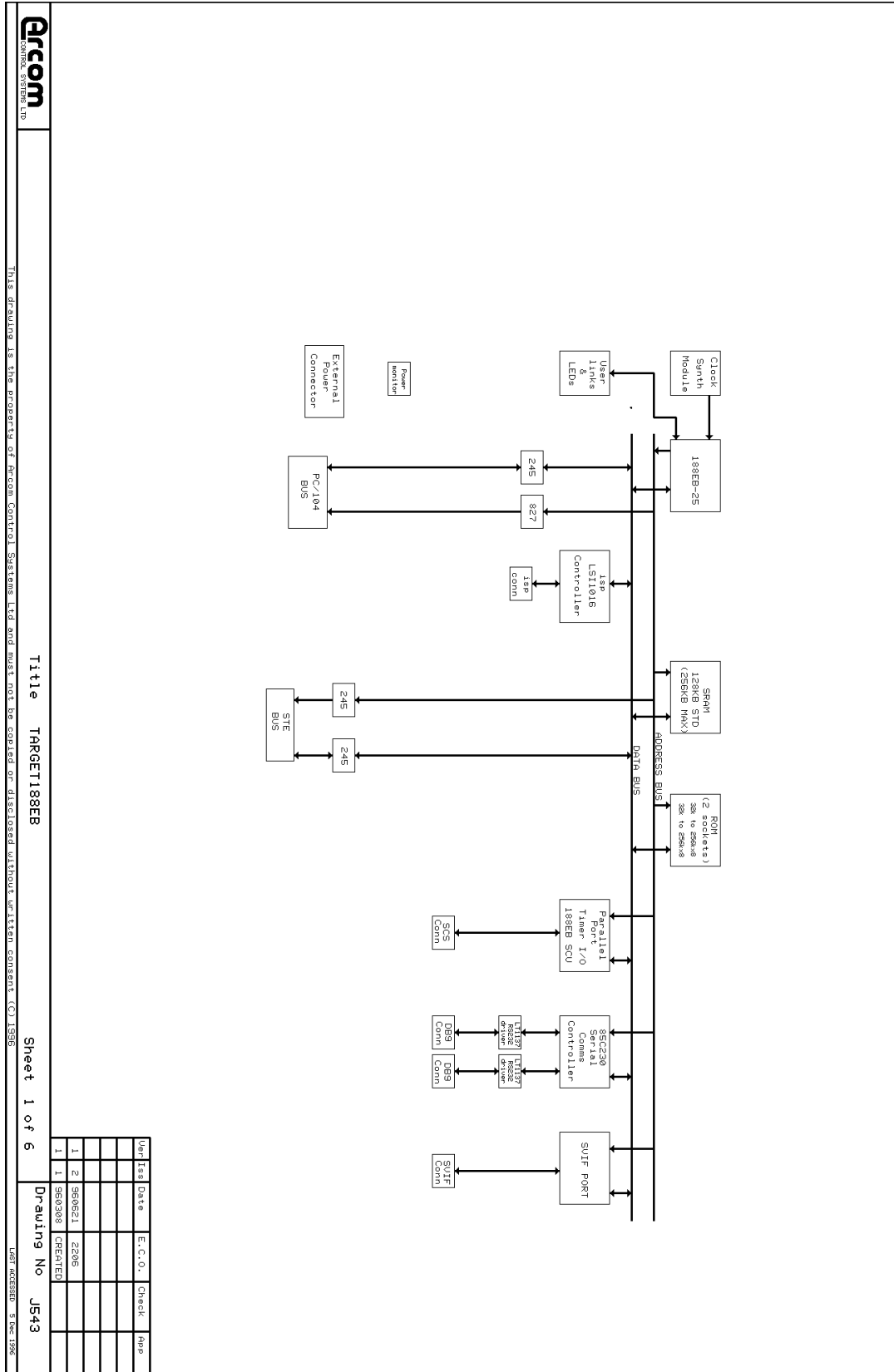
fax: 415-967-0995

IEEE P996 Draft Standard

IEEE Standards Office
445 Hoes Lane
Piscataway
NJ 08854
USA

Appendix E. Product Issue Changes

Appendix F. Circuit Diagrams



This drawing is the property of Arcom Control Systems Ltd and must not be copied or disclosed without written consent (C) 1996

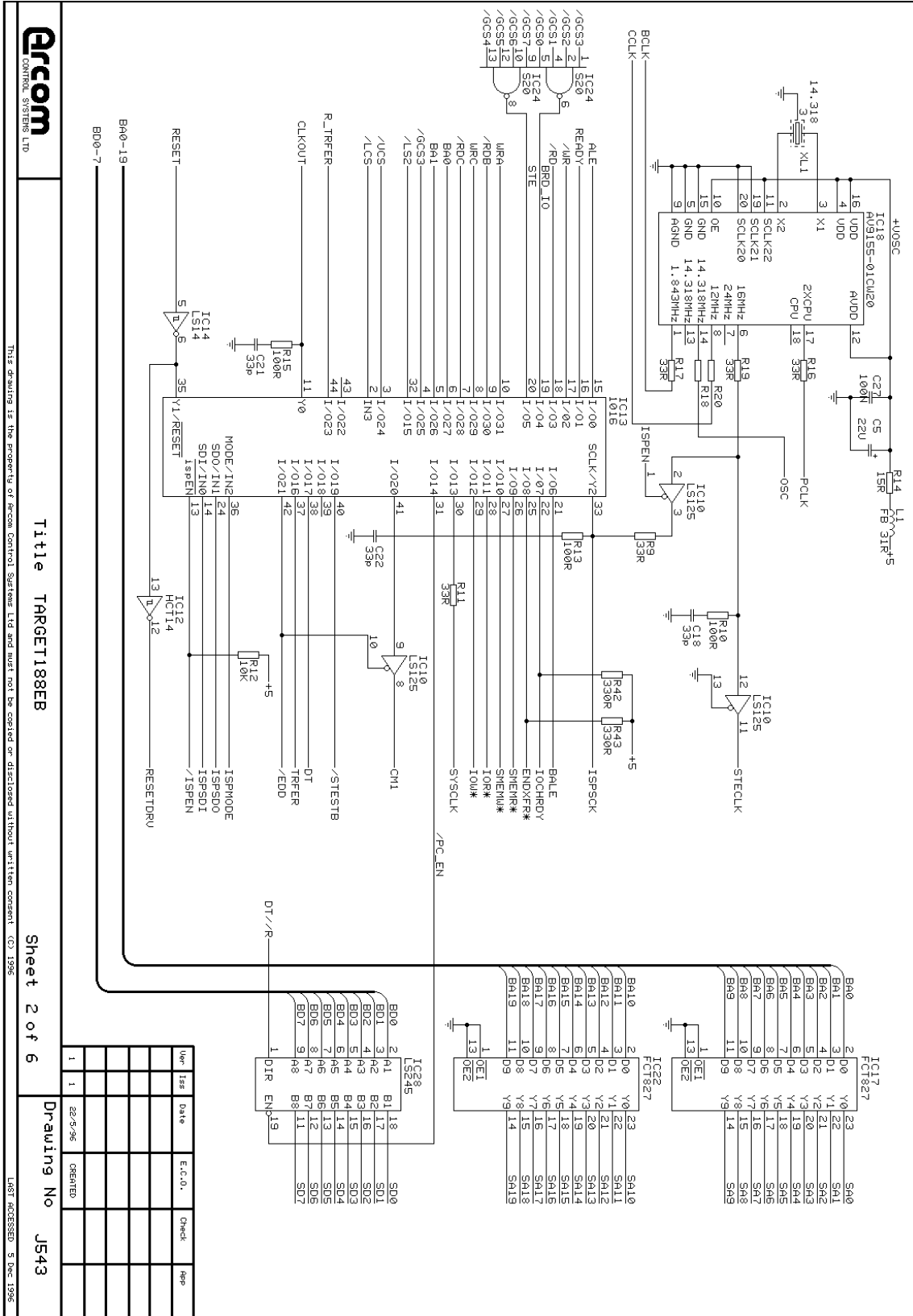
Title TARGET188EB

Sheet 1 of 6 Drawing No J543

Ver	Iss	Date	E.C.O.	Check	App
1	1	980621	2205		
1	1	980308	CREATED		

USER ACCESSIBLE 5 Dec 1996

Appendix F. Circuit Diagrams



Title TARGET188EB

Sheet 2 of 6

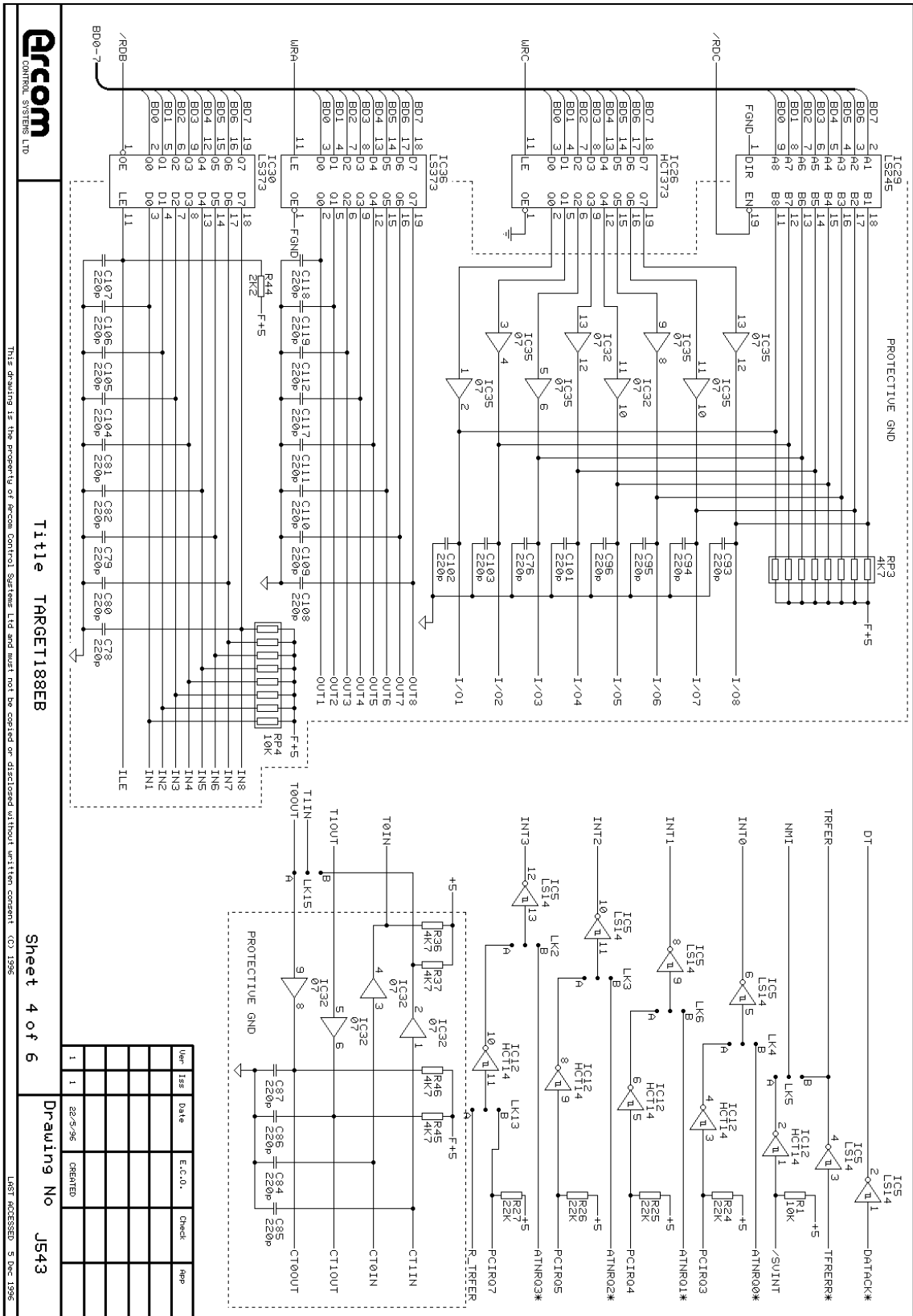
Drawing No J543

This drawing is the property of Arcom Control Systems Ltd and must not be copied or disclosed without written consent. © 1996

LAST REVISION: 5 Dec 1995

Ver	Iss	Date	E.C.O.	Check	App
1	1	22/5/96	CREATED		

Appendix F. Circuit Diagrams



Title TARGET188EB

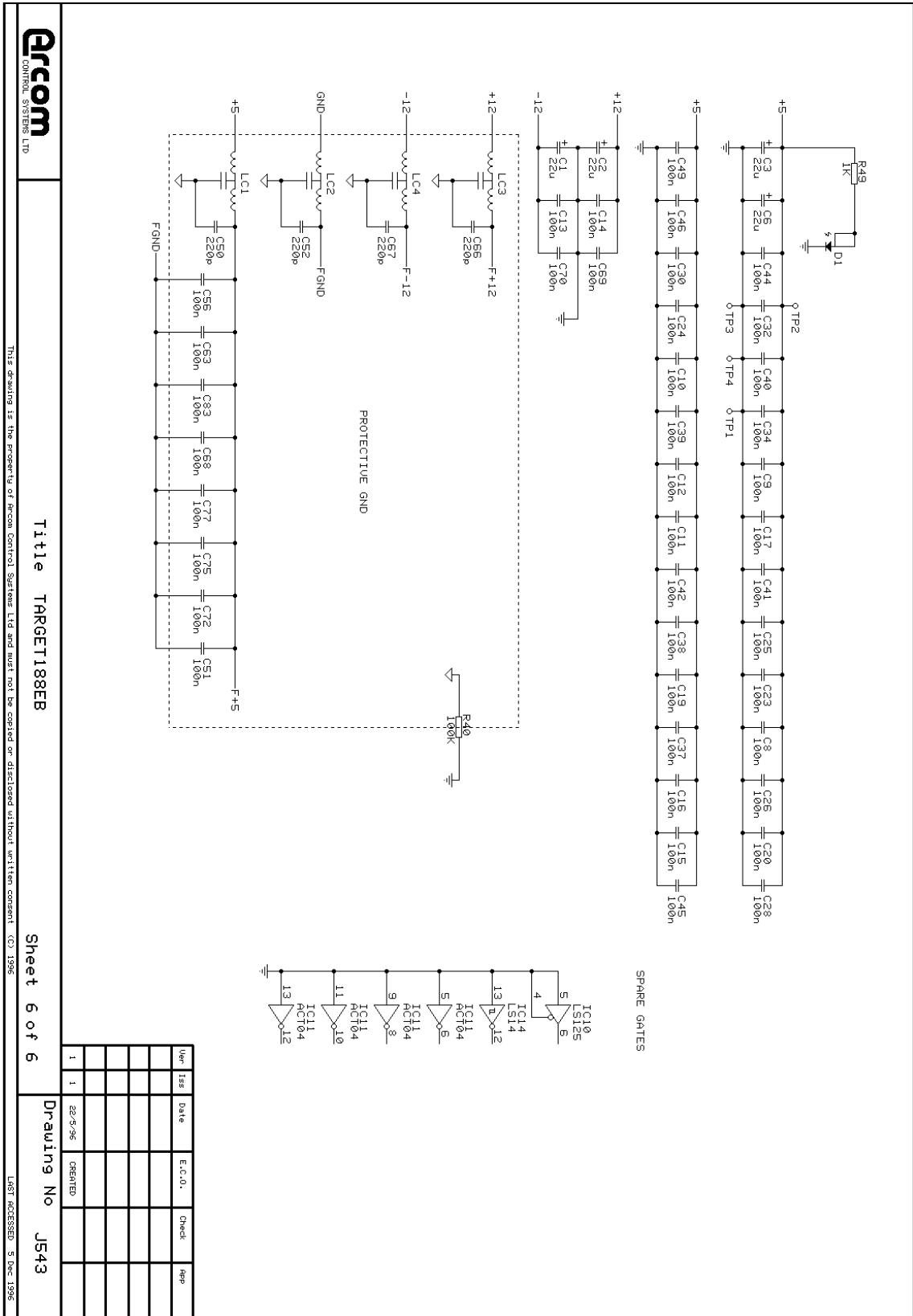
Sheet 4 of 6

Drawing No J543

This drawing is the property of Arcom Control Systems Ltd and must not be copied or disclosed without written consent. (C) 1996

LAST ACCESSSED 5 Dec 1996

No	Iss	Date	E.C.O.	Check	App
1	1	22/5/96	CREATED		



Title TARGET188EB

Sheet 6 of 6

Drawing No J543

This drawing is the property of Arcom Control Systems Ltd and must not be copied or disclosed without written consent © 1995

User	Iss	Date	E.C.O.	Check	App
1	1	22/5/96	CREATED		

LAST REVISION: 5 Dec 1995