

Evaluation Board for the **ADG5412BF**, Bidirectional Overvoltage Protected Quad SPST

FEATURES

Supply voltages

Dual supply: ± 5 V to ± 22 V

Single supply: 8 V to 44 V

Protected against overvoltage on switch pins

Signal voltages up to -55 V and $+55$ V

LED for visual overvoltage indication

Parallel interface compatible with 3 V logic

On-board LDO regulator for digital supply and control, if required

EVALUATION KIT CONTENTS

EVAL-ADG5412BFEBZ evaluation board

DOCUMENTS NEEDED

ADG5412BF data sheet

EVAL-ADG5412BFEBZ user guide

EQUIPMENT NEEDED

DC voltage source

± 22 V for dual supply

44 V for single supply

Optional digital voltage source: 3 V to 5 V

Analog signal source

Method to measure voltage, such as a DMM

GENERAL DESCRIPTION

The **EVAL-ADG5412BFEBZ** is the evaluation board for the **ADG5412BF**, which features four independently controlled single-pole/single-throw (SPST) switches. The **ADG5412BF** has overvoltage detection and protection circuitry on the switch pins and is protected against signals up to -55 V and $+55$ V in both the powered and unpowered states.

Figure 1 shows the **EVAL-ADG5412BFEBZ** in a typical evaluation setup. The **ADG5412BF** is soldered to the center of the evaluation board, and four wire screw terminals are provided to connect to each of the source and drain pins. Three screw terminals are used to power the device, with a fourth terminal used to provide a user defined digital voltage, if required. Alternatively, a low dropout (LDO) regulator is provided for 5 V digital voltage control and to supply the LED, which is mounted to provide visual indication of the fault status of the switch.

Full specifications on the **ADG5412BF** are available in the product data sheet, which should be consulted in conjunction with this user guide when using the evaluation board.

TYPICAL EVALUATION SETUP

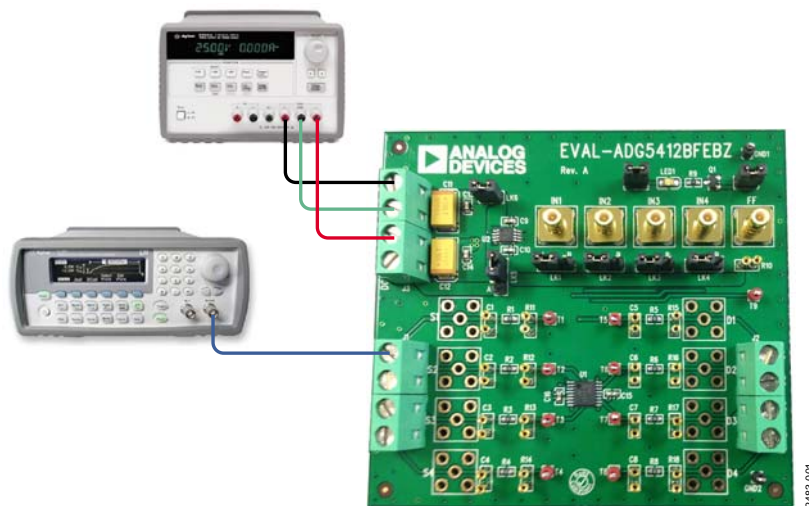


Figure 1. **EVAL-ADG5412BFEBZ** (on Right), Power Supply, and Signal Generator

TABLE OF CONTENTS

Features	1	Evaluation Board Setup Procedure	3
Evaluation Kit Contents.....	1	Evaluation Board Hardware.....	4
Documents Needed.....	1	Power Supply.....	4
Equipment Needed.....	1	Input Signals.....	4
General Description	1	Output Signals	4
Typical Evaluation Setup	1	Jumper Settings.....	5
Revision History	2	Link Headers.....	5
Getting Started	3	SMB Connectors.....	5

REVISION HISTORY

10/14—Revision 0: Initial Version

GETTING STARTED

EVALUATION BOARD SETUP PROCEDURE

The EVAL-ADG5412BFEBZ evaluation board is designed to be operated independently and does not require any additional evaluation boards or software to operate. An on-board LDO regulator is provided as the digital power supply for the LED and to manually control the ADG5412BF.

Supply the evaluation board with a dual power source of up to ±22 V or a single supply of up to 44 V by connecting VSS and GND together. If VDD is greater than 28 V, remove the header on Link LK6 to protect the on-board LDO regulator, and change the header on LK5 to Position A to use an alternative digital voltage supply connected to DC_V1.

A simple functionality test can be set up as follows:

1. Connect a power supply to J3. Connect VSS and GND together if a single supply is required.
2. Insert the header for LK6 to use the on-board LDO regulator, and place the header for LK5 to Position B.
3. LK1 through LK4 control the digital signals for each switch on the ADG5412BF.
 - a. In Position A, the switch is open and presents as an open circuit.
 - b. In Position B, the switch is closed and presents with a resistance of approximately 10 Ω.
4. The LED lights up to indicate that the switch is operating normally.

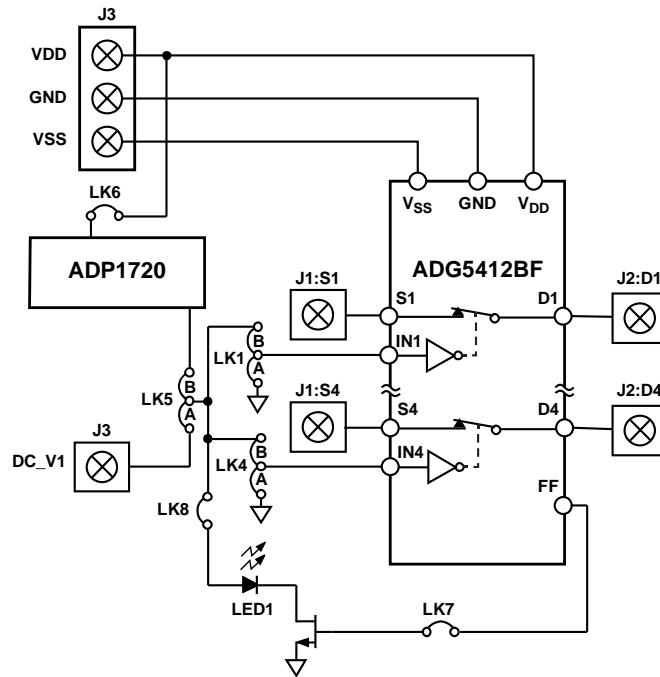


Figure 2. EVAL-ADG5412BFEBZ Block Diagram

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EVALUATION BOARD HARDWARE

The operation of the [ADG5412BF](#) is evaluated using the [EVAL-ADG5412BFEBZ](#). Figure 1 shows a typical evaluation setup where only a power supply and signal generator are required. Figure 2 shows the block diagram of the main components of the evaluation board.

Using this evaluation board, the [ADG5412BF](#) is used to pass signals from either the source or drain connectors. Both the source and drain pins have fault detection circuitry that react to an overvoltage event. During an overvoltage event, the switch is turned off, and the FF pin is pulled low. See the [ADG5412BF](#) data sheet for more details.

POWER SUPPLY

Connector J3 provides access to the supply pins of the [ADG5412BF](#). VDD, GND, and VSS link to the appropriate pins on the [ADG5412BF](#). For dual supply voltages, the evaluation board can be powered from ± 5 V to ± 22 V. For single supply voltages, the GND and VSS terminals must be connected together, and the evaluation board can be powered from 8 V to 44 V. Additionally, an on-board LDO regulator is provided for digital control voltage. A secondary voltage source can be connected to DC_V1 and used as the digital control voltages. To use DC_V1, place the header of LK5 into Position A. Do not expose the on-board LDO regulator to voltages greater than 28 V; remove LK6 and supply an alternative digital voltage via DC_V1, if required.

INPUT SIGNALS

Two 4-pin screw connectors are provided to connect to both the source and drain pins of the [ADG5412BF](#). Additional SMB connector pads are available if extra connections are required. The [ADG5412BF](#) is overvoltage protected on the source and drain sides, and each terminal (S1 to S4 or D1 to D4) can be presented with a voltage of up to +55 V or -55 V. See the [ADG5412BF](#) data sheet for more details.

Each trace on the source and drain side includes two sets of gold pin connectors, which can be used to place a load on the signal path to ground. A 0Ω resistor is placed in the signal path and can be replaced with a user defined value. The resistor combined with the gold pin connectors can be used to create a simple resistor-capacitor (RC) filter.

The [ADG5412BF](#) uses a parallel interface to control the operation of the switches. The switch operation can be manually controlled using the headers on LK1 to LK4, or an external controller can be interfaced directly to the control pins by using the SMB connectors (IN1 to IN4) and removing the link headers on LK1 to LK4.

OUTPUT SIGNALS

The only output from the [ADG5412BF](#) is the FF pin. This pin indicates the operating state of the device. On the evaluation board, the FF pin controls the operation of the LED. When the device is operating normally, the FF pin remains high, and the LED turns on. If an overvoltage is presented to any of the source pins, the FF pin is pulled low, and the LED turns off. An SMB connector is provided to interface the evaluation board with an external controller, and two gold pin connectors are provided to connect a pull-up resistor between the FF signal and the digital supply.

JUMPER SETTINGS

LINK HEADERS

The link headers are used to control the ADG5412BF manually, to configure the digital control voltage, and to isolate the LED from the rest of the system. Table 1 shows a summary of the link headers and how they are used on the evaluation board.

LK1 to LK4 are used to control the switches of the ADG5412BF. Position A opens each switch, and Position B closes the switch.

LK6 connects the on-board LDO regulator to the VDD supply. Remove this header to protect the LDO regulator from voltages higher than 28 V. Change the header on LK5 to Position A to use an alternative digital voltage connected to DC_V1.

LK8 connects the LED to the digital power supply, and LK7 connects the FF pin of the ADG5412BF to the LED control.

SMB CONNECTORS

The parallel interface of the ADG5412BF is controlled manually using the link headers of LK1 to LK4, or it can be accessed using the SMB connectors, IN1 to IN4. To use the SMB connectors, remove the link headers of LK1 to LK4. The FF SMB connector is used to access the FF digital output from the ADG5412BF.

Table 1. Link Header Descriptions

Link Header	Position	Description
LK1	A	S1/D1 switch open
	B	S1/D1 switch closed
LK2	A	S2/D2 switch open
	B	S2/D2 switch closed
LK3	A	S3/D3 switch open
	B	S3/D3 switch closed
LK4	A	S4/D4 switch open
	B	S4/D4 switch closed
LK5	A	On-board LDO regulator digital voltage
	B	DC_V1 digital voltage
LK6	Inserted	LDO regulator powered up
	Removed	LDO regulator unpowered
LK7	Inserted	FF pin connected to LED
	Removed	FF pin disconnected from LED
LK8	Inserted	LED connected to digital supply
	Removed	LED isolated



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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