Precision 5 Volt Reference

FEATURES

- Very Low Drift – 2ppm/°C Max TC
- Pin Compatible with LT1021-5, REF-02
- Output Sources 15mA, Sinks 10mA
- Excellent Transient Response Suitable for A-to-D Reference Inputs
- Noise Reduction Pin
- Excellent Long-Term Stability
- Less Than 1ppm p-p Noise (0.1Hz to 10Hz)

APPLICATIONS

- A-to-D and D-to-A Converters
- Digital Voltmeters
- Reference Standard
- Precision Current Source

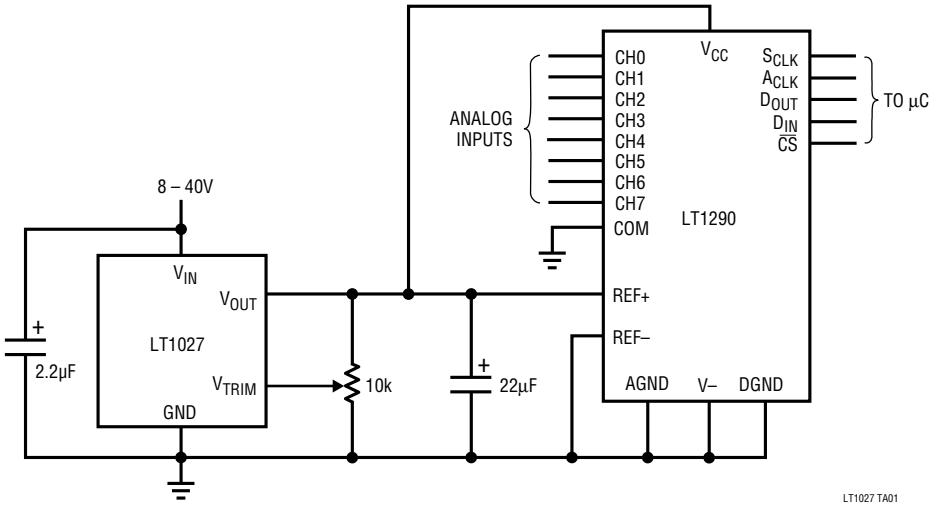
DESCRIPTION

The LT1027 is a precision reference with extra-low drift, superior accuracy, excellent line and load regulation and low output impedance at high frequency. This device is intended for use in 12- to 16-bit A-to-D and D-to-A systems where demanding accuracy requirements must be met without the use of power-hungry heated-substrate references. The fast-settling output recovers quickly from load transients such as those presented by A-to-D converter reference inputs. The LT1027 brings together both outstanding accuracy and temperature coefficient specifications.

The LT1027 reference is based on LTC's proprietary advanced sub-surface zener bipolar process which eliminates noise and stability problems associated with surface-breakdown devices.

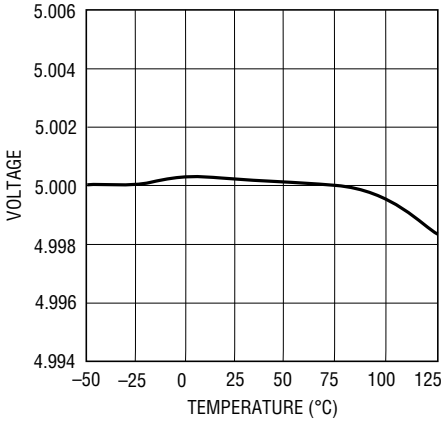
TYPICAL APPLICATION

Supplying V_{REF} and V_{CC} to the LTC1290 12-bit ADC



LT1027 TA01

Output Voltage

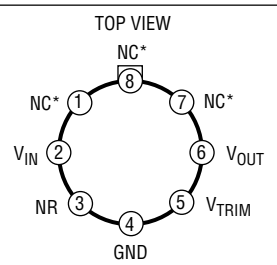


LT1027 G03

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{IN}) 40V
Input-Output Voltage Differential 35V
Output to Ground Voltage 7V
V_{TRIM} to Ground Voltage
  Positive 5V
  Negative ..... –0.3V
Output Short Circuit Duration
  V_{IN} > 20V ..... 10 sec
  V_{IN} ≤ 20V ..... Indefinite
Operating Temperature Range
  LT1027M ..... –55°C to 125°C
  LT1027C ..... 0°C to 70°C
Storage Temperature Range
  All Devices ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

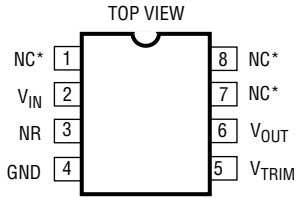
PACKAGE/ORDER INFORMATION



H PACKAGE
8-LEAD TO-5 METAL CAN

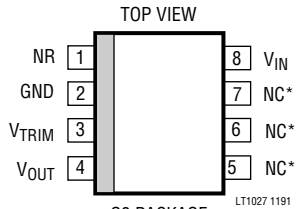
ORDER PART NUMBER

LT1027ACH
LT1027BCH
LT1027CCH
LT1027DCH
LT1027ECH
LT1027DMH
LT1027EMH



N8 PACKAGE
8-LEAD PLASTIC DIP

LT1027BCN8
LT1027CCN8
LT1027DCN8
LT1027ECN8



S8 PACKAGE
8-LEAD PLASTIC SOIC

LT1027ECS8

* CONNECTED INTERNALLY. DO NOT CONNECT EXTERNAL CIRCUITRY TO THESE PINS.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 10V, I_{LOAD} = 0, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	Output Voltage (Note 1)	LT1027A LT1027B, C, D LT1027E		4.999 4.9975 4.995	5.000 5.000 5.000	5.001 5.0025 5.005	V
TCV_{OUT}	Output Voltage Temperature Coefficient (Note 2)	LT1027A, B LT1027C LT1027D LT1027E	● ● ● ●		1 2 2 3	2 3 5 7.5	ppm/°C
	Line Regulation (Note 3)	8V ≤ V_{IN} ≤ 10V	 ●		6	12 25	ppm/V
		10V ≤ V_{IN} ≤ 40V			3	6	ppm/V
			●			8	ppm/mA
	Load Regulation (Note 3)	Sourcing Current 0 ≤ I_{OUT} ≤ 15mA	 ●		3	6 8	ppm/V
		Sinking Current 0 ≥ I_{OUT} ≥ –10mA	 ●		30	50 100	ppm/mA

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{IN} = 10V, I_{LOAD} = 0, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Supply Current		 ●		1.8	2.4 2.8	mA
	V_{TRIM} Adjust Range		●	±30	±50		mV
e_n	Output Noise (Note 4)	0.1Hz ≤ f ≤ 10Hz			3		μVp-p
		10Hz ≤ f ≤ 1kHz			2.0	4.0	μV_{RMS}
	Temperature Hysteresis	H package; ΔT = 25°C			10		ppm
	Long Term Stability	H package			20		ppm/month

The ● denotes specifications which apply over the operating temperature range.

Note 1: Output voltage is measured immediately after turn-on. Changes due to chip warm-up are typically less than 0.005%.

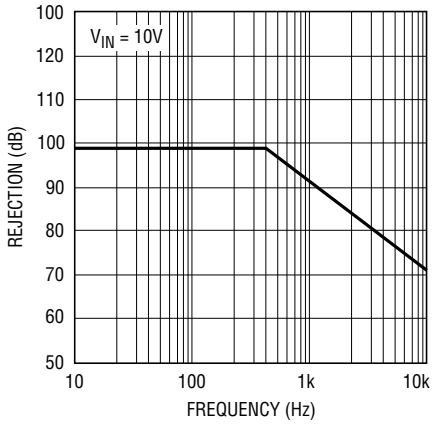
Note 2: Temperature coefficient is determined by the "box" method in which the maximum ΔV_{OUT} over the temperature range is divided by ΔT.

Note 3: Line and load regulation measurements are done on a pulse basis. Output voltage changes due to die temperature change must be taken into account separately. Package thermal resistance is 150°C/W for TO-5 (H), 130°C/W for plastic DIP (N8), and 180°C/W for plastic SOIC (S8).

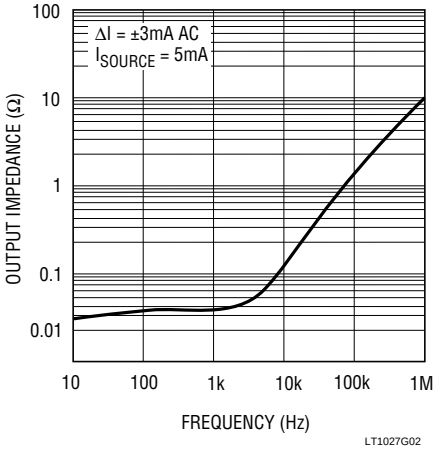
Note 4: RMS noise is measured with an 8-pole bandpass filter with a center frequency of 30Hz and a Q of 1.5. The filter output is then rectified and integrated for a fixed time period, resulting in an average, as opposed to RMS voltage. A correction factor is used to convert average to RMS. This value is then used to obtain RMS noise voltage in the 10Hz to 1000Hz frequency band. This test also screens for low-frequency "popcorn" noise within the bandwidth of the filter. Consult factory for 100% 0.1Hz to 10Hz noise testing.

TYPICAL PERFORMANCE CHARACTERISTICS

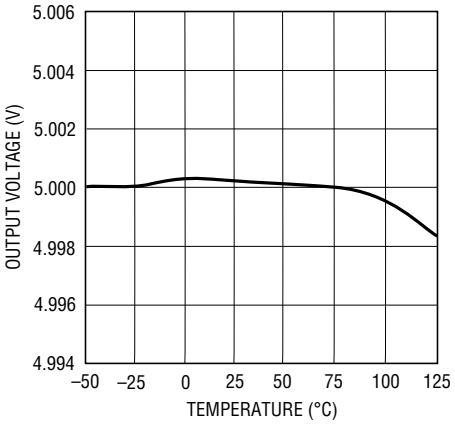
Ripple Rejection



Output Impedance vs Frequency

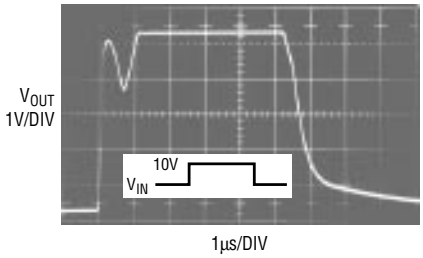


Output Voltage

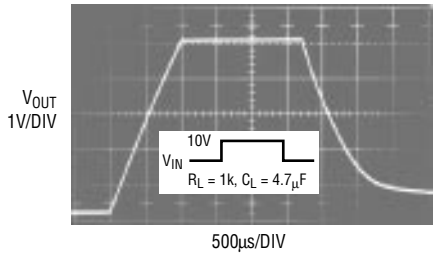


TYPICAL PERFORMANCE CHARACTERISTICS

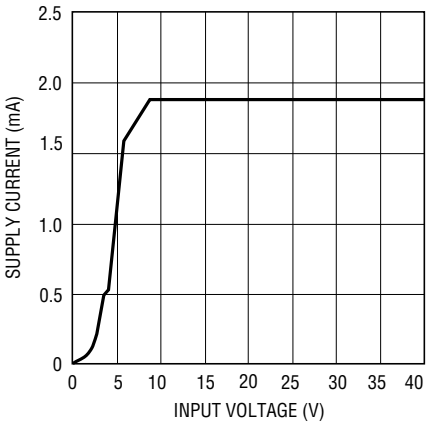
Start-Up and Turn-Off (No Load)



Start-Up and Turn-Off

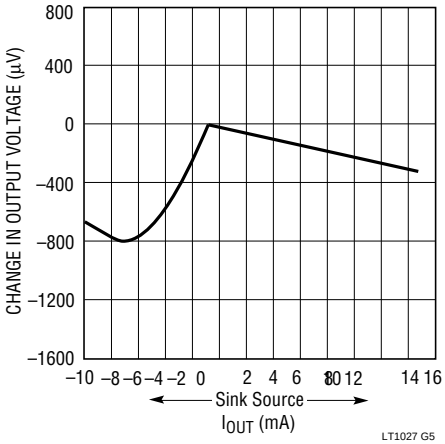


Quiescent Current



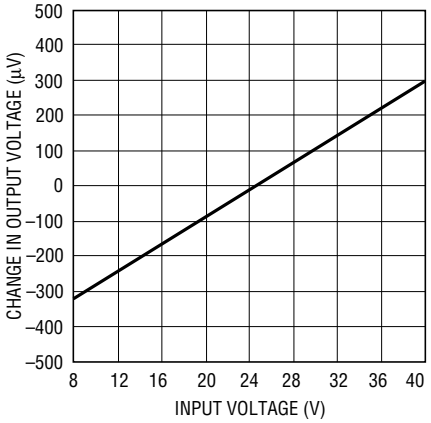
LT1027 G04

Load Regulation



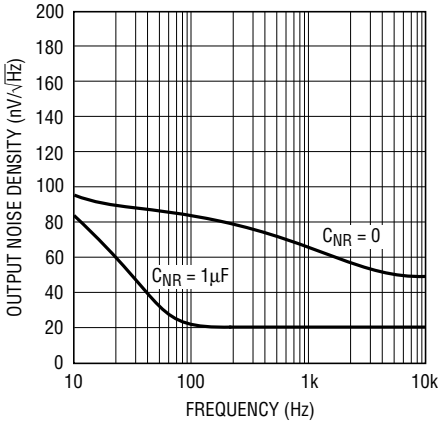
LT1027 G5

Line Regulation



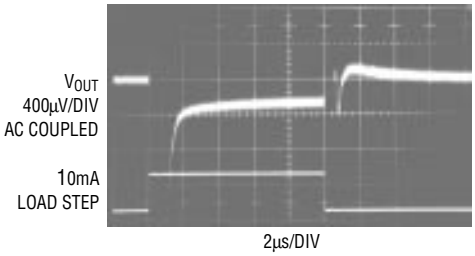
LT1027 G6

Output Noise Voltage Density

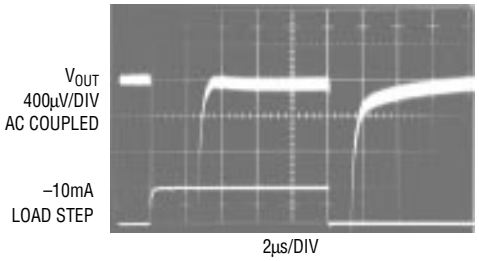


LT1027 G8

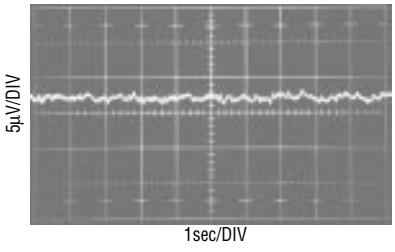
Output Settling Time (Sourcing)



Output Settling Time (Sinking)



0.1Hz to 10Hz Output Noise
Filtering = 1 zero at 0.1Hz
2 poles at 10Hz

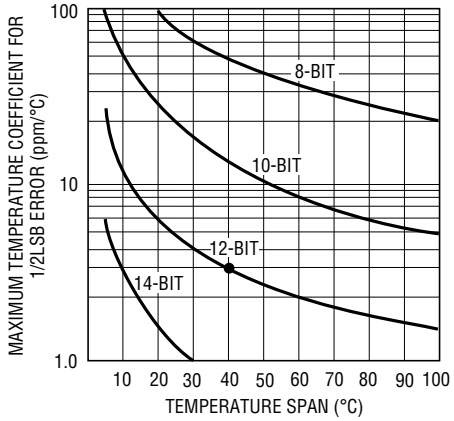


APPLICATIONS INFORMATION

Effect of Reference Drift on System Accuracy

A large portion of the temperature drift error budget in many systems is the system reference voltage. This graph indicates the maximum temperature coefficient allowable if the reference is to contribute no more than 1/2LSB error to the overall system performance. The example shown is a 12-bit system designed to operate over a temperature range from 25°C to 65°C. Assuming the system calibration is performed at 25°C, the temperature span is 40°C. It can be seen from the graph that the temperature coefficient of the reference must be no worse than 3ppm/°C if it is to contribute less than 1/2LSB error. For this reason, the LT1027 has been optimized for low drift.

Maximum Allowable Reference Drift



Trimming Output Voltage

The LT1027 has an adjustment pin for trimming output voltage. The impedance of the V_{ADJ} pin is about 20kΩ with an open circuit voltage of 2.5V. A ±30mV guaranteed trim range is achievable by tying the V_{ADJ} pin to the wiper of a 10k potentiometer connecting between the output and ground. Trimming output voltage does not affect the TC of the device.

Noise Reduction

The positive input of the internal scaling amplifier is brought out as the Noise Reduction (NR) pin. Connecting a 1μF Mylar capacitor between this pin and ground will reduce the wideband noise of the LT1027 from 2.0μV_{RMS} to approximately 1.2μV_{RMS} in a 10Hz to 1kHz bandwidth. Transient response is not affected by this capacitor. Start-up settling time will increase to several milliseconds due to the 7kΩ impedance looking into the NR pin. The capacitor *must* be a low-leakage type. Electrolytics are *not* suitable for this application. Just 100nA leakage current will result in a 150ppm error in output voltage. This pin is the most sensitive pin on the device. For maximum protection a guard ring is recommended. The ring should be driven from a resistive divider from V_{OUT} set to 4.4V (the open circuit voltage on the NR pin).

Transient Response

The LT1027 has been optimized for transient response. Settling Time is under 2μs when an AC-coupled 10mA load transient is applied to the output. The LT1027 achieves fast settling by using a class B NPN/PNP output stage. When sinking current, the device may oscillate with capacitive loads greater than 100pF. The LT1027 is stable with all capacitive loads when at no DC load or when sourcing current, although for best settling time either no output bypass capactor or a 4.7μF tantalum unit is recommended. An 0.1μF ceramic output capacitor will *maximize output ringing* and is *not* recommended.

Kelvin Connections

Although the LT1027 does not have true force-sense capability, proper hook-up can improve line loss and ground loop problems significantly. Since the ground pin of the LT1027 carries only 2mA, it can be used as a low-side sense line, greatly reducing ground loop problems on the low side of the reference. The V_{OUT} pin should be close to the load or connected via a heavy trace as the resistance of this trace directly affects load regulation. It is important to remember that a 1.22mV drop due to trace resistance is equivalent to a 1LSB error in a 5VFS, 12-bit system.

The circuits in Figures 1 and 2 illustrate proper hook-up to minimize errors due to ground loops and line losses. Losses in the output lead can be further reduced by adding a PNP boost transistor if load current is 5mA or higher. R2 can be added to further reduce current in the output sense load.

APPLICATIONS INFORMATION

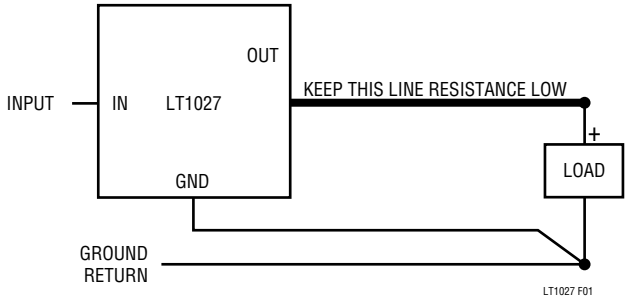


Figure 1. Standard Hook-Up

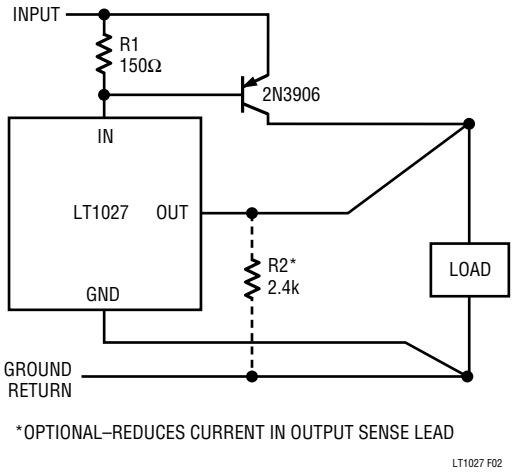
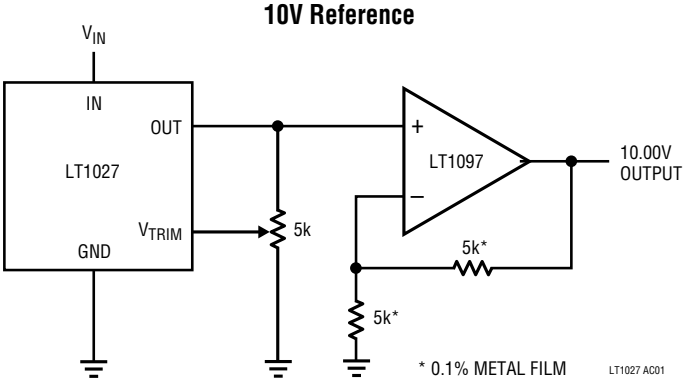


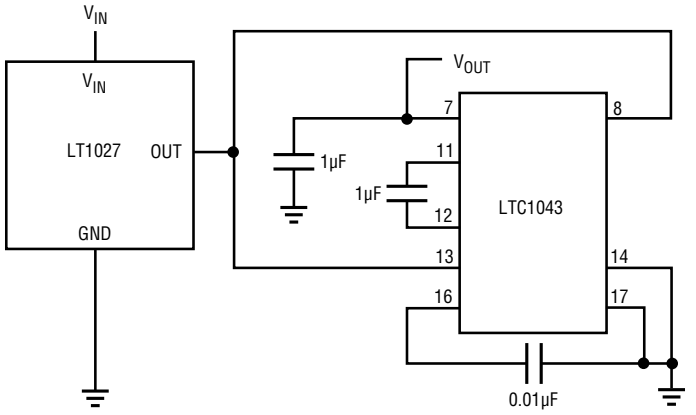
Figure 2. Driving Higher Load Currents

APPLICATION CIRCUITS

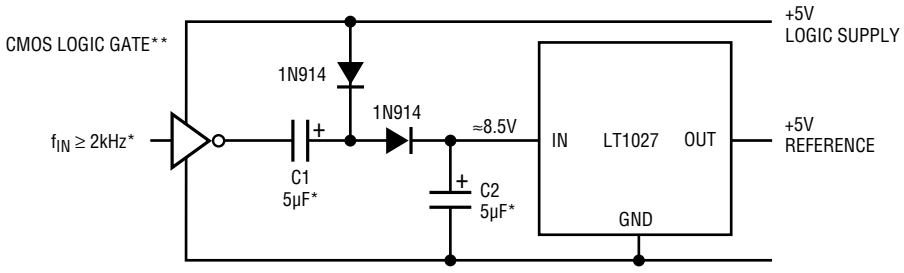
10V Reference



10V Reference



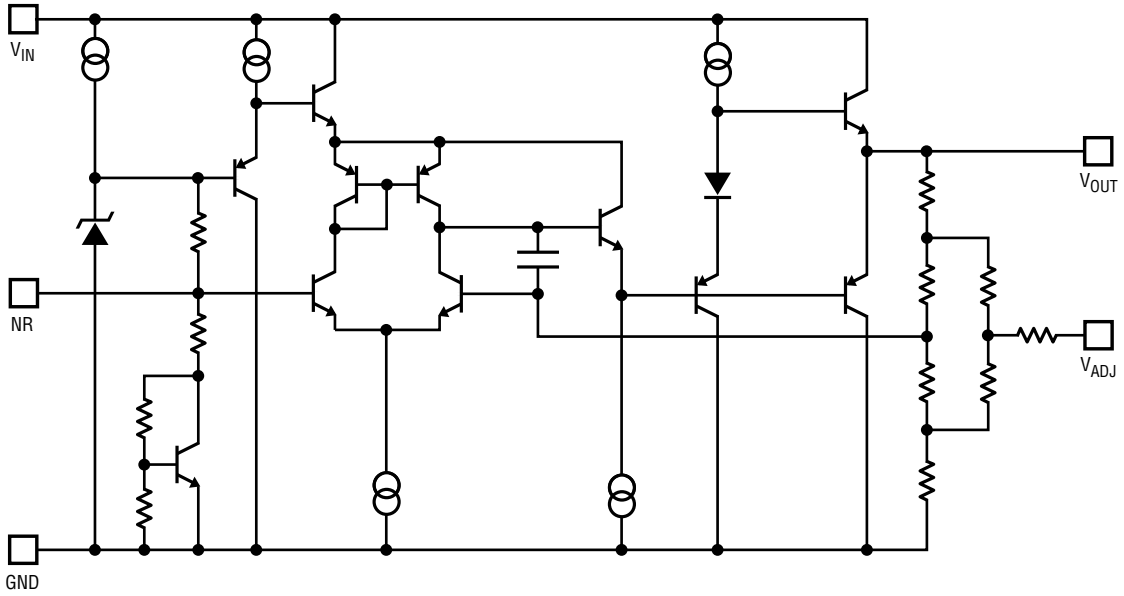
Operating 5V Reference from 5V Supply



*FOR HIGHER FREQUENCIES C1 AND C2 MAY BE DECREASED.
**PARALLEL GATES FOR HIGHER REFERENCE CURRENT LOADING.

LT1027 AC03

EQUIVALENT SCHEMATIC



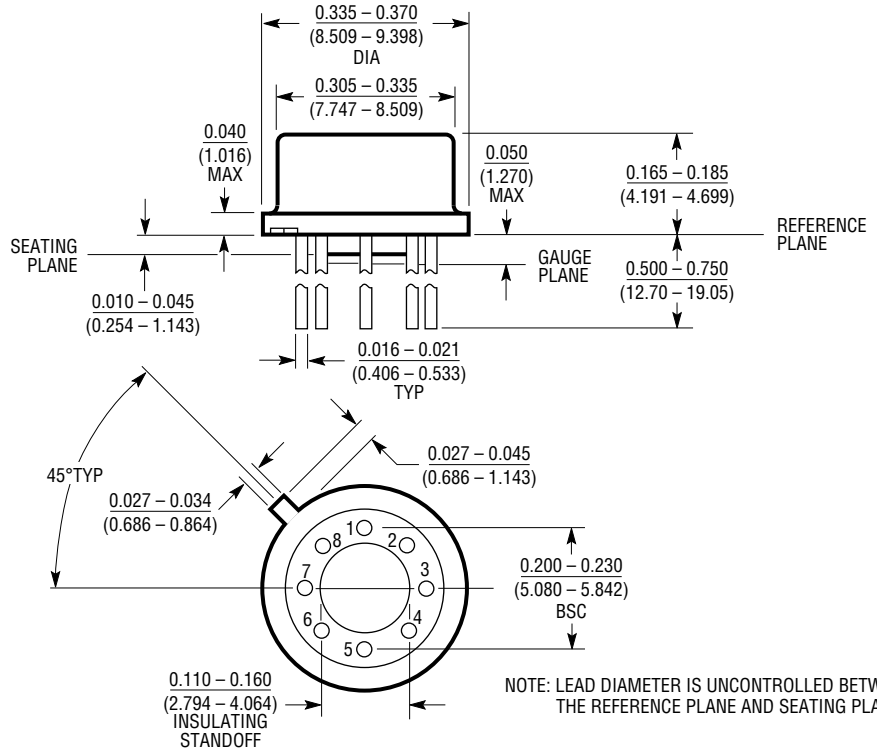
OUTPUT CURRENT LIMIT AND
BIAS CIRCUITS NOT SHOWN.

LT1027 ES01

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

H8 Package
8-Lead TO-5 Metal Can



T_{JMAX}	θ_{JA}	θ_{JC}
150°C	150°C/W	45°C/W

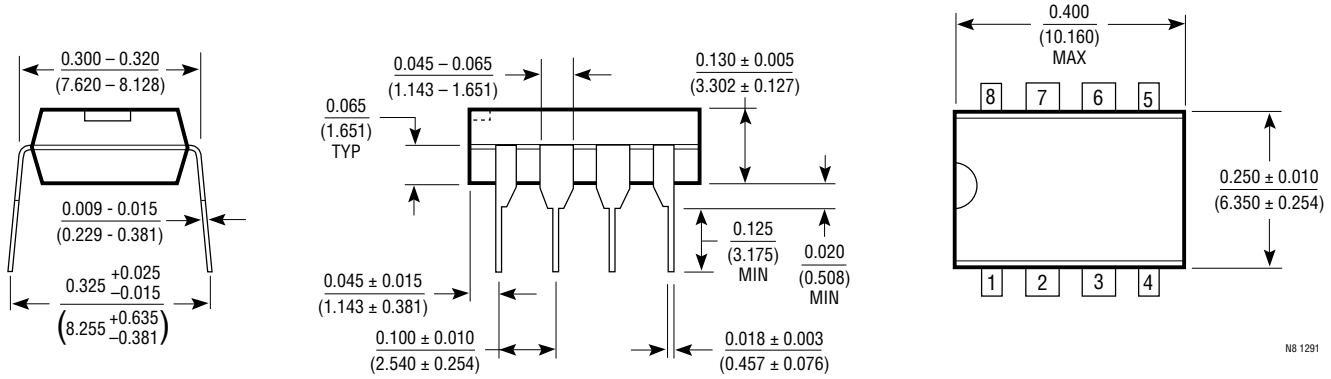
NOTE: LEAD DIAMETER IS UNCONTROLLED BETWEEN
THE REFERENCE PLANE AND SEATING PLANE.

H8 1191

PACKAGE DESCRIPTION

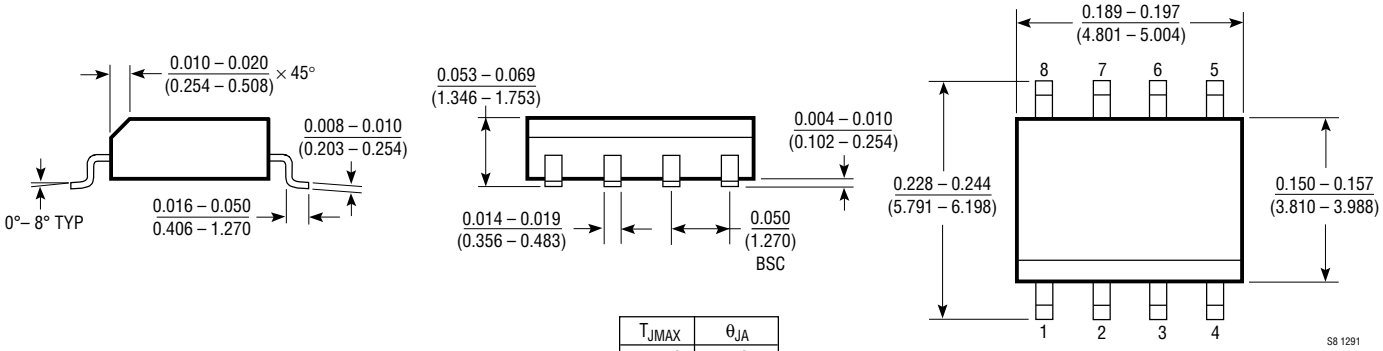
Dimensions in inches (millimeters) unless otherwise noted.

N8 Package
8-Lead Plastic DIP



T_{JMAX}	θ_{JA}
100°C	130°C/W

S8 Package
8-Lead SOIC



T_{JMAX}	θ_{JA}
100°C	180°C/W

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LT/GP 1291 10K REV 0