



STV240N75F3

N-channel 75 V, 2.3 mΩ, 200 A STripFET™ III Power MOSFET in PowerSO-10 package

Datasheet — production data

Features

Order code	V _{DSS}	R _{DS(on)} max	I _D (1)
STV240N75F3	75 V	< 2.6 mΩ	200 A

1. Current limited by package

- Conduction losses reduced
- Low profile, very low parasitic inductance

Applications

- Switching applications

Description

This device is an N-channel enhancement mode Power MOSFET produced using STMicroelectronics' STripFET™ III technology, which is specifically designed to minimize on-resistance and gate charge to provide superior switching performance.

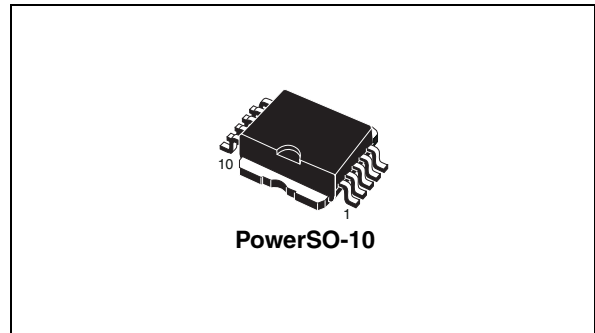


Figure 1. Internal schematic diagram

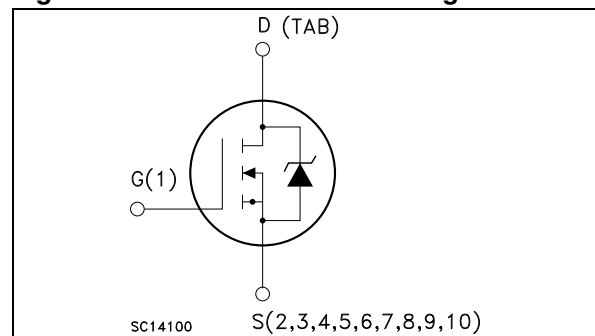


Figure 2. Connection diagram (top view)

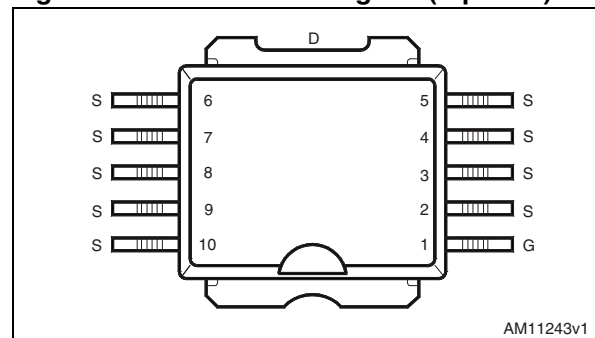


Table 1. Device summary

Order code	Marking	Package	Packaging
STV240N75F3	240N75F3	PowerSO-10	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	75	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	200	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	170	A
$I_{DM}^{(2)}$	Drain current (pulsed)	800	A
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	300	W
	Derating factor	2.0	W/ $^\circ\text{C}$
$E_{AS}^{(4)}$	Single pulse avalanche energy	600	mJ
T_{stg}	Storage temperature	-55 to 175	$^\circ\text{C}$
T_j	Operating junction temperature		$^\circ\text{C}$

1. Current limited by package
2. Pulse width limited by safe operating area
3. This value is rated according to R_{thj-c}
4. Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = 60\text{ A}$, $V_{DD} = 15\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.5	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	35	$^\circ\text{C/W}$

1. When mounted on 1 inch² FR-4 2 oz Cu.

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	75			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 75\text{ V}$, $V_{DS} = 75\text{ V}$, $T_C = 125\text{ °C}$			10 100	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 200	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on- resistance	$V_{GS} = 10\text{ V}$, $I_D = 120\text{ A}$		2.3	2.6	m Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	6800	-	pF
C_{oss}	Output capacitance			1100		pF
C_{rss}	Reverse transfer capacitance			50		pF
Q_g	Total gate charge	$V_{DD} = 37.5\text{ V}$, $I_D = 120\text{ A}$,	-	85	-	nC
Q_{gs}	Gate-source charge	$V_{GS} = 10\text{ V}$		30		nC
Q_{gd}	Gate-drain charge	(see Figure 15 and Figure 20)		26		nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 37.5\text{ V}$, $I_D = 60\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$, (see Figure 14 and Figure 19)	-	25	-	ns
t_r	Rise time			70		ns
$t_{d(off)}$	Turn-off delay time		-	100	-	ns
t_f	Fall time			15		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		200	A
$I_{SD}^{(2)}$	Source-drain current (pulsed)				800	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 120\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 120\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 20\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 21)	-	80		ns
Q_{rr}	Reverse recovery charge			180		nC
I_{RRM}	Reverse recovery current			4.5		A

1. Current limited by package
2. Pulse width limited by safe operating area
3. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 3. Safe operating area

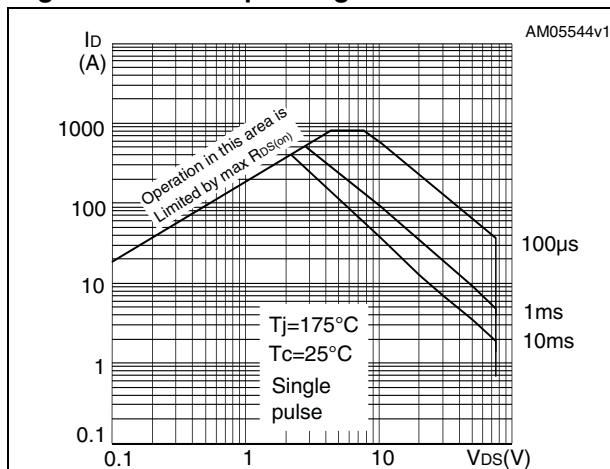


Figure 4. Thermal impedance

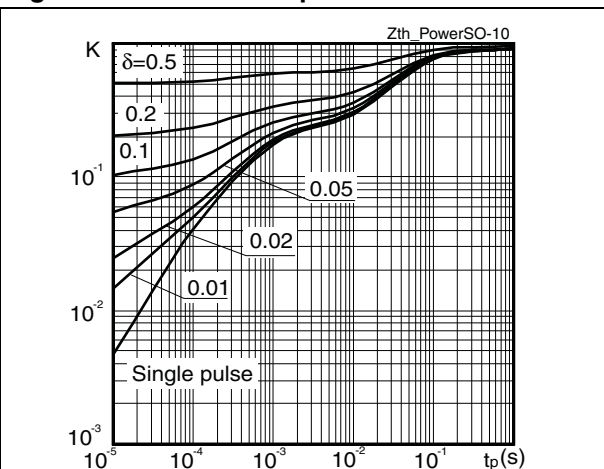


Figure 5. Output characteristics

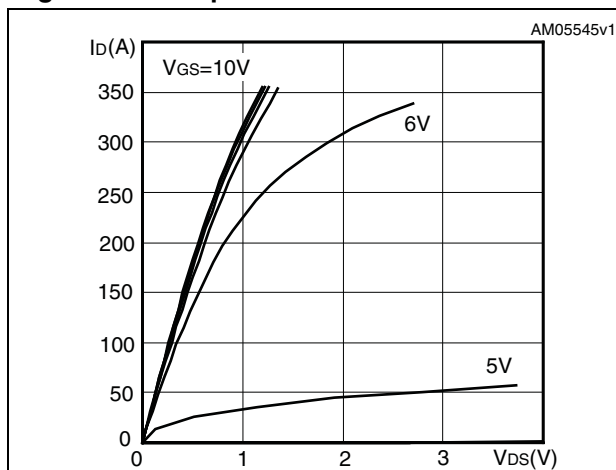


Figure 6. Transfer characteristics

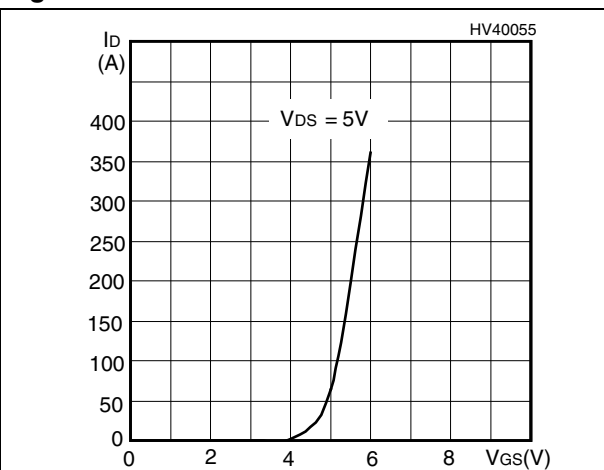
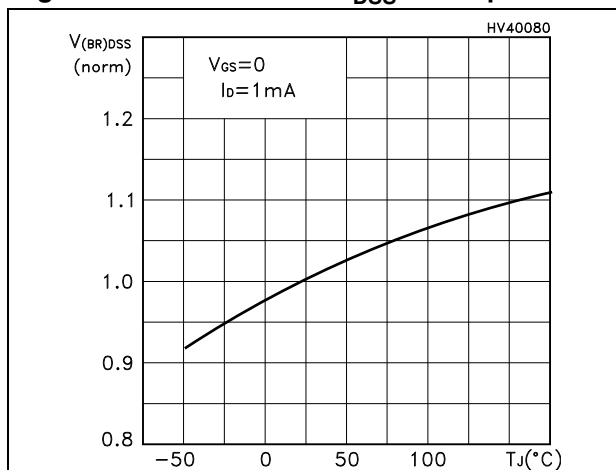
Figure 7. Normalized BV_{DSS} vs temperature

Figure 8. Static drain-source on-resistance

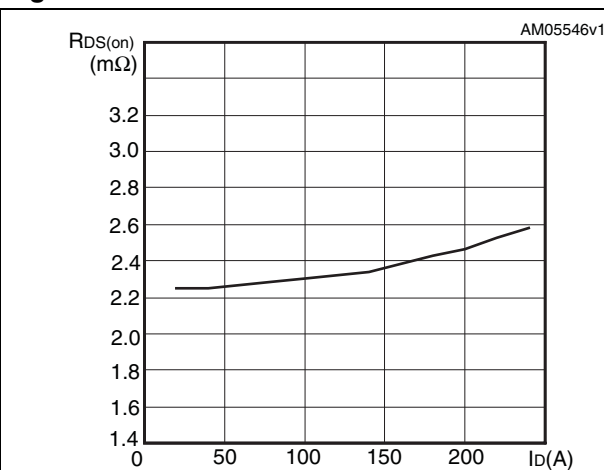


Figure 9. Gate charge vs gate-source voltage Figure 10. Capacitance variations

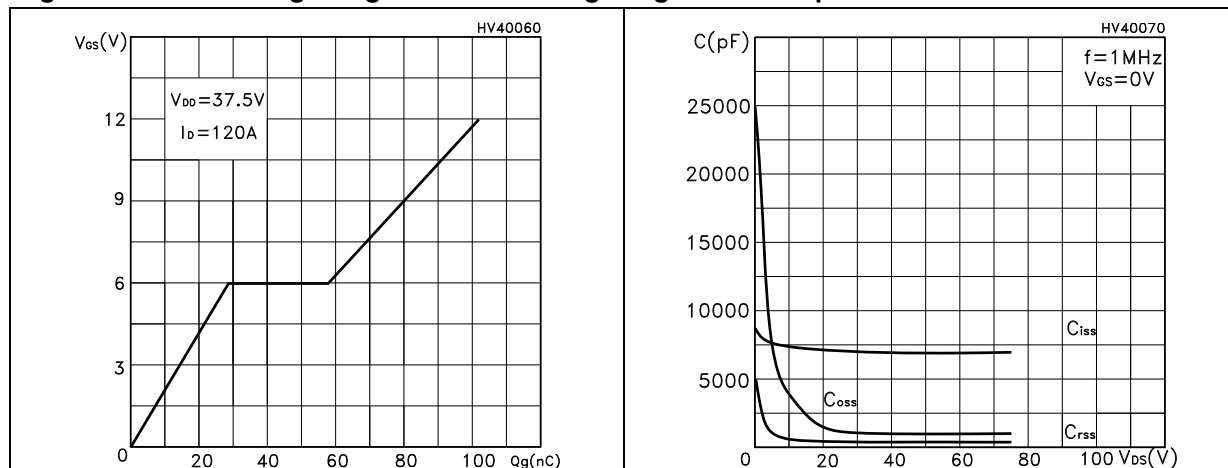


Figure 11. Normalized gate threshold voltage vs temperature Figure 12. Normalized on-resistance vs temperature

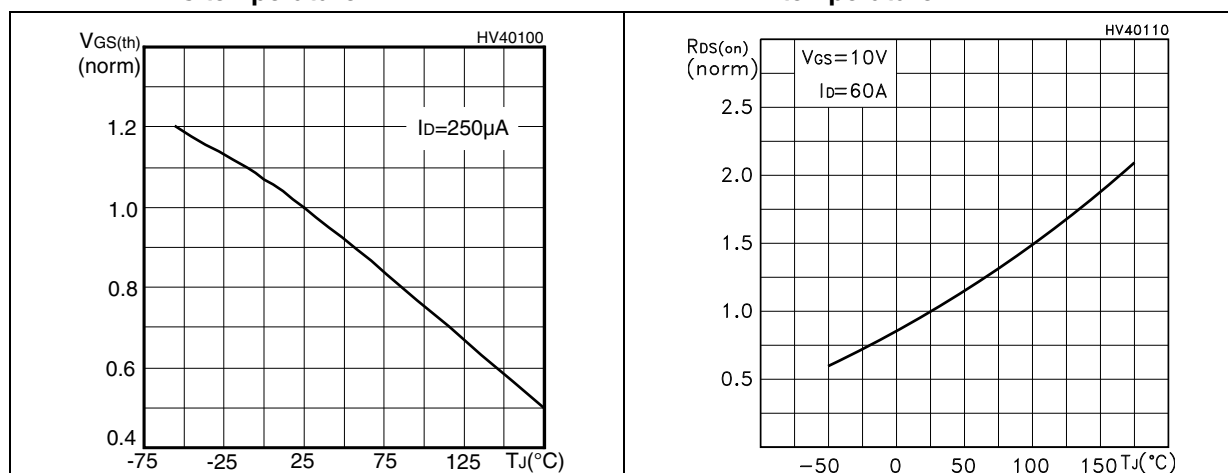
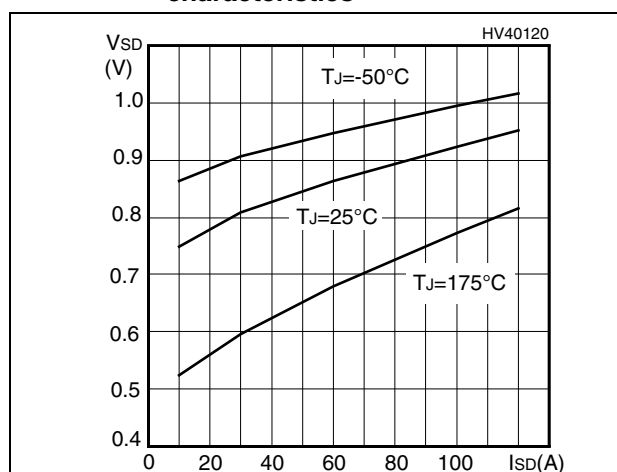


Figure 13. Source-drain diode forward characteristics



3 Test circuits

Figure 14. Switching times test circuit for resistive load

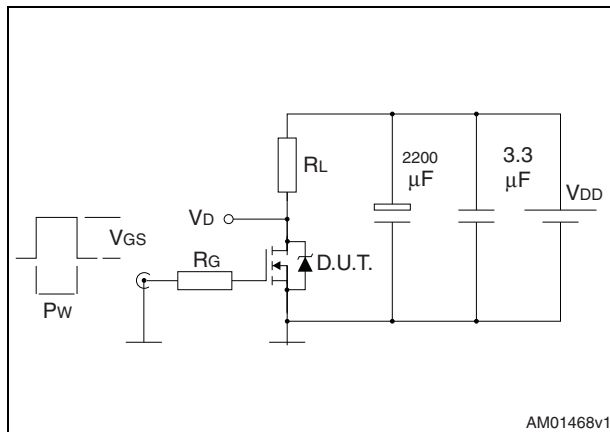


Figure 15. Gate charge test circuit

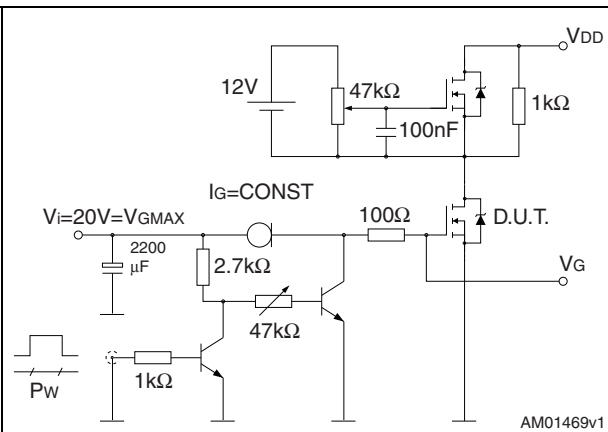


Figure 16. Test circuit for inductive load switching and diode recovery times

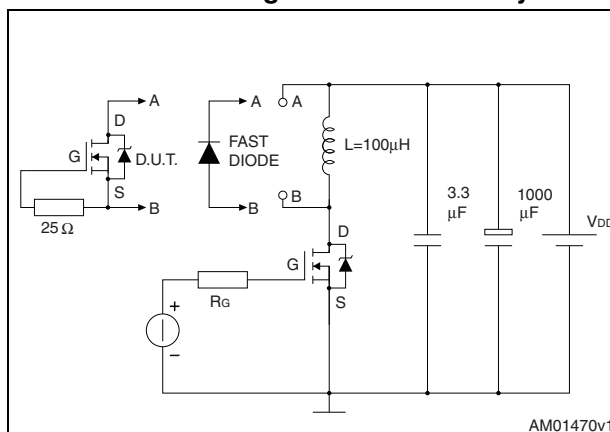


Figure 17. Unclamped inductive load test circuit

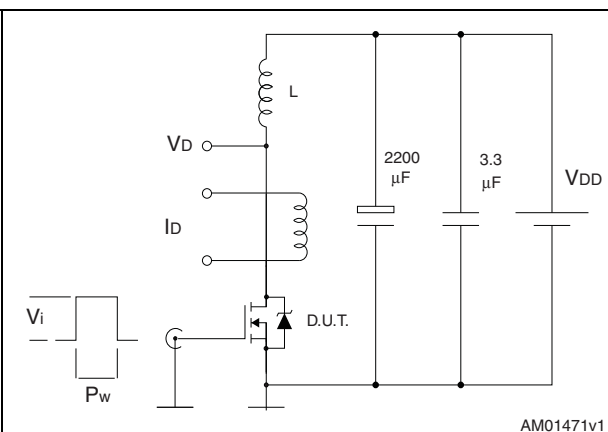


Figure 18. Unclamped inductive waveform

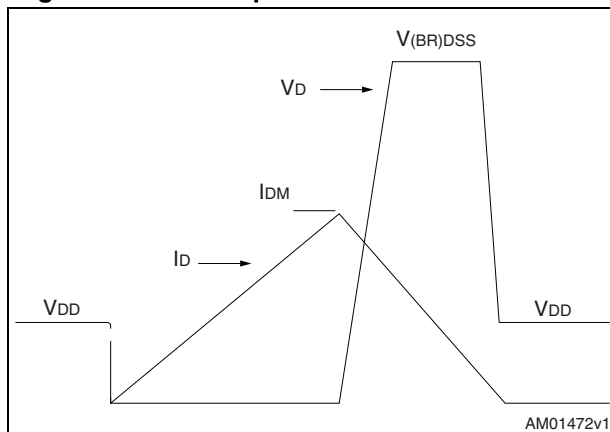


Figure 19. Switching time waveform

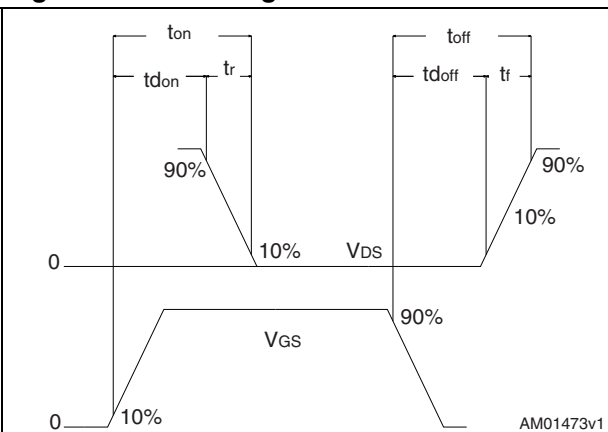


Figure 20. Gate charge test waveform

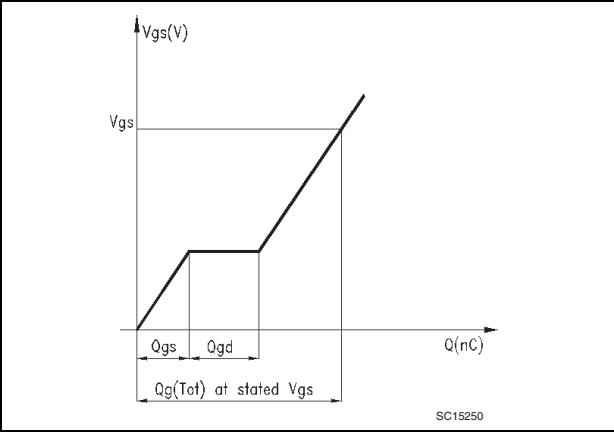
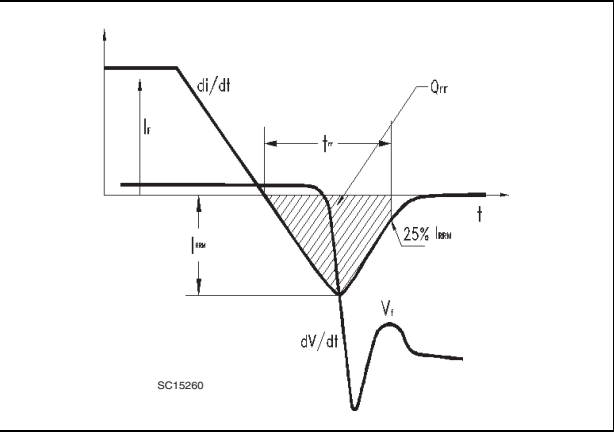


Figure 21. Diode recovery times waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. PowerSO-10 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			3.70
A1	0.00		0.10
A2	3.40		3.60
A3	1.25		1.35
b	0.40		0.53
c	0.35		0.55
D	9.40		9.60
D1 ⁽¹⁾	7.40		7.60
E	13.80		14.40
E1 ⁽¹⁾	9.30		9.50
E2	7.20		7.60
E3	5.90		6.10
e		1.27	
L	0.95		1.65
<	0°		8°

1. Resin protrusion not included (max value: 0.20 mm per side)

Figure 22. PowerSO-10 drawing

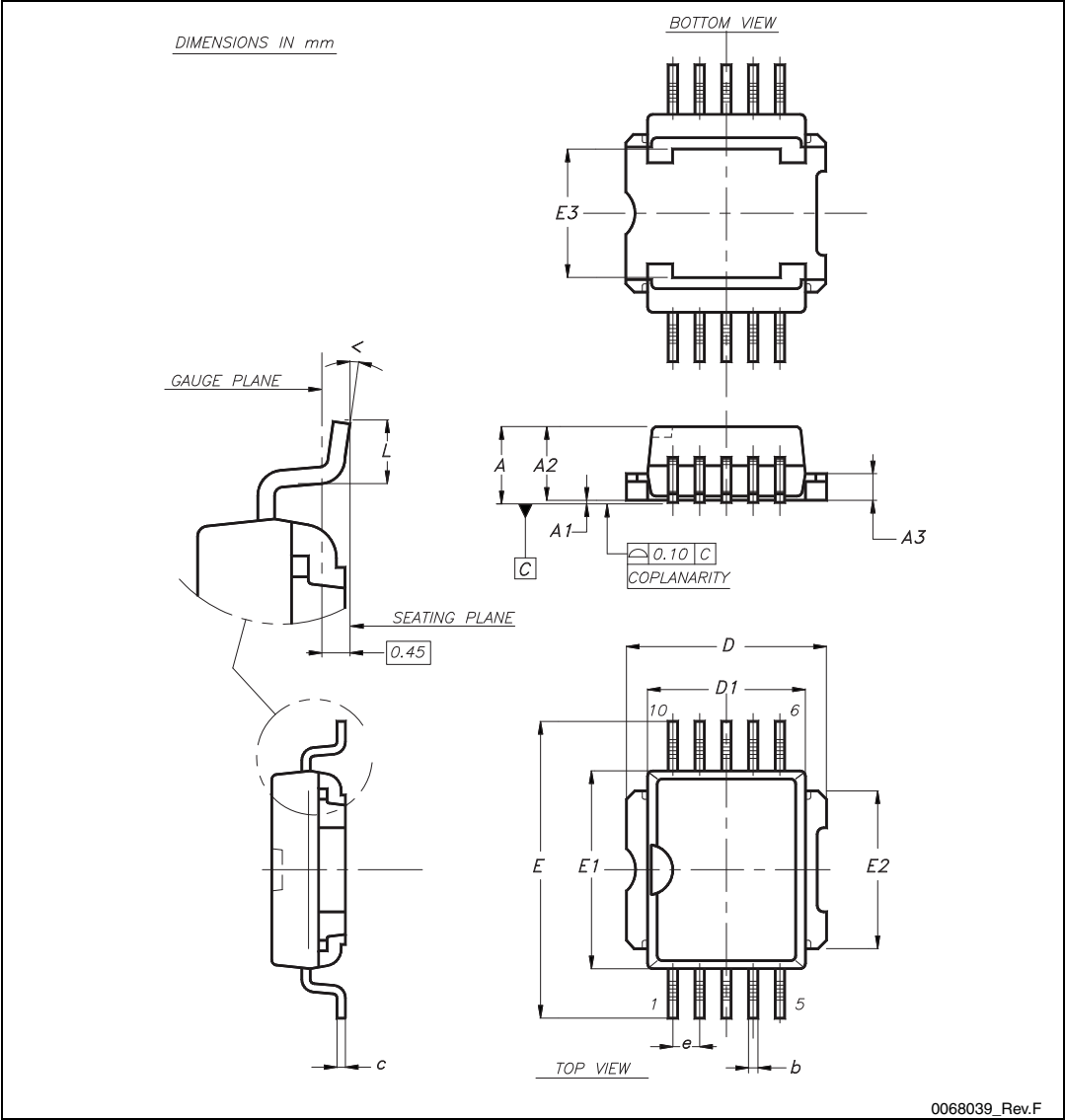
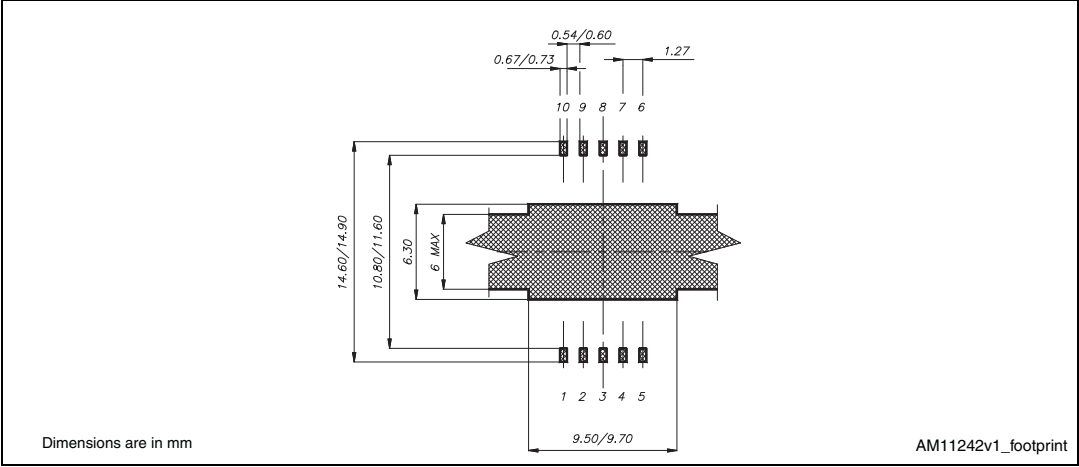


Figure 23. PowerSO-10 recommended footprint



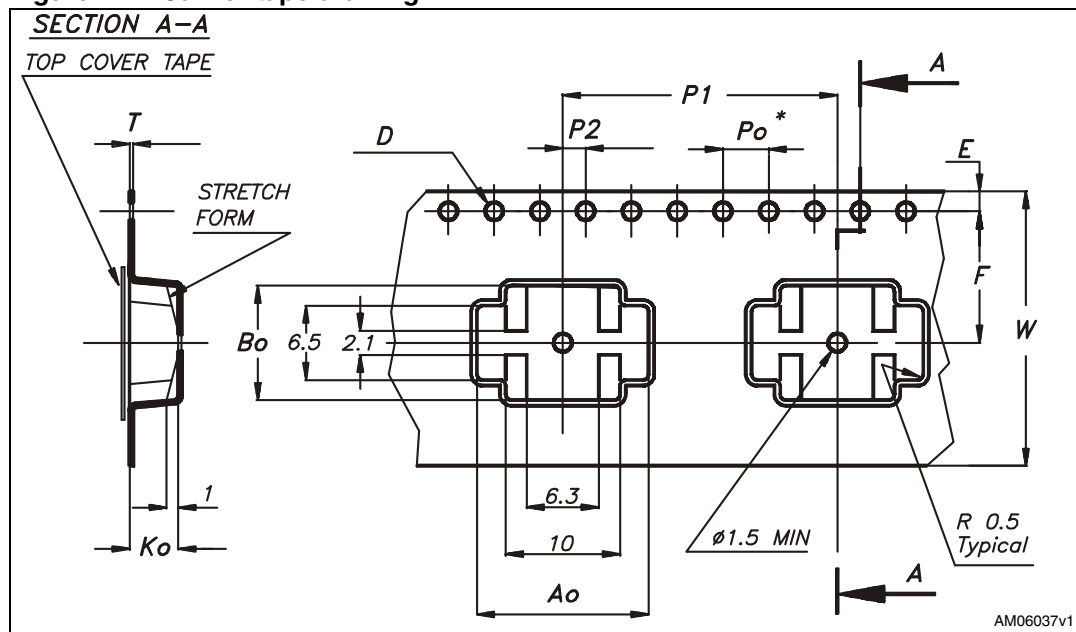
5 Packaging mechanical data

Table 9. Carrier tape dimensions

Ref.	mm		
	Min.	Typ.	Max.
A0	14.9	15.0	15.1
B0	9.9	10.0	10.1
K0	4.15	4.25	4.35
F	11.4	11.5	11.6
E	1.65	1.75	1.85
W	23.7	24.0	24.3
P2	1.9	2.0	2.1
P0	3.9	4.0	4.1
P1	23.9	24.0	24.1
T	0.025	0.30	0.35
D(Ø)	1.50	1.55	1.60

Note: 10 sprocket hole pitch cumulative tolerance ± 0.2 mm.

Figure 24. Carrier tape drawing (a)



a. Drawing is not to scale.

Table 10. Reel dimensions

Ref.	mm		
	Min.	Typ.	Max.
A			330
B	1.5		
C	12.8	13	13.2
D	20.2		
N	60		
G		24.4	
T			30.4

Note: 10 sprocket hole pitch cumulative tolerance ± 0.2 mm.

Figure 25. Reel drawing (b)

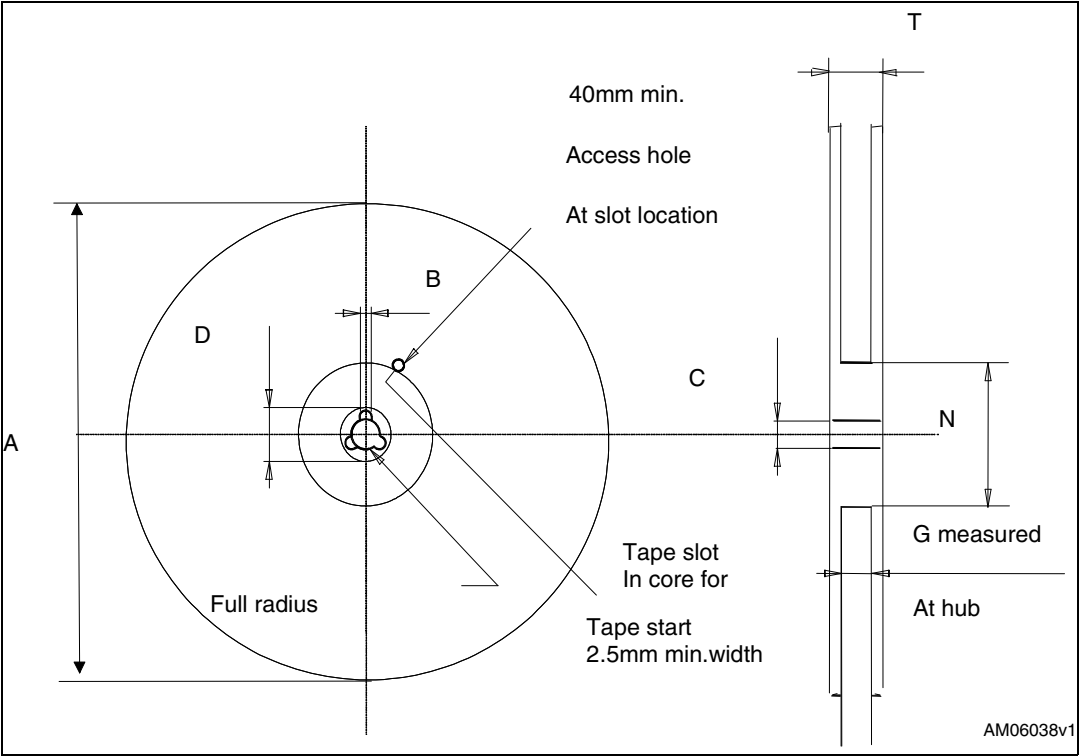


Table 11. Base/bulk quantities

Base qty.	Bulk qty.
	600

b. Drawing is not to scale.

6 Revision history

Table 12. Document revision history

Date	Revision	Changes
02-Apr-2008	1	Initial release
21-Jan-2010	2	– Document status promoted from preliminary data to datasheet. – Inserted new Section 5: Packaging mechanical data.
4-May-2012	3	Section 4: Package mechanical data has been updated: – Figure 23: PowerSO-10 recommended footprint has been added. – Minor text changes.

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