

Overview

ARIS is a development board oriented to Internet-of-Things application design, based on Renesas Synergy platform.

ARIS includes

- Renesas Synergy Cortex CPU
- On-board RAM and Flash memories
- Ethernet connectivity
- Wi-Fi module
- Bluetooth Low-Energy (4.1) module
- NFC transponder
- Inertial and environmental sensors

Revision History

R0.1

- ARIS schematic created

R0.9

- ARIS schematic - draft status

R0.9.1

- Fiducials added
- BLE optional SPI connection added

R1.0

- First prototypes

R1.1

- Production revision

Manufacturing / Mechanical

+ FM1	+ FM2
+ FM3	+ FM4
+ FM5	+ FM6

Notes



Arrow



Renesas Synergy



Segger

Title: **ARIS Board**

Section: Overview

Size: A4

Project code: PCBR15P02

Revision: R1.1.6

Date: 14/04/2016

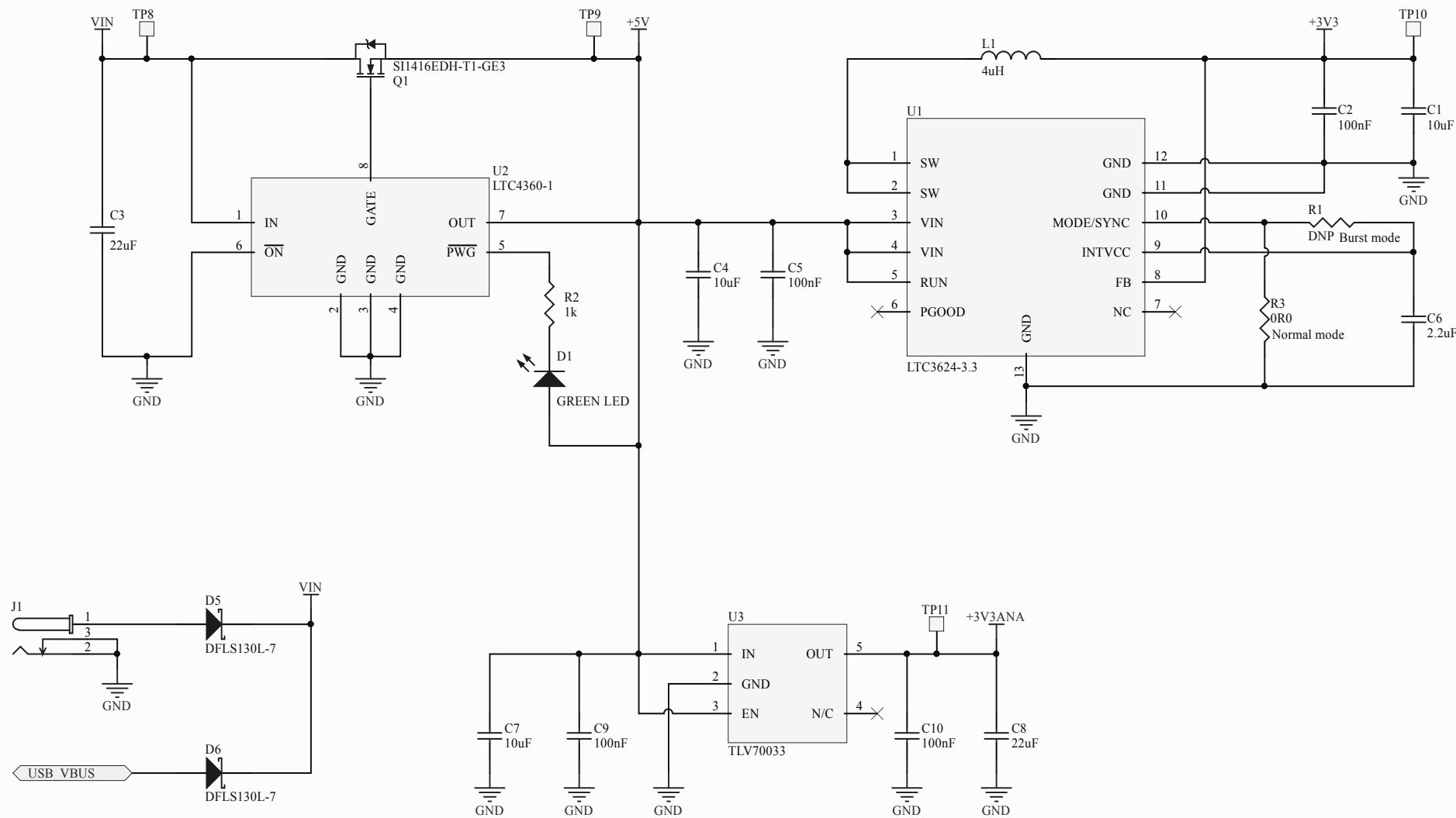
Time: 18:22:56

Sheet 1 of 14

File: Overview.SchDoc



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Title: **ARIS Board**

Section: **Power Supply**

Size: **A4** Project code: **PCBR15P02**

Revision: **R1.1.6**

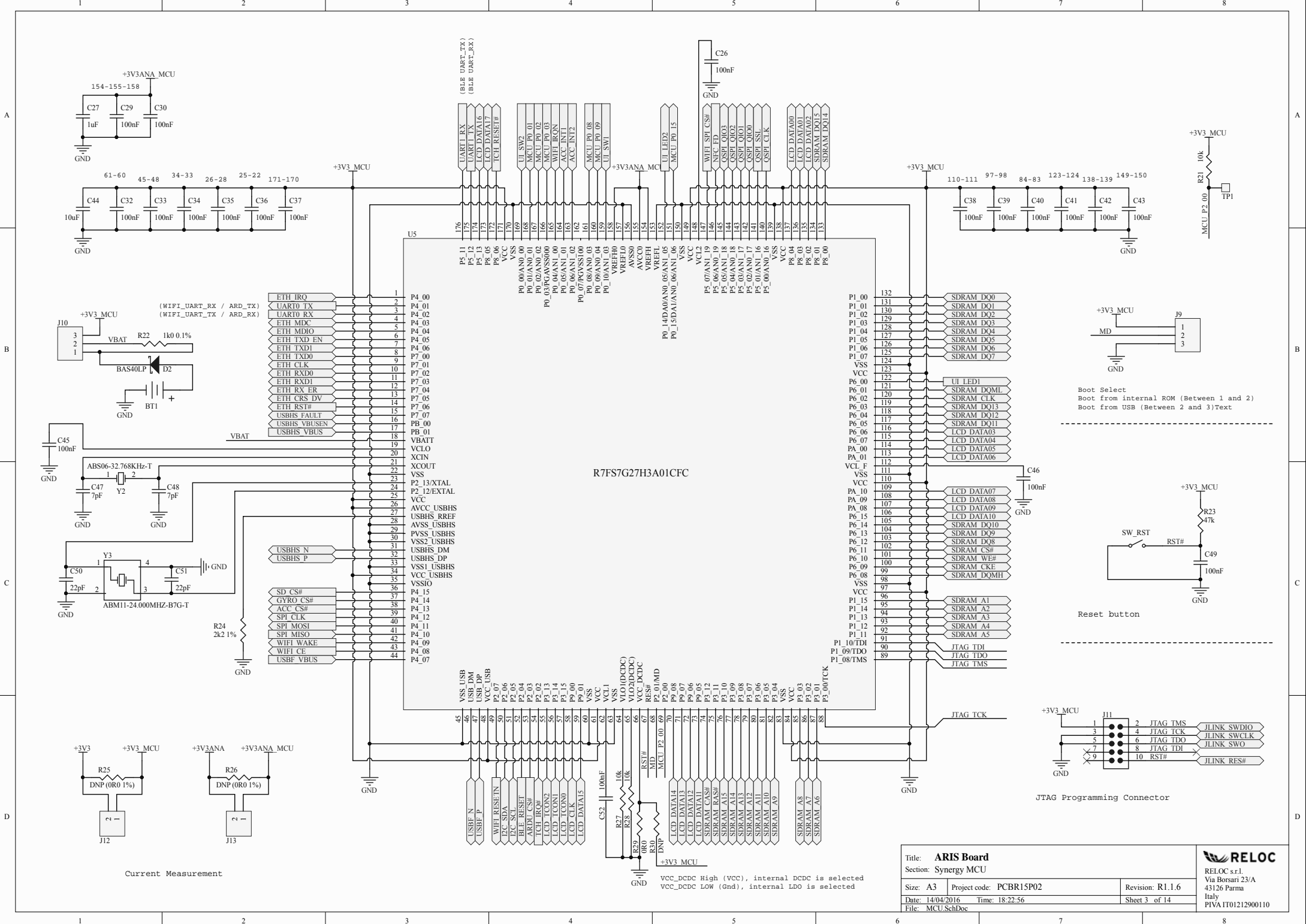
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File: **PowerSupply.SchDoc**

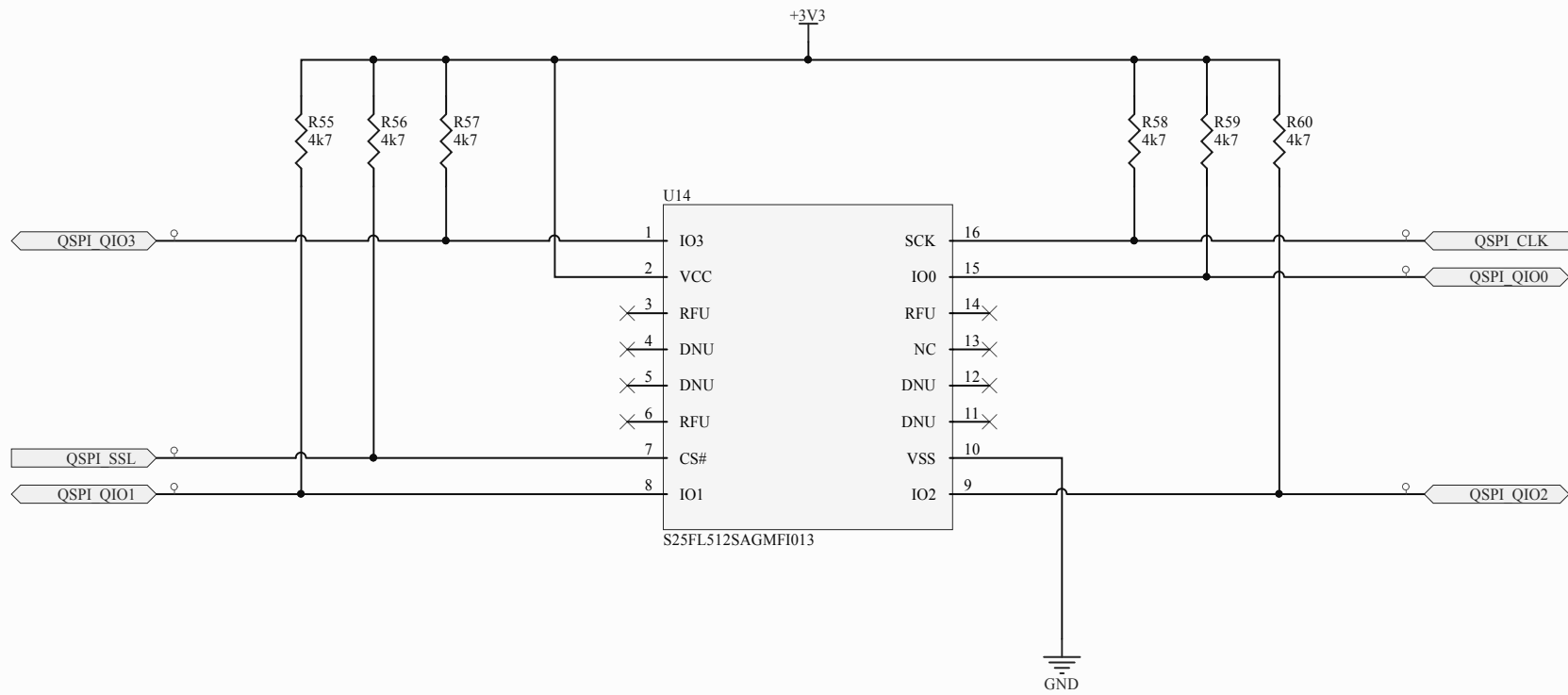



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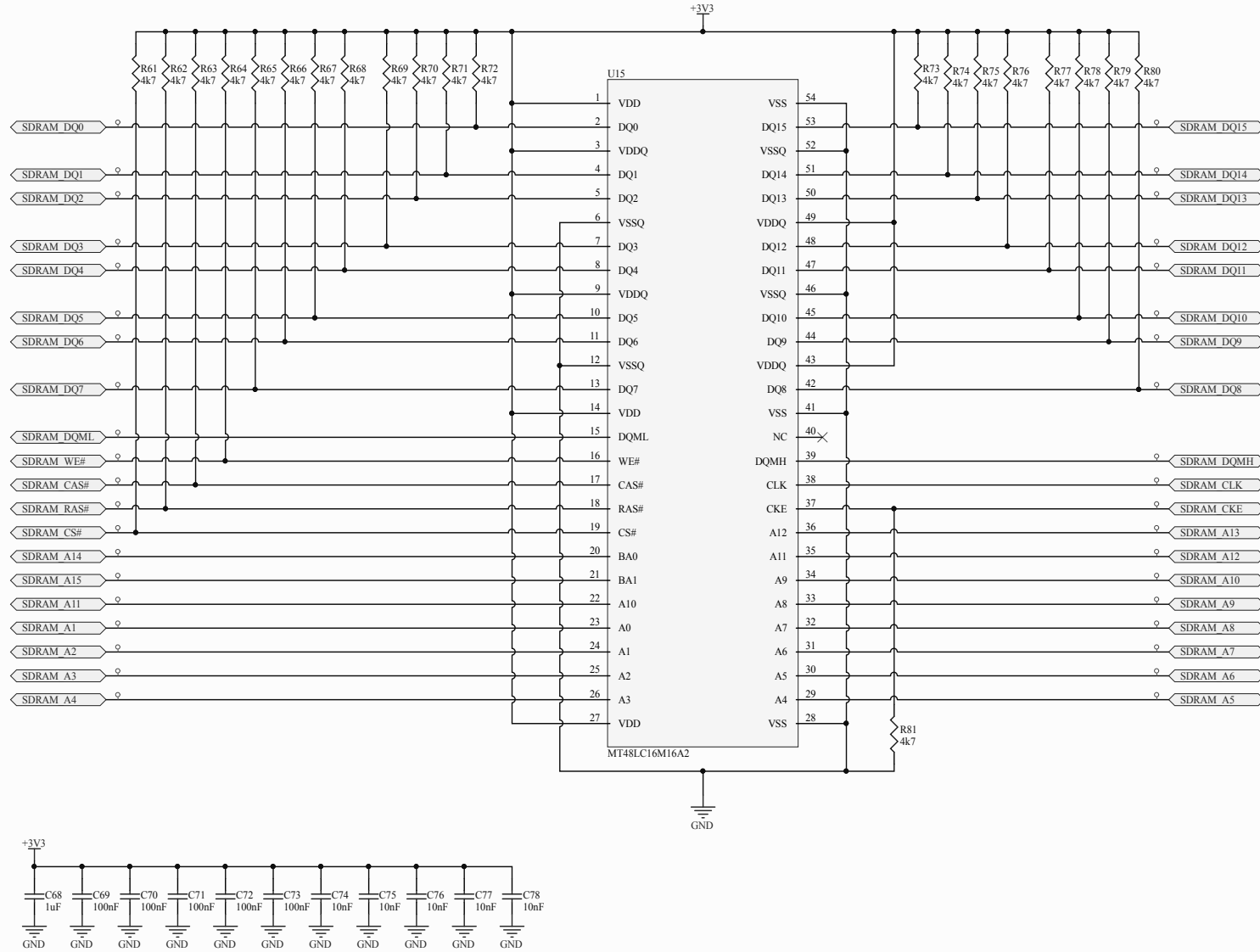
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Section: Synergy MCU		Sheet 3 of 14	
Size: A3	Project code: PCBR15P02	Date: 14/04/2016	Time: 18:22:56
File: MCU.SchDoc		Via Borsari 23/A 43126 Parma Italy PIVA.IT0121900110	

On-Board Memory - 512 Mbit Flash



Title: ARIS Board		 RELOC s.r.l. Via Borsari 23/A 43126 Parma Italy PIVA IT01212900110
Section: Flash Memory		
Size: A4	Project code: PCBR15P02	Revision: R1.1.6
Date: 14/04/2016	Time: 18:22:57	Sheet 4 of 14
File: Flash.SchDoc		

On-Board Memory - 256 Mbit RAM



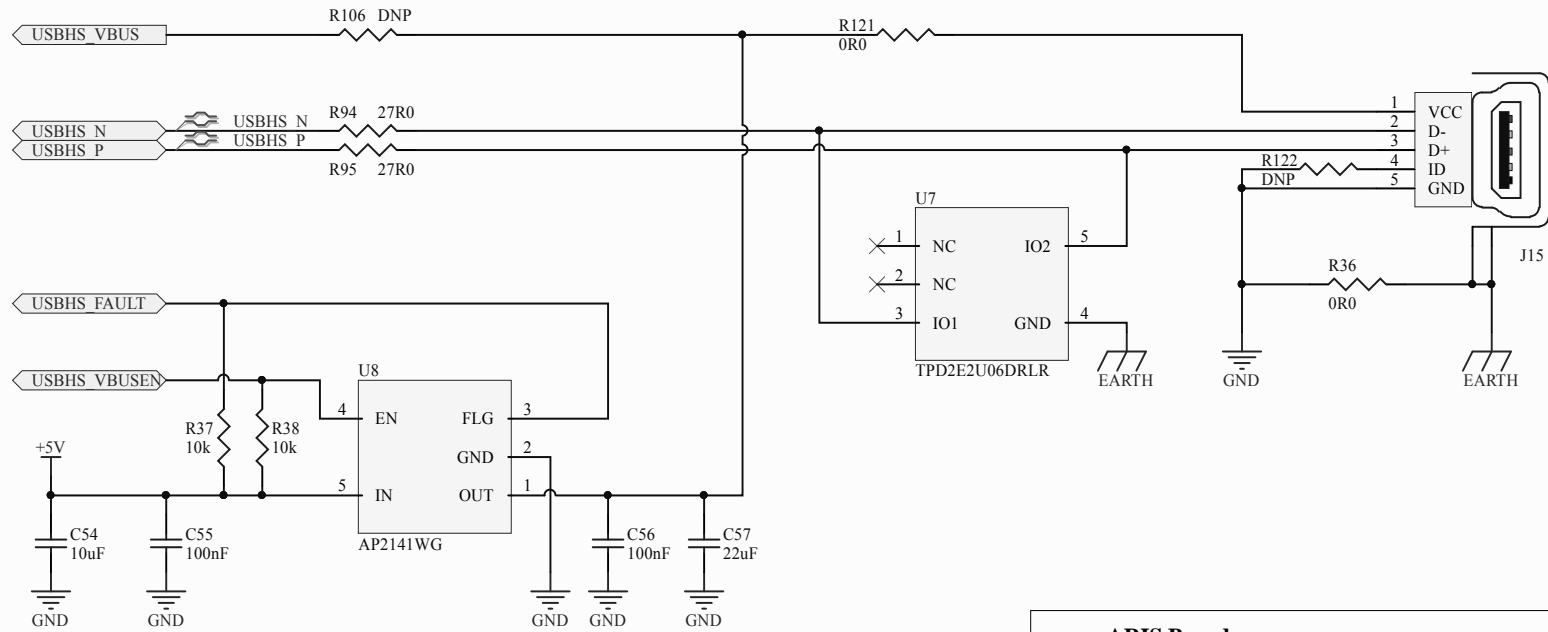
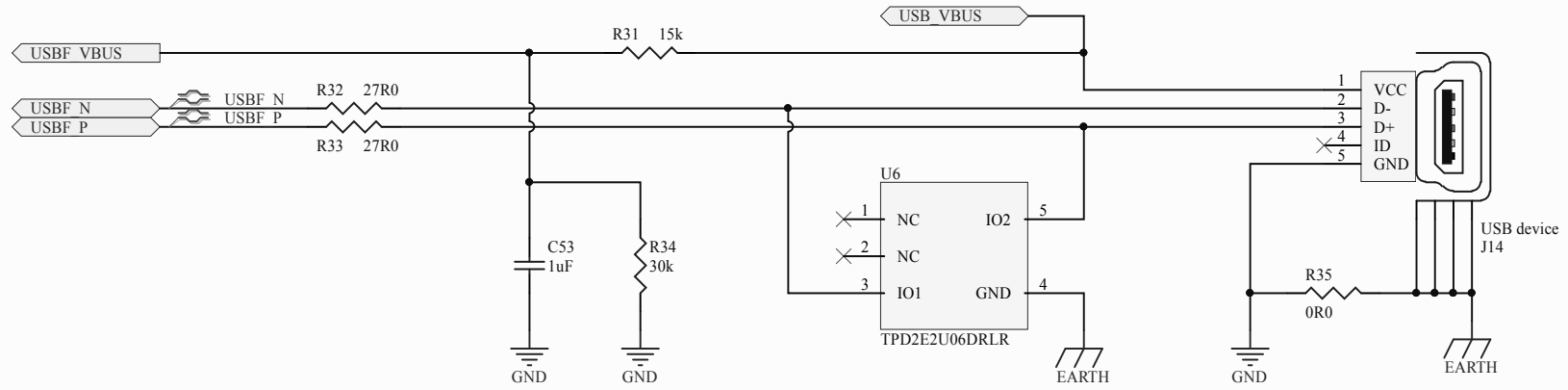
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Section: RAM			
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Date: 14/04/2016	Time: 18:22:57	Sheet 5 of 14	
File: RAM.SchDoc			

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Title: **ARIS Board**

Section: USB

Size: A4 | Project code: PCBR15P02

Revision: R1.1.6

Date: 14/04/2016 | Time: 18:22:57

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File: USB.SchDoc



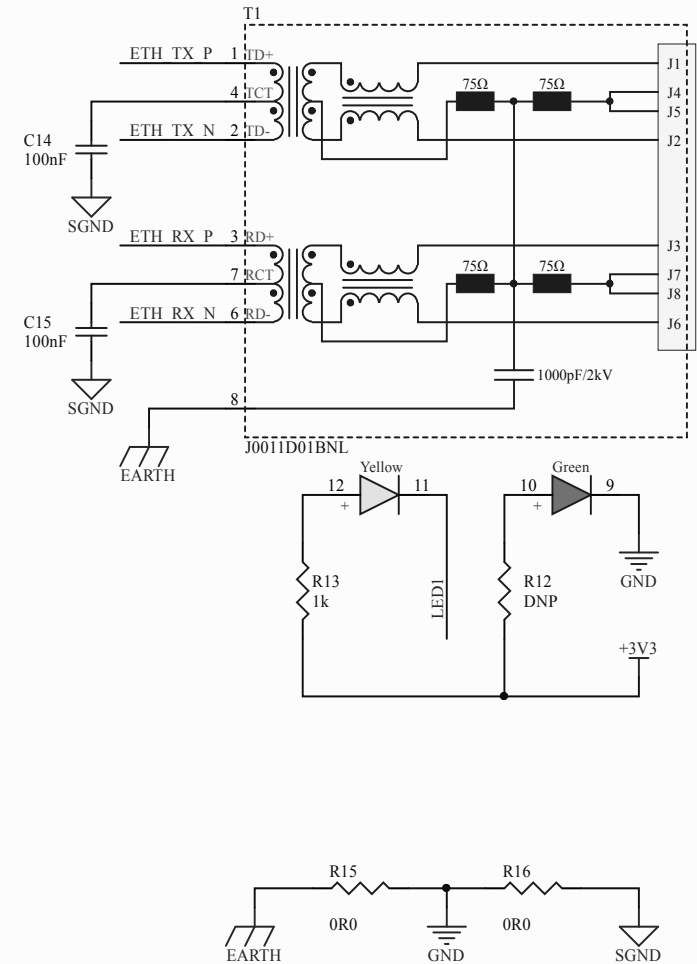
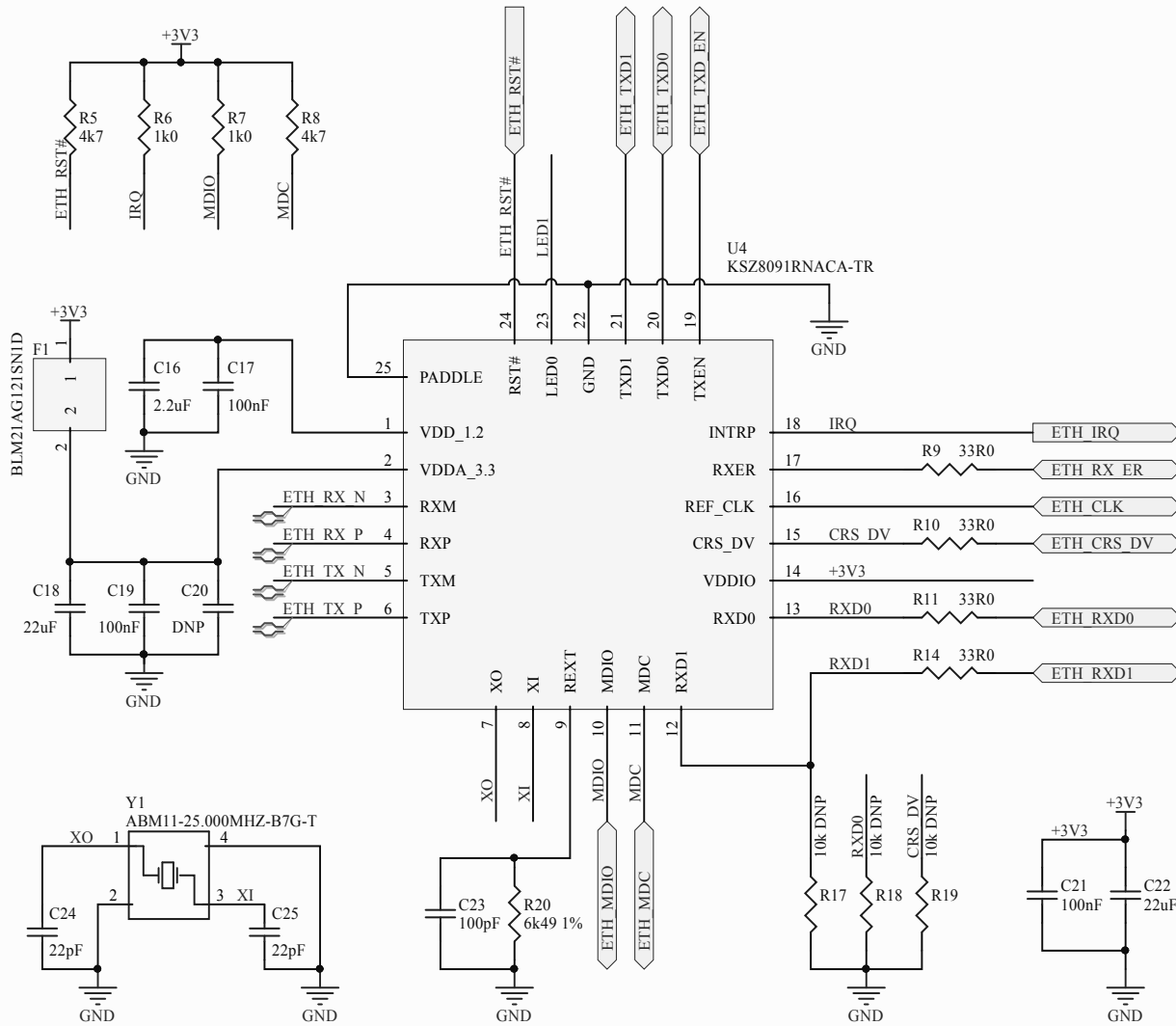
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Ethernet

1. The differential pair (TXP/N or RXP/N) should be routed using 5-mil trace width and 5-mil trace spacing in same length to create a 100ohm controlled trace.
2. Keep both traces of each differential pair as identical to each other as possible.
3. Route each differential pair on the same PCB layer. Avoid vias and pads in the path.
4. Route both TXP/N and RXP/N pairs away from all other signals, with at least four times of 5-mil trace space from other traces.

Title: **ARIS Board**

Section: Ethernet

Size: A4 Project code: PCBR15P02

Revision: R1.1.6

Date: 14/04/2016 Time: 18:22:57

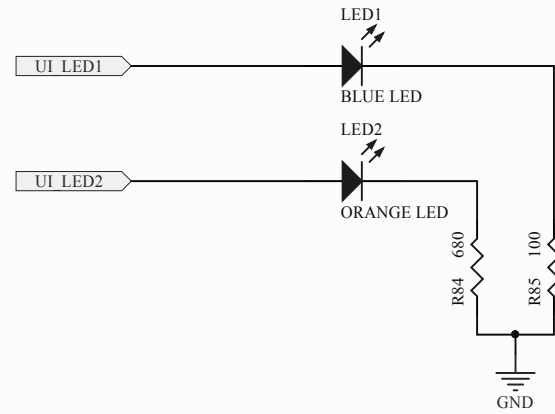
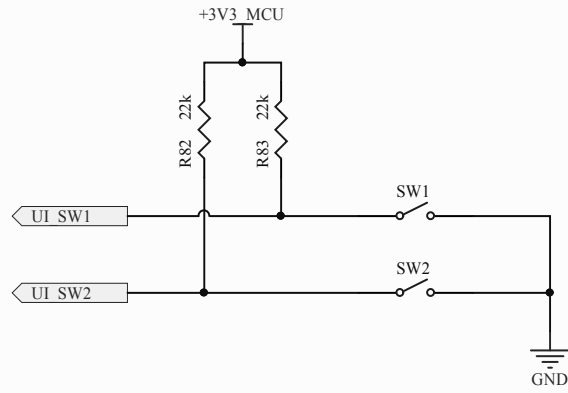
Sheet 7 of 14

File: Ethernet.SchDoc

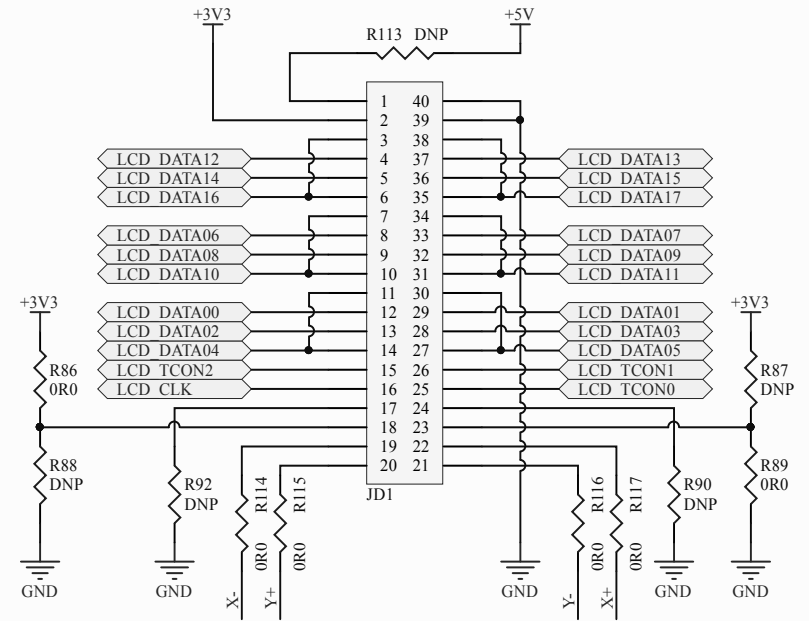
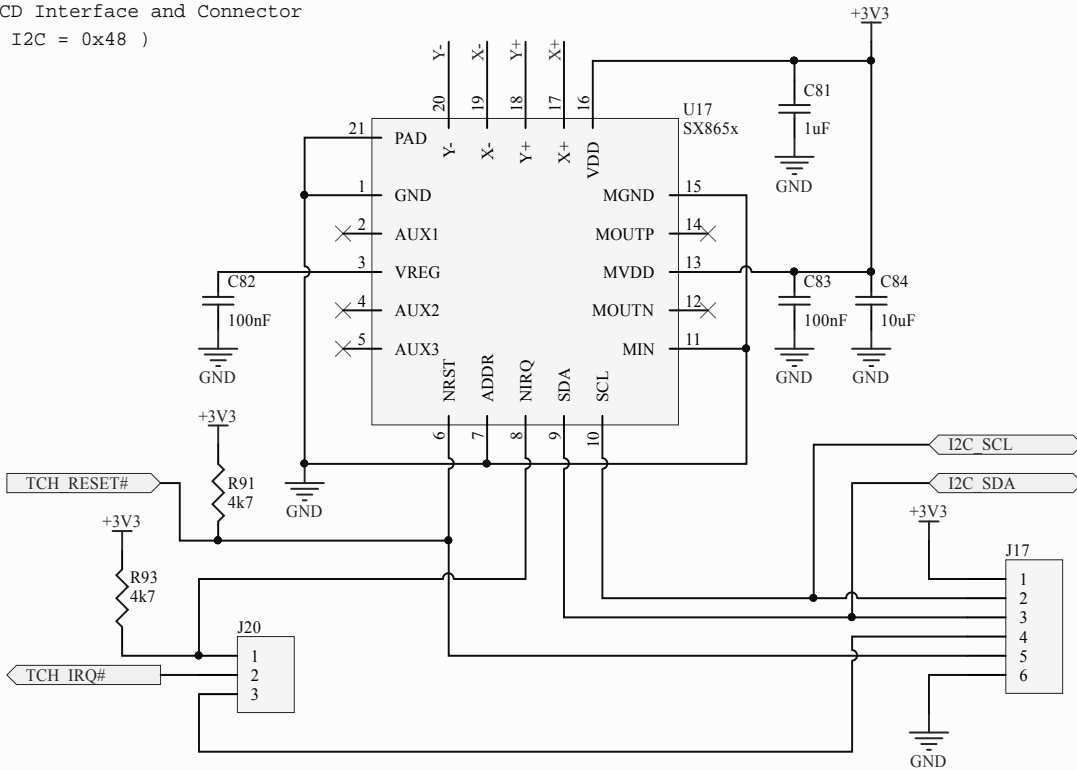


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LEDs and Switches



LCD Interface and Connector
(I2C = 0x48)



Title: **ARIS Board**
Section: User Interface

Size: A4 | Project code: PCBR15P02

Date: 14/04/2016 | Time: 18:22:57

File: UserInterface.SchDoc

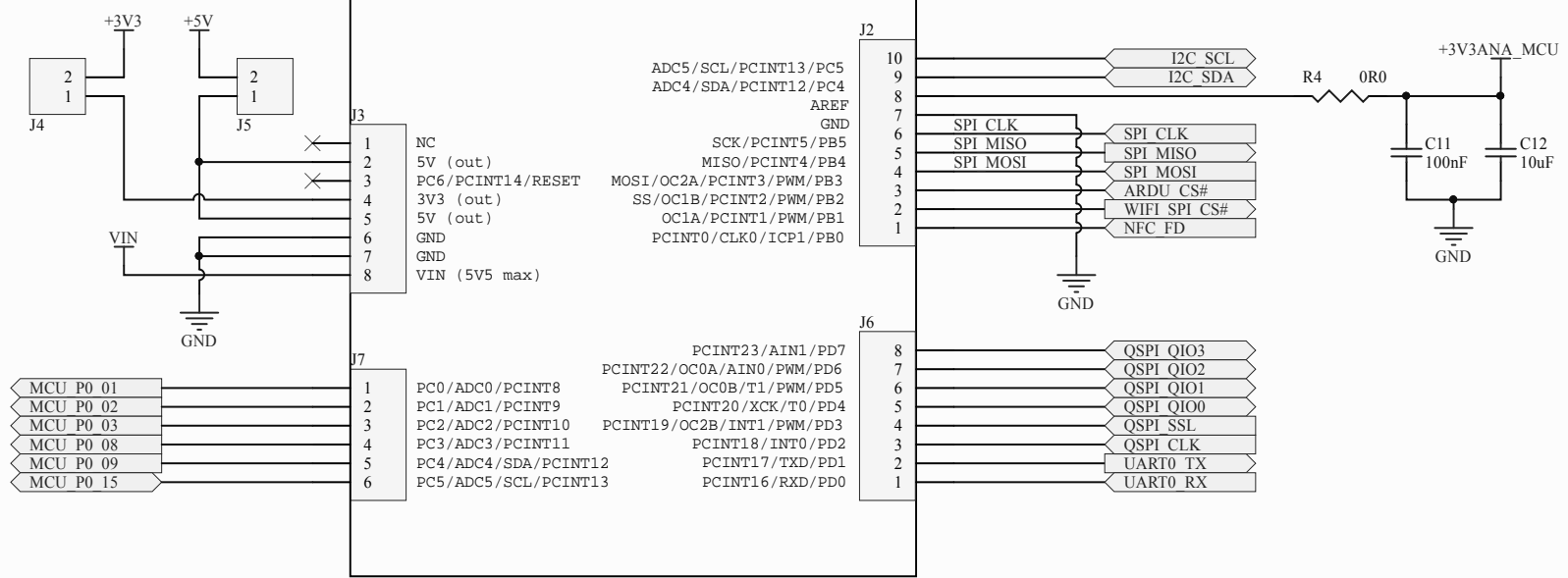
Revision: R1.1.6

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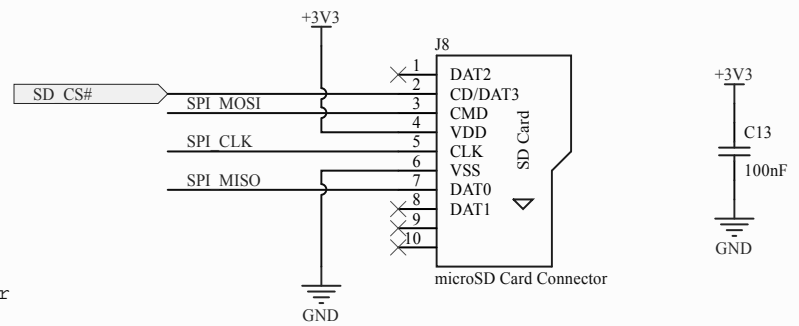


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Arduino UNO Shield Connector



SD Connector



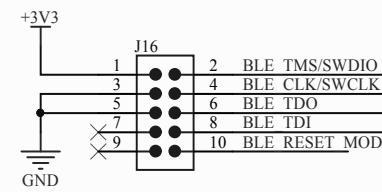
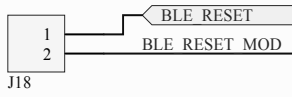
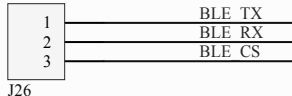
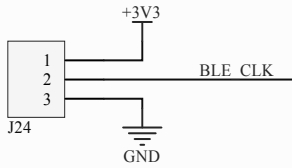
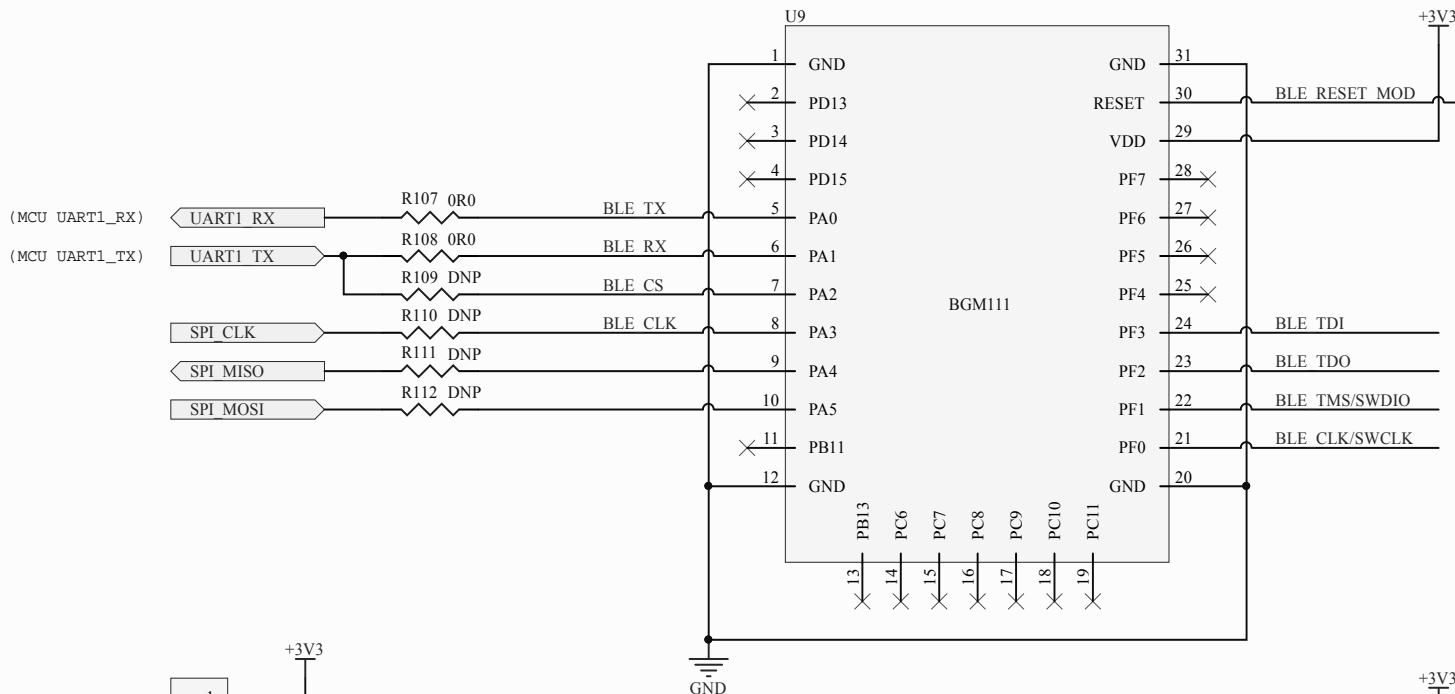
Title: ARIS Board		 RELOC s.r.l. Via Borsari 23/A 43126 Parma Italy PIVA IT01212900110
Section: Connectors		
Size: A4	Project code: PCBR15P02	Revision: R1.1.6
Date: 14/04/2016	Time: 18:22:57	Sheet 9 of 14
File: Connectors.SchDoc		

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JTAG Programming Connector

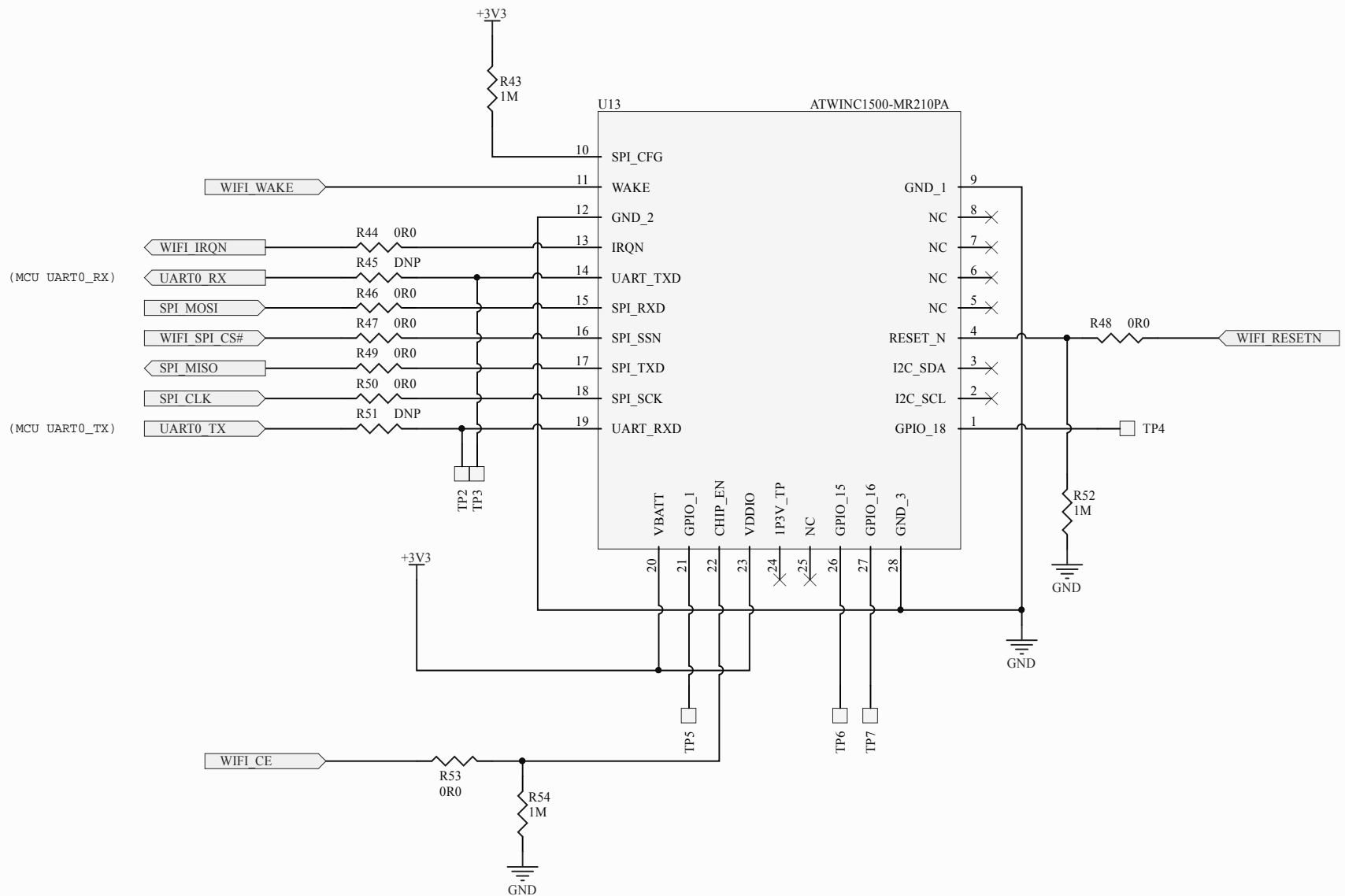
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Section: Bluetooth Low Energy			
Size: A4	Project code: PCBR15P02	Revision: R1.1.6	
Date: 14/04/2016	Time: 18:22:57	Sheet 10 of 14	
File: BLE.SchDoc			


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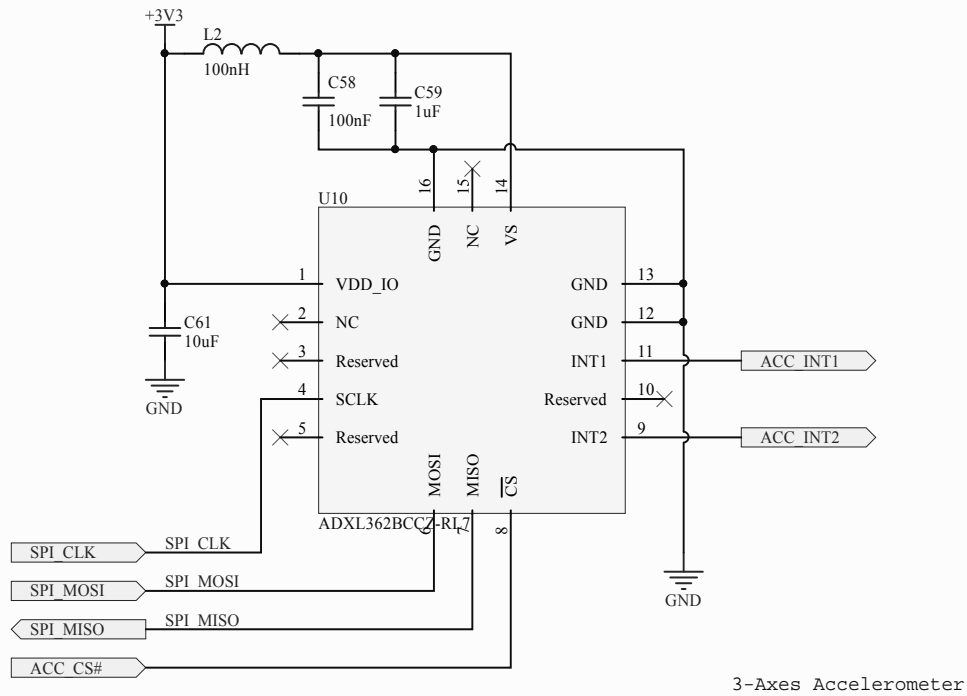
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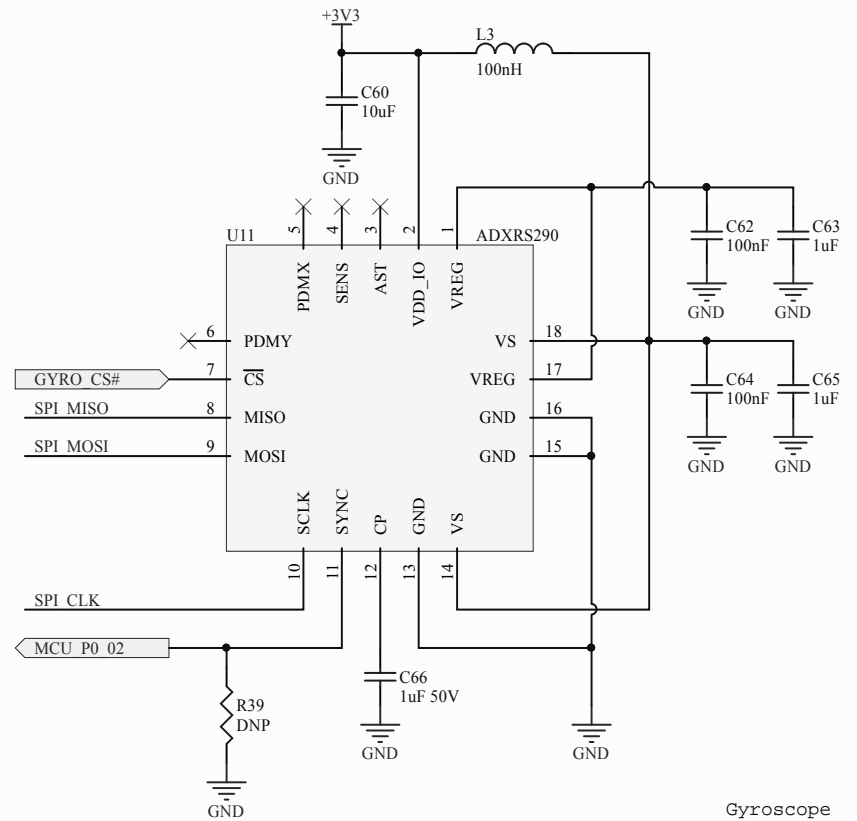
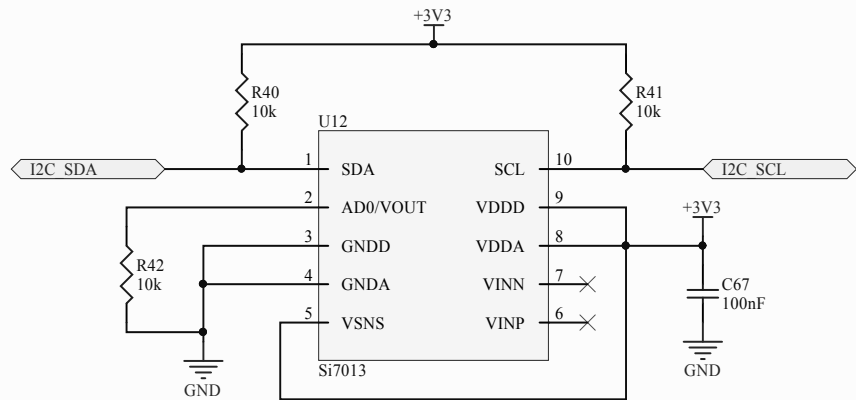
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Title: ARIS Board		 RELOC s.r.l. Via Borsari 23/A 43126 Parma Italy PIVA IT01212900110
Section: Wi-Fi		
Size: A4	Project code: PCBR15P02	Revision: R1.1.6
Date: 14/04/2016	Time: 18:22:57	Sheet 11 of 14
File: WiFi.SchDoc		



Temperature and Humidity Sensor
(I2C = 0x40)



Title: **ARIS Board**

Section: Sensors

Size: A4 Project code: PCBR15P02

Revision: R1.1.6

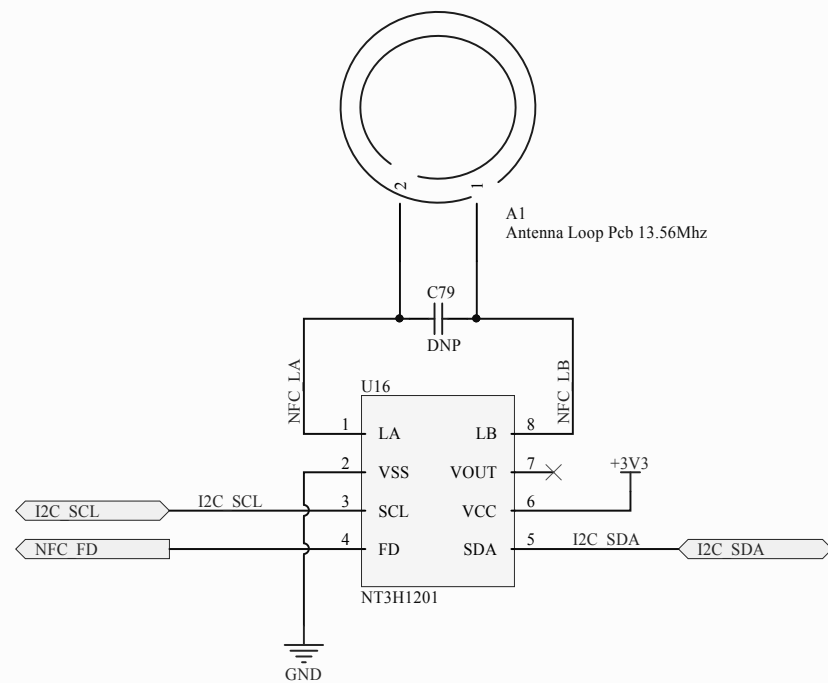
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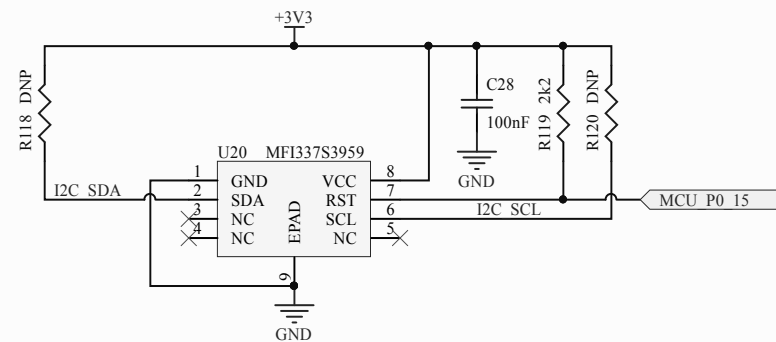
File: Sensors.SchDoc



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NFC Transponder
(I2C = 0x55)



Mfi authentication chip
(I2C = 0x10 - 0x11)

Title: **ARIS Board**

Section: NFC_Mfi

Size: A4 Project code: PCBR15P02

Revision: R1.1.6

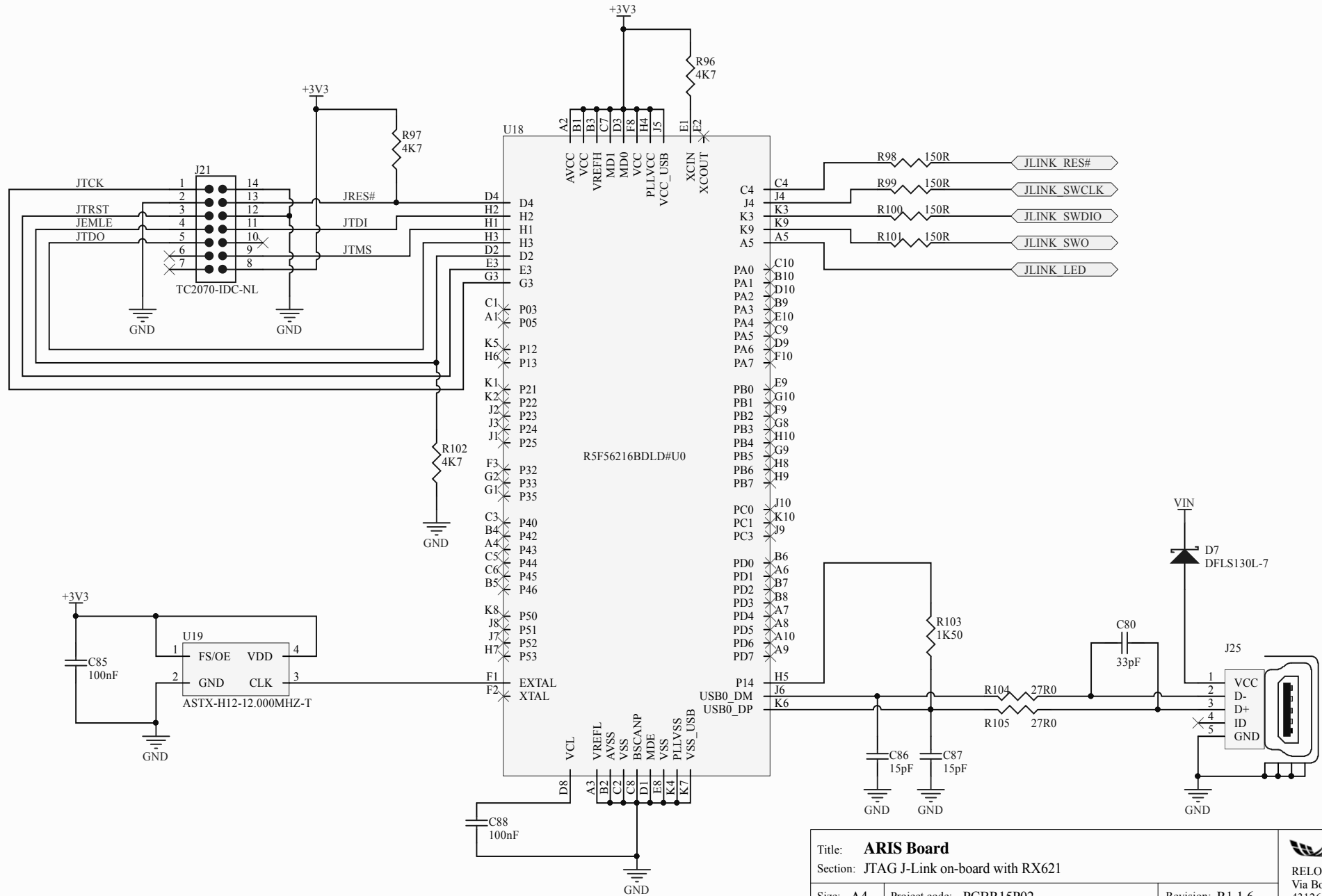
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File: NFC.SchDoc



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Title: ARIS Board			 RELOC s.r.l. Via Borsari 23/A 43126 Parma Italy PIVA IT01212900110
Section: JTAG J-Link on-board with RX621			
Size: A4	Project code: PCBR15P02	Revision: R1.1.6	
Date: 14/04/2016	Time: 18:22:58	Sheet 14 of 14	
File: JLink.SchDoc			