molex **PRODUCT SPECIFICATION**

PRODUCT SPECIFICATION
FOR HYPERJACK 1000 BASE-T 1x1 MAGNETIC CONNECTOR

SCOPE
This specification defines the functionality as well as the mechanical and electrical interfaces to the Molex 85793-series family of HyperJack 1000 Base-T 1x1 Magnetic Connector.

REVISION:	ECR/ECN INFORMATION:	TITLE:	SHEET No.
A	EC No: **MG2011-0036** DATE: **2010 / 11 / 16**	**PRODUCT SPECIFICATION FOR HYPERJACK™ 1000 BASE-T 1x1 MAGNETIC CONNECTOR**	**1** of **14**

DOCUMENT NUMBER:	CREATED / REVISED BY:	CHECKED BY:	APPROVED BY:
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1.0 PRODUCT DESCRIPTION

INTRODUCTION

The HyperJack 1000 Base-T 1x1 magnetic connector offers a simple solution for integrating gigabit magnetics and the RJ-45 connector interface into one integrated package with guaranteed signal integrity, gigabit ethernet, common mode termination and EMI shielding. The connector includes up to two LED's.

PRODUCT NAME AND SERIES NUMBER

Single port HyperJack 1000 Base-T 1x1 85793 Series Connector.
See SD-85793-101 for information on dimensions, materials, plating, markings & product options.

FEATURES

- 10/100/1000 Base-T magnetics
- Integrated Common Mode Termination Circuitry
- Temperature range: 0°C to 70°C, see section 4.4.4 for more details
- Integrated LEDs
- 2250V DC isolation

SAFETY AGENCY APPROVALS

UL File Number……………………Pending

APPLICABLE DOCUMENTS AND SPECIFICATIONS

Molex sales drawing

See SD-85793-101 for information on dimensions, materials, plating and markings.

Molex Packaging Spec

PK-85759-001

IEEE 802.3 Amendment

Data Terminal Equipment (DTE) Power via Media Dependent Interface (MDI) Enhancements

IEC 60603-7-1

TIA-568-C

FCC PART 68

1.1 ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Maximum Currents	
LED's	±20mA
PHY, MDI Pins	±1A
Temperature Ranges	
Operating (case temp)	0°C to 70°C
Storage	-55°C to 70°C

Table 1 – Absolute Max Ratings

2.0 ELECTRICAL CHARACTERISTICS

LED TERMINALS

LED's						
V_F	Forward voltage drop, I_F = 20mA	Yellow LED.	2.0		2.5	V
		Green LED.	1.75		2.35	V
		Orange LED.	1.7		2.30	V
I_O	Luminous intensity, I_F = 20mA	Yellow LED.	5		10	mcd
		Green LED.	5		10	mcd
		Orange LED.	5		10	mcd

Table 2 - Electrical Characteristics

3.0 SYSTEM OVERVIEW

3.1 MAGNETIC WIRING SCHEMATIC DIAGRAM

The following is the magnetic wiring schematic diagram for the Ethernet terminals on the HyperJack 1000 Base-T 1x1 magnetic connector.

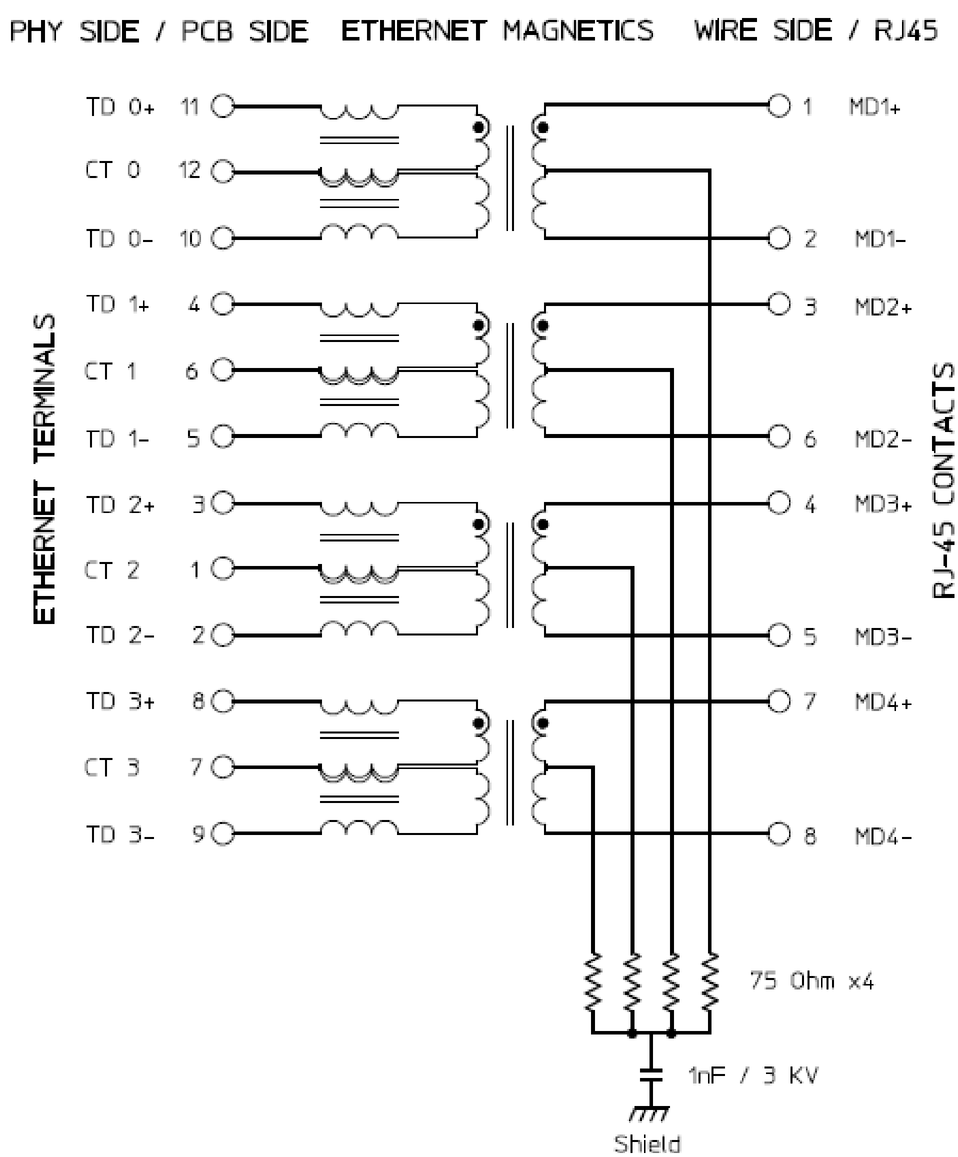

Figure 1 –Ethernet magnetic wiring schematic diagram with common mode termination components

3.2 TERMINAL DESCRIPTION/FUNCTION FOR HYPERJACK 1000 POE PLUS ENABLED 1X1

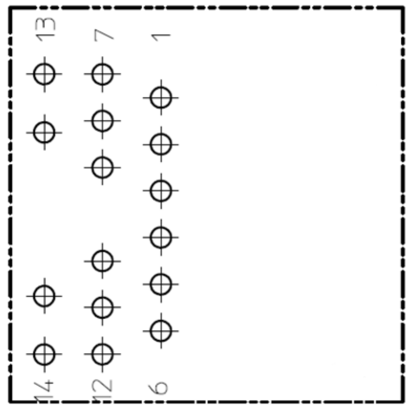

Figure 2 – Terminal Description

3.2.1 PIN FUNCTIONS

ETHERNET TERMINALS

CT0:CT3: Pins 12, 6, 1 & 7. Input used to apply a DC voltage bias required by PHY transceivers. CT pins connect to the centre taps of all internal Ethernet transformers on the PHY side. In most applications the CT pin is connected to the positive supply rail that powers the PHY chip, but consult the PHY data sheet to be sure. Do not add components (e.g. resistors, chokes, ferrites) in series with the CT pin unless the PHY data sheet recommends it. The CT pins should be coupled to Ground via capacitors to act as the return line for the Ethernet data lines (MD1+/- through MD4+/-). This ground should be the ground plane for the PHY and should be isolated from any voltage traces or planes. Connection to chassis ground is at the discretion of the system designer.

TD0+/-: Pins 11 & 10. Differential data lines from the transformer that connects to pins 1 and 2 on the RJ45 connector.

TD1+/-: Pins 4 & 2. Differential data lines from the transformer that connects to pins 3 and 6 on the RJ45 connector.

TD2+/-: Pins 3 & 2. Differential data lines from the transformer that connects to pins 4 and 5 on the RJ45 connector.

TD3+/-: Pins 8 & 9. Differential data lines from the transformer that connects to pins 7 and 8 on the RJ45 connector.

LED Terminal Detail

The below image details the front of the connector and highlights the two LED locations on the HyperJack 1000 Base-T 1x1 Magnetic Connector. Note there is also a Non-LED version.

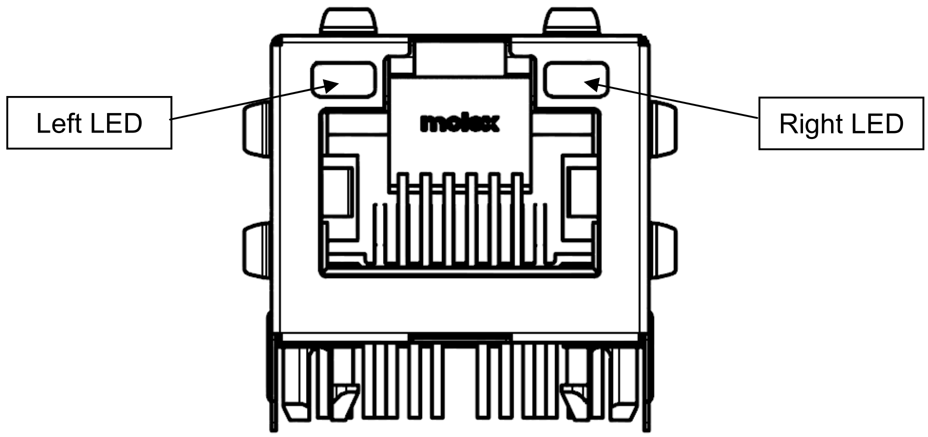

Figure 3 - Image of connector front face indicating LED's

Right LED, Pins 13 & 14: Pins for the LED on the right side of the module (looking from the front with pins facing down).

Left LED, Pins 15 & 16: Pins for the LED on the left side of the module (looking from the front with pins facing down).

The 85793 series connectors allows for two independent LED's with external pins to customer PCB

Note on LED isolation: Section 4.1.2 of this document details the isolation requirements for the connector, as part of that, the LED's are defined as being part of the PHY side isolation group. If using the independent LED's to indicate any user defined operation, great care must be taken to ensure that sufficient isolation is maintained.

See Sales Drawing for detailed options on LED colours and Part Numbers.

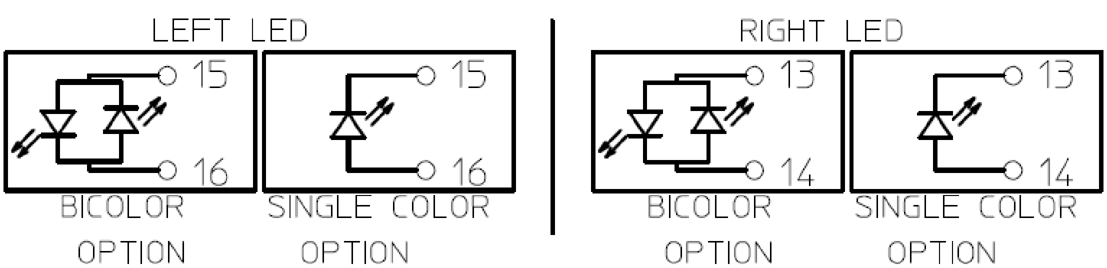

Figure 4 - LED Schematics

4. PCB LAYOUT GUIDELINES

4.1.1 PHY INTERFACE

The data lines TD[0:3]+/- should be routed as controlled-impedance traces, preferably as differential pairs to reduce crosstalk. The traces should be designed for a differential-mode impedance of 100Ω. Internal routing layers are recommended to reduce EMI and avoid isolation issues. (See Section 4.1.2: Isolation.)

The plane layers directly adjacent to the routing layers should be Ground and/or the supply rail that connects to CT. If some other supply rail is used for one of these planes, place a 0.1μF decoupling cap from that rail to PHY Ground near the connector and another cap near the PHY chip. Avoid routing signal traces over cuts or holes in the planes.

4.1.2 ISOLATION

The connector interface must withstand at least 2250V DC for 60 seconds without breaking down. The test voltage is applied between the MDI pins (usually with all 8 pins tied together) and chassis. There are two groups of signals that must be isolated from each other:

- The PHY-side group: PHY Voltage, PHY Ground, TD[0:3]+/-, CT[0:3], LED Pins and Shield.
- The MDI-side group: RJ-45 pins,

Signals in the same group can be close together, but signals from the other group must be far enough apart to meet the isolation requirements. Figure 5 shows the minimum spaces between signals of different groups. The LED's may be assigned to different groups. Normally the LED's are driven by the PHY, so pins 13-16 are part of the PHY-side group. If one of the LED's is driven by another isolated source then extreme caution is advised.

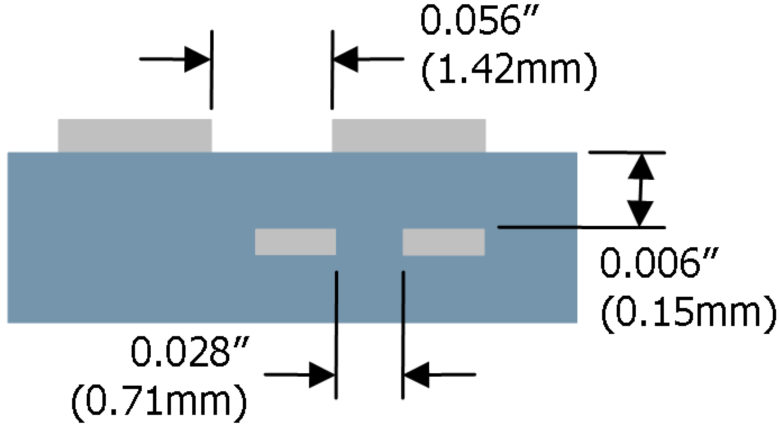

Figure 5 – Minimum Spaces

The most effective way to isolate signals is vertically; routing each group on different layers. Vertical isolation is preferred because the required space is much smaller. Most PC boards are made from FR-4, which has a dielectric strength of at least 500V/mil. So the minimum dielectric thickness is (2250V)/(500V/mil) = 4.5 mils. However, during the lamination process the prepreg flows into the etched spaces between traces, the finished dielectric layer can be slightly pinched near the edges of traces. Therefore it is recommended to use at least 6 mils of prepreg between layers where signals from different groups can cross over each other.

Figure 6 shows an example of a 6-layer board. The connector is mounted on the top side, chassis ground is assigned to layer 1. The MDI side group is routed on the bottom layer.

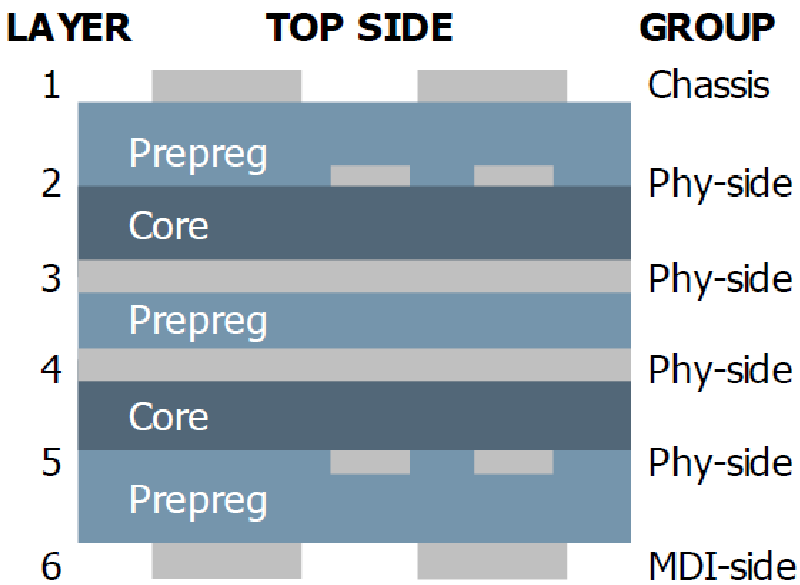

Figure 6 – Example PCB Stack-up

In this example, the top and bottom prepreg layers separate signals from different groups, so these should be at least 6 mils thick. However, the middle prepreg and core layers can be thinner because they separate layers that are all in the same signal group. If a surface layer must be used to route some of the signals, use the surface on the opposite side of the board from the connector; in this way surface traces do not have to pass directly under the edge of the shield.

Note: All dimensions given are guides and be taken literally, the user should exercise caution and best engineering practice to ensure that no isolation issues occur.

PERFORMANCE

5.1 ELECTRICAL REQUIREMENTS

ITEM	DESCRIPTION	TEST CONDITION	REQUIREMENT
1	**Visual Inspection**	*IEC 60512-1-1 Test 1a*	There shall be no defects that would impair normal operation
2	**Initial contact resistance (Low Level)**	Mated connectors: Max test voltage 20mV DC or AC peak, test current100 mA DC or AC peak Arrangement acc. IEC60603-7-5 / 7.2 *IEC 60512-2-1 Test 2a*	**20 mΩ** MAXIMUM [Initial]
3	**Insulation Resistance**	Mate connectors with a voltage of 100 V DC ±15V DC between each contact and screen to all others *IEC 60512-3-1 Test 3a Method A*	**500 MΩ** MINIMUM
4	**HiPot (Voltage Proof / Isolation)**	IEC 60950-1: 2001 Subclause 5.2.2. 2250V DC for 60 seconds.	No breakdown

5.2 MECHANICAL REQUIREMENTS

ITEM	DESCRIPTION	TEST CONDITION	REQUIREMENT
5	**Insertion and withdrawal forces**	Insert and withdraw a plug Speed: 10 mm/s max *IEC60512-13-2-Test 13b*	Maximum insertion and withdrawal force: **30 N (shielded connector)**
6	**Effectiveness of connector coupling devices**	Rate of load application 44,5 N/s max. *IEC60512-8-Test 15f*	**50 N** for **60 s ± 5s.**
7	**Mechanical operation / Durability (Half rated cycles)**	Speed: 10 mm/s max. Rest: 1 s min. (when mated and when unmated) Operations: 750 Locking device inoperative *IEC60512 Test 9a*	Contact Resistance: **20 mΩ** max. (change from initial)
8	**Vibration**	f= 10 to 500 Hz Ampl. = 0.35 mm Accel. 50 m/s^2 10 sweeps /axis *IEC60512 Test 6d*	Contact disturbance: Discontinuity **10 µs.** maximum No damage Dielectric withstanding voltage: no breakdown Contact Resistance: Max. change from initial **20 mΩ** (shield: **100 mΩ**)
9	**Mechanical gauging**	*IEC60603-7-5 Annex L*	Passing Go / No go test
10	**Gauging continuity**	All signal contacts and screen specimens *IEC60603-7-5 Annex A*	Contact disturbance: **10 µs** maximum

5.3 ENVIRONMENTAL REQUIREMENTS

ITEM	DESCRIPTION	TEST CONDITION	REQUIREMENT
11	**Solderability**	Solder time 3 ± 0.5 seconds Solder bath method Solder temperature: 260°C +0/-5°C	**95** % of the immersed area must show no voids
12	**Rapid change of temperature**	-40°C to +70°C 25 cycles t=30 min Recovery time 2h *IEC60068-2-14*	Appearance: No damage Contact resistance: **20 mΩ** max. change from initial Dielectric withstanding voltage: no breakdown Insulation resistance: **500 MΩ** min.
13	**Cyclic damp heat**	Cycles: 21 Low temperature: 25° C High temperature: 65° C Cold subcycle: –10° C Humidity: 93% Mated and unmated *IEC60068-2-38*	
14	**Flowing mixed gas corrosion**	4 days, mated state and unmated state *IEC60512 Test 11g*	
15	**Electrical load and temperature**	500h @ 70°C Current: with 0.5A and without current Recovery period 2h *IEC60512 Test 9b*	
16	**Damp heat steady state**	21 days *IEC60068-2-78*	

5.4 TRANSMISSION CHARACTERISTICS

ITEM	DESCRIPTION	TEST CONDITION	REQUIREMENT (ALL TYPES)
17	**Insertion loss (dB)**	Mated Connectors ES-85740-001	1.0 MHz - 9.9 MHz: **0.4+0.1*log(F)** 10.0 MHz - 49.9 MHz: **0.5+0.3*log(F/10)** 50.0 MHz – 79.9 MHz: **1+1.4*log(F/80)** 80.0 MHz – 100.0 MHz: **1.3+3*log(F/100)**
18	**Return loss (dB)**	Mated Connectors ES-85740-001	1.0 MHz to 9.9MHz: **27** 10.0 MHz to 100.0 MHz: **27-17*log(F/10)**
19	**NEXT loss (dB)**	Mated connectors, pair to pair ES-85740-001	1.0 MHz to 5.9 MHz: **50** 6.0 MHz to 49.9 MHz: **45-16*log(F/10)** 50.0 MHz to 100.0 MHz: **25-30*log(F/100)**
20	**CMR (dB)**	Mated Connectors ES-85740-001	1.0 MHz to 9.9 MHz: **34** 10.0 MHz to 79.9 MHz: **27** 80.0 MHz to 199.9 MHz: **27-14.5*log(F/80)** 200 MHz to 399.9 MHz: **21.5-39*log(F/200)** 400.0 MHz to 1000.0 MHz: **10**
21	**OCL (µH min)**	PHY and Wire Side ES-85740-001	8mA bias current @ 100kHz, 100mV **350µH**

F in MHz

ITEM	DESCRIPTION	GROUP P	GROUP AP	GROUP BP	GROUP CP	GROUP DP	GROUP EP	GROUP FP
1	Visual Inspection	1	7,12	8	4	4		6
2	Contact Resistance	2	5,9	3,5	2	5		3,5
3	Insulation Resistance	3	4	6	3	2		4
4	HiPot	4	6,14	7		3		
5	Insertion Withdrawal		1,10					
6	Effectiveness of Connector Coupling		2,11					
7	Durability (half rated cycles)			1,4				
8	Vibration				1			
9	Gauging					6		
10	Gauging Continuity					7		
11	Solderability		13					
12	Rapid Change of Temperature		3					
13	Cyclic Damp Heat		8					2
14	Flowing Mixed Gas Corrosion			2				
15	Electrical Load and Temperature					1		
16	Damp Heat Steady State							1
17	Insertion Loss						1	
18	Return Loss						2	
19	NEXT						3	
20	CMR						4	
21	OCL						5	

Group P to be completed on all samples before testing begins
Where contact resistance measurements are not possible, Insertion Loss should be completed instead

3.0 PACKAGING

Parts shall be packaged to protect against damage during handling, transit and storage. (Refer to sales drawings)

4.0 ESD PROTECTION

To avoid damage by an electrostatic discharge while installing the connector, ESD packaging has been used. For more details see PK-85793-001.

5.0 GAGES AND FIXTURES

Arrangement for contact resistance test:
Arrangement acc. IEC60603-7-5 / 7.2

Arrangement for vibration test:
Arrangement acc. IEC60603-7-5 / 7.3

6.0 QUALITY ASSURANCE PROVISIONS

The applicable Molex Inspection plan specifies the sampling acceptable quality level to be used. Dimensional and functional requirements shall be in accordance with applicable product drawings and this specification.