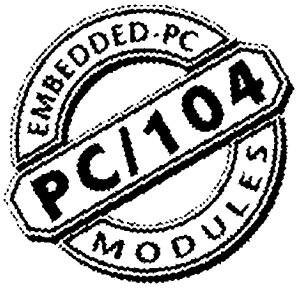
Arcom - SBC104

PC Compatible
CPU Board

Arcom
CONTROL SYSTEMS



Arcom - SBC104

PC Compatible CPU Board

Technical Manual

Warning

Handling

This board contains static sensitive devices. Observe anti-static precautions at all times. Unpacking and installation of the board should be undertaken in an anti-static working area.

Battery

Note: The board is supplied with the battery supply isolated. Move Link 3 to position A before using the board.

The board is fitted with a Nickel Metal Hydride rechargeable battery. Do not short circuit the battery or place the board on a metal surface where the battery terminals could be shorted.
Dispose of the battery with care. Do not incinerate, crush or otherwise damage the battery.

Electromagnetic Compatibility (EMC)

The SBC104 is classified as a 'component' with regard to the European Community EMC regulations and it is the users responsibility to ensure that systems using the board are compliant with the appropriate EMC standards.

Product Information

Full information about other Arcom PC/104 products is available via the FaxBack System, (Telephone numbers are listed below), or by contacting our Website at:
http://www.arcom.co.uk

Additional useful contact information:
Customer Support : (Tel) **+44 (0)1223 412428,** (Fax) **+44 (0)1223 403400,** (email) **support@arcom.co.uk**
Sales : (Tel) **+44 (0)1223 411200,** (Fax) **+44 (0)1223 410457,** (email) **sales@arcom.co.uk**

United Kingdom
Arcom Control Systems Ltd
Clifton Road
Cambridge CB1 4WH, UK
tel: +44 (0) 1223 411200
fax: +44 (0) 1223 410457
FoD: 01223 240600

United States
Arcom Control Systems Inc
13510 South Oak Street
Kansas City MO 64145,
USA
tel: (816) 941 7025
fax: (816) 941 0343
FoD: 800 747 1097

France
Arcom Control Systems
Centre d'affaires SCALDY
23, rue Colbert
7885 SAINT QUENTIN
Cedex, FRANCE
tel: 0800 90 84 06
fax: 0800 90 84 12
FoD: 0800 90 23 80

Germany
Arcom Control Systems
Kostenlose Infoline:
tel: 0130 824 511
fax: 0130 824 512
FoD: 0130 860 449

Belgium
Groen Nummer:
tel: 0800 7 3192
fax:: 0800 7 3191

Netherlands
Gratis 06 Nummer:
tel: 06022 11 36
fax:: 06022 11 48

Arcom CONTROL SYSTEMS

Contents

Revision History

Manual	PCB	Comments	
Issue A	V1 Iss 2	961122	First full release of Manual
Issue B	V1 Iss 2	970107	Minor edits throughout the Manual
Issue C	V1 Iss 2	970227	Inclusion of ROM-DOS 6.22

Introduction

The SBC104 is a PC-compatible 386SX/486SXLC processor board supporting a PC/104 bus interface which, with a PC/104 VGA CRT/flat panel display module, can form a complete DOS compatible PC for embedded applications. The board is fitted with 2 or 4 Mbytes of DRAM, 1 Mbyte of FlashFile™ memory and optionally 128 Kbyte of battery backed SRAM. System BIOS and extensions are contained in a 128 Kbyte EPROM. Onboard peripheral ports include COM1 and COM2, a floppy disk controller, hard disk (IDE) controller and keyboard interface.

The board is available in the following variants:

SBC104-386 or SBC104-486

Each may be supplied with 2MBytes or 4MBytes of DRAM and optionally 128KBytes of SRAM.

Features

- 25MHz 80386SX or 50MHz TI 486SXLC processor
- TI486SXLC includes 8KByte internal cache
- PC-AT architecture
- 2 or 4 Mbytes DRAM
- 1 Mbyte of FlashFile memory
- Includes Arcom Flash Filing System
- Includes ROM-DOS 6.22
- Optional 128 Kbyte of battery backed SRAM
- Battery backed Real Time Clock
- FDD interface via vertical 34-way header
- HDD IDE interface via vertical 40-way header
- COM 1 & 2 serial ports via individual 9-way D-type plugs
- AT Keyboard interface via a 6-way 'Mini' DIN socket
- Mini buzzer for audible alarm
- Watchdog Timer generating an NMI or optional Reset (3 second timeout)
- PC/104 interface, 16-bit, single Master only
- 11 mAHr Ni-MH battery: Full charge time = 70 hours
  Hold-up time = 550 hours
  Battery life = 6 years @ 25°C
- Operating temperature range: **386SX**
  (no air flow) +5°C to +65°C (With battery fitted)
  -20°C to +70°C (Without battery)
  486SXLC
  +5°C to +50°C (With battery fitted)
  -20°C to +50°C (Without battery)
- Power consumption: @ +5V 600mA
- MTBF (using generic figures from MIL-HDBK-217F at ground benign) : 161,000 hours. *(Note: Figures do not include the battery.)*
- Single Eurocard form factor

Arcom also manufactures a range of PC/104 modules for use with the SBC104. These include optoisolated digital and analogue I/O, relay output and multi-port serial communications.

Software

The SBC104 board is supplied with Arcom Flash Filing System and ROM-DOS 6.22 pre-loaded. The board only requires a +5V power supply, an optional PC/104 VGA board and a keyboard to start and will boot up from the embedded flash to the DOS 'C' prompt.

The board is supplied with a bootable utility disk containing the following files:

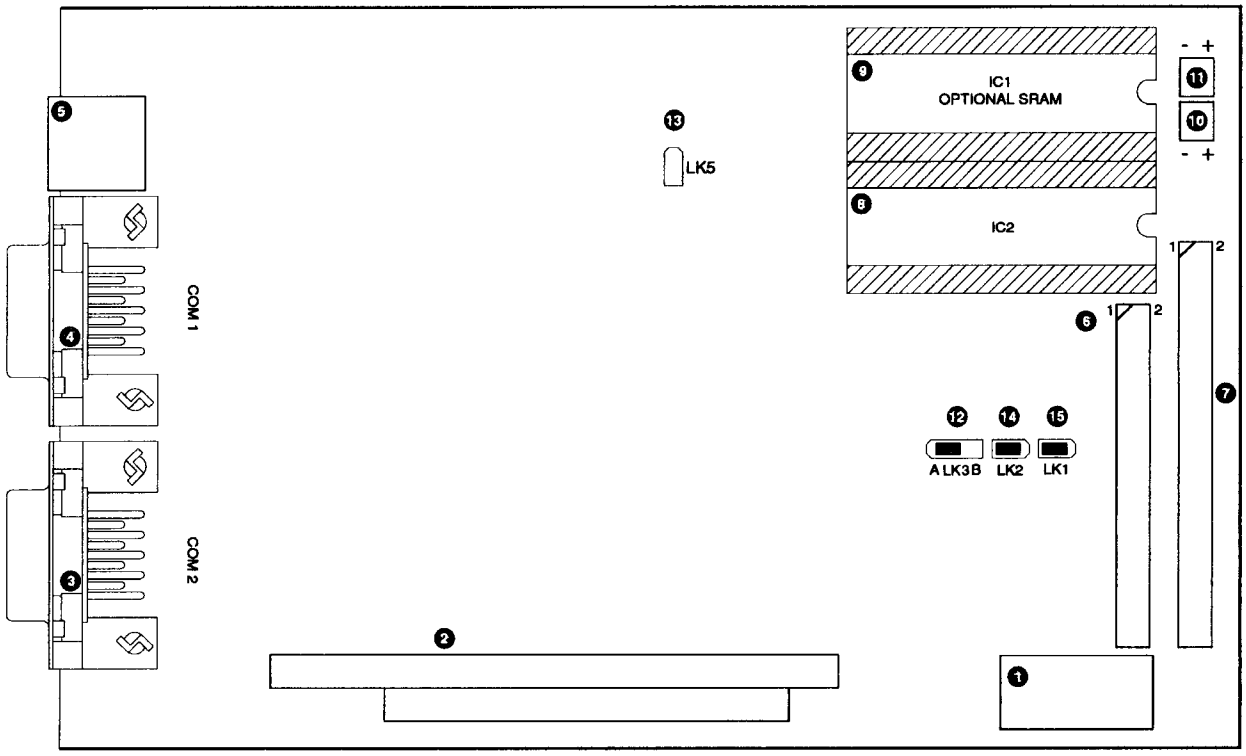
- All ROM-DOS 6.22 files.
- All Arcom Flash Filing System Files.
- SRAMDISK.SYS - Device driver to use SRAM as high speed read/write drive.
- RDUSER.DOC - Self extracting ZIP file for the full ROM-DOS 6.22 User Manual.
- MS-Word 6.0 file (ROMDOS.DOC) - Comparative review of ROM-DOS 6.22 and MS-DOS 6.22 and a list of additional commands.

If the system is booted from the floppy disk drive using the SBC104 Utility Disk, the operator is prompted to either boot to the A: prompt or to reload AFFS and ROM-DOS onto the SBC104 Flash.

NOTE: Arcom Flash Filing System (AFFS), is the generic name given to the ported Flash Filing System called CardTrick™. *Both CardTrick and ROM-DOS 6.22 are trademarks of Datalight Inc.* Each SBC104 includes two small license labels to identify the installed Datalight product. Do not remove.

Installation

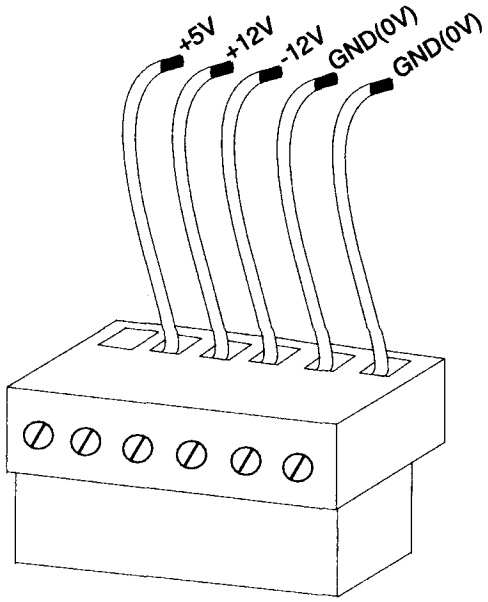
SBC104 Layout



1. Power Connector
2. 16 bit PC/104 Interface Connector
3. COM2 Connector
4. COM1 Connector
5. Keyboard Connector
6. FDD Interface Connector
7. HDD IDE Interface Connector
8. BIOS EPROM
9. Optional Battery Backed 128 KByte SRAM Socket
10. External IDE LED Connector
11. External Reset Switch Connector
12. Battery Link LK3 — A = Connected, B = Isolated
13. LK5 Watchdog Reset Link
14. LK2 Enable COM2 interrupt to IRQ3
15. LK1 Enable COM1 interrupt to IRQ4

Power Connections

The board only requires +5V for normal operation. If however any additional PC/104 modules are fitted, +/- 12V may also be required. These should be connected to the plug-in terminal block of PL5 (1) as shown. The board typically requires 600mA for normal operation.

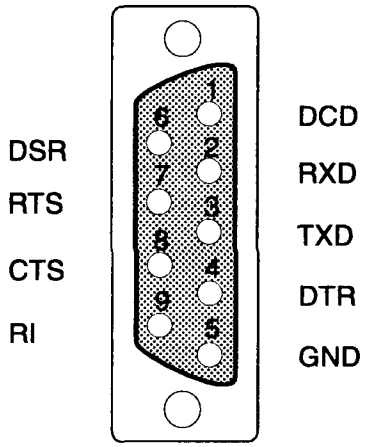


PC/104 Interface

Both 8-bit and 16-bit modules can be fitted to the SBC104. The board complies with the PC/104 specification with the exception that the MASTER* signal line is not implemented on the CD connector. The SBC104 is therefore the only master allowed on the system bus.

Care should be taken when installing modules, especially 16-bit types. Ensure that all pins are correctly aligned with the sockets on the SBC104 before pushing the module home. The module should then be secured with the fixing kit provided with the add on module.

COM1 & COM2 Connections



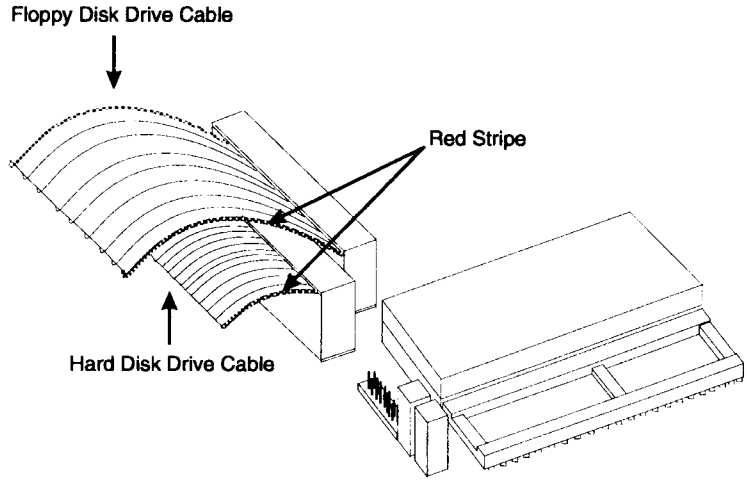
Keyboard Connection

The SBC104 will interface to a standard PC-AT keyboard. A 5-pin DIN socket to 6-pin 'Mini' DIN plug adaptor cable is required.

Floppy Disk Drive & Hard Disk Drive Connections

An FDD and HDD can be connected to the SBC104 using standard 34-way and 40-way ribbon cable assemblies respectively. The ribbon cable IDC connectors should be fitted as shown.

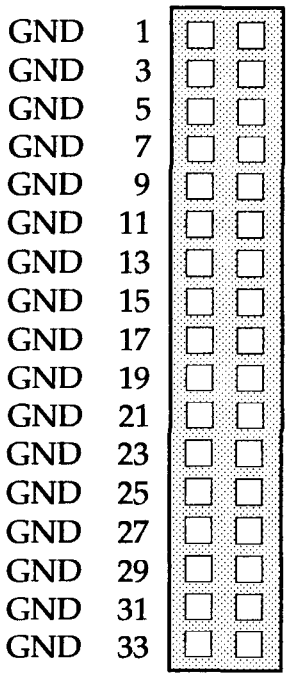
NOTE: The floppy disk header should be connected to the drive using standard ribbon cable. No modified (twisted) cable is required.



40-way IDE HDD Connector

/RST	1	2	GND
IDE D7	3	4	D8
D6	5	6	D9
D5	7	8	D10
D4	9	10	D11
D3	11	12	D12
D2	13	14	D13
D1	15	16	D14
D0	17	18	D15
GND	19	20	n/c
n/c	21	22	GND
/IOWR	23	24	GND
/IORD	25	26	GND
n/c	27	28	n/c
n/c	29	30	GND
IRQ14	31	32	/IOCS16
A1	33	34	n/c
A0	35	36	A2
/HDCS0	37	38	/HDCS1
Drive access LED	39	40	GND

34-way Floppy Disk Drive Header



GND	1	2	Low Current
GND	3	4	n/c
GND	5	6	n/c
GND	7	8	/Index
GND	9	10	/Drive 0
GND	11	12	/Drive 1
GND	13	14	n/c
GND	15	16	/Motor 0/1
GND	17	18	Direction
GND	19	20	/Step
GND	21	22	/Write Data
GND	23	24	/Write Gate
GND	25	26	/Track 0
GND	27	28	/Write Protect
GND	29	30	/Read Data
GND	31	32	Head Select
GND	33	34	Disk Changed

System BIOS

The SBC104 board is fitted with Chips and Technologies SCATSX BIOS. The BIOS includes special extensions to support the Flash Filing System. This feature allows the board to boot directly from the Flash drive. An extension is also included to ensure that the DOS clock correctly interprets the date information in the next millennium.

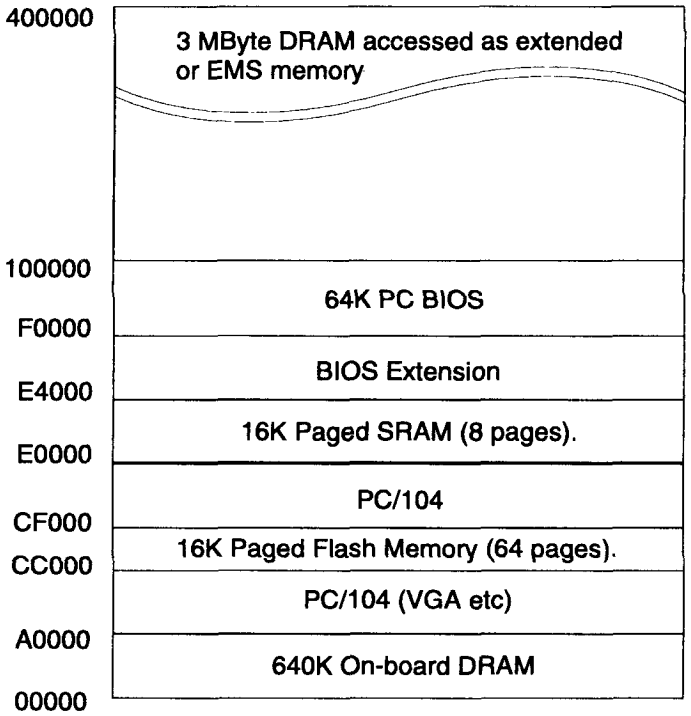
SRAM

A 32-pin DIL socket (IC1) is fitted to the board to allow the installation of a 128 Kbyte SRAM i.c. by the customer. SRAMS should be standard low power (-L) versions with an access time <120ns. Back-up is provided by the on-board Ni-MH battery. The SRAM may be initialised as a battery backed DOS drive by adding SRAMDISK.SYS in your CONFIG.SYS file as follows: DEVICE = SRAMDISK.SYS SBC104

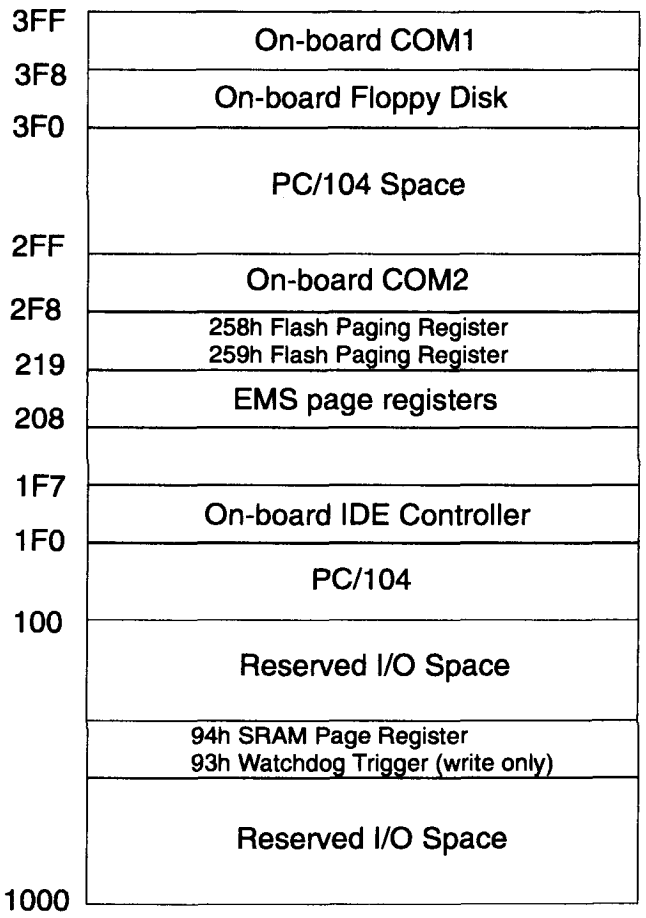
Watchdog Timer

The Watchdog is not active after system reset. After the first access to the Watchdog (write any value to I/O port 93h), this must be repeated within a 3 second period. If this does not occur, the NMI line will be asserted. If LK5 is inserted, the SBC104 will be reset.

Memory Map



I/O Map



On-board I/O Registers

258h

This register is cleared at reset.

D7	Flash Memory enable bit (low to enable)
D6	Reserved
D5	Reserved
D4	Reserved
D3	Flash Memory low page address (A17)
D2	Flash Memory low page address (A16)
D1	Flash Memory low page address (A15)
D0	Flash Memory low page address (A14)

259h

This register is cleared at reset.

D7	Not used
D6	Not used
D5	Not used
D4	Not used
D3	Not used
D2	Not used
D1	Flash Memory upper page address (A19)
D0	Flash Memory upper page address (A18)

94h

D7	SRAM write enable bit (High to enable, cleared at reset)
D6	Not used
D5	Not used
D4	Not used
D3	Not used
D2	SRAM page address (A16)
D1	SRAM page address (A15)
D0	SRAM page address (A14)

93h Watchdog Timer

Writing to this address will trigger the watchdog timer. This must be re-triggered within 3 seconds to avoid generating an NMI or if LK5 is fitted a system reset.

Appendix A.

PC/104 Connector Pin Assignments

Pin Number	SK2 Row A	SK2 Row B	SK1 Row C	SK1 Row D
0	--	--	0V	0V
1	IOCHCHK*	0V	SBHE*	MEMCS16*
2	SD7	RESETDRV	LA23	IOCS16*
3	SD6	+5V	LA22	IRQ10
4	SD5	IRQ9	LA21	IRQ11
5	SD4	--	LA20	IRQ12
6	SD3	--	LA19	IRQ15
7	SD2	-12V	LA18	--
8	SD1	ENDXFR*	LA17	DACK0*
9	SD0	+12V	MEMR*	DRQ0
10	IOCHRDY	--	MEMW*	DACK5*
11	AEN	SMEMW*	SD8	DRQ5
12	SA19	SMEMR*	SD9	DACK6*
13	SA18	IOW*	SD10	DRQ6
14	SA17	IOR*	SD11	DACK7*
15	SA16	DACK3*	SD12	DRQ7
16	SA15	DRQ3	SD13	+5V
17	SA14	DACK1*	SD14	--
18	SA13	DRQ1	SD15	0V
19	SA12	REFRESH*	--	0V
20	SA11	SYSCLK	--	--
21	SA10	IRQ7	--	--
22	SA9	--	--	--
23	SA8	IRQ5	--	--
24	SA7	IRQ4 *(Note 1)*	--	--
25	SA6	IRQ3 *(Note 2)*	--	--
26	SA5	--	--	--
27	SA4	TC	--	--
28	SA3	BALE	--	--
29	SA2	+5V	--	--
30	SA1	OSC (14.318MHZ)	--	--
31	SA0	0V	--	--
32	0V	0V	--	--

(Note 1) Link 2 must be removed to use this PC/104 interrupt line.
(Note 2) Link 1 must be removed to use this PC/104 interrupt line.

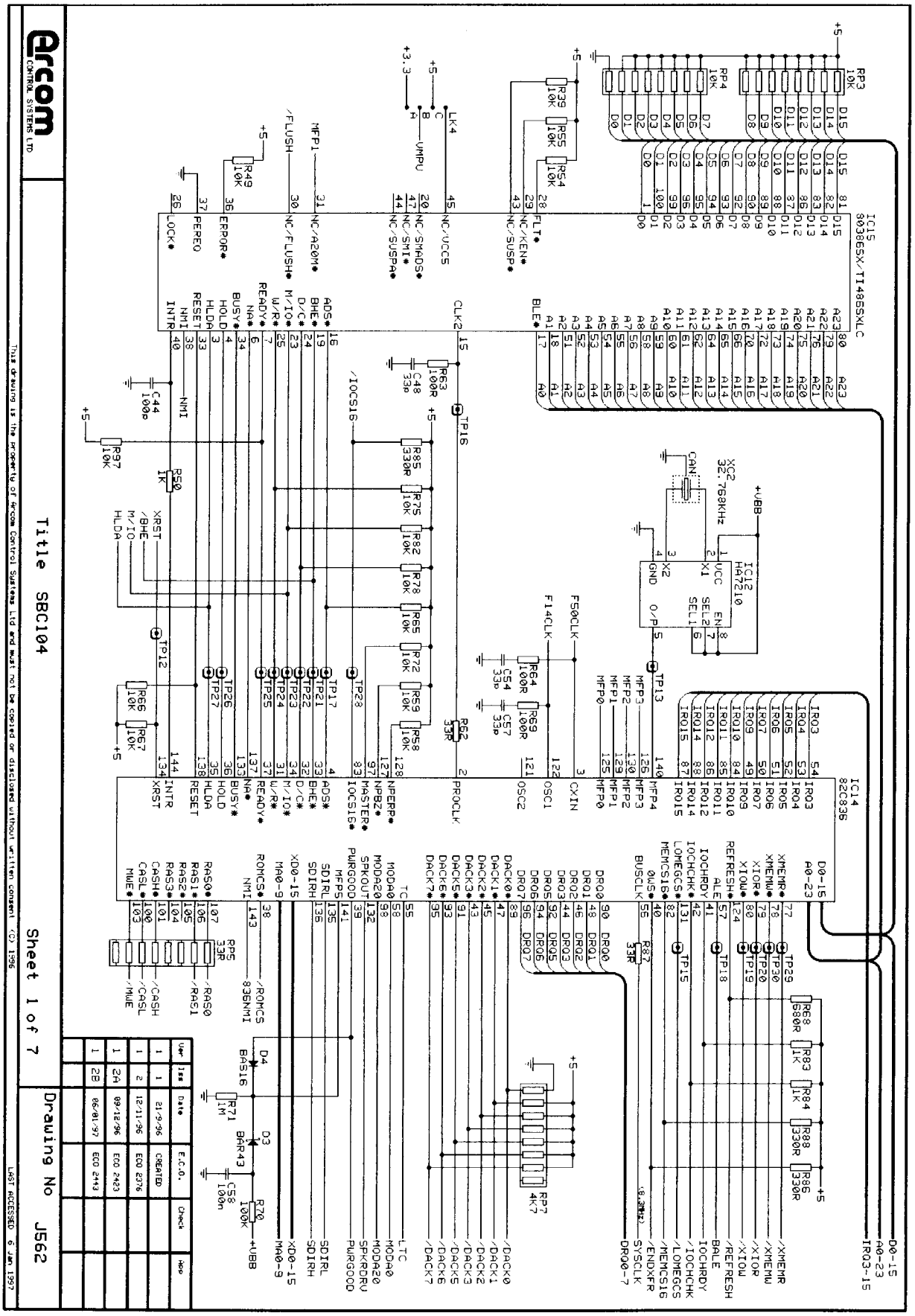
Appendix B

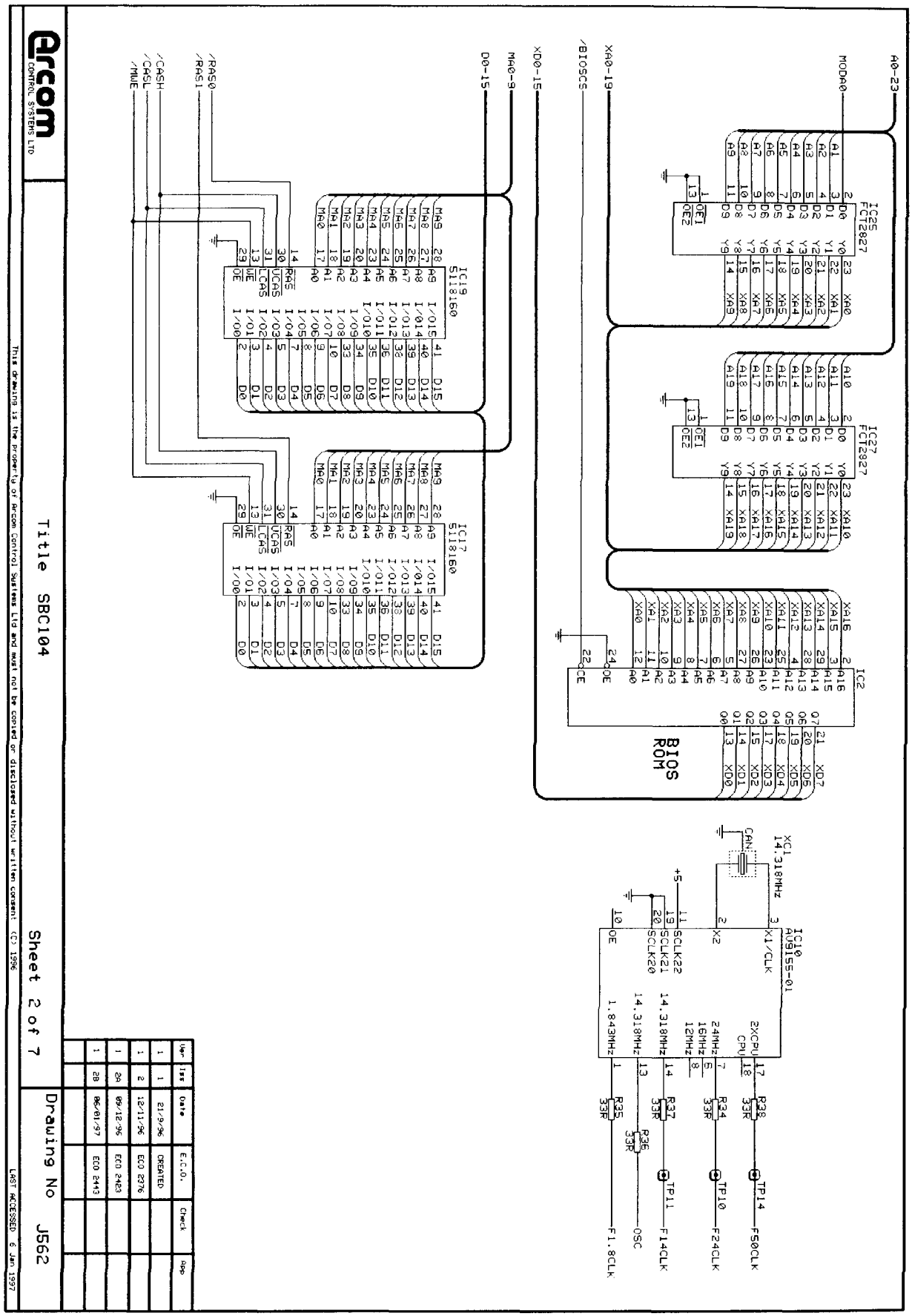
Audible Signals

The BIOS provides audio alert signals during the Power On Self Test. Each of these is specified below. In each case, long and short refer to the time period of the beep.

Audio Alert	Condition	Description
1 long	POST Passed	This indicates that all of the Power On Self Test (POST) hardware tests completed without encountering any errors.
1 long	POST Failed	This is caused by failure of one of the Power On Self Test (POST) hardware tests.
1 long & 2 short	Video Adaptor Failure	Video BIOS ROM Failure Checksum error encountered.
1 long & 3 short	Video Failure	This is caused by one of three possible hardware problems: 1. The Video DAC failed 2. The monitor detection process failed 3. The video RAM test failed
3 short	64K RAM Failed	The system BIOS could not rely on the integrity of the memory due to a failure of the base 64K of system RAM.

Appendix C. Circuit Diagrams





Ver	Iss	Date	E.C.O.	Check	App
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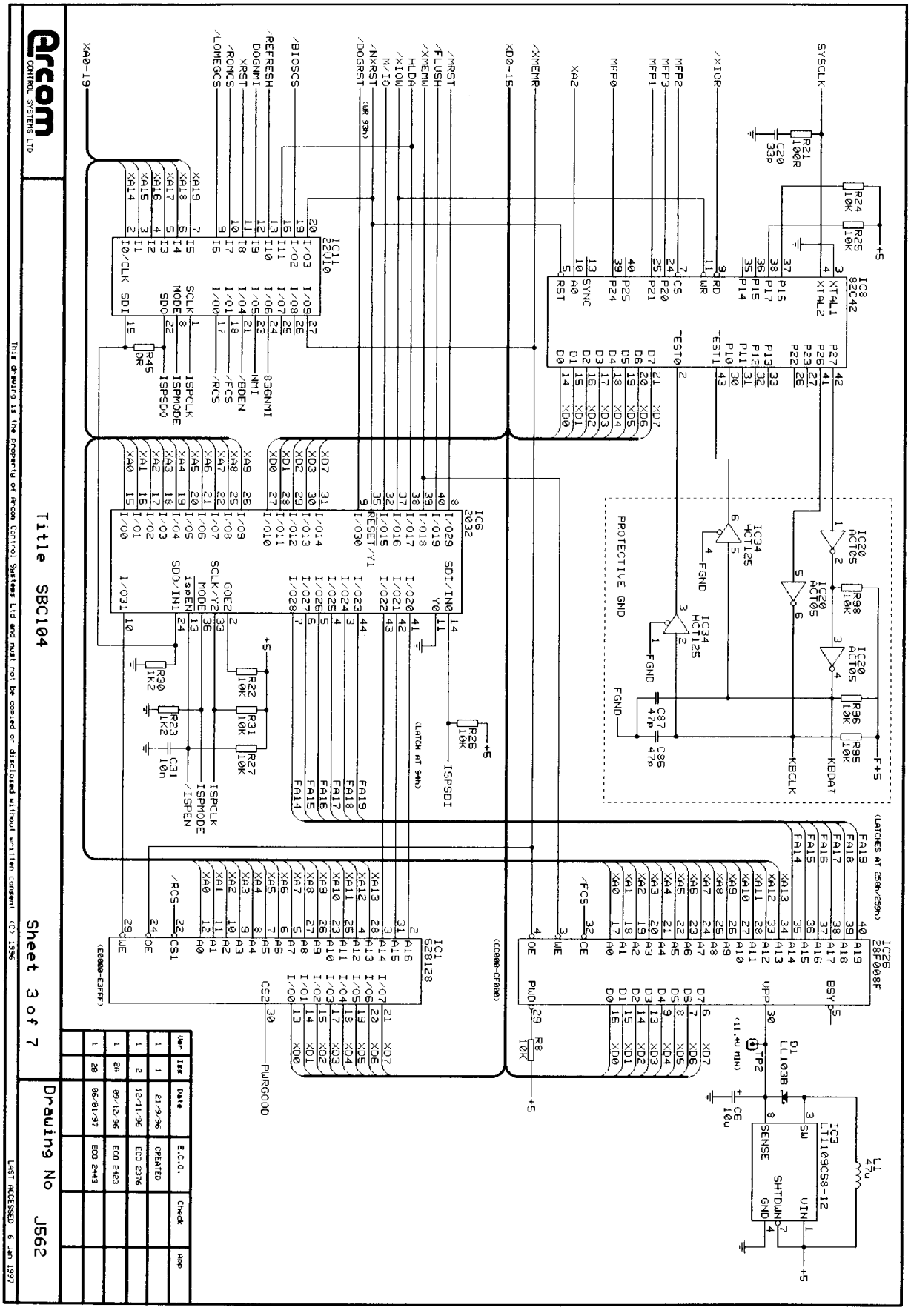
1	2	12/11/96	ECO 2376		
1	2a	05/12/96	ECO 2423		
1	2B	06/01/97	ECO 2443		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Title SBC104
Sheet 3 of 7
Drawing No J562
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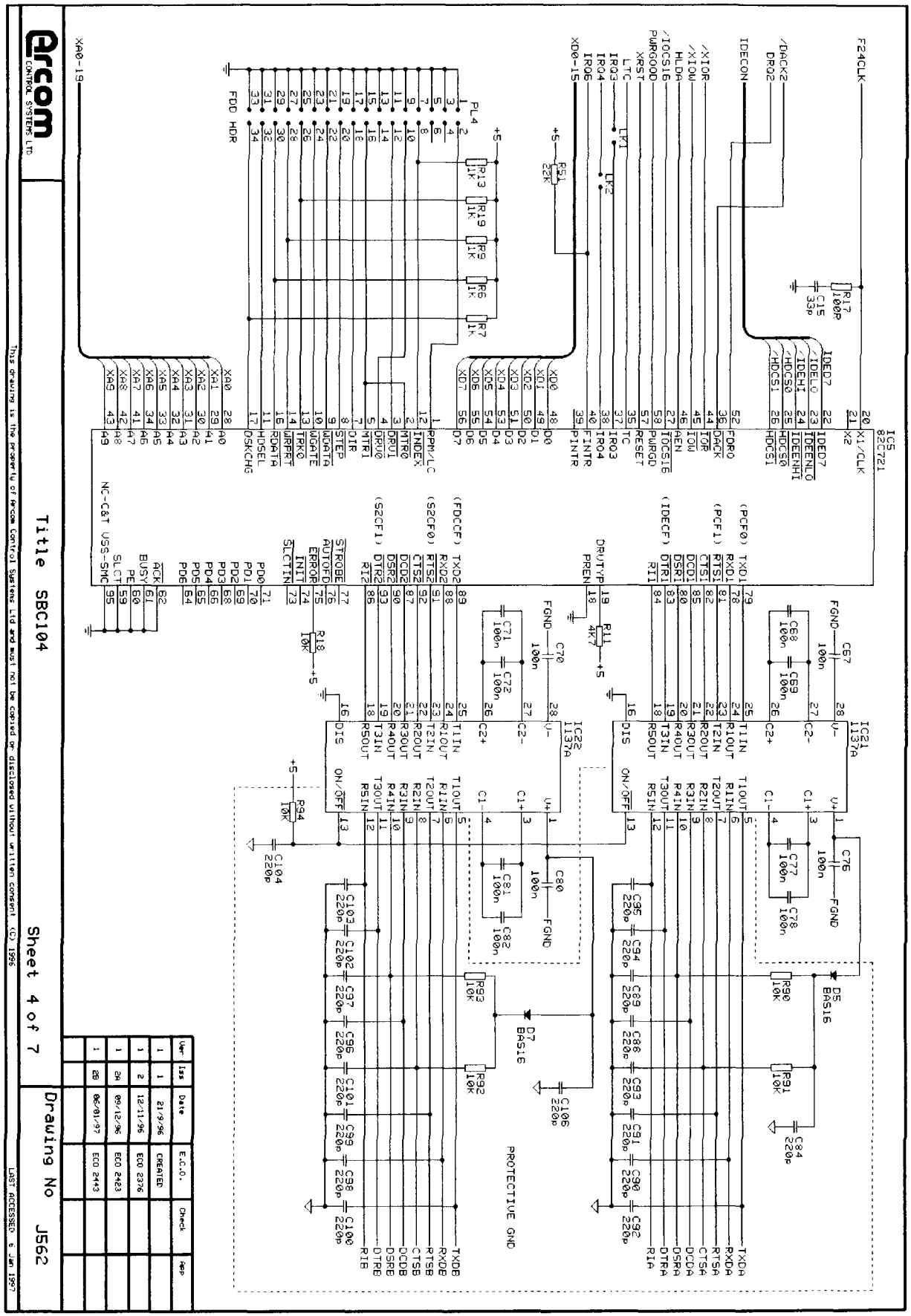
Iss Date E.C.O. Check App
1 21-9-96 CREATED
2 12-11-96 ECO 2376
2A 09-12-96 ECO 2423
2B 06-01-97 ECO 2443
SYSCLK
/XIOR
/XIOW
/XMEMR
/XMEMW
XD0-15
XA0-19
/MRST
/FLUSH
HLDA
M/IO
/NXRST
/DOGRST
/REFRESH
/BIOSCS
/ROMCS
/LOMEGCS
XRST
DOGNMI
/FCS
/RCS
/BDEN
/NMI
836NMI
ISPCLK
ISPMODE
ISPSDO
ISPSDI
/ISPEN
PROTECTIVE GND
FGND
KBCLK
KBDAT
+5
+F5
PWRGOOD
IC8 82C42
IC11 22V10
IC6 2032
IC20 ACT05
IC34 HCT125
IC1 S28128
IC26 28F008F
IC3 LT1109CS8-12
R21 100R
C20 33p
R24 10K
R25 10K
R98 10K
R96 10K
R95 10K
R45 0R
R30 1K2
R23 1K2
R22 10K
R31 10K
R27 10K
R26 10K
R8 10K
C31 10n
C87 47p
C86 47p
C6 10u
L1 47u
D1 LL103B
TP2
(11.4V MIN)
(LATCHES AT 250ns/230ns)
(LATCH AT 94ns)
(C0000-CF000)
(E0000-E3FFF)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Sheet 4 of 7
Drawing No J562
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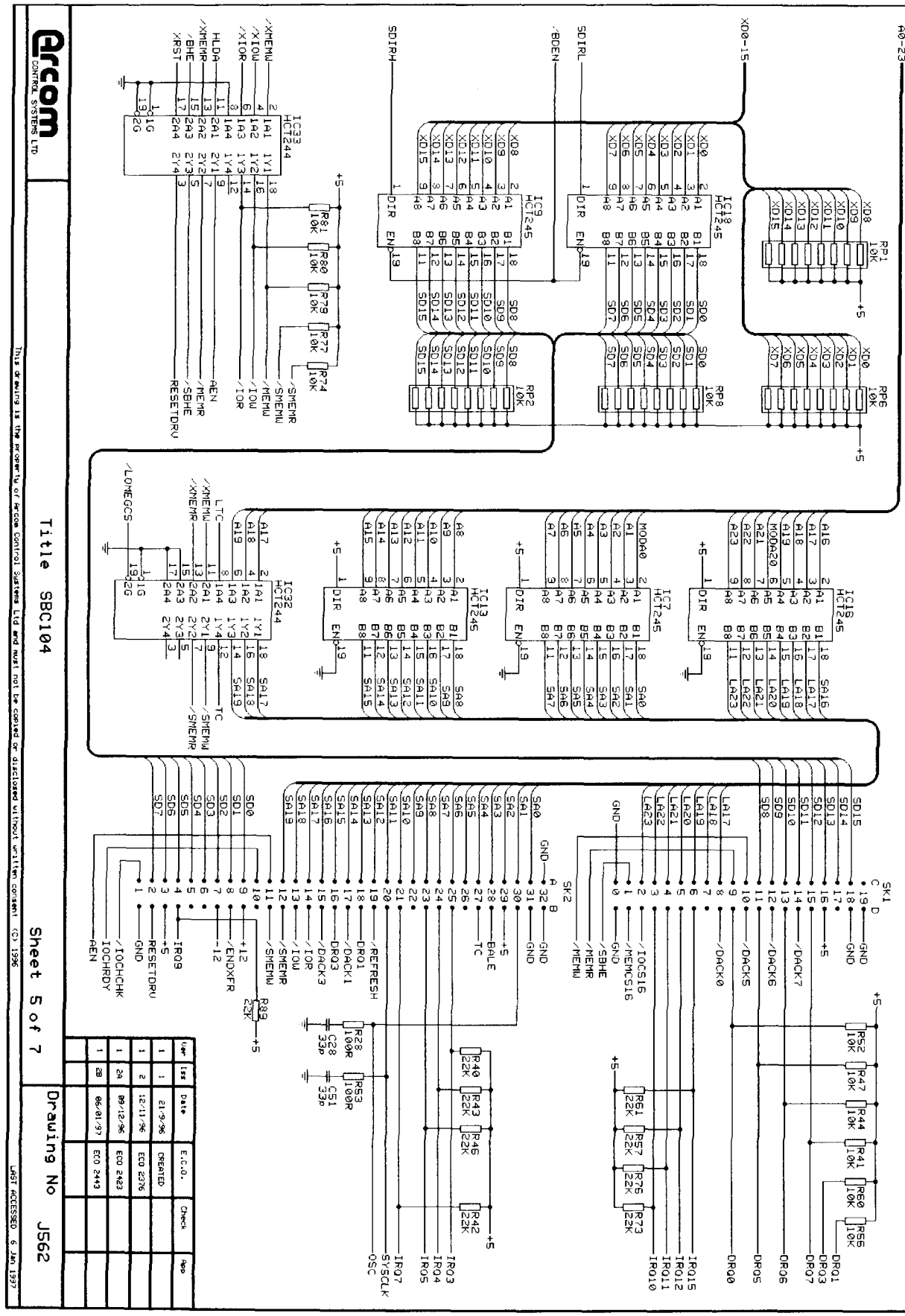
LAST ACCESSED: 6 JAN 1997
F24CLK
XA0-19
XD0-15
IDECON
/DACK2
DRQ2
/XIOR
/XIOW
HLDA
/IOCS16
PURGOOD
XRST
LTC
IRQ3
IRQ4
IRQ6
IC5 82C721
FDD HDR
PL4
IC21 1137A
IC22 1137A
PROTECTIVE GND
D5 BAS16
D7 BAS16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Sheet 5 of 7
Drawing No J562
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LAST ACCESSED 6 Jan 1997
A0-23
XD0-15
SDIRH
SDIRL
BDEN
/XMEMW
/XIOW
/XIOR
HLDA
/XMEMR
/BHE
/XRST
AEN
/MEMR
/SBHE
RESETDRV
/SMEMR
/MEMW
/IOW
/IOR
/LOMEGCS
TC
/SMEMW
/SMEMR
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
+12
/ENDXFR
IRQ9
+5
RESETDRV
GND
/IOCHCHK
IOCHRDY
AEN
/REFRESH
/DACK1
DRQ3
/DACK3
/IOR
/IOW
/SMEMW
/SMEMR
BALE
TC
SYSCLK
OSC
IRQ7
IRQ4
IRQ5
IRQ3
/IOCS16
/MEMCS16
/SBHE
/MEMR
/MEMW
IRQ15
IRQ12
IRQ11
IRQ10
/DACK5
/DACK6
/DACK7
/DACK0
DRQ5
DRQ6
DRQ7
DRQ0
DRQ1
DRQ3
DRQ7
IC33 HCT244
IC9 HCT245
IC18 HCT245
IC7 HCT245
IC13 HCT245
IC19 HCT245
IC32 HCT244
SK1
SK2
RP1 10K
RP2 10K
RP8 10K
RP6 10K
R81 10K
R80 10K
R79 10K
R77 10K
R74 10K
R89 22K
R28 100R
R53 100R
C28 33p
C51 33p
R40 22K
R43 22K
R46 22K
R42 22K
R52 10K
R47 10K
R44 10K
R41 10K
R60 10K
R55 10K
R61 22K
R57 22K
R76 22K
R73 22K
Iss
Date
E.C.O.
Check
Rev
1
21-9-96
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2
12-11-96
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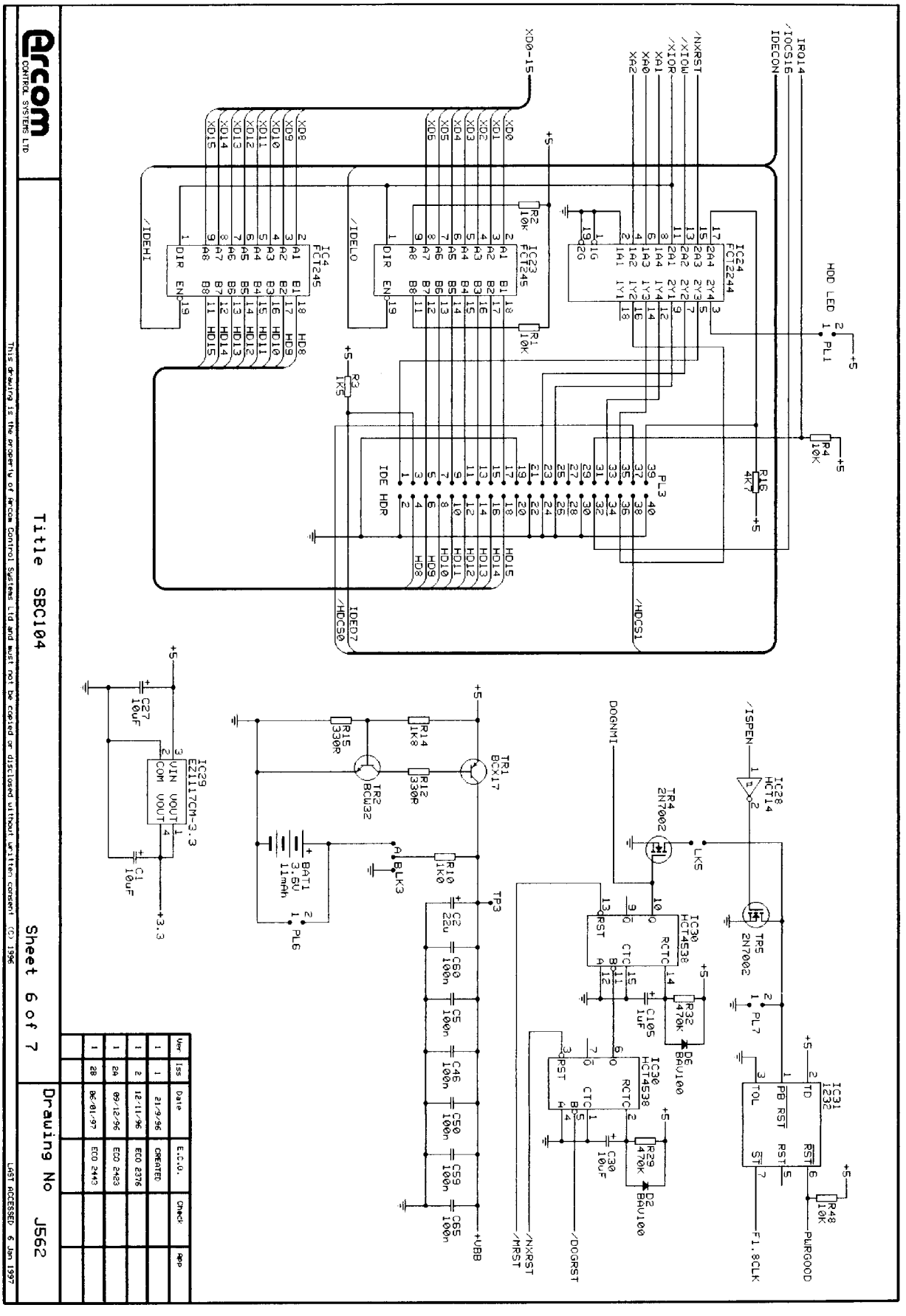
2A
09-12-96
ECO 2423
1
2B
06-01-97
ECO 2443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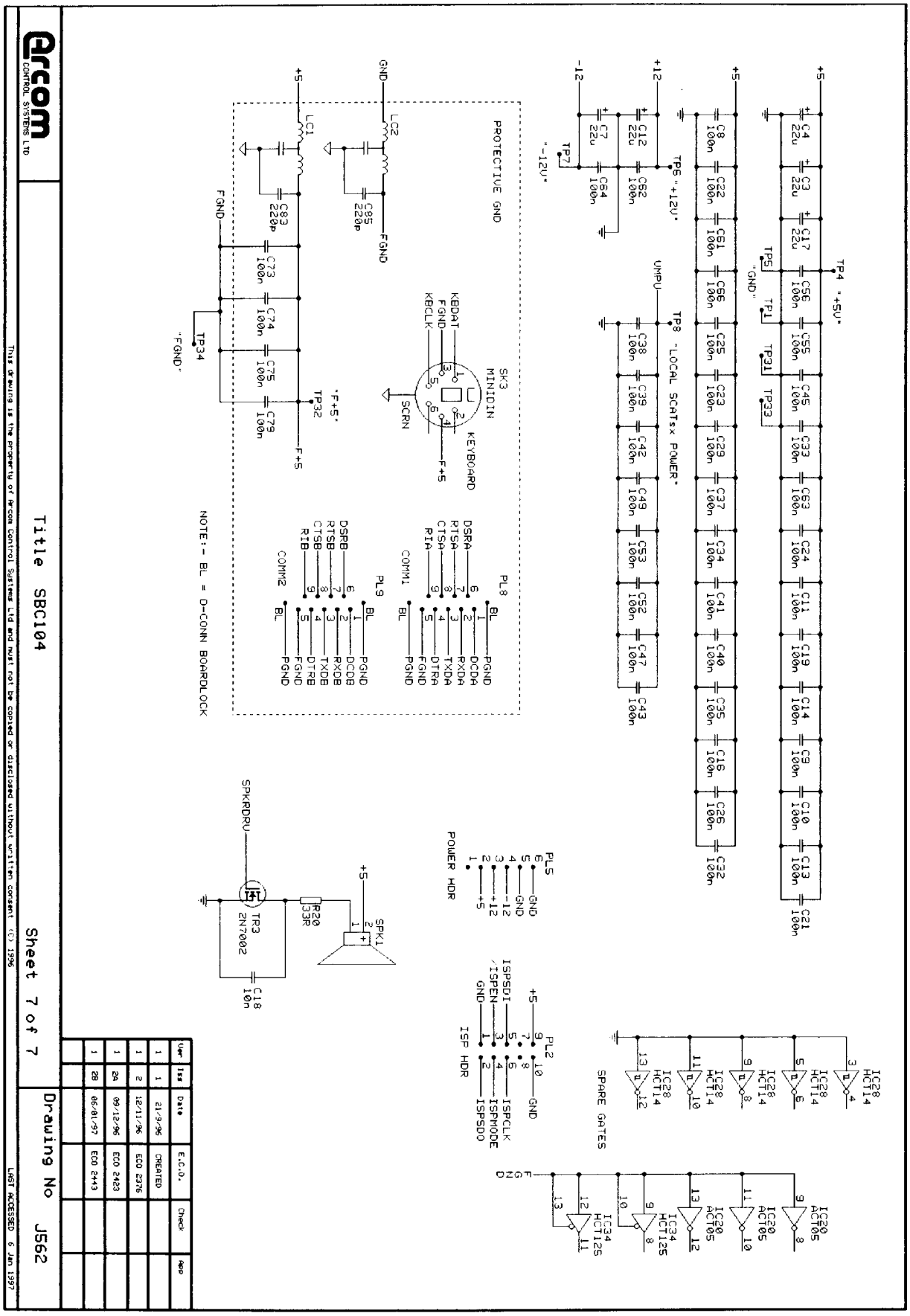
1 2 12-11-96 ECO 2376
1 2A 09-12-96 ECO 2423
1 2B 06-01-97 ECO 2443
IRQ14
/IOCS16
IDECON
/NXRST
/XIOW
/XIOR
XA1
XA0
XA2
XD0-15
IC24 FCT2244
IC23 FCT245
IC4 FCT245
/IDEHI
/IDELO
IDED7
/HDCS0
/HDCS1
IDE HDR
HDD LED
PL1
PL3
R1 10K
R2 10K
R3 1K5
R4 10K
R16 4K7
IC28 HCT14
IC30 HCT4538
IC31 1232
TR1 BCX17
TR2 BCW32
TR4 2N7002
TR5 2N7002
DE BAV100
D2 BAV100
BAT1 3.5V 11mAh
PL6
PL7
LK3
LK5
IC29 EZ1117CM-3.3
C27 10uF
C1 10uF
C2 22u
C60 100n
C5 100n
C46 100n
C50 100n
C59 100n
C65 100n
C105 1uF
C30 10uF
R10 1k0
R12 330R
R14 1K8
R15 330R
R32 470K
R29 470K
R48 10K
TP3
+VBB
+3.3
DOGNMI
/ISPEN
/NXRST
/MRST
/DOGRST
PURGOOD
F1.8CLK


Arcom CONTROL SYSTEMS LTD
Title SBC104
Sheet 7 of 7
Drawing No J562
PROTECTIVE GND
SK3 MINIDIN KEYBOARD
PL8
PL9
COMM1
COMM2
NOTE:- BL = D-CONN BOARDLOCK
"+5V"
"GND"
"+12V"
"-12V"
"LOCAL SCATsx POWER"
"FGND"
"F+5"
SPKRDRV
TR3 2N7002
SPK1
POWER HDR
PL5
PL2
ISP HDR
SPARE GATES
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United Kingdom

Arcom Control Systems Ltd
Clifton Road
Cambridge
cb1 4wh, UK
tel: +44 (0)1223 411200
fax: +44 (0)1223 410457
e-mail: sales@arcom.co.uk
support@arcom.co.uk

United States

Arcom Control Systems Inc
13510 South Oak Street
Kansas City MO 64145, USA
tel: +1 (816) 941 7025
fax: +1 (816) 941 0343

France

Arcom Control Systems
Centre d' affaires SCALDY
23, rue Colbert
78885 SAINT QUENTIN
Cedex, FRANCE
tel: Numéro Vert 0800 90 84 06
fax: Numéro Vert 0800 90 84 12

Germany

Arcom Control Systems
Kostenlose Infoline:
tel: 0130 824 511
fax: 0130 824 512