

Datasheet

Industrial DRAM

DDR5 SODIMM Series



Specifications Overview

- **Capacity**
 - 8GB, 16GB, 32GB, 48GB
- **Form Factor**
 - DDR5 SODIMM
- **Performance**
 - 4800 = 38.4 GB/s
 - 5600 = 44.8 GB/s
- **Temperature Range**
 - Operation temperature:
 - Normal temperature: -20°C ~ 95°C
 - Wide temperature: -40°C ~ 105°C
- **Power Consumption**
 - Supply Voltage: DC +1.1V ± 5%
- **Compliant Specifications**
 - RoHS



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Revision History

Revision	Date	Description
1.0	2022/08	First Release
1.1	2022/09	Add DDR5-5600
1.2	2023/06	Add DDR5 8GB (1Gx16) Update IDD Specification
1.3	2023/10	Add Hynix Solution Update Normal Temperature to -20°C Update IDD Specification
1.4	2023/12	Update Temperature
1.5	2024/09	Adjust Format Add DDR5 48GB (3Gx8)
1.6	2024/10	Update Wide Temperature
1.7	2024/12	Revise 1.2 Features Update Overview
1.8	2025/08	Update Order Information
1.9	2025/12/2	Update Datasheet Format & Order Information
2.0	2025/12/5	Add CXMT Solution
2.1	2026/03/19	Add Spectek Solution



1. Product Description

1.1 Overview

Silicon Power Computer & Communications industrial DRAM products are JEDEC standard 262-Pin low power Double Data Rate 5 (DDR5) Synchronous DRAM Small Outline Dual In-Line Memory Module (SODIMM). DDR5 SODIMM provide a high-performance, flexible 8-byte interface in a space-saving footprint. It is commonly used as the main memory in computers and other devices due to its cost-effectiveness and relatively high speed.

1.2 Features

- Fast data transfer rates:

Module Transfer Rates	Supported Transfer Rates	
	DDR5-4800(CL40)	DDR5-5600 (CL46)
DDR5-4800	V	
DDR5-5600	V	V

- Single or Dual rank
- $V_{DD} = V_{DDQ} = 1.1V \pm 0.06V$
- Terminated clock, control and command/address
- Halogen-free
- Data bus inversion (DBI) for data bus
- Integrated serial presence-detect (SPD) EEPROM
- Fly-by topology
- Gold edge contacts



2. Specification

2.1 Physical Dimension

2.1.1 Dimension

Table 1: Physical Dimension

Parameter	Dimension
Length	69..60 ± 0.1mm
Width	30.0 ± 0.1mm
Thickness (connector)	1.2mm ± 0.1mm

2.1.2 Weight

- 9.5g ± 10%

2.2 Performance

- DDR5-4800 (PC5-38400)
- DDR5-5600 (PC5-44800)

2.3 Environmental Conditions

Table 2: Environmental Conditions

Feature	Operating	Storage
Temperature (Normal Grade)	-20°C ~ 95°C	-55°C ~ 110°C
Humidity	10% ~ 95% RH, non-condensing	
Vibration	20G (Peak-to-Peak), 80~2000 Hz	
Shock	1,500G, 0.5ms	

Notice:

- Vibration: Duration, 30 min x 3 axis.
- Shock: 1500G, 0.5msec, half-sine wave, 3 times in each direction, total = 18 times (6 directions).
- Temperature: The temperature reading is for the environment defined as Ta.

2.4 Compliance Specifications

- RoHS

3. Functional Description

3.1 Pin Assignment

Table 3: Pin Assignment

262-Pin DDR5 SODIMM Front								262-Pin DDR5 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol		
1	VIN_BVLK	67	VSS	13 1	CK0_A_t	19 7	VSS	2	HSA	68	DQ21_A	13 2	CK1_A_t	19 8	DQ7_B
3	VIN_BVLK	69	DQ22_A	13 3	CK0_A_c	19 9	DQ8_B	4	HSCL	70	VSS	13 4	CK1_A_c	20 0	VSS
5	RFV	71	VSS	13 5	VSS	20 1	VSS	6	HSDA	72	DQ23_A	13 6	VSS	20 2	DQ9_B
7	PWR_GOOD	73	DQ24_A	13 7	CK0_B_t	20 3	DQ10_B	8	PWR_EN	74	VSS	13 8	CK1_B_t	20 4	VSS
9	VSS	75	VSS	13 9	CK0_B_c	20 5	VSS	10	VSS	76	DQ25_A	14 0	CK1_B_c	20 6	DQ11_B
11	DQ0_A	77	DQ26_A	14 1	VSS	20 7	DQS1_B_c	12	DQ1_A	78	VSS	14 2	VSS	20 8	VSS
13	VSS	79	VSS	14 3	RFV	20 9	DQS1_B_t	14	VSS	80	DQ27_A	14 4	CA12_B	21 0	DM1_B_n
15	DQ2_A	81	DQS3_A_c	14 5	CA11_B	21 1	VSS	16	DQ3_A	82	VSS	14 6	CA10_B	21 2	VSS
17	VSS	83	DQS3_A_t	14 7	VSS	21 3	DQ12_B	18	VSS	84	DM3_A_n	14 8	VSS	21 4	DQ13_B
19	DM0_A_n	85	VSS	14 9	CA9_B	21 5	VSS	20	DQS0_A_	86	VSS	15 0	CA8_B	21 6	VSS
21	VSS	87	DQ28_A	15 1	CA7_B	21 7	DQ14_B	22	DQS0_A_	88	DQ29_A	15 2	CA6_B	21 8	DQ15_B
23	DQ4_A	89	VSS	15 3	VSS	21 9	VSS	24	VSS	90	VSS	15 4	VSS	22 0	VSS
25	VSS	91	DQ30_A	15 5	CA5_B	22 1	DQ16_B	26	DQ5_A	92	DQ31_A	15 6	CA4_B	22 2	DQ17_B
27	DQ6_A	93	VSS	15 7	CA3_B	22 3	VSS	28	VSS	94	VSS	15 8	CA2_B	22 4	VSS
29	VSS	95	CB0_A	15 9	VSS	22 5	DQ18_B	30	DQ7_A	96	CB1_A	16 0	VSS	22 6	DQ19_B
31	DQ8_A	97	VSS	16 1	CS0_B_n	22 7	VSS	32	VSS	98	VSS	16 2	CA1_B	22 8	VSS
33	VSS	99	CB2_A	16	RESET_n	22	DM2_B_n	33	DQ09_A	10	DQS4_A_	16	CA0_B	23	DQS2_B_

262-Pin DDR5 SODIMM Front								262-Pin DDR5 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol		
3				3		9		4		0	c	4		0	c
3	DQ10_A	10	VSS	16	CS1_B_n	23	VSS	3	VSS	10	DQS4_A_t	16	VSS	23	DQS2_B_t
5		1		5		1		6		2		6		2	
3	VSS	10	CB3_A	16	VSS	23	DQ20_B	3	DQ11_A	10	VSS	16	CB0_B	23	VSS
7		3		7		3		8		4		8		4	
3	DQS1_A_c	10	VSS	16	DQS4_B_c	23	VSS	4	VSS	10	CS0_A_n	17	VSS	23	DQ21_B
9		5		9		5		0		6		0		6	
4	DQS1_A_t	10	CA0_A	17	DQS4_B_t	23	DQ22_B	4	DM1_A_n	10	ALERT_n	17	CB1_B	23	VSS
1		7		1		7		2		8		2		8	
4	VSS	10	CA1_A	17	VSS	23	VSS	4	VSS	11	CS1_A_n	17	VSS	24	DQ23_B
3		9		3		9		4		0		4		0	
4	DQ12_A	11	VSS	17	CB3_B	24	DQ24_B	4	DQ13_A	11	VSS	17	CB2_B	24	VSS
5		1		5		1		6		2		6		2	
4	VSS	11	CA2_A	17	VSS	24	VSS	4	VSS	11	CA3_A	17	VSS	24	DQ25_B
7		3		7		3		8		4		8		4	
4	DQ14_A	11	CA4_A	17	DQ0_B	24	DQ26_B	5	DQ15_A	11	CA5_A	18	DQ1_B	24	VSS
9		5		9		5		0		6		0		6	
5	VSS	11	VSS	18	VSS	24	VSS	5	VSS	11	VSS	18	VSS	24	DQ27_B
1		7		1		7		2		8		2		8	
5	DQ16_A	11	CA6_A	18	DQ2_B	24	DQS3_B_c	5	DQ17_A	12	CA7_A	18	DQ3_B	25	VSS
3		9		3		9		4		0		4		0	
5	VSS	12	CA8_A	18	VSS	25	DQS3_B_t	5	VSS	12	CA9_A	18	VSS	25	DM3_B_n
5		1		5		1		6		2		6		2	
5	DQ18_A	12	VSS	18	DM0_B_n	25	VSS	5	DQ19_A	12	VSS	18	DQS0_B_c	25	VSS
7		3		7		3		8		4		8		4	
5	VSS	12	CA10_A	18	VSS	25	DQ28_B	6	VSS	12	CA11_A	19	DQS0_B_t	25	DQ29_B
9		5		9		5		0		6		0		6	
6	DM2_A_n	KEY		19	DQ4_B	25	VSS	6	DQS2_A_c	KEY		19	VSS	25	VSS
1				1		7		2				2		8	
6	VSS	12	CA12_A	19	VSS	25	DQ30_B	6	DQS2_A_t	12	RFV	19	DQ5_B	26	DQ31_B
3		7		3		9		4		8		4		0	
6	DQ20_A	12	VSS	19	DQ6_B	26	VSS	6	VSS	13	VSS	19	VSS	26	VSS
5		9		5		1		6		0		6		2	

Notes: 1. On modules with nominal transfer rates <6400 MT/s, this pin is RFU. On modules with nominal transfer rates ≥6400 MT/s, this pin is NPP (no pin present).

3.2 Pin Description

Table 4: Pin Description

Symbol	Type	I/O Level	Description
CK0_A_t, CK0_A_c, CK1_A_t, CK1_A_c, CK0_B_t, CK0_B_c, CK1_B_t, CK1_Bc,	Input	VDD	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA0_A - CA12_A, CA0_B - CA12_B	Input	VDD	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi cycle, the pins may not be interchangeable between devices on the same bus.
CS0_A_n - CS1_A_n, CS0_B_n - CS1_B_n	Input	VDD	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks.
DQ0_A - DQ31_A, DQ0_B - DQ31_B	Input/ Output	VDDQ	Data Input/Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst.
CB0_A - CB3_A, CB0_B - CB3_B	Input/ Output	VDDQ	DIMM ECC check bits
DQS0_A_t - DQS4_A_t DQS0_A_c - DQS4_A_c DQS0_B_t - DQS4_B_t DQS0_B_c - DQS4_B_c	Input/ Output	VDDQ	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR5 SDRAM supports differential data strobe only and does not support single-ended.

Symbol	Type	I/O Level	Description
DM0_A_n-DM3_A_, DM0_B_n-DM3_B_n	Input	VDDQ	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5]=1. .
ALERT_n	Input/ Output	VDD	Alert: If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin mVst be bounded to VDDQ on board.
RESET_n	Input	VDD	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n mVst be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ,
HSCL	Input	1.0V	Host SidebandBus bus clock, supplied by the controller.
HSDA	Input/ Output	1.0V	Host SidebandBus data, connected from the controller to Hub or Host bus Target devices.
HSA	Input	2.1V max	Host SidebandBus bus device ID address pin; input to a hub or other client device to distinguish between identical devices in the I3C-Basic/I2C address range.
RFV			Reserved for Future use. No on DIMM electrical connection is present.
PWR_GOOD	Input/ Output	Open Drain	Power good indicator. Open Drain output. The PMIC floats this pin high when VIN_Bulk input supply as well as enabled output buck regulators and all LDO regulator tolerance threshold is maintained as configured in appropriate register. The PMIC drives this pin low when VIN_Bulk input goes below the threshold or configured in the appropriate register or and LDO output regulator exceeds the threshold tolerance. Input: The PMIC disables its output regulators when this pin is low. The LDO outputs shall remain on.

Symbol	Type	I/O Level	Description
PWR_EN	Input	3.3V	PMIC Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator. this signal is connected to PMIC's VR_EN pin.
VIN_BVLK	Supply	5V	5V power input supply to the PMIC for analog circuits.
VSS	Supply		Ground

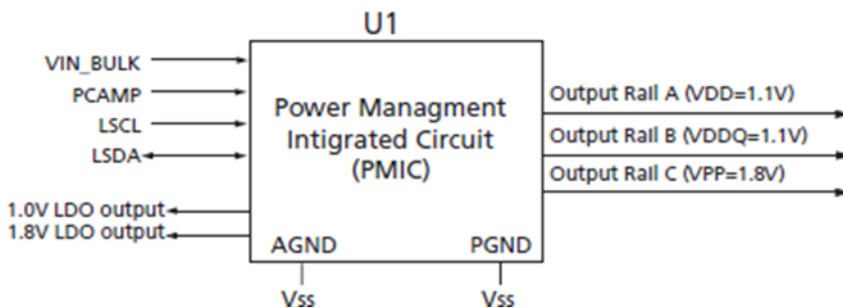
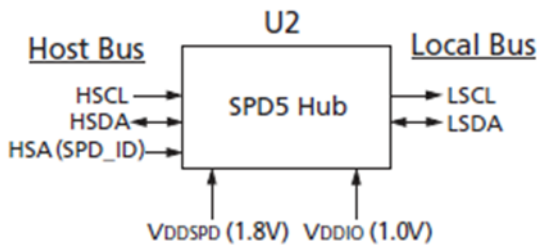
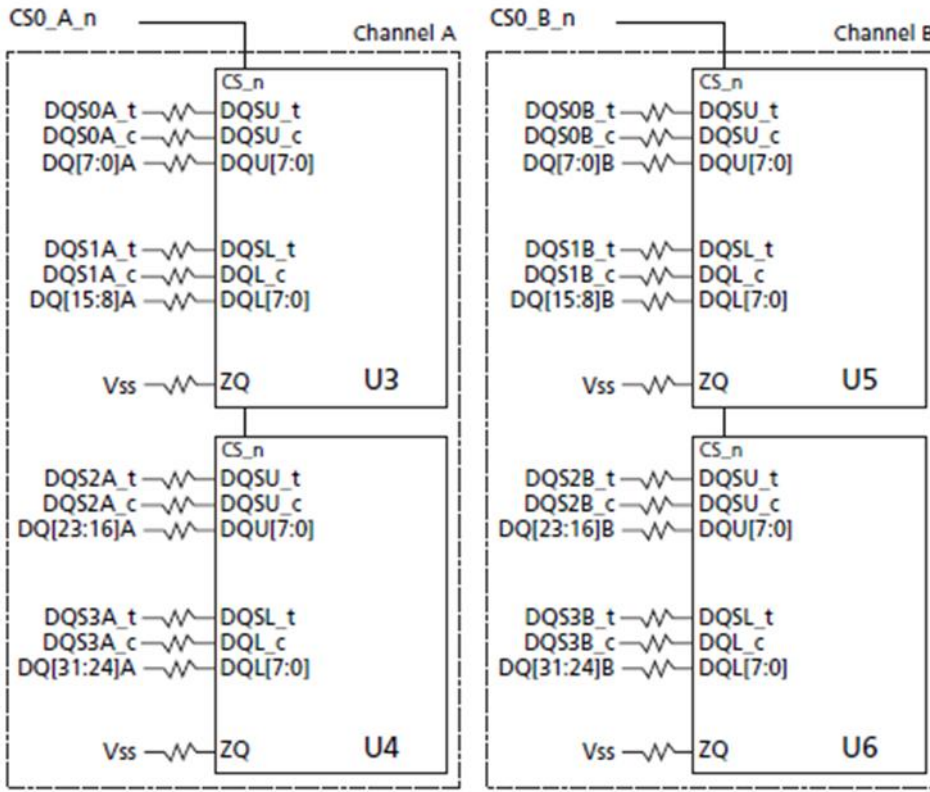
3.3 Absolute Maximum DC Ratings

Table 5: Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units
VDDSPD	Storage temperature	-65 ~ 150	°C
VDDIO	Supply voltage	-0.5 ~ 2.1	V
VDDSPD	Supply voltage	-0.5 ~ 2.1	V
HSA	HSA pin	-0.5 ~ 2.1	V
HSCL, HSDA, LSCL, LSDA	HSCL, HSDA, LSCL, LSDA pins	-0.5 ~ 3.6	V

4. Block Diagram & Simplified Mechanical Drawing

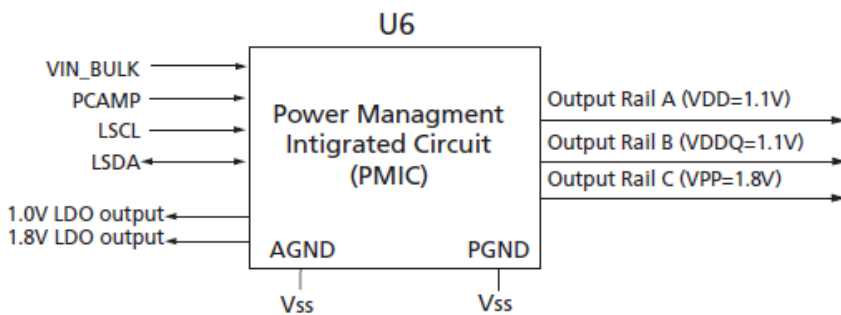
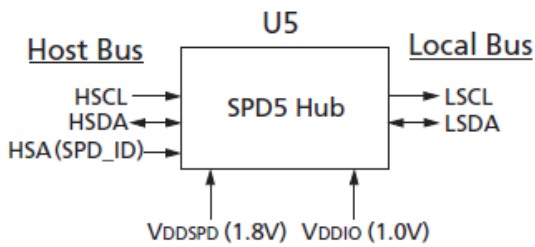
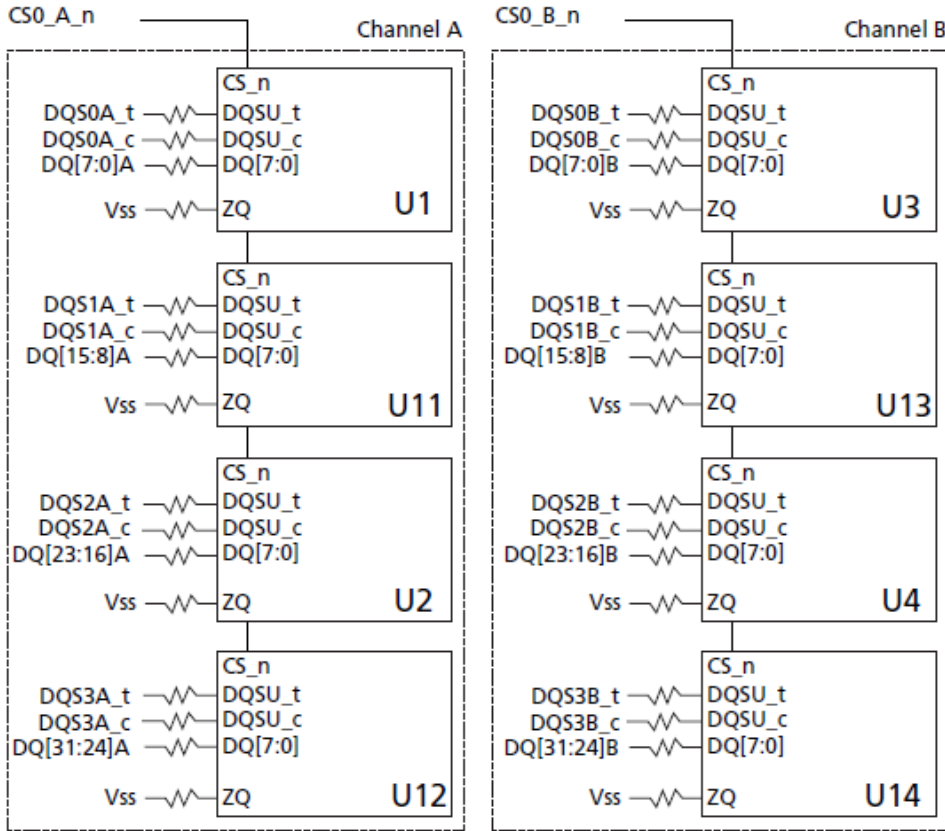
4.1 Block Diagram (x16 1 Rank without ECC)



Notes:

1. The ZQ ball on each DDR5 component is connected to an external $240\Omega \pm 1\%$ resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.
2. Functional block diagram is for reference only.

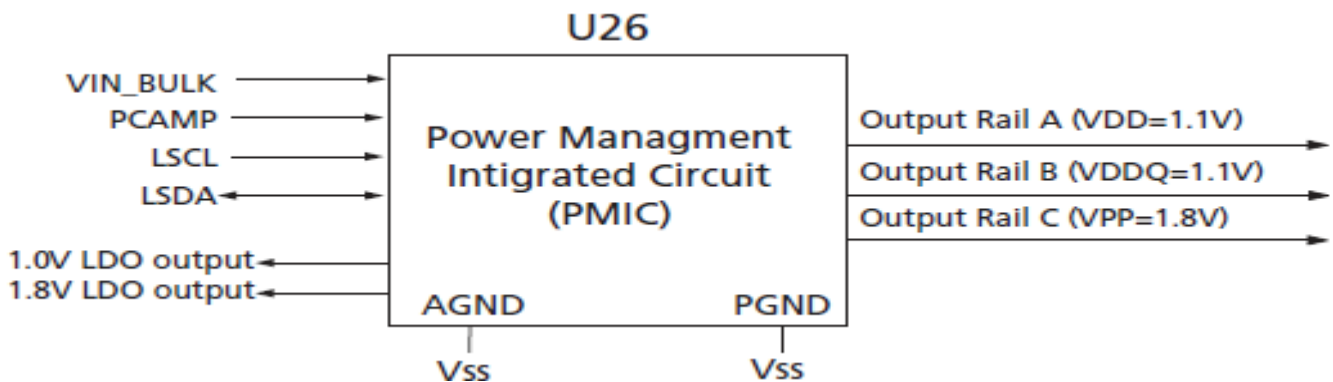
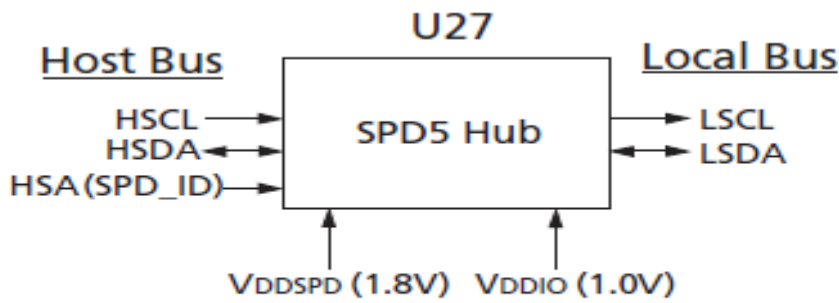
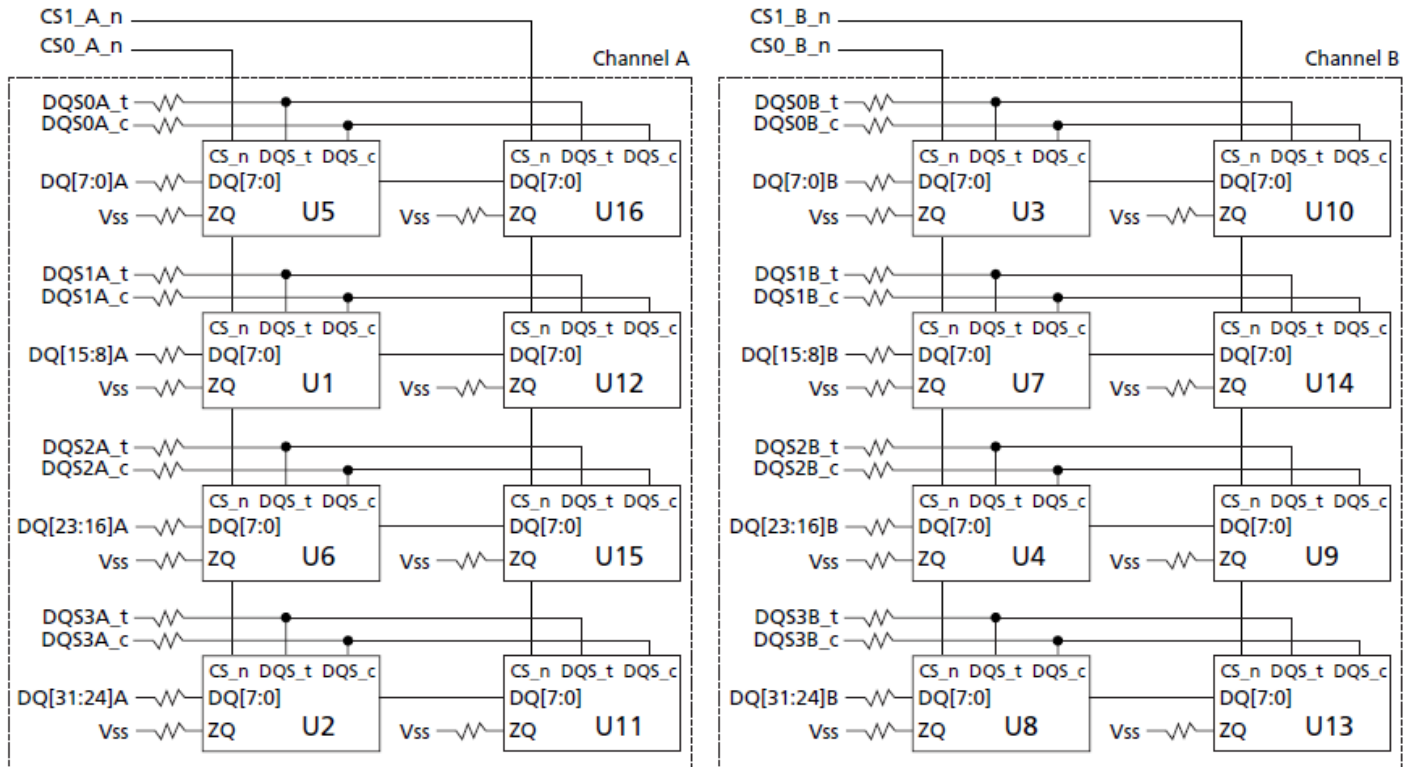
4.2 Block Diagram (x8 1 Rank without ECC)



Notes:

1. The ZQ ball on each DDR5 component is connected to an external 240Ω ±1% resistor that is tied to groVnd. It is used for the calibration of the component's ODT and output driver.
2. Functional block diagram is for reference only.

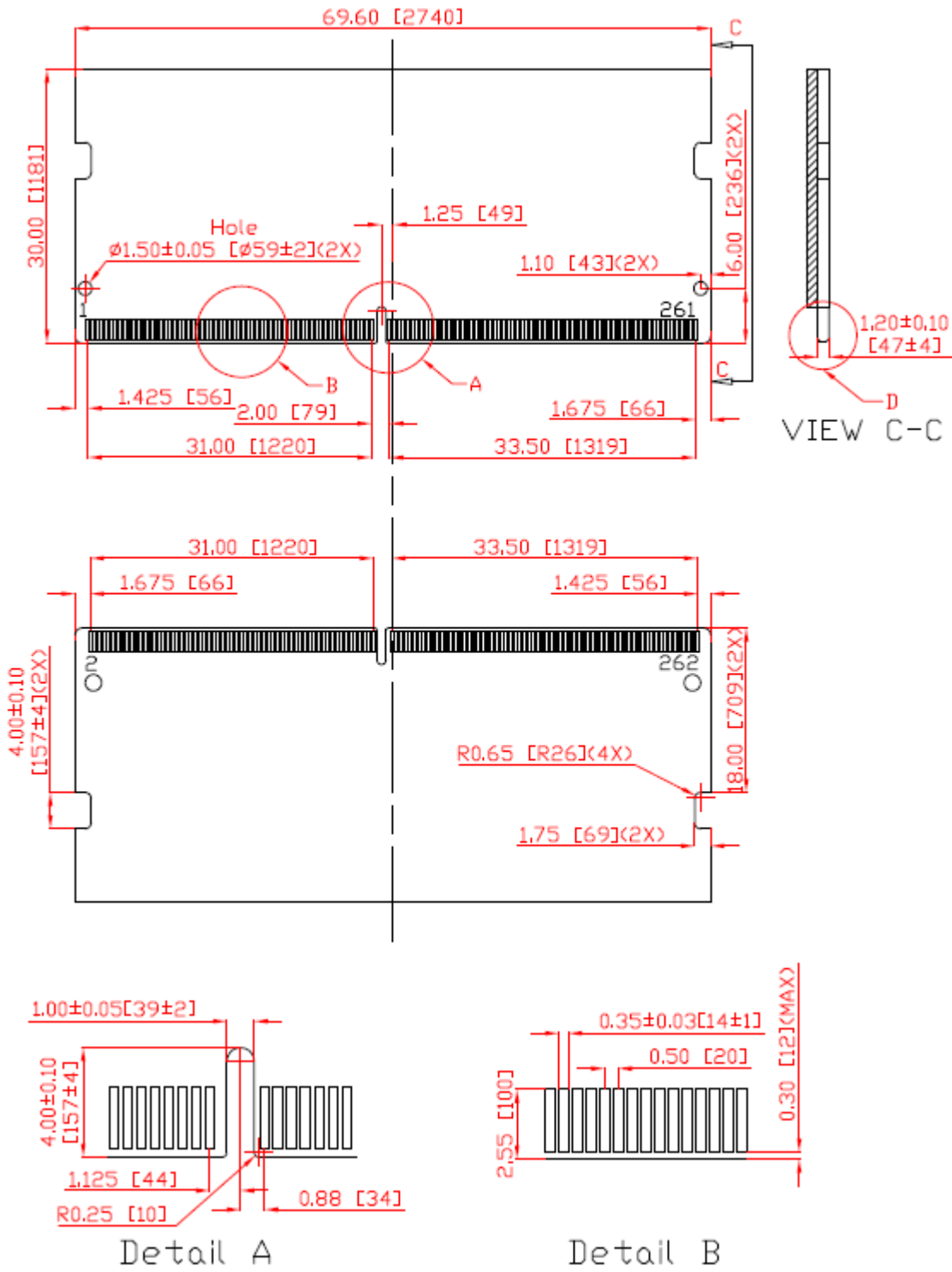
4.3 Block Diagram (x8 2 Ranks without ECC)



Notes: 1. The ZQ ball on each DDR5 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

2. Functional block diagram is for reference only.

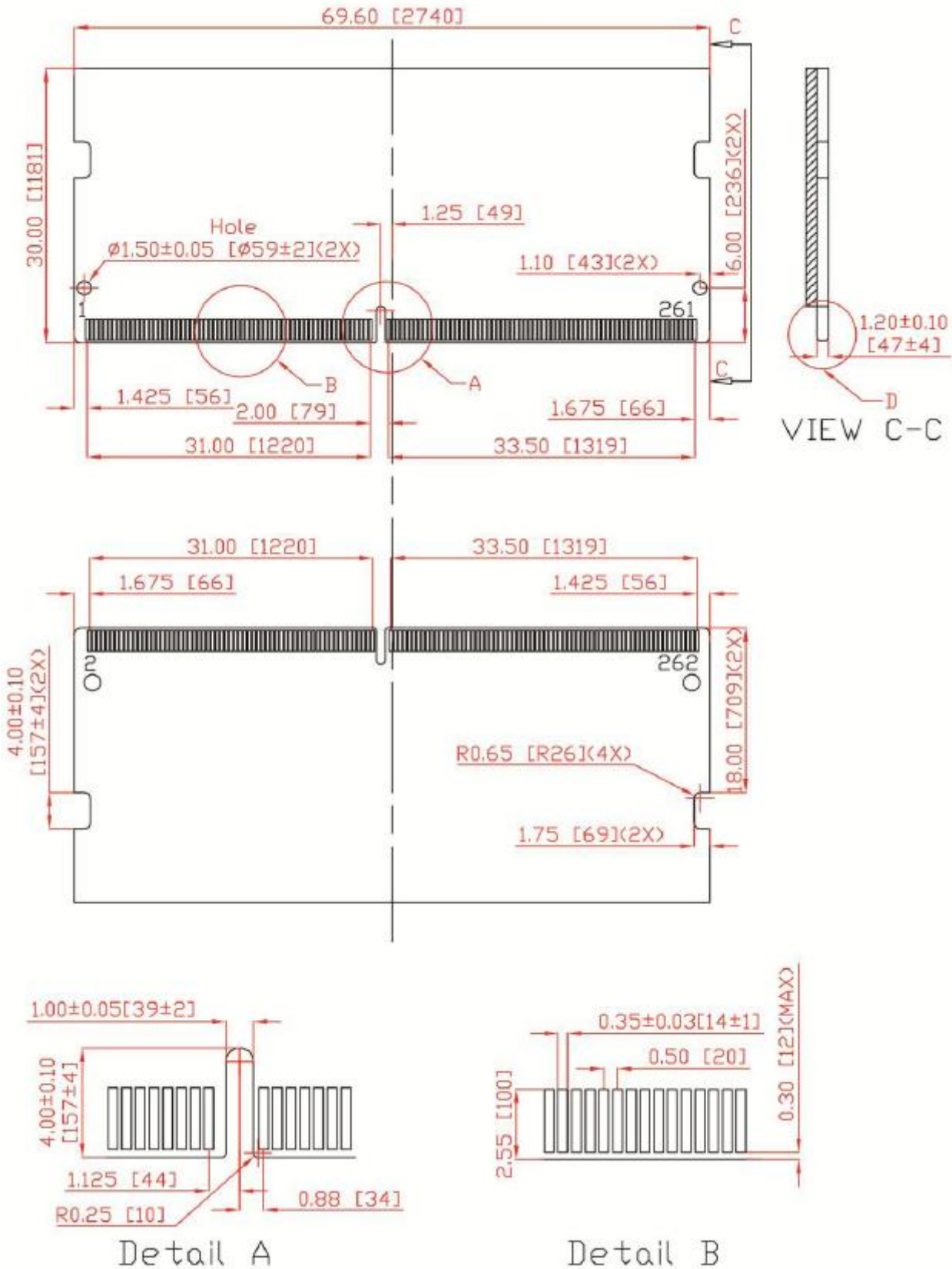
4.4 Simplified Mechanical Drawing (64bits SODIMM x16 1 Rank)



Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Notes: 2. The dimensional diagram is for reference only.

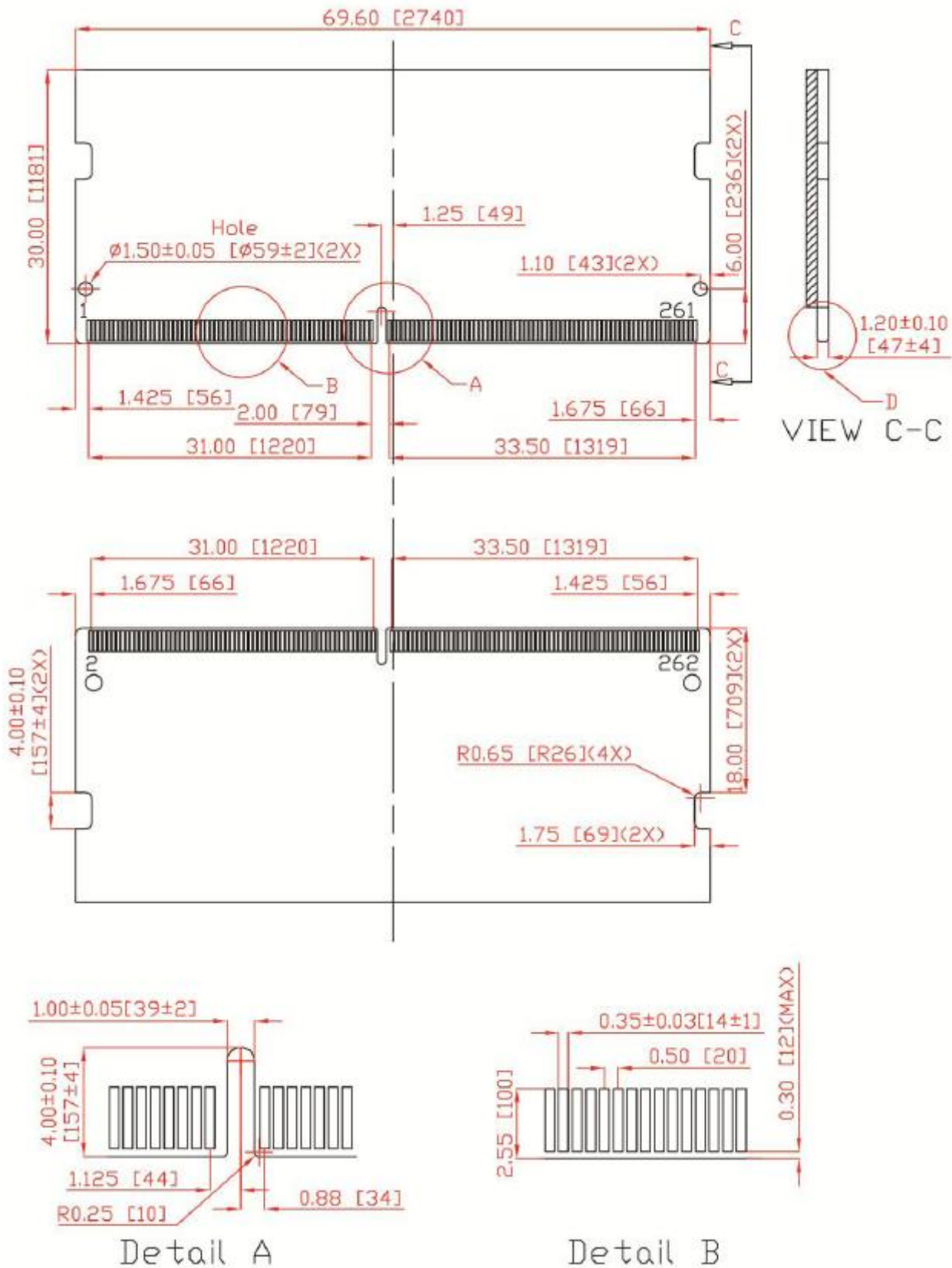
4.5 Simplified Mechanical Drawing (64bits SODIMM x8 1 Rank)



Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Notes: 2. The dimensional diagram is for reference only.

4.6 Simplified Mechanical Drawing (64bits SODIMM x8 2 Ranks)



5. Ordering Information

5.1 Part Number Definition

Table 6: Part Number Definition

Code	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	S	P	0	4	8	G	I	S	V	U	5	6	0	P	H	0
Code 1-2: Brand	SP: Silicon Power															
Code 3-6: Capacity	008G: 8GB; 016G: 16GB; 032G: 32GB; 048G: 48GB															
Code 7: Product	I: Industrial Product Line															
Code 8-9: Type & Form Factor	S: SODIMM; V: DDR5															
Code 10: Operation Temperature	U: Normal Temperature -20°C ~ 95°C V: Wide Temperature -40°C ~ 105°C															
Code 11-13: Model Series	480:4800; 560: 5600															
Code 14: Chip Specification	F: 2Gx8 G: 1Gx16 P: 3Gx8															
Code 15: Chip Brand	H: Hynix; N: Nanya; 2: CXMT; T: Spectek															
Code 16: Reserved	0: Standard															
Code 17-18 (Option)	For Customization															

5.2 Ordering Information Table

Capacity	Part Number	Module Density & Configuration	Bandwidth	Data Rate	Timing
Normal Temperature (-20°C ~ 95°C)					
8GB	SP008GISVU480GH0	8GB (1Gbx64) 1Gx16, 1Rank	38.4GB/s	DDR5-4800	40-39-39
	SP008GISVU560GH0	8GB (1Gbx64) 1Gx16, 1Rank	44.8GB/s	DDR5-5600	46-45-45
	SP008GISVU560GN0	8GB (1Gbx64) 1Gx16, 1Rank	44.8GB/s	DDR5-5600	46-45-45
	SP008GISVU560GT0	8GB (1Gbx64) 1Gx16, 1Rank	44.8GB/s	DDR5-5600	46-45-45
16GB	SP016GISVU480FH0	16GB (2Gbx64) 2Gx8, 1Rank	38.4GB/s	DDR5-4800	40-39-39
	SP016GISVU560FH0	16GB (2Gbx64) 2Gx8, 1Rank	44.8GB/s	DDR5-5600	46-45-45
	SP016GISVU560FT0	16GB (2Gbx64) 2Gx8, 1Rank	44.8GB/s	DDR5-5600	46-45-45

Capacity	Part Number	Module Density & Configuration	Bandwidth	Data Rate	Timing
	SP016GISVU560F20	16GB (2Gbx64) 2Gx8, 1Rank	44.8GB/s	DDR5-5600	46-45-45
32GB	SP032GISVU480FH0	32GB (4Gbx64) 2Gx8, 2Ranks	38.4GB/s	DDR5-4800	40-39-39
	SP032GISVU560FH0	32GB (4Gbx64) 2Gx8, 2Ranks	44.8GB/s	DDR5-5600	46-45-45
48GB	SP048GISVU560PH0	48GB (6Gbx64) 3Gx8, 2Ranks	44.8GB/s	DDR5-5600	46-45-45
Wide Temperature (-40°C ~ 105°C)					
8GB	SP008GISVV560GH0	8GB (1Gbx64) 1Gx16, 1Rank	44.8GB/s	DDR5-5600	46-45-45
	SP008GISVV560GN0	8GB (1Gbx64) 1Gx16, 1Rank	44.8GB/s	DDR5-5600	46-45-45
16GB	SP016GISVV480FH0	16GB (2Gbx64) 2Gx8, 1Rank	38.4GB/s	DDR5-4800	40-39-39
	SP016GISVV560FH0	16GB (2Gbx64) 2Gx8, 1Rank	44.8GB/s	DDR5-5600	46-45-45
32GB	SP032GISVV480FH0	32GB (4Gbx64) 2Gx8, 2Ranks	38.4GB/s	DDR5-4800	40-39-39
	SP032GISVV560FH0	32GB (4Gbx64) 2Gx8, 2Ranks	44.8GB/s	DDR5-5600	46-45-45
48GB	SP048GISVV560PH0	48GB (6Gbx64) 3Gx8, 2Ranks	44.8GB/s	DDR5-5600	46-45-45



5.3 Appendix

Table 7: Abbreviation

Item	Abbreviation	Description
1	MTBF	Mean Time Between Failures
2	ECC	Error Correction Code
3	TCG	Trusted Computing Group
4	AES	Advanced Encryption Standard
5	OP	Over Provisioning
6	PS	Power Shield
7	DC	Direct Current
8	DRAM	Dynamic Random Access Memory
9	WAF	Write Amplification Factor
10	WLE	Wear Leveling Efficiency
11	Ta	Ambient Temperature
12	LBA	Logical Block Address

Contact Information

Silicon Power Computer & Communications Incorporation, a solid state memory or storage business company, provides total solutions in the design and marketing of SSD, Flash Module, and Industry Card products. For further supporting or detail information related to the products, please inform us through the following contact email address: isupport@silicon-power.com. We will response the requests soon.