CY3280-BK1

# Universal CapSense® Controller Basic Kit 1 User Guide

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# Contents

# 1. Introduction

Thank you for your interest in the CY3280-BK1 Universal CapSense® Controller (UCC) Basic Kit 1. The kit contains CY3280-20x34 and CY3280-21x34 Universal CapSense Controller boards. These boards are designed for easy prototyping of CY8C20x34 and CY8C21x34 CapSense family designs with predefined control circuitry and plug-in hardware. The kit also includes programming hardware and I2C-to-USB bridge for tuning and data acquisition.

This guide provides details on the kit contents, installation procedures, hardware descriptions, schematics, and the bill of materials. The document also demonstrates how to use the code examples that accompany the kit. Visit www.cypress.com/go/CY3280-BK1 for the latest information about this kit.

## 1.1 Kit Contents

- Universal CapSense Controller boards
  - CY3280-20x34 UCC board
  - CY3280-21x34 UCC board
- Universal CapSense Controller board accessories
  - Universal CapSense modules
    - CY3280-SLM Universal CapSense Linear Slider Module
    - CY3280-BBM Universal CapSense Prototyping Module
    - 1.5 mm and 3 mm thick polycarbonate overlays with adhesive
  - CY3217-MiniProg1 programmer
    - Mini USB 2.0 retractable cable
  - CY3240-I2USB Bridge
- Chip Samples
  - CY8C20434-12LQXI
  - CY8C21434-24LQXI
- Software and documentation
  - CY3280-BK1 kit CD
    - PSoC Designer installation file
    - CY3280-BK1 specific code examples
    - CY3280-BK1 kit guide
    - CY3280-BK1 hardware design files
    - CY3280-BK1 quick start guide

## 1.2 Factory Default Configuration

When shipped, the CY3280-20x34 and CY3280-21x34 boards are preprogrammed to run the CapSense projects described in 5.1 My First CapSense (CY8C20x34) Project and 5.2 My First CapSense (CY8C21x34) Project, respectively.

## 1.3 Additional Learning Resources

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article "How to Design with PSoC® 1, PowerPSoC®, and PLC – KBA88292". Following is an abbreviated list for PSoC 1:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP
- In addition, PSoC Designer includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 1 are:
  - Getting Started with PSoC® 1 – AN75320
  - PSoC® 1 - Getting Started with GPIO – AN2094
  - PSoC® 1 Analog Structure and Configuration – AN74170
  - PSoC® 1 Switched Capacitor Analog Blocks – AN2041
  - Selecting Analog Ground and Reference – AN2219

**Note:** For application notes related to CY8C29X66 devices, click here.

- Development Kits:
  - CY3210-PSoCEval1 supports all PSoC 1 Mixed-Signal Array families, including automotive, except CY8C25/26xxx devices. The kit includes an LCD module, potentiometer, LEDs, and breadboarding space.
  - CY3214-PSoCEvalUSB features a development board for the CY8C24x94 PSoC device. Special features of the board include USB and CapSense development and debugging support.

**Note:** For development kits related to CY8C29X66 devices, click here.

The MiniProg1 and MiniProg3 devices provide interfaces for flash programming and debug.

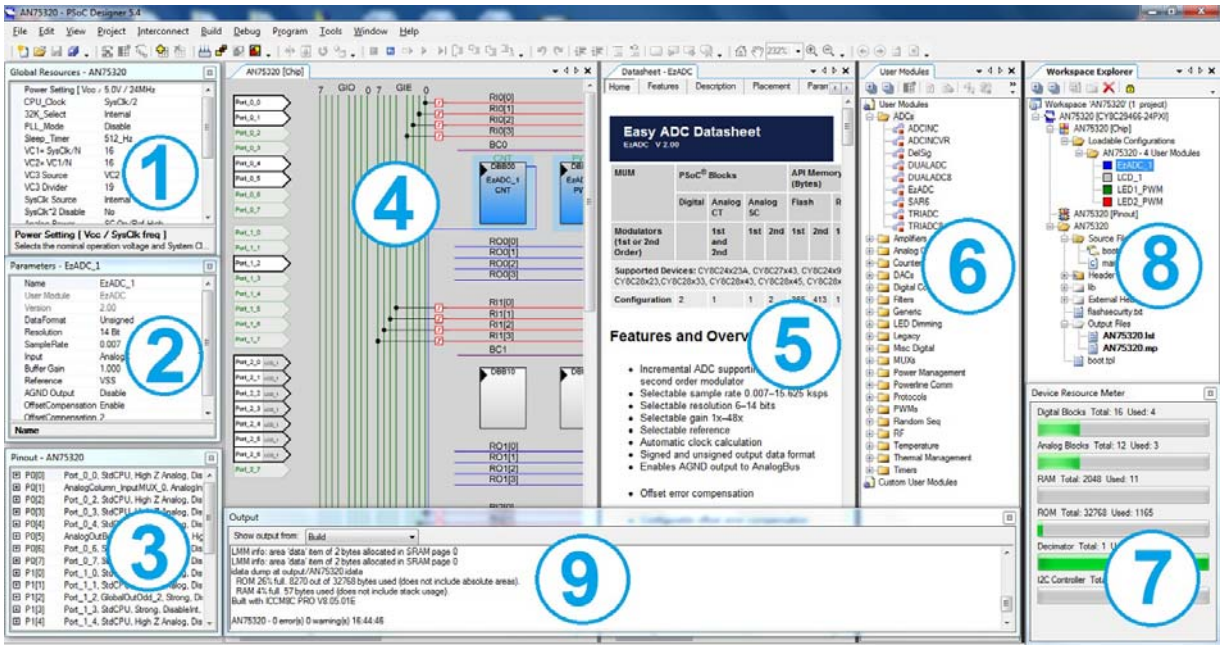
### 1.3.1 PSoC Designer

PSoC Designer is a free Windows-based Integrated Design Environment (IDE). Develop your applications using a library of pre-characterized analog and digital peripherals in a drag-and-drop design environment. Then, customize your design leveraging the dynamically generated API libraries of code. Figure 1-1 shows PSoC Designer windows. **Note:** This is not the default view.

1. **Global Resources –** all device hardware settings.
2. **Parameters –** the parameters of the currently selected User Modules.
3. **Pinout –** information related to device pins.
4. **Chip-Level Editor –** a diagram of the resources available on the selected chip.
5. **Datasheet –** the datasheet for the currently selected UM
6. **User Modules –** all available User Modules for the selected device.
7. **Device Resource Meter –** device resource usage for the current project configuration.
8. **Workspace –** a tree level diagram of files associated with the project.
9. **Output –** output from project build and debug operations.

**Note:** For detailed information on PSoC Designer, go to PSoC® Designer > Help > Documentation > Designer Specific Documents > IDE User Guide.

Figure 1-1. PSoC Designer Layout



### 1.3.2 Code Examples

The following webpage lists the PSoC Designer based Code Examples. These Code Examples can speed up your design process by starting you off with a complete design, instead of a blank page and also show how PSoC Designer User modules can be used for various applications.

http://www.cypress.com/go/CapSenseCodeExamples

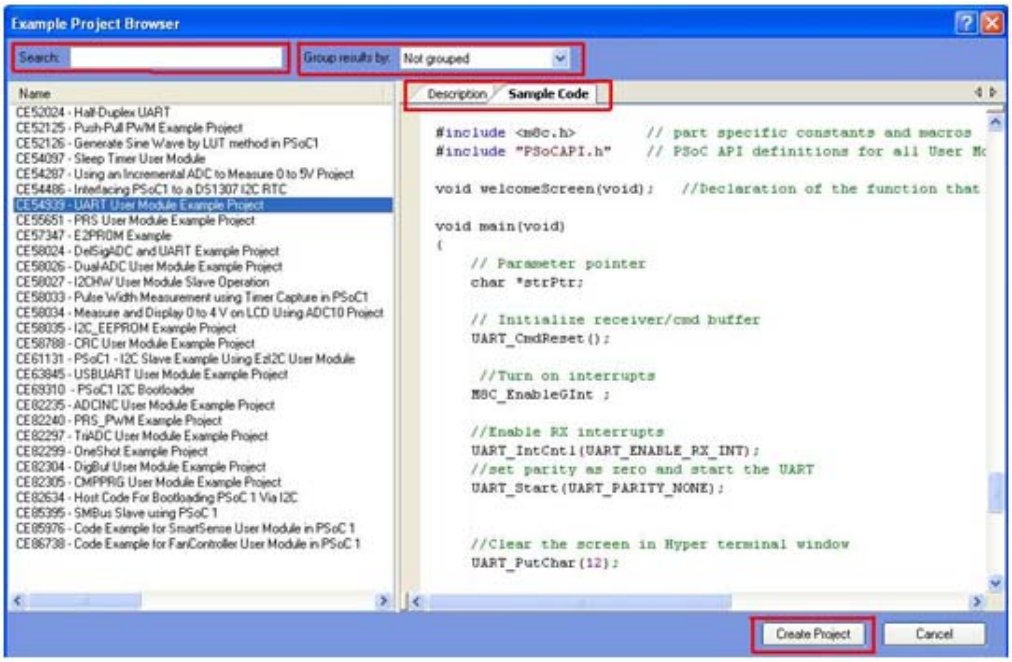
To access the Code Examples integrated with PSoC Designer, follow the path **Start Page** > **Design Catalog** > **Launch Example Browser** as shown in Figure 1-2.

Figure 1-2. Code Examples in PSoC Designer

In the Example Projects Browser shown in Figure 1-3, you have the following options.

- Keyword search to filter the projects.
- Listing the projects based on Category.
- Review the datasheet for the selection (on the Description tab).
- Review the code example for the selection. You can copy and paste code from this window to your project, which can help speed up code development, or
- Create a new project (and a new workspace if needed) based on the selection. This can speed up your design process by starting you off with a complete, basic design. You can then adapt that design to your application.

Figure 1-3. Code Example Projects, with Sample Codes



### 1.3.3 PSoC Designer Help

Visit the PSoC Designer home page to download the latest version of PSoC Designer. Then, launch PSoC Designer and navigate to the following items:

- **IDE User Guide:** Choose **Help** > **Documentation** > **Designer Specific Documents** > **IDE User Guide.pdf**. This guide gives you the basics for developing PSoC Creator projects.
- **Simple User module Code Examples:** Choose **Start Page** > **Design Catalog** > **Launch Example Browser**. These code examples demonstrate how to configure and use PSoC Designer User modules.
- **Technical Reference Manual:** Choose **Help** > **Documentation** > **Technical Reference Manuals**. This guide lists and describes the system functions of PSoC devices.
- **User module datasheets:** Right-click a User module and select “Datasheet.” This datasheet explains the parameters and APIs of the selected user module.
- **Device Datasheet:** Choose **Help** > **Documentation** > **Device Datasheets** to pick the datasheet of a particular PSoC device.
- **Imagecraft Compiler Guide:** Choose **Help** > **Documentation** > **Compiler and Programming Documents** > **C Language Compiler User Guide.pdf**. This guide provides the details about the Imagecraft compiler specific directives and Functions.

### 1.3.4 Technical Support

If you have any questions, our technical support team is happy to assist you. You can create a support request on the Cypress Technical Support page.

If you are in the United States, you can talk to our technical support team by calling our toll-free number: +1-800-541-4736. Select option 8 at the prompt.

You can also use the following support resources if you need quick assistance.

- Self-help
- Local Sales Office Locations

## 1.4 Acronyms

Table 1-1. Acronyms Used in this Document

| Acronym | Definition | Acronym | Definition |
|---|---|---|---|
| ADC | analog-to-digital converter | LSB | least significant bit |
| AEC | Automotive Electronic Council | MSB | most significant bit |
| BBM | bread board module | PCB | printed circuit board |
| BK1 | basic kit 1 | PRS | pseudo-random sequence |
| CSA_EMC | CapSense successive approximation electromagnetic compatible | PSoC | Programmable System-on-Chip |
| CSD | CapSense Sigma Delta | PWD | pulse width discriminator |
| DC | direct current | PWM | pulse width modulator |
| EEPROM | electronically erasable programmable read-only memory | QFN | quad flat no leads |
| GPIO | general purpose input/output | SLM | slider module |
| I2C | inter-integrated circuit | SOIC | small-outline integrated circuit |
| ICE | in-circuit emulator | SPI | serial peripheral interface |
| IDE | integrated design environment | SSOP | shrunk small outline package |
| IRDA | Infrared Data Association | UART | universal asynchronous receiver / transmitter |
| ISSP | In-system serial programmer | USB | universal serial bus |
| LED | light emitting diode | | |

## 1.5 Documentation Conventions

Table 1-2. Document Conventions for Guides

| Convention | Usage |
|---|---|
| `Courier New` | Displays file locations, user entered text, and source code:<br>`C:\ ...cd\icc\` |
| *Italics* | Displays file names and reference documentation:<br>Read about the *sourcefile.hex* file in the *PSoC Designer User Guide*. |
| [**Bracketed, Bold**] | Displays keyboard commands in procedures:<br>[**Enter**] or [**Ctrl**] [**C**] |
| File > Open | Represents menu paths:<br>File > Open > New Project |
| **Bold** | Displays commands, menu paths, and icon names in procedures:<br>Click the **File** icon and then click **Open**. |
| Times New Roman | Displays an equation:<br>2 + 2 = 4 |
| Text in gray boxes | Describes cautions or unique functionality of the product. |

# 2. Getting Started

This chapter describes how to install and configure the CY3280-BK1 Universal CapSense Controller kit.

## 2.1 Kit Installation

To install the kit software, follow these steps:

1. Insert the kit DVD into the DVD drive of your PC. The DVD is designed to auto-run and the kit installer startup screen appears.

   **Note** You can also download the latest installer from www.cypress.com/go/CY3280-BK1. Three types of installers are available for download:

   a. CY3280-BK1 ISO (Create DVD): This file (ISO image) is an archive of the optical disc provided with the kit. You can use it to create an installer DVD or extract information using WinRar or similar tools.

   b. CY3280-BK1 Kit Setup: This executable file installs the DVD contents, which includes PSoC Programmer, PSoC Designer, code examples, kit hardware files, and user documents.

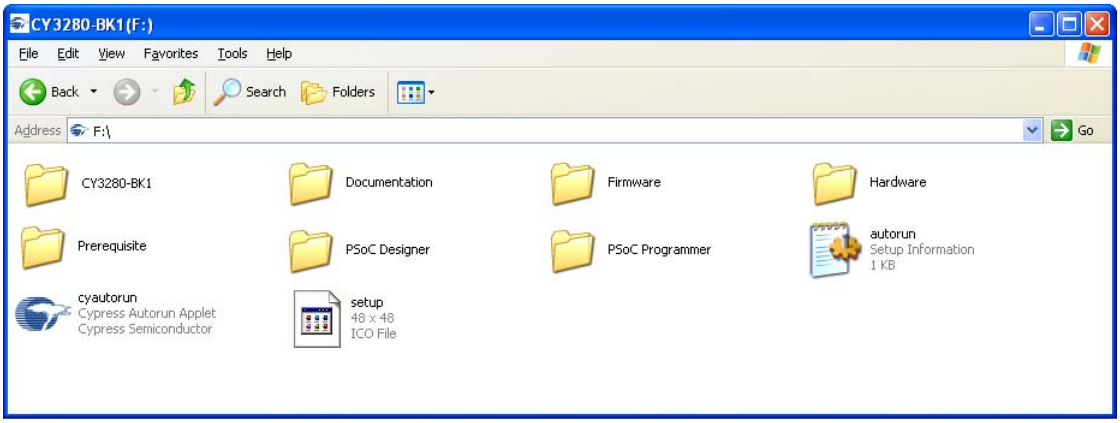
   c. CY3280-BK1 Kit Only (without prerequisites): This executable file installs only the kit contents, which includes kit code examples, hardware files, and user documents.

2. Click **Install CY3280-BK1** to start the installation, as shown in Figure 2-1.

Figure 2-1. Kit Installer Startup Screen

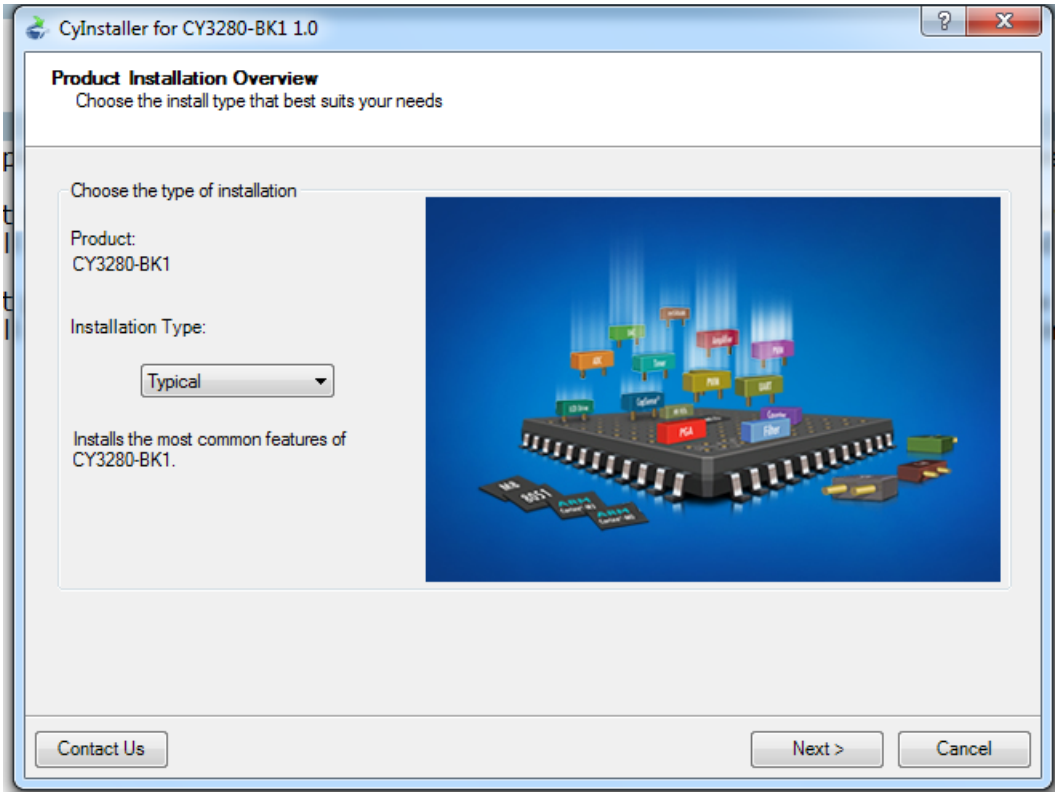
**Note** If auto-run does not execute, double-click the *cyautorun.exe* file on the root directory of the DVD, as shown in Figure 2-2.

Figure 2-2. Root Directory of DVD



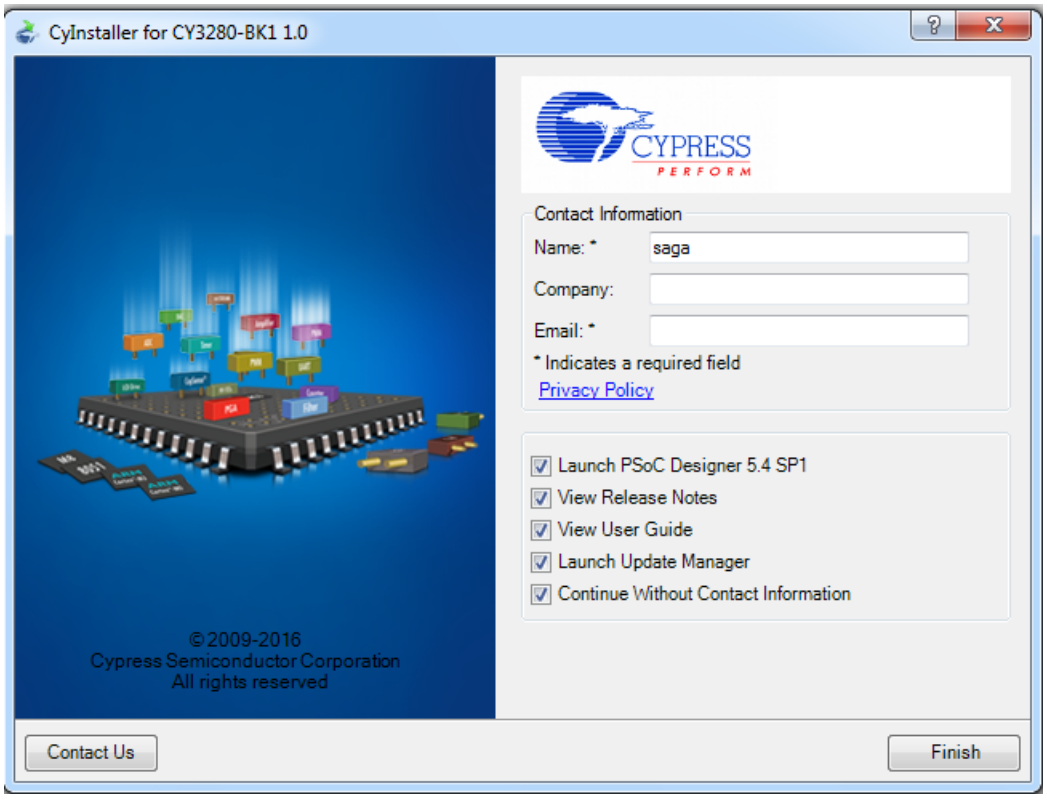

3. The InstallShield Wizard screen appears. On this screen, choose the folder location to install the setup files. You can change the location for the setup files using **Change**.
4. On the Product Installation Overview screen, select the installation type that best suits your requirement. The drop-down menu has three options - **Typical**, **Custom**, and **Complete**, as shown in Figure 2-3.
5. Click **Next** to start the installation.

Figure 2-3. Installation Type Options



6. When the installation begins, a list of packages appears on the Installation Page. A green check mark appears adjacent to every package that is downloaded and installed.
7. Wait until all the packages are downloaded and installed successfully.
8. Click **Finish** to complete the installation, as shown in Figure 2-4.

Figure 2-4. Installation Complete



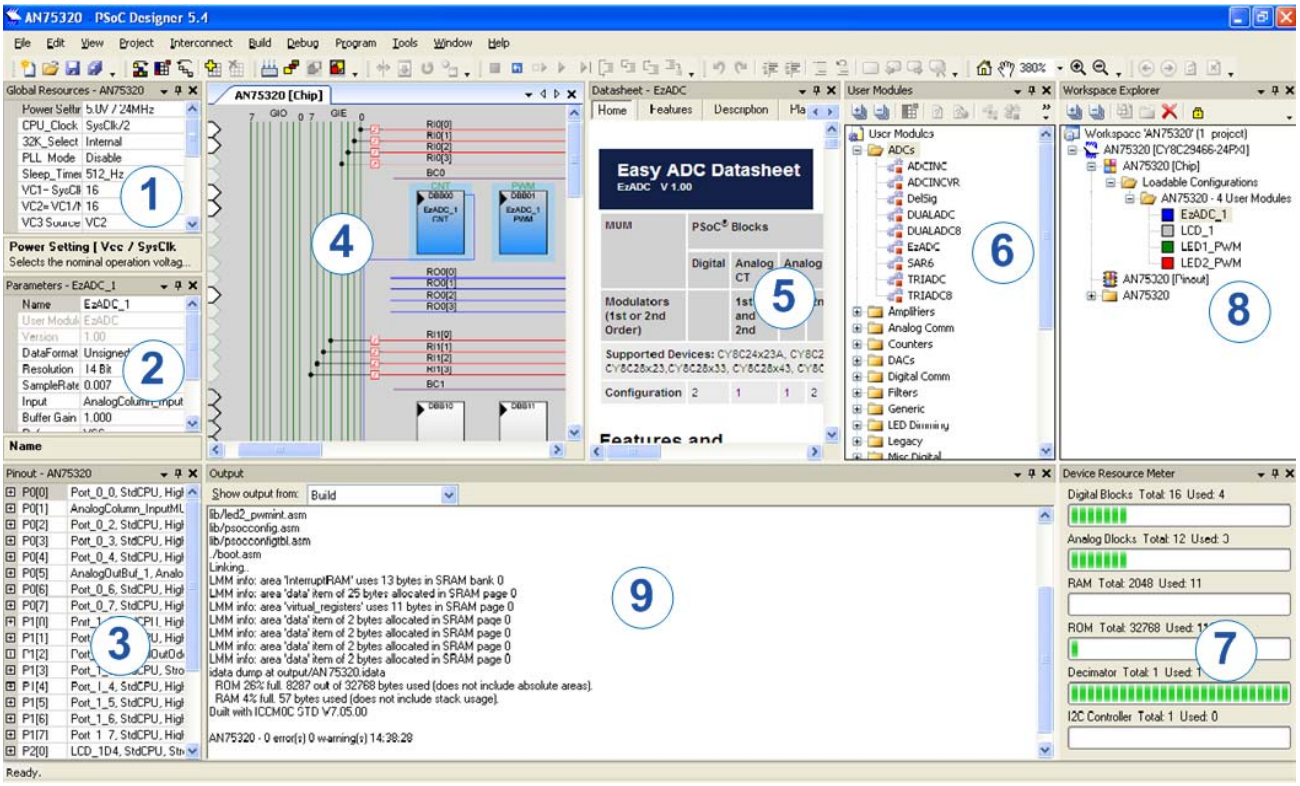

**Note** Advanced users can go to Code Examples chapter on page 41.

## 2.2 PSoC Designer

PSoC Designer 5.4 SP1 is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. You can develop applications using a library of pre-characterized analog and digital peripherals in a drag-and-drop design environment. Then customize your design, leveraging the dynamically generated API libraries of code. Finally, debug and test your designs with the integrated debug environment including in-circuit emulation and standard software debug features.

1. To open the application, click **Start > All Programs > Cypress > PSoC Designer <version> > PSoC Designer <version>**.
2. Click **File > New Project**, to create a new project; click **File > Open Project** to work with an existing project.

Figure 2-5. PSoC Designer Interconnect View




3. To experiment with the code examples, go to Code Examples chapter on page 41.

**Note** For more details on PSoC Designer, see the PSoC Designer IDE Guide located at: `<Install_Directory>\PSoC Designer\<version>\Documentation`

The default `<Install directory>` on Windows 32-bit platforms is `C:\Program Files\Cypress` and on Windows 64-bit platforms is `C:\Program Files(x86)\Cypress`.

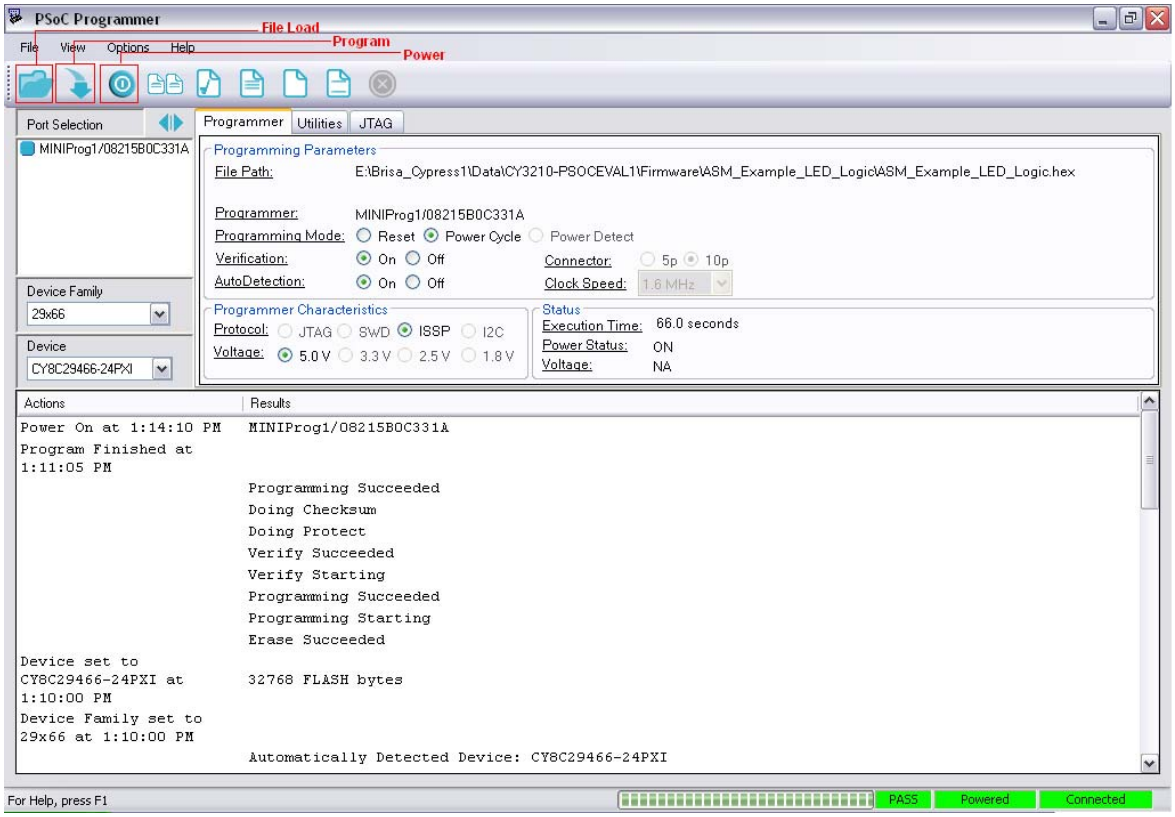
See Additional Learning Resources on page 6 for links to PSoC Designer training. The PSoC Designer quick start guide is available at: www.cypress.com/?rID=47954.

## 2.3 PSoC Programmer

PSoC Programmer is a stand-alone utility for programming PSoC devices.

1. Click **Start > All Programs > Cypress > PSoC Programmer <version> > PSoC Programmer <version>**.
2. Select the MiniProg from **Port Selection**, as shown in Figure 2-6.

Figure 2-6. PSoC Programmer Window




3. Click **File Load** to load the hex file.
4. Use the **Program** button to program the hex file onto the chip.
5. When programming is successful, “Programming Succeeded” appears in the Actions pane.
6. Close PSoC Programmer.

**Note** For more details on PSoC Programmer, see the user guide at the following location: `<Install_Directory>:\Program Files\Programmer\<version>\Documents.`

The default `<Install directory>` on Windows 32-bit platforms is `C:\Program Files\Cypress` and on Windows 64-bit platforms is `C:\Program Files(x86)\Cypress`.

## 2.4 Bridge Control Panel Overview

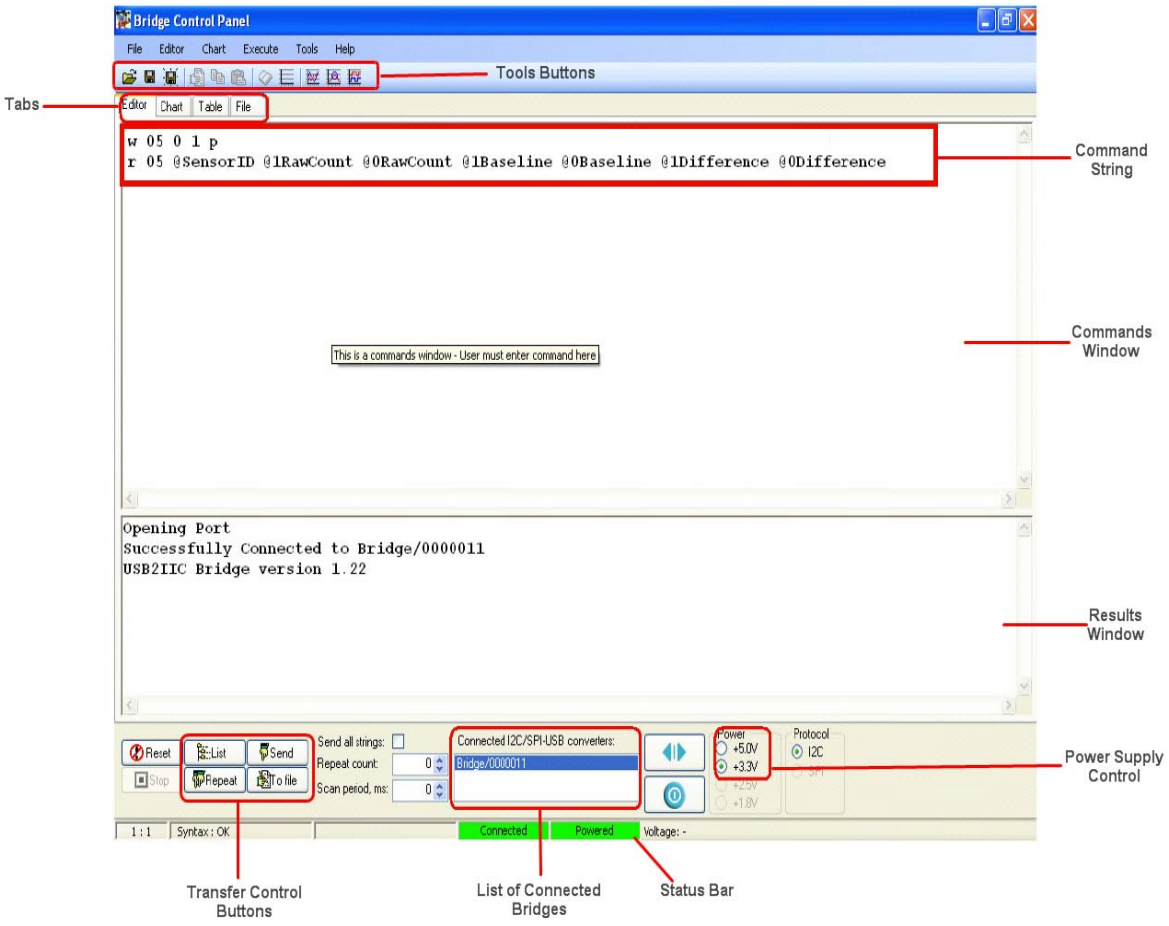
The Bridge Control Panel is used with CY3240-I2USB Bridge to enable communication with I2C slave devices. This program is used to configure I2C devices as well as acquire and process data received from I2C slave devices. The Bridge Control Panel helps to optimize, debug, and calibrate the target applications.

The main features of the application are as follows:

- Controls power supply of connected devices
- Supports I2C protocol
- Searches and displays a list of devices connected to the bridge
- Supports high-speed data reading from slave device (ToFile mode of bridge)
- Configures the bridge to work at 50 k, 100 k, and 400 k CLK speed on I2C bus
- For SPI protocol support: selects shift direction type (MSB first, LSB first), selects mode (00 and 01) frequency
- Provides a simple format to input and output data for communication. The input data can be interpreted as variables of varying length
- Includes different variables settings such as type, scaling, and offset
- Supports a variety of data presentation and storage through charts, tables, and other formats
- Saves and loads variable configurations for use with different I2C slaves
- Saves and loads commands line files
- Supports I2C boot loader file format

To open the application, click **Start > All Programs > Cypress > Bridge Control Panel 1.2 > Bridge Control Panel 1.2**.

Figure 2-7. Bridge Control Panel




For more details on the Bridge Control Panel, see application note AN2352 - Communication - I2C USB Bridge Usage or access the help topics in the Bridge Control Panel menu bar.

# 3. Kit Operation

The CY3280-BK1 Universal CapSense Controller kit is designed for easy prototyping of CapSense designs with predefined control circuitry and plug-in hardware. The kit comes with controller boards for the CY8C20x34 and CY8C21x34 PSoC devices as well as a breadboard module and a button/slider module.

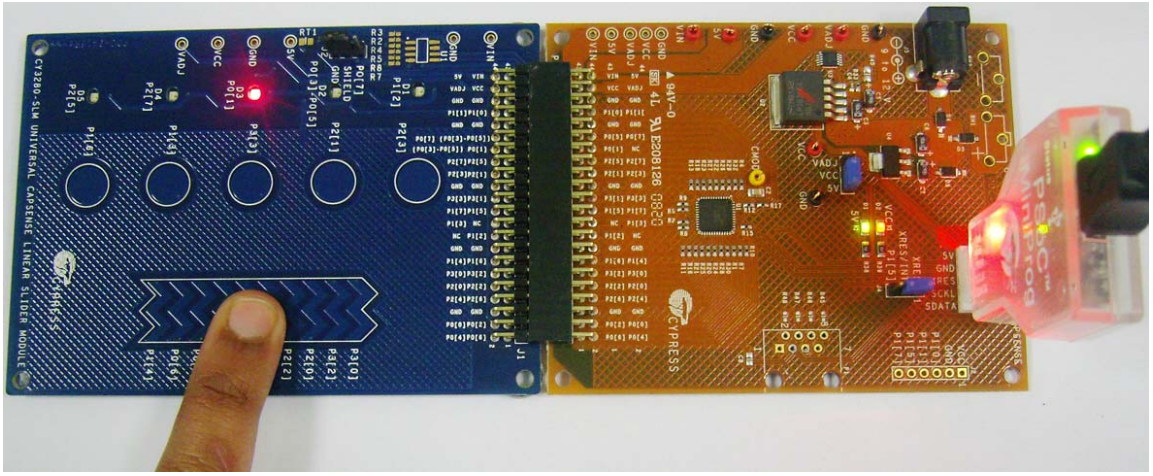
## 3.1 Evaluating the CY3280-20x34 CapSense Controller

To evaluate the default project programmed on CY3280-20x34 UCC, follow these steps.

1. Connect the CY3280-SLM board to the CY3280-20x34 UCC board's P2 connector.
2. In the CY3280-20x34 boards, place the jumper on header J1 to short pins 2 and 3.
3. In the CY3280-SLM board, place the jumper on header J2 to short pins 2 and 3.
4. Connect MiniProg1 to the CY3280-20x34 UCC board's ISSP connector (J3); connect it to your PC using a USB cable.
5. Open PSoC Programmer.
6. Click **Connect**; connect MiniProg1 to the PC.
7. Click the **Toggle** button to power the board.
8. Touch and move the linear slider on the CY3280-SLM module board. The corresponding LEDs on the CY3280-SLM board light up.
9. Touch a button. The corresponding LED on the CY3280-SLM module board lights up.

   You can touch multiple buttons simultaneously; the linear slider and buttons can also be used at the same time.

Figure 3-1. LED Glows on Slider Touch

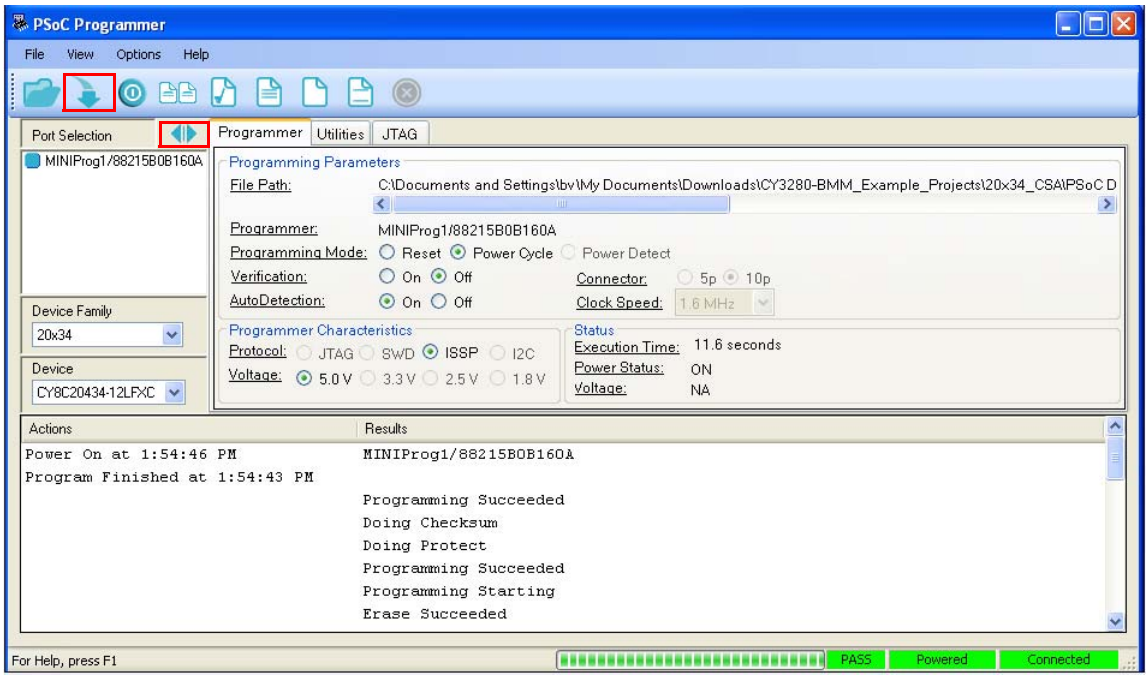


If the default project programmed on CY3280-20x34 UCC is erased, follow these steps.

1. Open PSoC Programmer.
2. Click **Connect**; connect MiniProg1 to the PC.
3. Browse and load the *CY3280_20x34_SLM.hex* file.

   **Note** The hex file is located at: `<Install_Directory>:\Cypress\CY3280-BK1 \<version>\Firmware\CY3280_20x34_SLM`
4. Click the **Program** button to program the device.

Figure 3-2. Program the Device



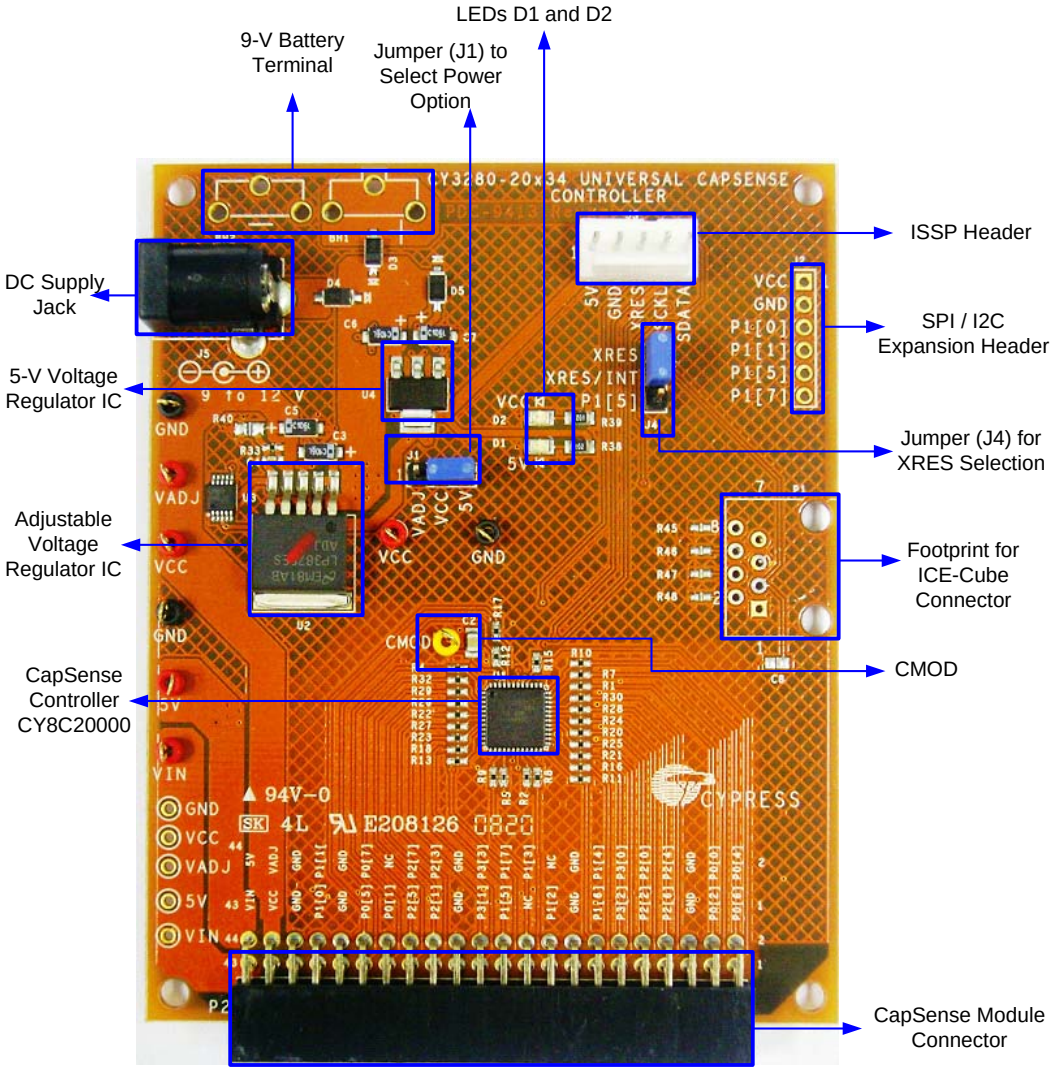

Similar steps can be followed to evaluate the CY3280-21x34 CapSense controller.

# 4. Hardware

## 4.1 CY3280-20x34 Universal CapSense Controller Board

The CY3280-20x34 Universal CapSense Controller Kit is designed to prototype rapidly and develop CapSense-based solutions around the CY8C20x34 family of CapSense controllers. The following figure highlights important board components and connectors.

Figure 4-1. CY3280-20x34 Universal CapSense Controller Kit - Top View



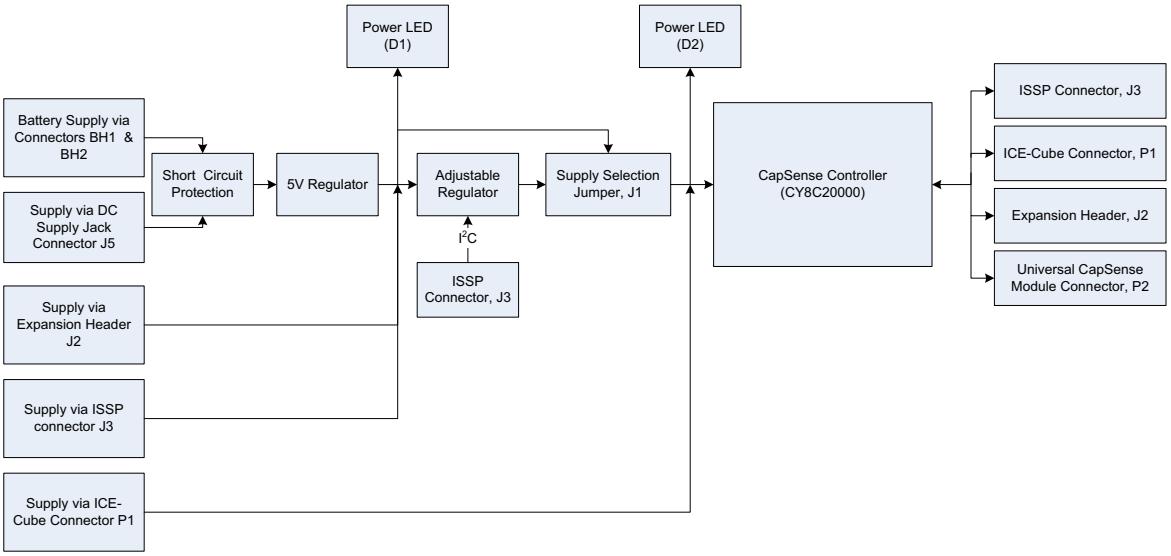
### 4.1.1 System Block Diagram

Figure 4-2 shows the block diagram of the CY3280-20x34 Universal CapSense Controller Kit.

The kit can be powered from five different sources; to select a source, place the jumper on power select header J1. Power supply from the battery connector and the DC socket is short-circuit protected to avoid mishap due to accidental short between these sources. The 5-V regulator output, supply from expansion header, and supply from ISSP connector are shorted. Supply from the ICE-Cube connector is fed directly to the CapSense controller. An I2C controlled variable power supply is also part of this kit.

Any Universal CapSense Module board can be connected to the kit via the Universal CapSense Module connector P2. SPI and auxiliary I2C pins from the CapSense controller are routed to the expansion header, J2. Connector P1 is used to interface ICE-Cube, the emulator needed for in-circuit debugging of CapSense projects. The CapSense controller is programmed through the ISSP connector J3 using MiniProg1.

Figure 4-2. System Block Diagram of CY3280-20x34 Universal CapSense Controller Board



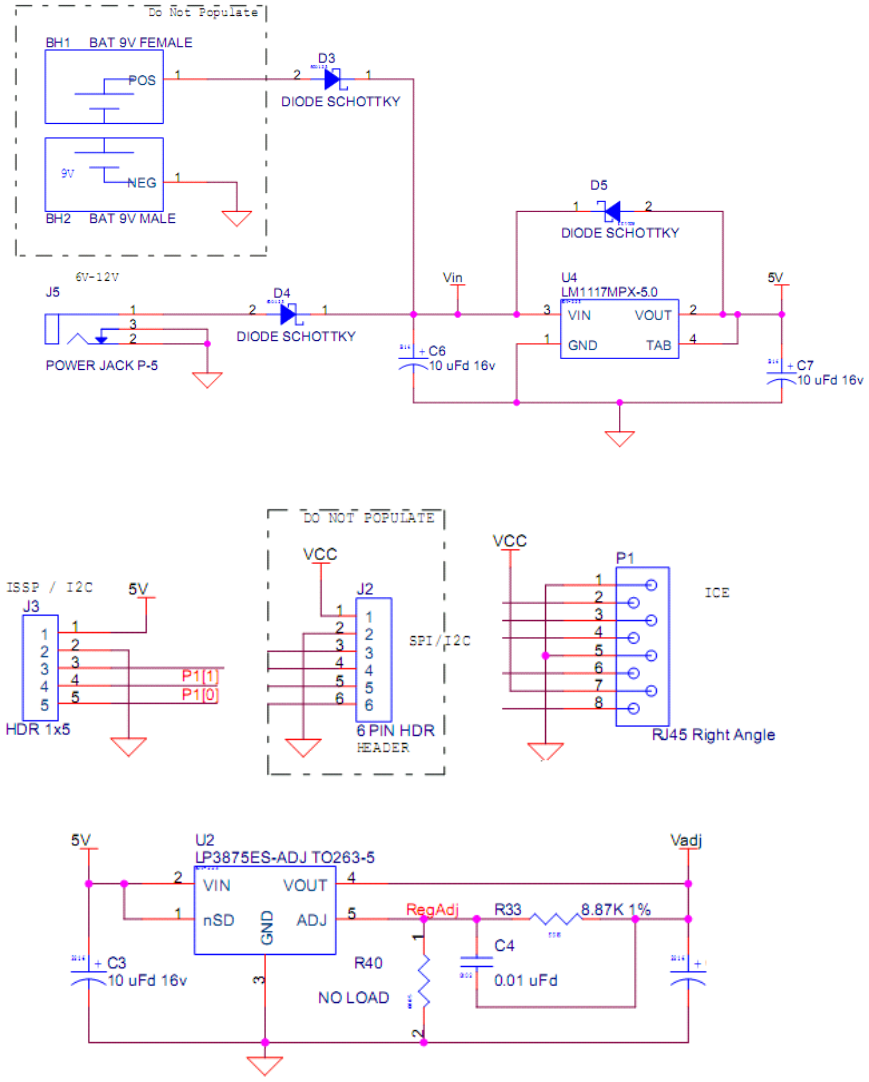
## 4.1.2 Power Sources

### *4.1.2.1 Power Supply Nets*

The board has several power nets. Following are the definitions of the different power nets.

- VIN (9 V or 12 V): This is the input power before it is fed into any of the regulators. A 9-V to 12-V power supply adapter or a 9-V battery is used as the source.
- 5 V: This is fed by the 5-V regulator output, pin#1 of J2 or pin#1 of J3.
- VADJ/Vadj: This is fed by 5 V and is the output of the onboard adjustable regulator.
- VCC: This is the power from either 5 V or VADJ. The source of VCC can be chosen using the J1 header. It is used to power the CapSense controller.

Figure 4-3. Power Supply System Schematic



## 4.1.3 Power Supply Configuration Examples

### *4.1.3.1 Power CapSense Controller at +5 V from Onboard Regulator*

1. Connect a 9-V to 12-V power supply adapter to the DC power socket J5 or connect a 9-V alkaline battery to the battery terminals. (Battery terminals on BH1 and BH2 are not mounted in the kit.)
2. Place the jumper on header J1 to select 5 V as VCC.

### *4.1.3.2 Power CapSense Controller from Onboard Adjustable Regulator*

1. Connect a 9-V to 12-V power supply adapter to the DC power socket J5 or connect a 9-V alkaline battery to the battery terminals. (Battery terminals should be soldered on footprints BH1 and BH2.) You can also apply source at pin#1 of J2 or pin#1 of J3.
2. Place the jumper on header J1 to select VADJ as VCC.

### *4.1.3.3 Power CapSense Controller Directly from ISSP Header*

1. Insert the MiniProg1 or I2USB Bridge to the ISSP header J3. Power the connected device.
2. Place the jumper on header J1 to select 5 V as VCC.

### *4.1.3.4 Power CapSense Controller from ICE-Cube*

Connect the RJ-45 socket from ICE-Cube to connector P1. There are no specific requirements for placing jumper on header J1.

## 4.1.4 Hardware Description

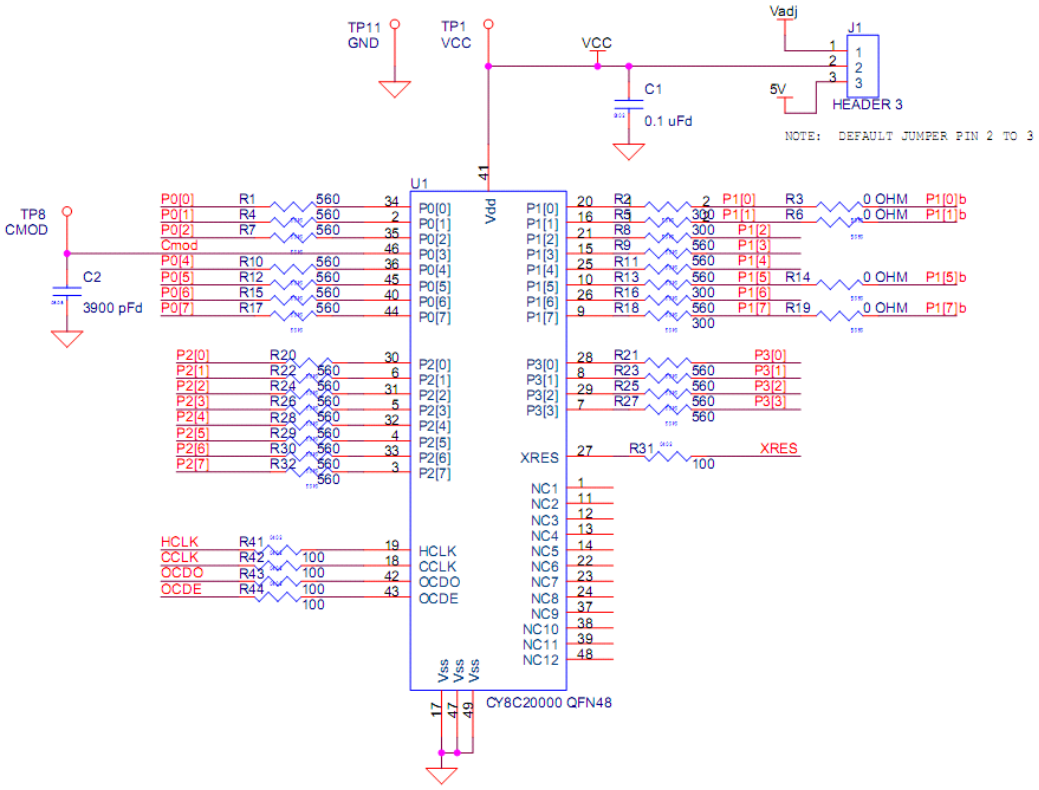
### *4.1.4.1 CapSense Controller (CY8C20x34)*

CY8C20000 48-QFN is the onboard CapSense controller. CY8C20000 supports programming and in-circuit debugging of PSoC Designer projects targeted for the CY8C20x34 family of devices.

Cypress's CY8C20x34 is a low-power, high-performance, programmable touch-sensing controller family that has the following features:

- CapSense Successive Approximation Electromagnetic Compatible (CSA_EMC) capacitive sensing technology
- Supports up to 25 capacitive buttons and 6 sliders
- Proximity sensing up to 2 cm (with onboard PCB trace)
- 2.4 V to 5.25 V operating voltage
- Up to 28 GPIOs
- Communication interfaces:
  - I2C slave with 50 kHz, 100 kHz, or 400 kHz selectable speed
  - SPI master/slave 46.9 kHz to 3 MHz selectable speed
- EEPROM emulation
- 8 KB flash and 512 B RAM
- Variety of packages: 16-QFN, 24-QFN, 32-QFN, 48-QFN, 8-SOIC, 16-SOIC, 28-SSOP, 30-Ball WLCSP
- Watchdog and sleep timers

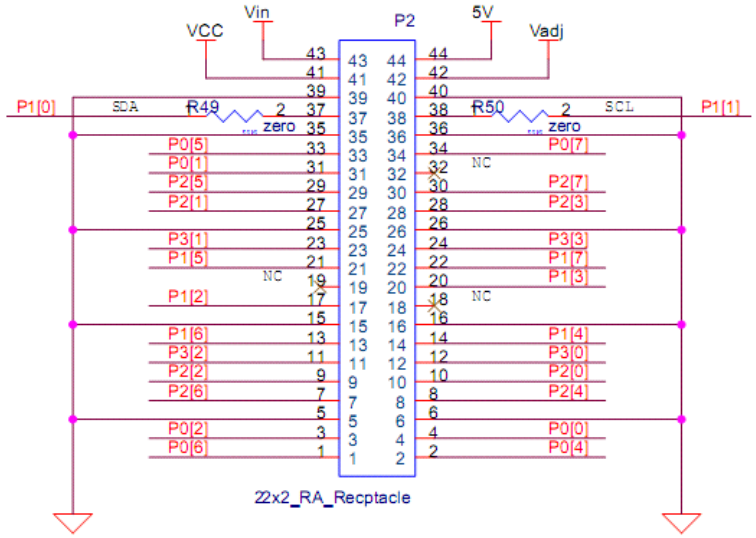
Figure 4-4. CapSense Controller CY8C20000 Schematic




### 4.1.4.2 *Universal CapSense Module Connector*

The CY3280-20x34 has an expansion port, P2, designed to connect the UCC module boards. The controller board can be used with any of the Universal CapSense module boards. The boards can be interfaced to the CY3280-20x34 via the 44-pin connector, P2. The pin mapping for the port P2 is shown in the following figure.

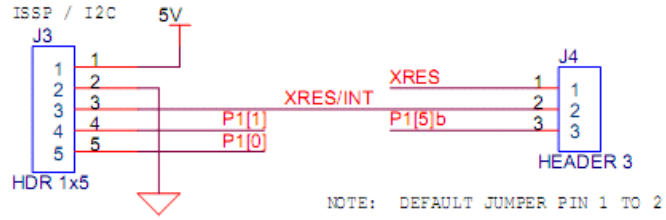
Figure 4-5. Universal CapSense Module Connector Schematic



### 4.1.4.3 ISSP

In-system serial programmer (ISSP) is used to program the device using MiniProg1. Plug in the MiniProg device to the ISSP header J3. The ISSP connector is also used to connect the I2USB bridge to communicate between the PC and controller board. The pin mapping for the ISSP connector is shown in the following figure.

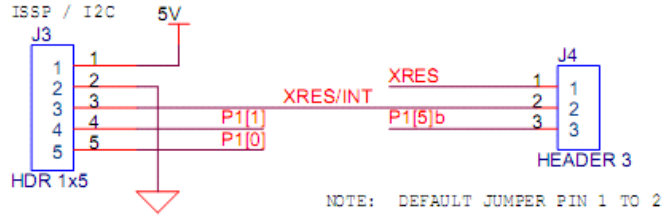
Figure 4-6. ISSP Header J3 Schematic




### 4.1.4.4 XRES Pin Selection Header

XRES/INT (pin# 3 of ISSP header J3) is routed to either XRES or P1_5 pin of the CapSense controller. The selection is made using the J4 header.

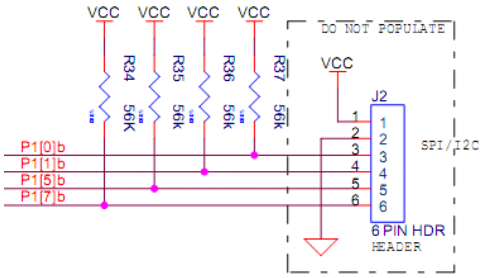
Figure 4-7. XRES Pin Selection Header J4 Schematic




### 4.1.4.5 Expansion Header

SPI and auxiliary I2C pins (P1_5, P1_7) of the CapSense controller are routed to the expansion header J2.

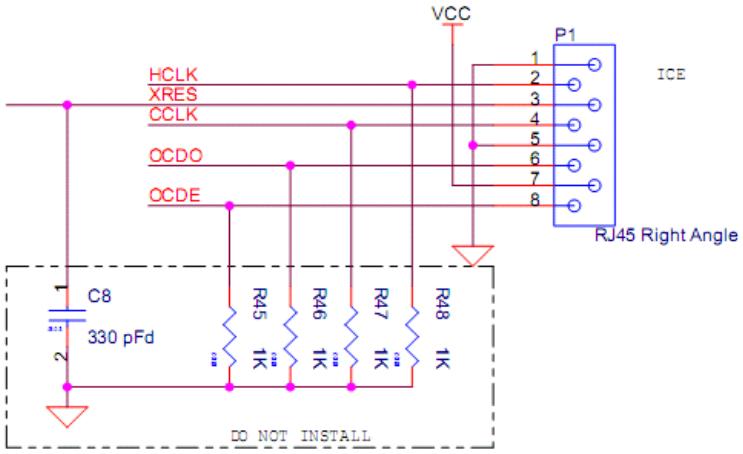
Figure 4-8. Expansion Header J2 Schematic



### 4.1.4.6 *ICE-Cube Debug Connector*

The ICE-Cube debugger allows to debug and view the content of specific memory locations. The ICE-Cube debugger can be connected to the board through port P1. The following figure shows the schematic view of the ICE-Cube debug connector.

Figure 4-9. ICE-Cube Debug Connector P1 Schematic




**Note** The current revision of the kit has known issues with debugging and the connector is not populated; see the release notes for a workaround.

### 4.1.4.7 *Adjustable Regulator - VADJ*

The CY3280-20x34 Universal CapSense Controller board has an on-board adjustable regulator. Regulated 5-V output from LM117 is used as the source. The factory setting is 3.3 V.

VADJ being the output of LP387ES-ADJ, follows this equation:

VADJ = 1.216 × (1 + Rx / Ry)

Where,

Rx is the resistance between VOUT and ADJ terminal of regulator LP3875. From the schematic, Rx corresponds to 8.87 KΩ.

Ry is the resistance between ADJ and GND terminal of regulator LP3875. Load Ry is adjusted by sending I2C commands via ISSP connector J3.

I2C command format to vary Ry

W <7bit I2C Address = 0x2D> <0x00> <$(\text{Data Byte})_{16}$>

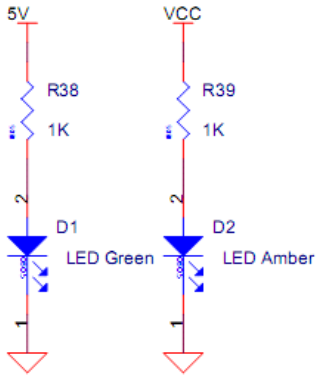
Where,

Ry = $(\text{Data Byte})_{10}$ × (10K/256)

### 4.1.4.8 Power LEDs

The LEDs are used to show the status of the controller board. LED D1 lights up when the board is powered by any of the power sources. LED D2 lights up when the CapSense controller is powered.

Figure 4-10. LEDs D1 and D2 Schematic




### 4.1.4.9 CMod

CMod is the test point provided on the CY3280-20x34 Universal CapSense Controller board to probe voltage on capacitor C2.

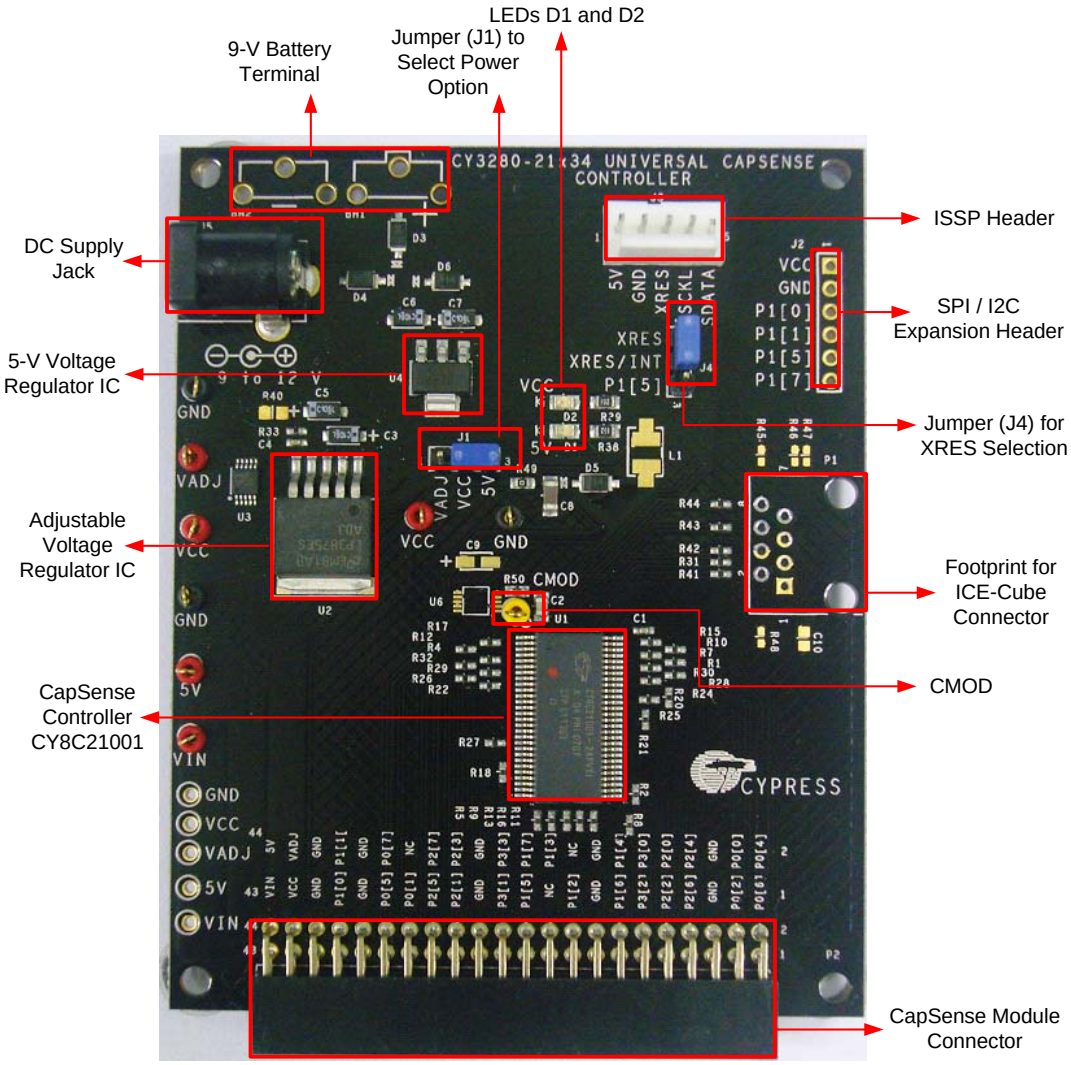
Capacitor C2, popularly known as modulation/integration capacitor (CMod), is the only external component required by the CapSense CSA_EMC algorithm.

For more details on CMod, see the CSA_EMC User Module datasheet.

## 4.2 CY3280-21x34 Universal CapSense Controller Board

The CY3280-21x34 Universal CapSense Controller Kit is designed to prototype rapidly and develop CapSense-based solutions around CY8C21x34 family of CapSense controllers. The following figure highlights important board components and connectors.

Figure 4-11. CY3280-21x34 Universal CapSense Controller Kit - Top View



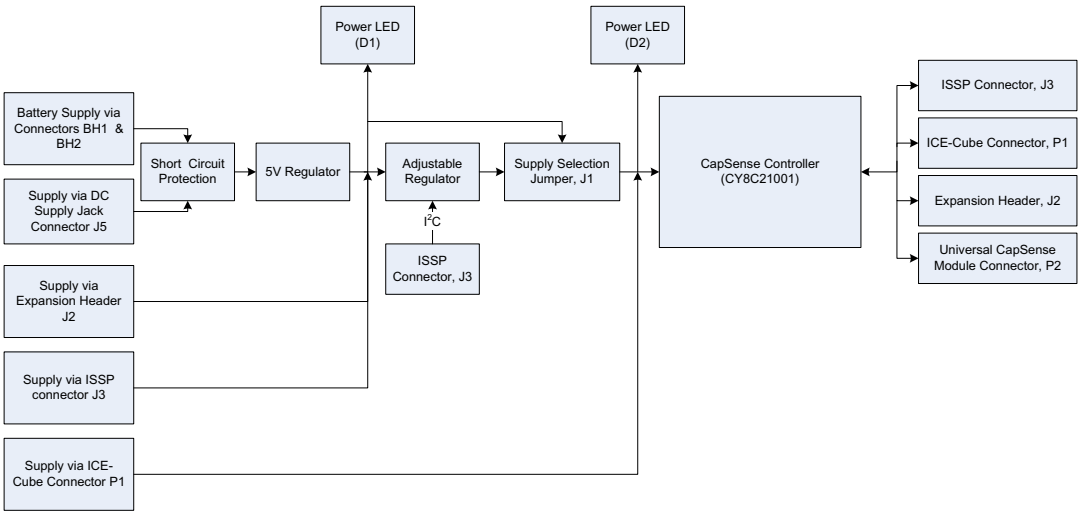
### 4.2.1 System Block Diagram

Figure 4-12 shows the block diagram of the CY3280-21x34 Universal CapSense Controller kit.

The kit can be powered from five different sources; to select a source, place the jumper on power select header J1. Power supply from the battery connector and DC socket is short-circuit protected to avoid mishap due to accidental short between these sources. The 5-V regulator output, supply from expansion header, and supply from ISSP connector are shorted. Supply from the ICE-Cube connector is fed directly to the CapSense controller. An I2C-controlled variable power supply is also part of the kit.

Any Universal CapSense Module board can be connected to the kit via the Universal CapSense Module connector P2. SPI and auxiliary I2C pins from the CapSense controller are routed to expansion header, J2. Connector P1 is used to interface ICE-Cube, the emulator needed for in-circuit debugging of CapSense projects. CapSense controller is programmed through the ISSP connector J3 using MiniProg1.

Figure 4-12. System Block Diagram of CY3280-21x34 Universal CapSense Controller Board



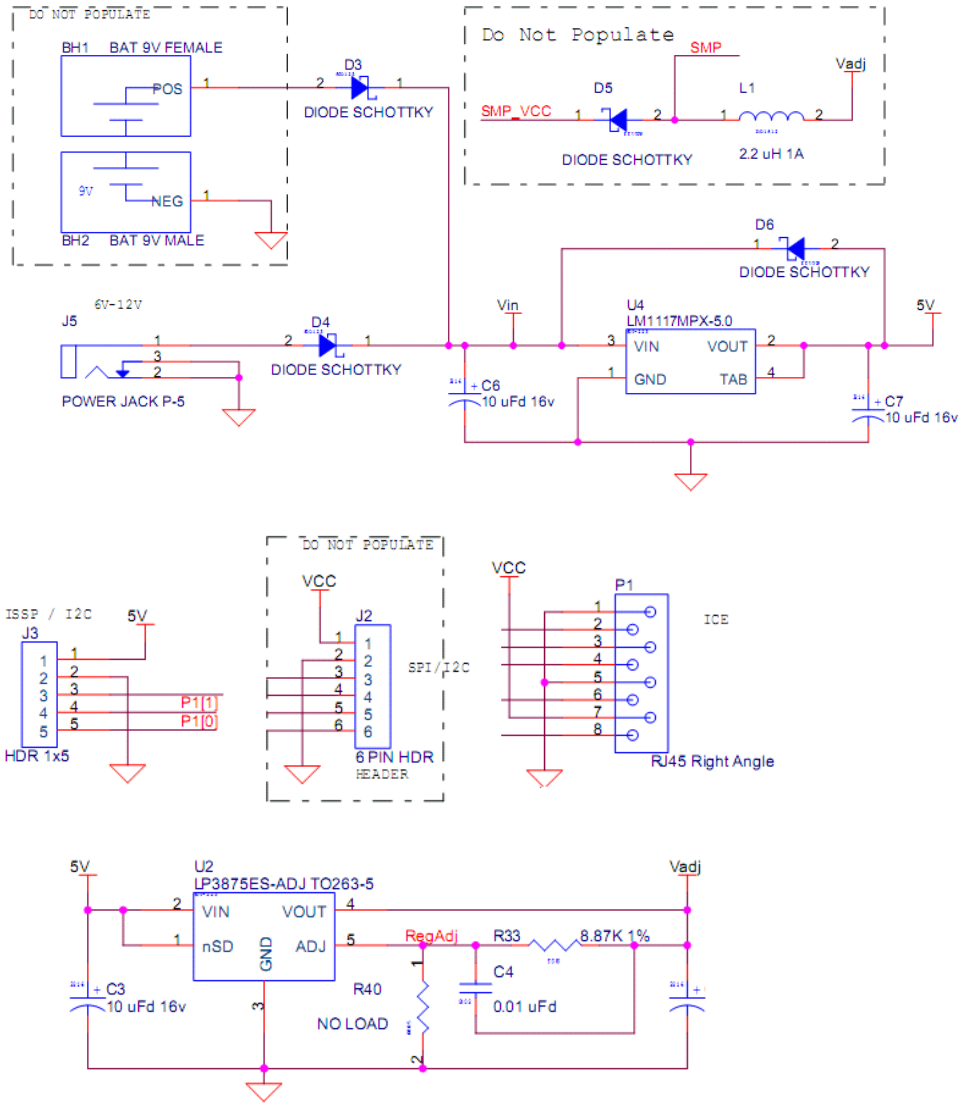
## 4.2.2 Power Sources

### *4.2.2.1 Power Supply Nets*

The board has several power nets. Following are the definitions of the different power nets.

- VIN (9 V or 12 V): This is the input power before it is fed to any of the regulators. A 9-V to 12-V power supply adapter or a 9-V battery is used as the source.
- 5 V: This is fed by the 5-V regulator output, pin#1 of J2 or pin#1 of J3.
- VADJ/Vadj: This is fed by 5 V and is the output of the onboard adjustable regulator.
- VCC: This is the power from either 5 V or VADJ. The source of VCC can be chosen using the J1 header.
- SMP_VCC: This is fed by VCC (filtered) or voltage pump. It is used to power the CapSense controller.

Figure 4-13. Power Supply System Schematic



## 4.2.3 Power Supply Configuration Examples

### *4.2.3.1 Power CapSense Controller at +5 V from Onboard Regulator*

1. Connect a 9-V to 12-V power supply adapter to the DC power socket J5 or connect a 9-V alkaline battery to the battery terminals. (Battery terminals on BH1 and BH2 are not mounted in the kit.)
2. Place the jumper on header J1 to select 5 V as VCC.

### *4.2.3.2 Power CapSense Controller from Onboard Adjustable Regulator*

1. Connect a 9-V to 12-V power supply adapter to the DC power socket J5 or connect a 9-V alkaline battery to the battery terminals. (Battery terminals should be soldered on footprints BH1 and BH2.) You can also apply source at pin#1 of J2 or pin#1 of J3.
2. Place the jumper on header J1 to select VADJ as VCC.

### *4.2.3.3 Power CapSense Controller Directly from ISSP Header*

1. Insert MiniProg1 or I2C-USB Bridge to the ISSP header J3. Power the connected device.
2. Place the jumper on header J1 to select 5 V as VCC.

### *4.2.3.4 Power CapSense Controller from ICE-Cube*

Connect the RJ-45 socket from ICE-Cube to connector P1. There are no specific requirements for placing jumper on header J1.

## 4.2.4 Hardware Description

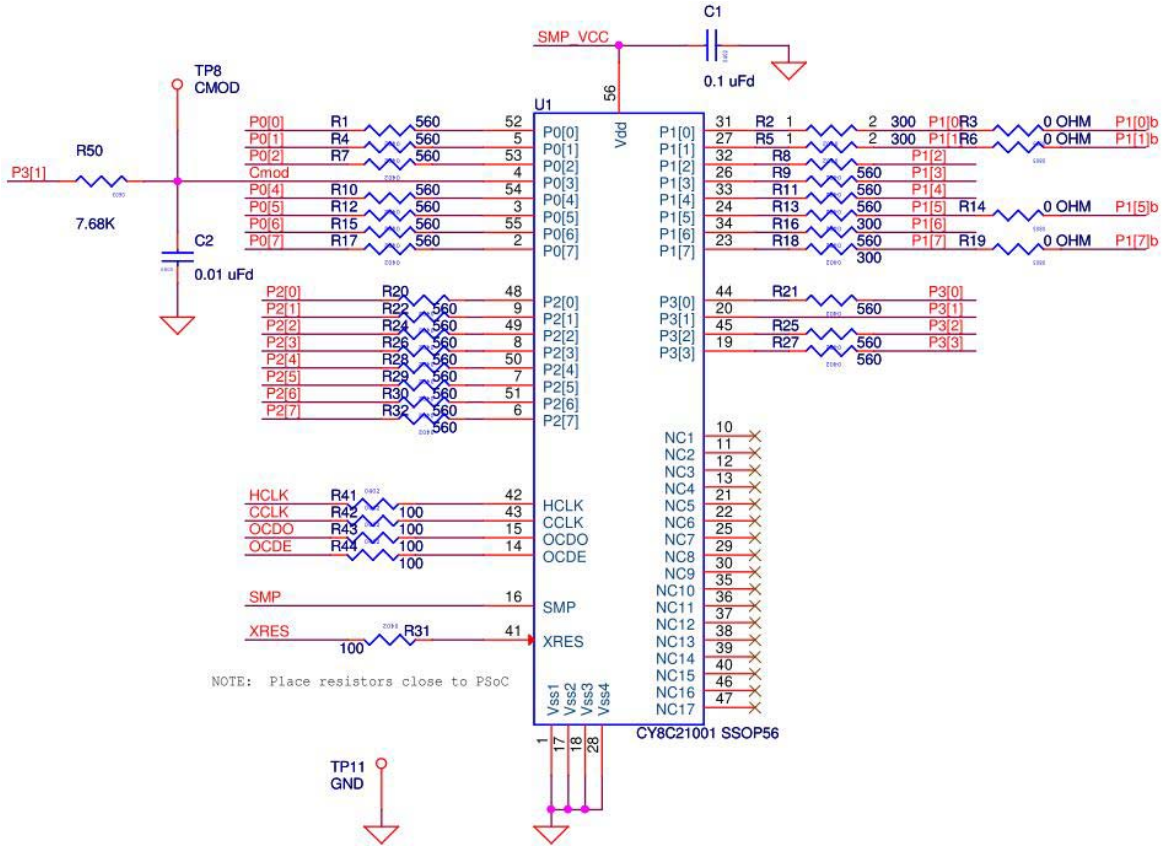
### *4.2.4.1 CapSense Controller (CY8C21x34)*

The CY8C21001 56-SSOP is the onboard CapSense controller. CY8C21001 supports programming and in-circuit debugging of PSoC Designer projects targeted for the CY8C21x34 family of devices.

Cypress's CY8C21x34 is a low-power, high-performance, programmable touch sensing controller family. It has the following features:

- CapSense Sigma Delta (CSD) capacitive sensing technology
- Supports up to 24 capacitive buttons and 4 sliders
- Proximity sensing up to 5 cm (with onboard PCB trace)
- Water tolerant performance with shield electrode
- 2.4 V to 5.25 V operating voltage
- Up to 28 GPIOs
- I2C communication with master, slave, and multi-master configurations
- Four digital blocks provide:
  - Counter, timer, PWM, PRS, PWD (pulse width discriminator)
  - SPI, UART, IRDA, and one-wire communication protocols
- Single slope incremental ADC (with CSDADC)
- EEPROM emulation
- 8-KB flash and 512-B RAM
- Internal main oscillator up to 48 MHz with a 24-MHz system clock
- Variety of packages: 16-SOIC, 20-SSOP, 28-SSOP, 32-QFN, and 56-SSOP
- AEC qualified automotive grade parts - CY8C21334 and CY8C21534

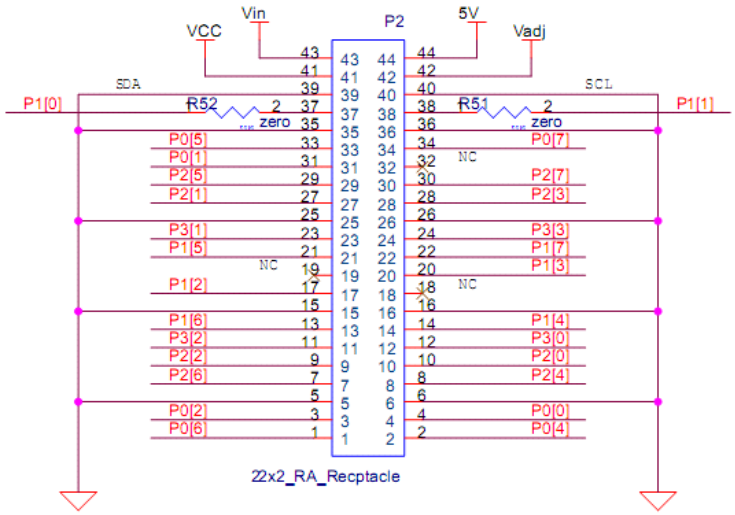
Figure 4-14. CapSense Controller CY8C21001 Schematic




### 4.2.4.2 *Universal CapSense Module Connector*

The CY3280-21x34 has an expansion port, P2, designed to connect UCC module boards. The controller board can be used with any of the Universal CapSense module boards. The boards can be interfaced to the CY3280-21x34 via the 44-pin connector P2. The pin mapping for the port P2 is shown in the following figure.

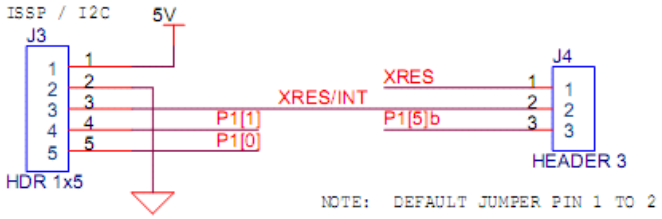
Figure 4-15. Universal CapSense Module Connector Schematic



### 4.2.4.3 ISSP

ISSP is used to program the device using MiniProg1. Plug in the MiniProg device to the ISSP header J3. The ISSP connector is also used to connect the I2USB bridge to communicate between the PC and controller board. The pin mapping for the ISSP connector is shown in the following figure.

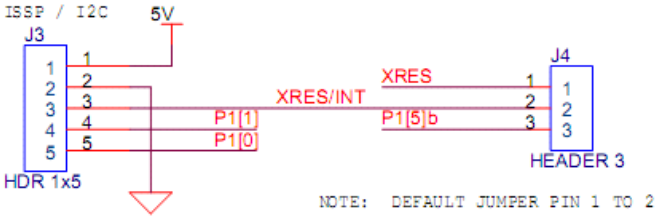
Figure 4-16. ISSP Header J3 Schematic




### 4.2.4.4 XRES Pin Selection Header

XRES/INT (pin# 3 of ISSP header J3) is routed to either XRES or P1_5 pin of the CapSense controller. The selection is made using J4 header.

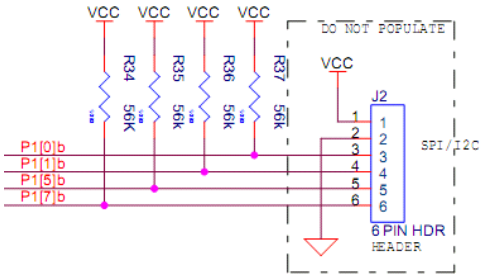
Figure 4-17. XRES Pin Selection Header J4 Schematic




### 4.2.4.5 Expansion Header

SPI and auxiliary I2C pins (P1_5, P1_7) of the CapSense controller are routed to the expansion header J2.

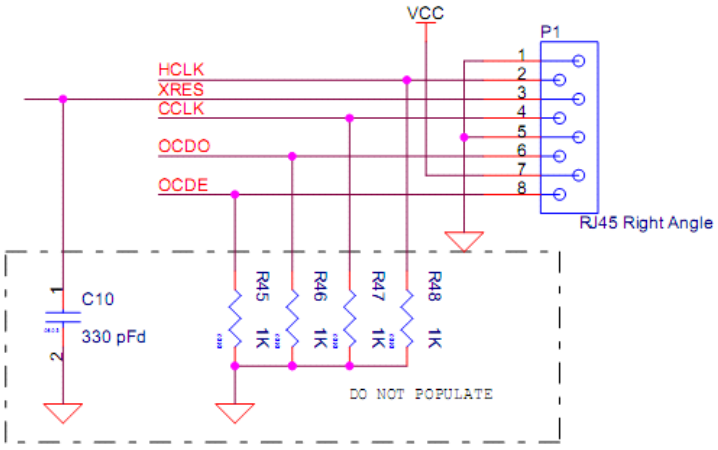
Figure 4-18. Expansion Header J2 Schematic



### 4.2.4.6 *ICE-Cube Debug Connector*

The ICE-Cube debugger allows to debug and view the content of specific memory locations. The ICE-Cube debugger can be connected to the board through port P1. The following figure shows the schematic view of the ICE-Cube debug connector.

Figure 4-19. ICE-Cube Debug Connector P1 Schematic




**Note** The current revision of the kit has known issues with debugging and the connector is not populated; see the release notes for the workaround.

### 4.2.4.7 *Adjustable Regulator - VADJ*

The CY3280-21x34 Universal CapSense Controller board has an onboard adjustable regulator. Regulated 5-V output from LM117 is used as the source. The factory setting is 3.3 V.

VADJ being the output of LP387ES-ADJ, follows this equation:

VADJ = 1.216 × (1 + Rx / Ry)

Where,

Rx is the resistance between VOUT and ADJ terminal of regulator LP3875. From the schematic, Rx corresponds to 8.87 KΩ.

Ry is the resistance between ADJ and GND terminal of regulator LP3875. Load Ry is adjusted by sending I2C commands via ISSP connector J3.

I2C command format to vary Ry.

W <7bit I2C Address = 0x2D> <0x00> <$(\text{Data Byte})_{16}$>

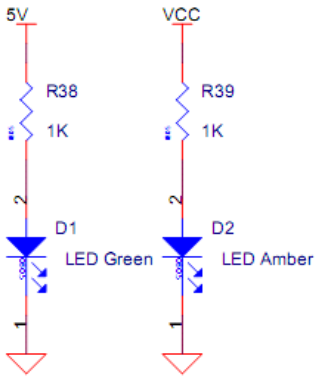
Where,

Ry = $(\text{Data Byte})_{10}$ × (10K/256)

### 4.2.4.8 Power LEDs

The LEDs are used to show the status of the controller board. LED D1 lights up when the board is powered by any of the power sources. LED D2 lights up when the CapSense controller is powered.

Figure 4-20. LEDs D1 and D2 Schematic




### 4.2.4.9 CMod

CMod is the test point provided on the CY3280-21x34 Universal CapSense Controller board to probe voltage on capacitor C2.

Capacitor C2 popularly known as modulation capacitor (CMod) is one of the external component required by the CapSense_CSD algorithm. The other component is the resistor Rb (R50).

For more details on CMod and Rb, see the CSD User Module datasheet.

## 4.3 Board Accessories

### 4.3.1 CY3280-SLM Universal CapSense Linear Slider Module Board

CY3280-SLM board consists of five CapSense buttons, one linear slider (with 10 sensors), and five LEDs. The module board can be connected to the Universal CapSense Controller board via a 44-pin receptacle connector J1.

Shield traces on the board can be either connected to ground or to the shield electrode pin of the CapSense controller. A 3-pin header J2 is used to select between ground and shield electrode.

The board also provides footprints for an optional I2C EEPROM and thermistor, which are not populated by default.

Figure 4-21. CY3280-SLM Universal CapSense Linear Slider Module Board

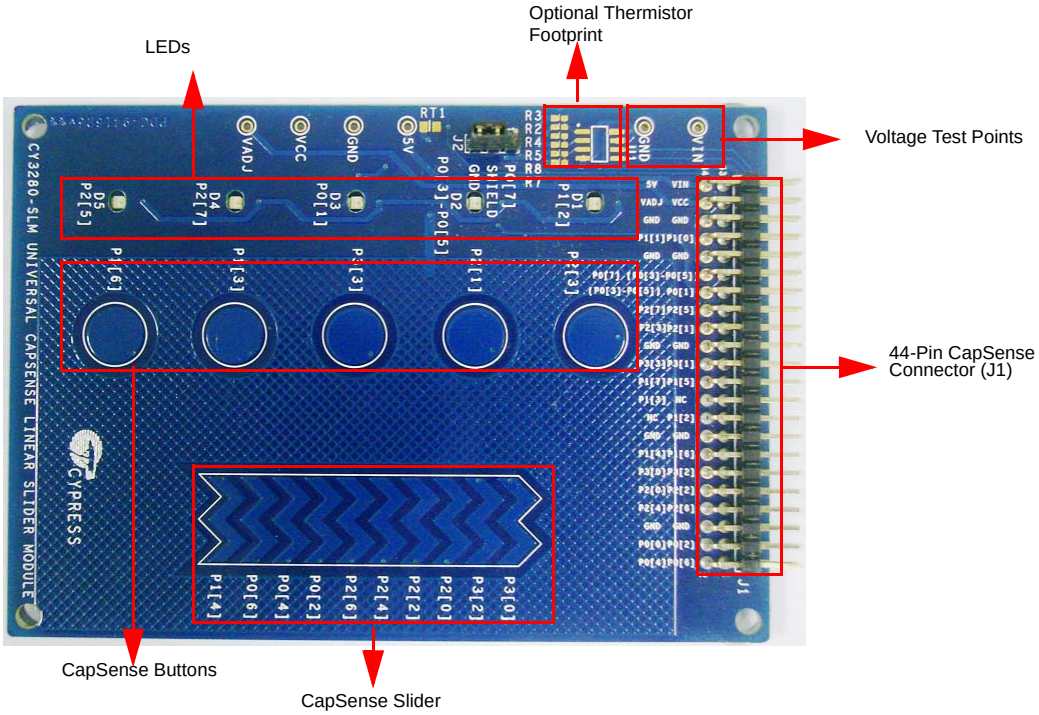
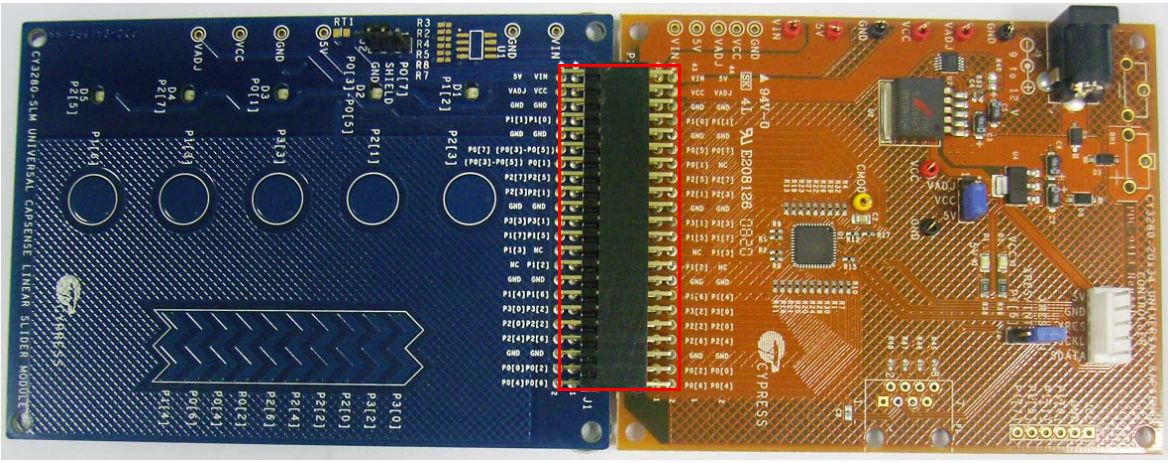


Figure 4-22. CY3280-SLM Connected to CY3280-20x34 Universal CapSense Controller Board



## 4.3.2 CY3280-BBM Universal CapSense Prototyping Module Board

The CY3280-BBM Universal CapSense Prototyping Module provides access to every pin routed to the 44-pin connector on the attached UCC board. Use the prototyping module board with a Universal CapSense Controller to implement additional functionality that is not part of other single-purpose Universal CapSense module boards.

Figure 4-23. CY3280-BBM Universal CapSense Prototyping Module Board

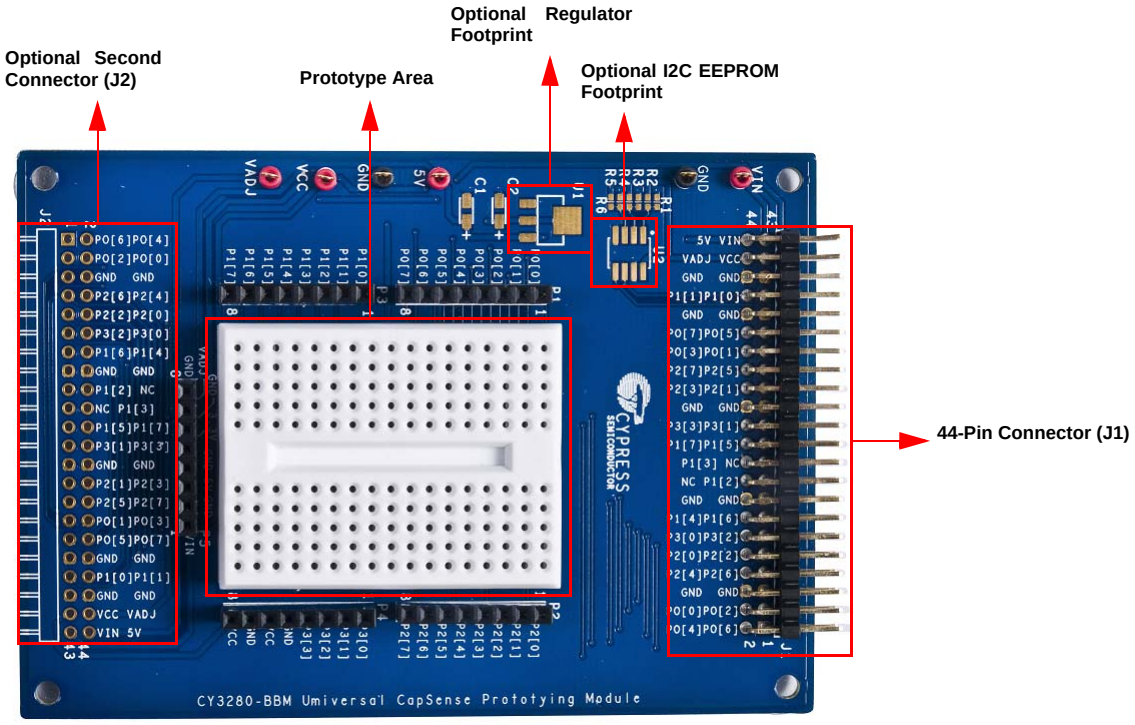
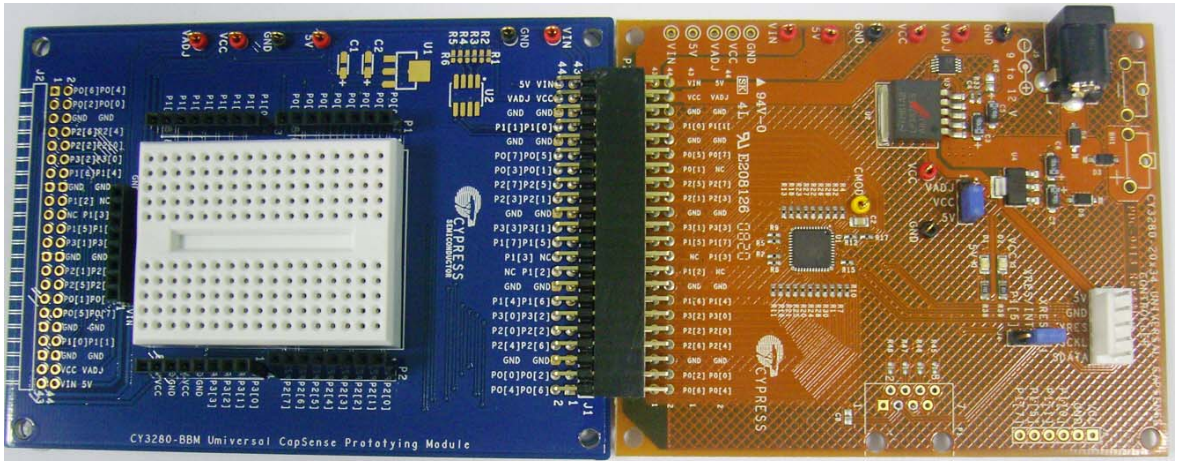


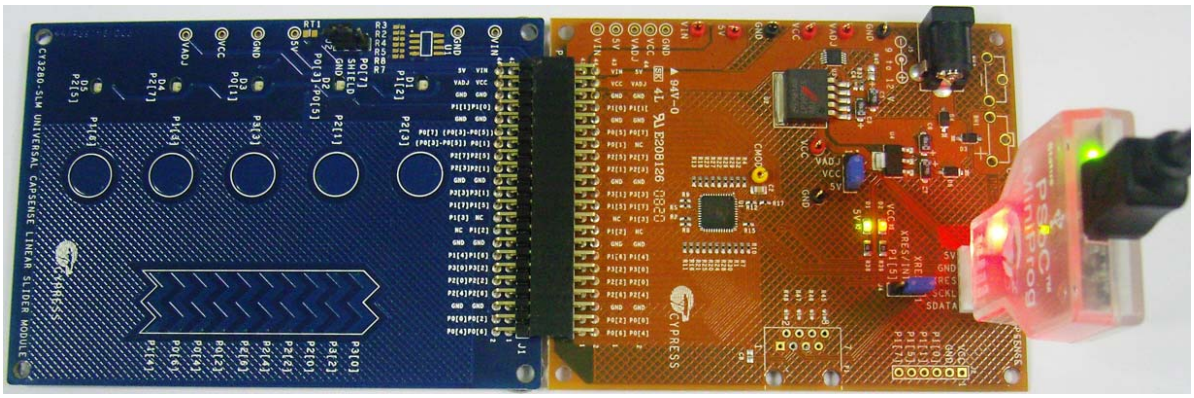
Figure 4-24. CY3280-BBM Connected to CY3280-20x34 Universal CapSense Controller Board




### 4.3.3 CY3217-MiniProg1 PSoC Programmer

CY3217-MiniProg1 is an inexpensive programmer for PSoC devices. MiniProg1 also supports all programmable CapSense controllers. ISSP header J3 on the CY3280-Universal CapSense Controller board is used to connect MiniProg1.

Figure 4-25. MiniProg1 Connected to CY3280-20x34 Universal CapSense Controller Board

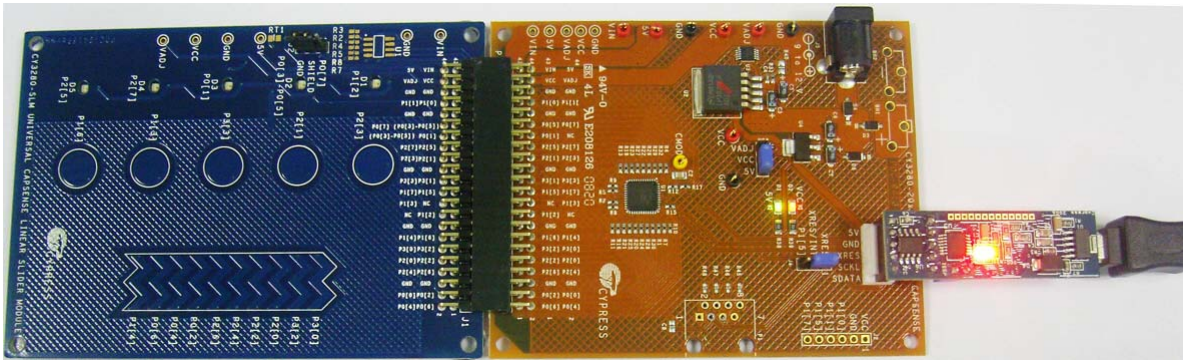


### 4.3.4 CY3240-I2USB Bridge

The main purpose of the I2C-USB bridge is to test, tune, and debug programs that have an I2C slave interface. It is also useful for data acquisition and regulation under PC control.

By default, the I2C-USB bridge is connected to the ISSP header J3 on the CY3280-20x34 Universal CapSense Controller board.

Figure 4-26. I2C-USB Bridge Connected to CY3280-20x34 Universal CapSense Controller Board



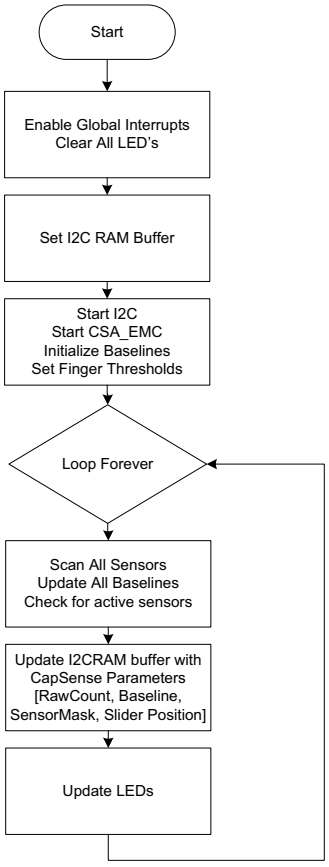
# 5. Code Examples

This section walks you through the high-level design process to open, build, program, and run code examples using the CY3280-BK1 Universal CapSense Controller Kit.

## 5.1 My First CapSense (CY8C20x34) Project

This project demonstrates how to use the CapSense CSA_EMC User Module to scan buttons and sliders on the CY3280-SLM module board. The CSA_EMC User Module scans all the buttons continuously and stores the raw count, baseline, button on/off state, and slider centroid position in a structure defined by I2C_REGS. This structure is exposed to an I2C master to allow reading by the EzI2Cs User Module. LED User Modules are used to control LEDs based on detected finger touch.

Figure 5-1. Firmware Flow

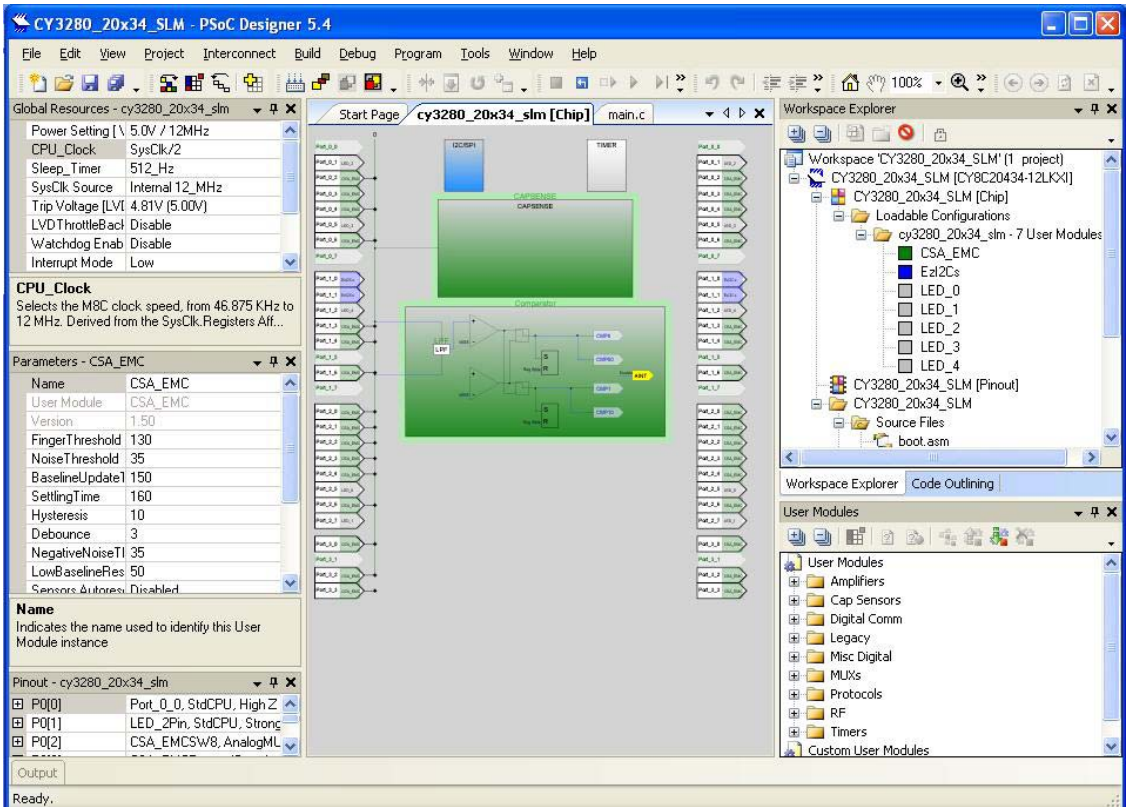


### 5.1.1 Loading My First CapSense Project

1. Open PSoC Designer.
2. In the Start page, navigate to **File > Open Project/Workspace**.
3. Navigate to the project directory `<Install_Directory>\CY3280-BK1\<version>\Firmware.`
4. Move the Firmware folder to a writable directory and then open it
5. Open the folder CY3280_20x34_SLM.
6. Double-click on *CY3280_20x34_SLM.app.*

The project opens in the Chip Editor view. All project files are in the Workspace Explorer.

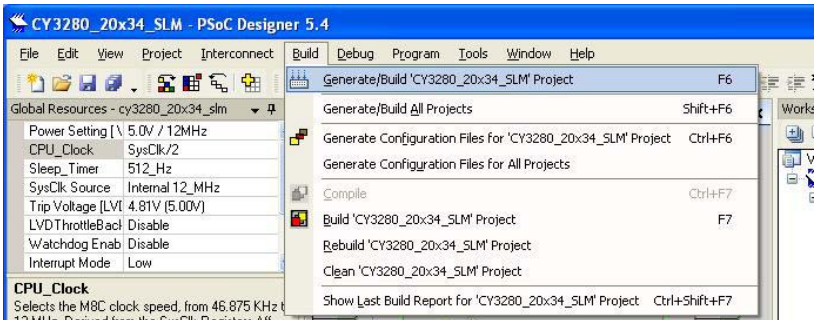
Figure 5-2. PSoC Designer Chip Editor View




### 5.1.2 Building My First CapSense Project

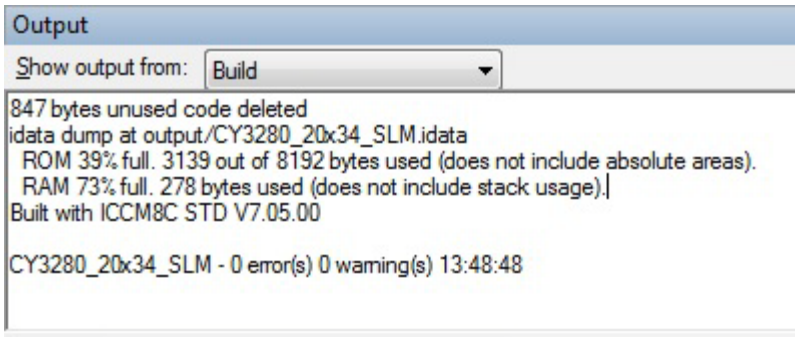
Select **Build > Generate/Build 'CY3280_20x34_SLM Project**.

Figure 5-3. Build Project



PSoC Designer builds the project and displays comments in the Output window. When you see the message that the project is built with 0 errors and 0 warnings, you are ready to program the device.

Figure 5-4. Output Window

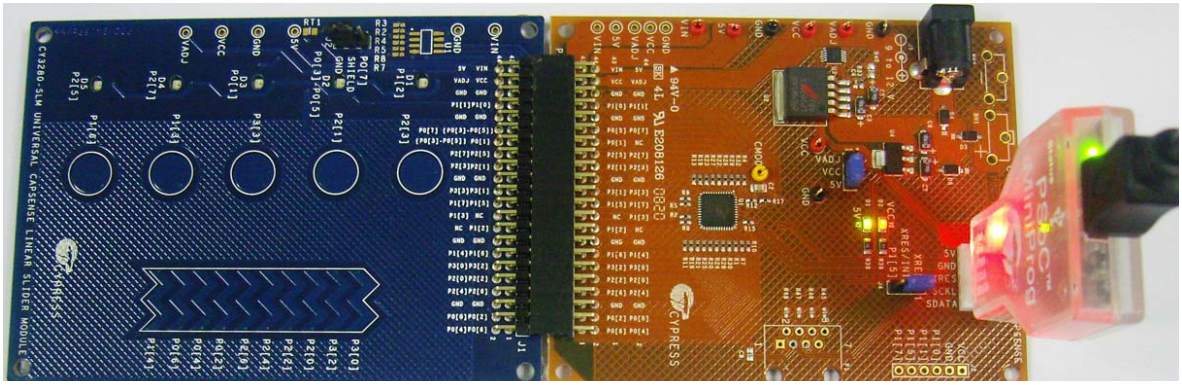



## 5.1.3 Setting up the Board

This section demonstrates the setup of CY3280-SLM with CY3280-20x34 Universal CapSense Controller board.

1. Connect the CY3280-SLM board to the P2 receptacle connector of the CY3280-20x34 Universal CapSense Controller boards.
2. In the CY3280-20x34 board, place jumper on header J1 to short pins 2 and 3. This setting allows the CapSense controller to be powered from ISSP connector J3.
3. In the CY3280-20x34 board, place jumper on header J4 to short pins 1 and 2. This setting routes the XRES pin of the CapSense controller to pin 3 of ISSP connector J3.
4. In the CY3280-SLM board, place jumper on header J2 to short pins 2 and 3. This setting connects the shield traces on the CY3280-SLM board to ground.
5. Connect your computer to the CY3280-20x34 Universal CapSense Controller board's ISSP connector J3 using MiniProg1 and a USB cable.

Figure 5-5. Board Setup



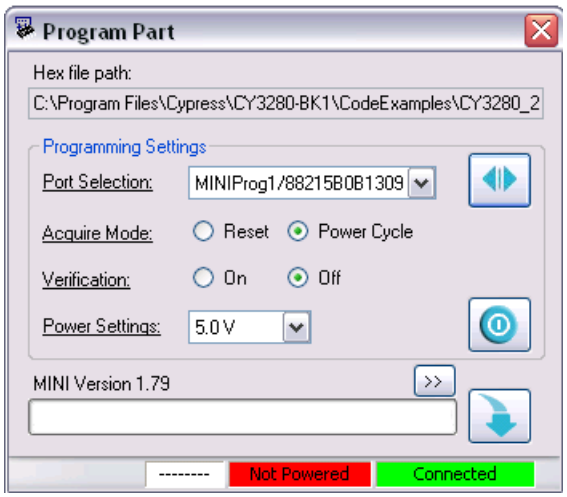
## 5.1.4 Programming My First CapSense Project

1. Open **Program Part** in PSoC Designer by selecting **Program > Program Part**.
2. In the Program Part window:
   a. Select **MiniProg1** in the **Port Selection** box.
   b. Set **Acquire Mode** to **Power Cycle**.
   c. Set **Verification** to **ON**. This ensures that the downloaded checksum matches the actual checksum.

d. Set **Power Settings** to **5.0V**.
e. Click the program arrow to program the device.

3. Wait until programming is completed.

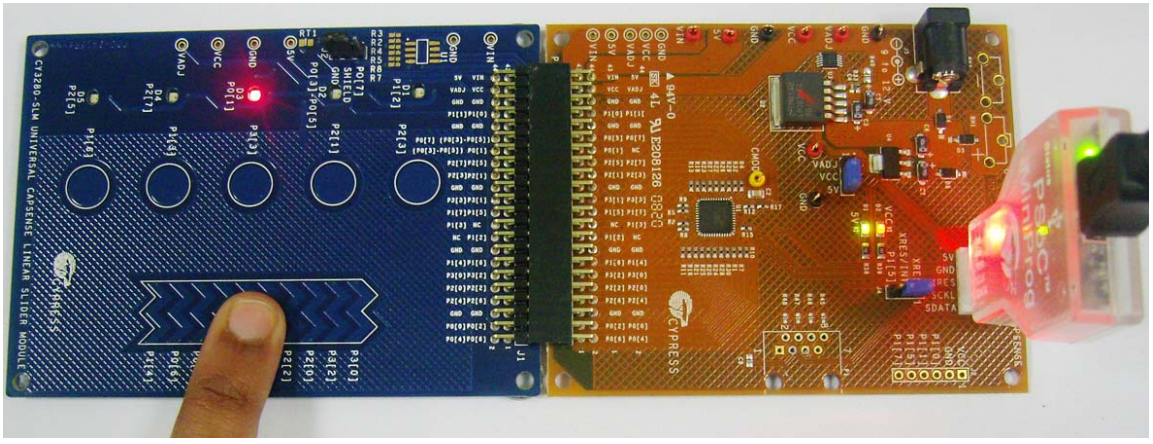
Figure 5-6. Program Part View




## 5.1.5 Running My First CapSense Project

1. Power the board at 5 V using MiniProg1 or from any of the sources listed in Power Sources on page 31.
2. Touch the linear slider on the CY3280-SLM module board. The corresponding LEDs on the CY3280-SLM board light up.
3. Touch a button. The corresponding LED on the CY3280-SLM module board lights up. Multiple buttons can be touched at the same time. The linear slider and buttons can also be used simultaneously.

Figure 5-7. LED2 Glows when Linear Slider is Touched



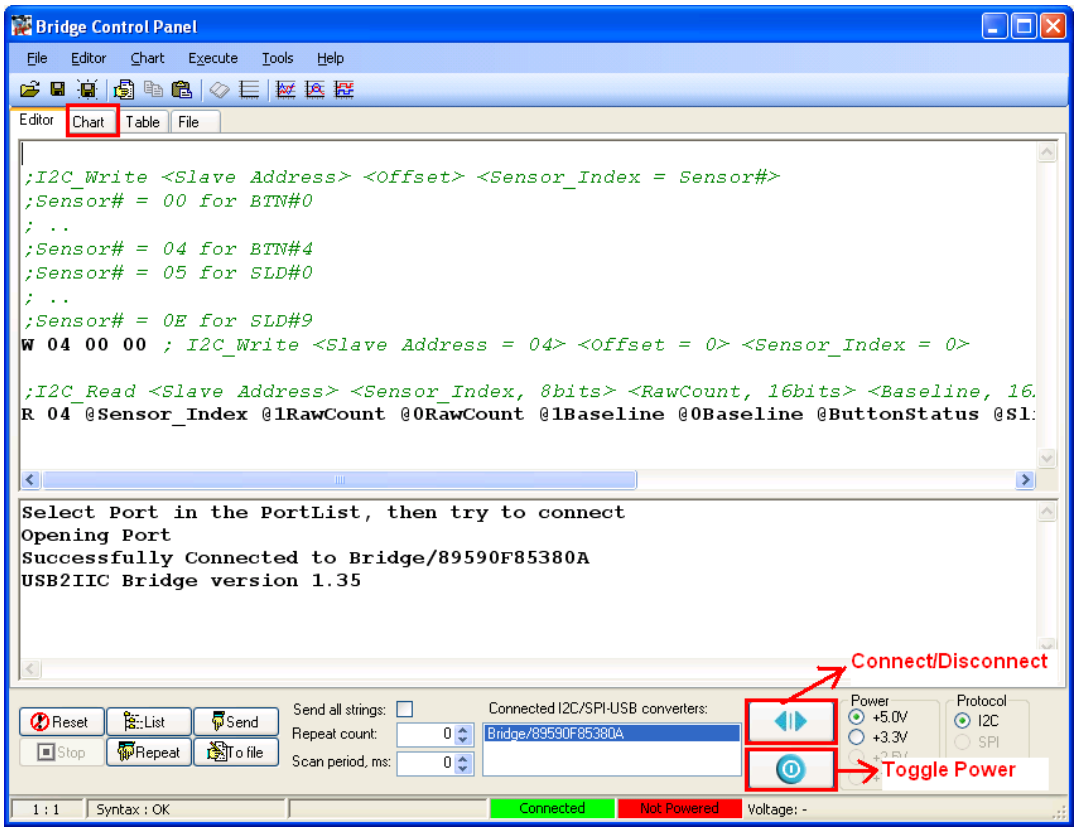
## 5.1.6 Reading CapSense Data over I2C

1. Connect your computer to the CY3280-20x34 Universal CapSense Controller board's ISSP connector J3 using I2C-USB bridge and a USB cable.
2. Go to **Start > Cypress > Open Bridge Control Panel**.

   **Note** Bridge Control Panel is installed as part of the PSoC Programmer installation process.

3. Select the device from the **Connected I2C/SPI-USB converters:** window and click on the **Connect/Disconnect** button.
4. Power the CY3280-20x34 CapSense Controller board at 5 V.
5. Select **File > Open File**. Load *CY3280-20x34.iic* from `<Install_Directory>\CY3280-BK1\<version>\Firmware\CY3240_I2USB_Configuration files`.
6. Select **Charts > Variable Settings**. Load *CY3280-20x34.ini* from `<Install_Directory>\CY3280-BK1\<version>\Firmware\CY3240_I2USB_Configuration files`. Click **OK** to return to the main window.

Figure 5-8. Bridge Control Panel View




7. Sample data read:
   a. Reading raw count and baseline of P1[6]/BTN0:
   i. Send I2C write instruction W 04 00 00 once.
   ii. Press the **Repeat** button to send the following I2C read instruction continuously `R 04 @Sensor_Index @1RawCount @0RawCount @1Baseline @0Baseline @ButtonStatus @SliderPosition.`
   iii. Go to the **Chart** tab to view raw count and baseline of P1[6]/BTN0.
   b. Reading raw count and baseline of P1[4]/SLD0:
   i. Send I2C write instruction W 04 00 05 once.
   ii. Press the **Repeat** button to send the following I2C read instruction continuously `R 04 @Sensor_Index @1RawCount @0RawCount @1Baseline @0Baseline @ButtonStatus @SliderPosition.`
   iii. Go to the **Chart** tab to view raw count and baseline of P1[4]/SLD0.

See 5.1.6.1 CapSense Sensor Data for information on how to view raw count and baseline data of other CapSense button and slider segments.

### 5.1.6.1 CapSense Sensor Data

The CY8C20x34 board firmware updates the raw count and baseline value of a CapSense sensor to the I2C register continuously. The contents of the I2C register are read and output to the GUI whenever an I2C read command is sent to the slave. By default, the output is always Button 0 data.

To view the raw count and baseline of any other CapSense sensor, the sensor number or the sensor index should be specified to the slave using a I2C write command.

The write command syntax is as follows:
`W <Slave Address> <Offset> <Sensor_Index>`

Slave_Address - 04 (constant)

Offset - 00 (constant)

Sensor_Index - See Table 5-1

Table 5-1. Sensor Index

| No. | Pinout | Button/Slider segment | Sensor_Index |
|---|---|---|---|
| 1 | P1[6] | BTN0 | 0 |
| 2 | P1[3] | BTN1 | 1 |
| 3 | P3[3] | BTN2 | 2 |
| 4 | P2[1] | BTN3 | 3 |
| 5 | P2[3] | BTN4 | 4 |
| 6 | P1[4] | SLD0 | 5 |
| 7 | P0[6] | SLD1 | 6 |
| 8 | P0[4] | SLD2 | 7 |
| 9 | P0[2] | SLD3 | 8 |
| 10 | P2[6] | SLD4 | 9 |
| 11 | P2[4] | SLD5 | 0A |
| 12 | P2[2] | SLD6 | 0B |
| 13 | P2[0] | SLD7 | 0C |
| 14 | P3[2] | SLD8 | 0D |
| 15 | P3[0] | SLD9 | 0E |

For example, to read the Button 2/P3[3] data, first send a write command as follows:
`W 04 00 02`

Then, read the data by sending the read command
`R 04 @Sesnor_Index @1RawCount @0RawCount @1Baseline @0BaseLine @ButtonStatus @SliderPosition`

Similarly, to read the Slider 6/P2[2] data, send the write command as follows:
`W 04 00 0B`

Then, read the data by sending the read command
`R 04 @Sesnor_Index @1RawCount @0RawCount @1Baseline @0BaseLine @ButtonStatus @SliderPosition`

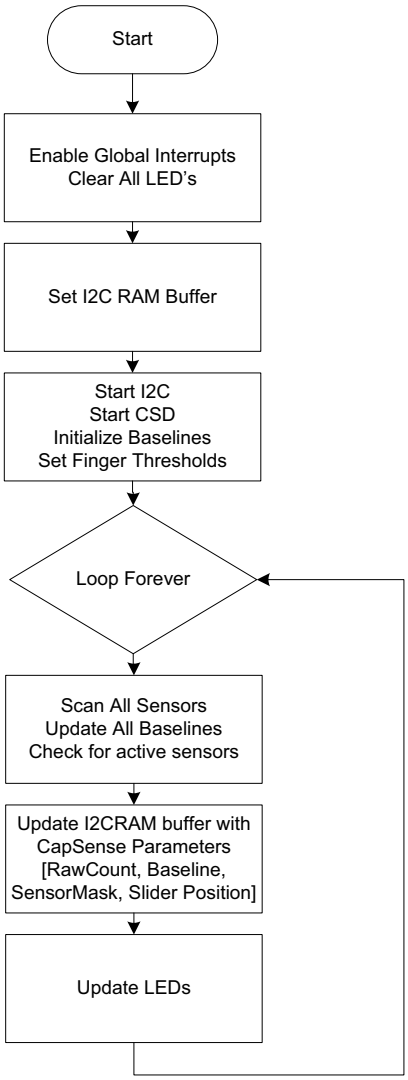
### 5.1.7 Tuning for Overlay

The code example accompanying the kit is not tuned with overlay. For the code example to work with the 1.5-mm and 3-mm acrylic overlays, the CSA_EMC User Module parameters must be adjusted. See the Tuning section of the user module datasheet for details; to select this datasheet, right-click on the CSA_EMC User Module in Workspace Explorer.

## 5.2 My First CapSense (CY8C21x34) Project

This project demonstrates how to use the CapSense CSD User Module to scan buttons and sliders on the CY3280-SLM module board. The CSD User Module scans all the buttons continuously and stores the raw count, baseline, button on/off state, and slider centroid position in a structure defined by I2C_REGS. This structure is exposed to an I2C master to allow reading by the EzI2Cs User Module. LED User Modules are used to control LEDs based on detected finger touch.

Figure 5-9. Firmware Flow

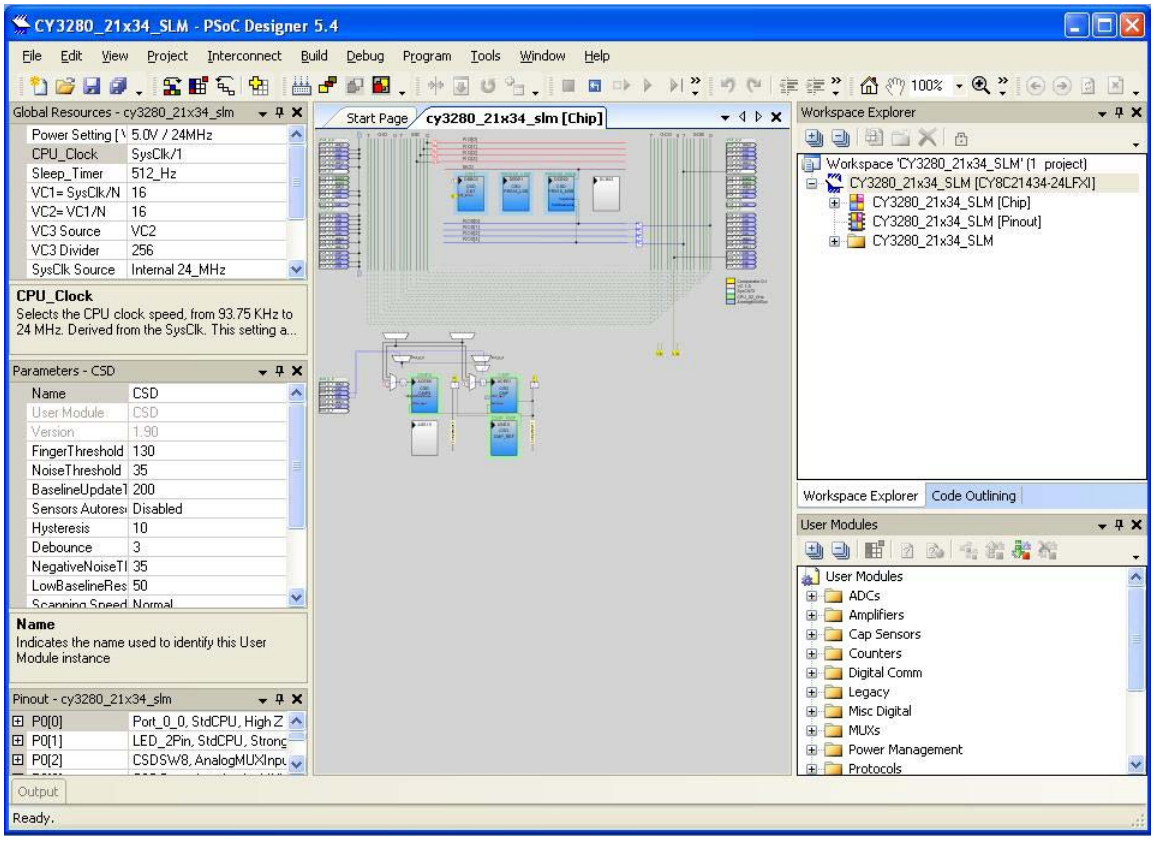


### 5.2.1 Loading My First CapSense Project

1. Open PSoC Designer.
2. In the Start page, go to **File > Open Project/Workspace**.
3. Navigate to the project directory `<Install_Directory>\CY3280-BK1\<version>\Firmware\`.
4. Move the Firmware folder to a writable directory and then open it
5. Open the folder CY3280_21x34_SLM.
6. Double-click *CY3280_21x34_SLM.app*.

The project opens in the Chip Editor view. All project files are in the Workspace Explorer.

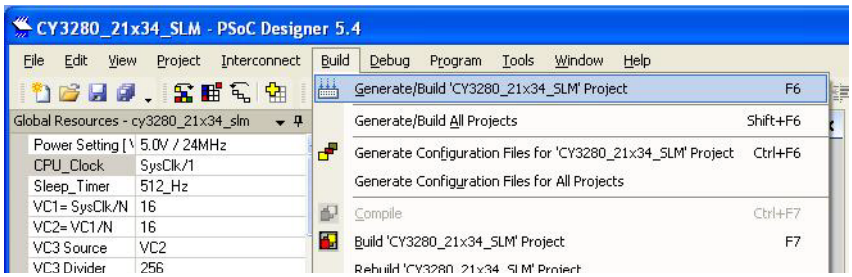
Figure 5-10. PSoC Designer Chip Editor View




### 5.2.2 Building My First CapSense Project

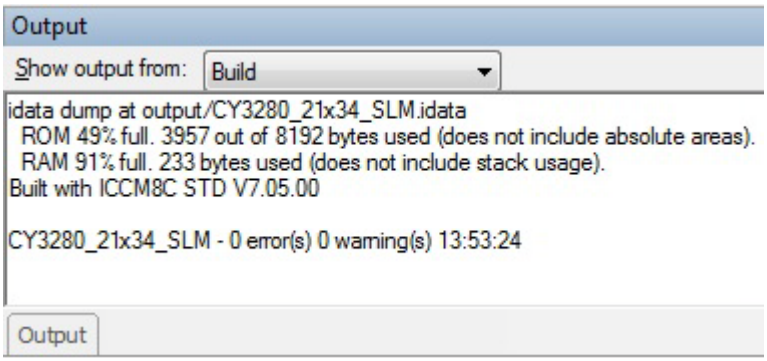
Select **Build > Generate/Build CY3280_21x34_SLM Project**.

Figure 5-11. Build Project



PSoC Designer builds the project and displays comments in the Output window. When you see the message that the project is built with 0 errors and 0 warnings, you are ready to program the device.

Figure 5-12. Output Window

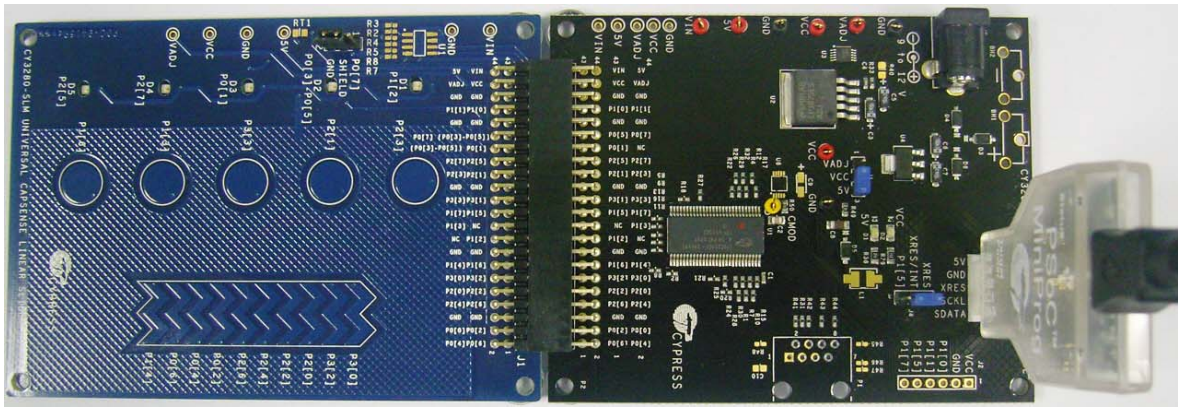



## 5.2.3 Setting up the Board

This section demonstrates the setup of CY3280-SLM with CY3280-21x34 Universal CapSense Controller board.

1. Connect the CY3280-SLM board to the P2 receptacle connector of the CY3280-21x34 Universal CapSense Controller boards.
2. In the CY3280-21x34 board, place jumper on header J1 to short pins 2 and 3. This setting allows the CapSense Controller to be powered from ISSP connector J3.
3. In the CY3280-21x34 board, place jumper on header J4 to short pins 1 and 2. This setting routes the XRES pin of the CapSense controller to pin 3 of ISSP connector J3.
4. In the CY3280-SLM board, place jumper on header J2 to short pins 2 and 3. This setting connects the shield traces on the CY3280-SLM board to ground.
5. Connect your computer to the CY3280-21x34 Universal CapSense Controller board's ISSP connector J3 using MiniProg1 and a USB cable.

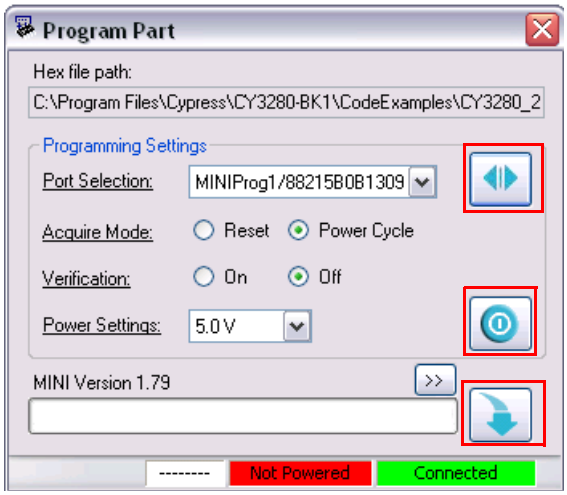
Figure 5-13. Board Setup



### 5.2.4 Programming My First CapSense Project

1. Open **Program Part** in PSoC Designer by selecting **Program > Program Part**.
2. In the Program Part window:
   a. Select **MiniProg1** in the **Port Selection** box.
   b. Set **Acquire Mode** to **Power Cycle**.
   c. Set **Verification** to **ON**. This ensure that the downloaded checksum matches the actual checksum.
   d. Set **Power Settings** to **5.0V**.
   e. Click the program arrow to program the device.
3. Wait until programming is completed

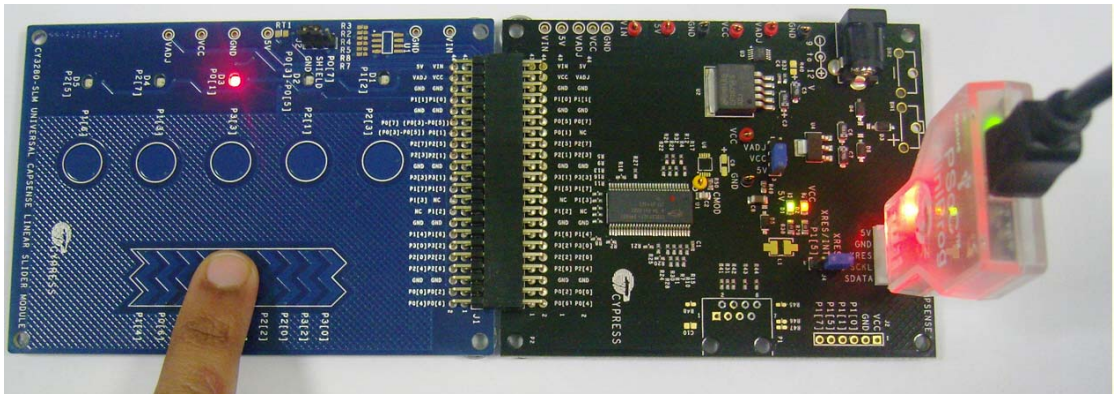
Figure 5-14. Program Part View




### 5.2.5 Running My First CapSense Project

1. Power the board at 5 V using MiniProg1 or from any one of the sources listed in Power Sources on page 31.
2. Touch the linear slider on the CY3280-SLM module board. The corresponding LEDs on the CY3280-SLM board light up.
3. Touch a button. The corresponding LED on the CY3280-SLM module board lights up. Multiple buttons can be touched at the same time. The linear slider and buttons can also be used simultaneously.

Figure 5-15. LED2 Glows when Linear Slider is Touched

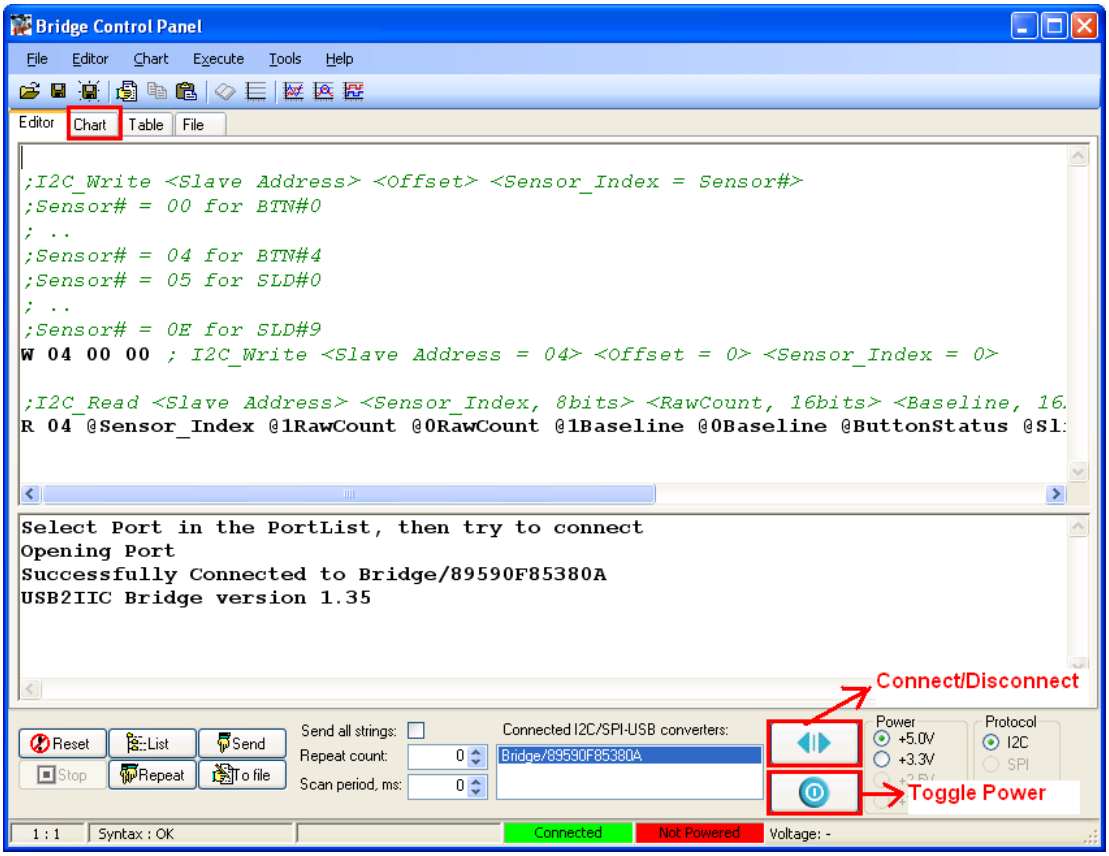


### 5.2.6 Reading CapSense Data Over I2C

1. Connect your computer to the CY3280-21x34 Universal CapSense Controller board's ISSP connector J3 using the I2C-USB bridge and a USB cable
2. Go to **Start > Cypress > Open Bridge Control Panel**.

   **Note** Bridge Control Panel is installed as part of the PSoC Designer installation process.
3. Select the device from the **Connected I2C/SPI-USB converters:** window and click on the **Connect/Disconnect** button.
4. Power the CY3280-21x34 CapSense Controller board at 5 V.
5. Select **File > Open File**. Load *CY3280-21x34.iic* from `<Install_Directory>\CY3280-BK1\<version>\Firmware\CY3240_I2USB_Configuration files`.
6. Select **Charts > Variable Settings**. Load *CY3280-21x34.ini* from `<Install_Directory>\CY3280-BK1\<version>\Firmware\CY3240_I2USB_Configuration files`. Click **OK** to return to the main window.

Figure 5-16. Bridge Control Panel View




7. Sample data read:

   a. Reading raw count and baseline of P1[6]/BTN0:

   i. Send I2C write instruction W 04 00 00 once.

   ii. Press the **Repeat** button to send the following I2C read instruction continuously `R 04 @Sensor_Index @1RawCount @0RawCount @1Baseline @0Baseline @ButtonStatus @SliderPosition`.

   iii. Go to the **Chart** tab to view raw count and baseline of P1[6]/BTN0.

b. Reading raw count and baseline of P1[4]/SLD0:

i. Send I2C write instruction W 04 00 05 once.

ii. Press the **Repeat** button to send the following I2C read instruction continuously `R 04 @Sensor_Index @1RawCount @0RawCount @1Baseline @0Baseline @ButtonStatus @SliderPosition`.

iii. Go to the **Chart** tab to view raw count and baseline of P1[4]/SLD0.

**Note** See CapSense Sensor Data on page 46 for information on how to view raw count and baseline data of other CapSense button and slider segments.

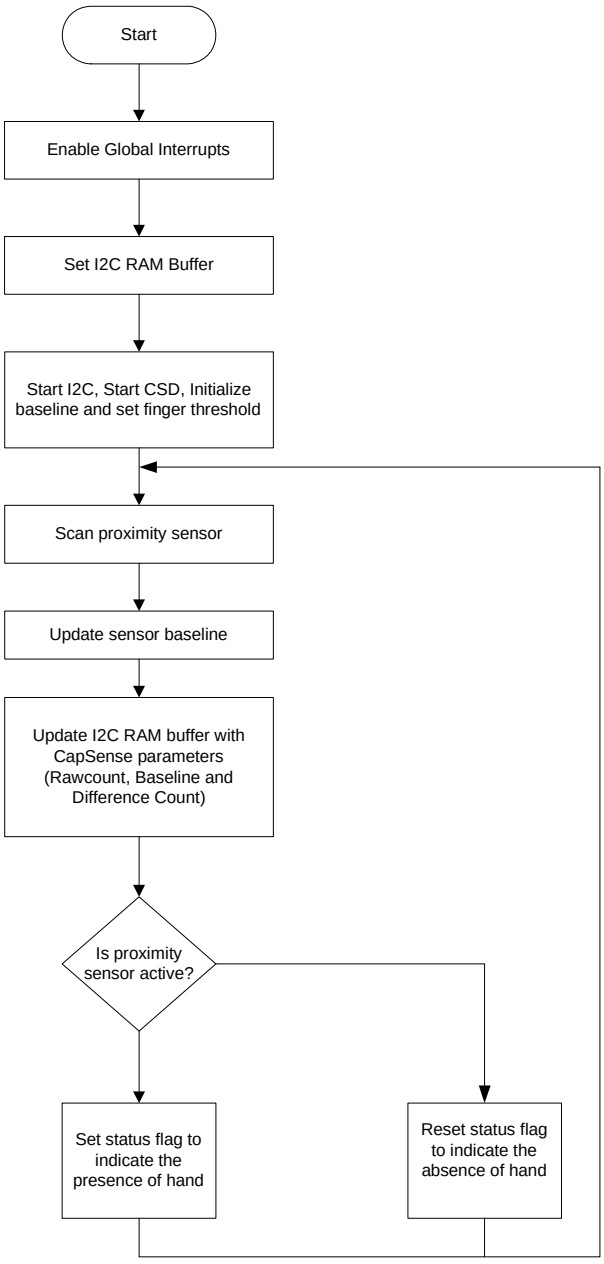
### 5.2.7 Tuning for Overlay

The code example accompanying the kit is not tuned with overlay. For the code example to work with the 1.5-mm and 3-mm acrylic overlays, the CSD User Module parameters must be adjusted. See the Tuning section in the user module datasheet for details; to select the datasheet, right-click on the CSD User Module listed in Workspace Explorer.

## 5.3 Proximity Sensing Project (CY8C21x34)

This project demonstrates how to implement proximity sensing using a wire loop. When the user's hand moves towards the wire loop, the "Status" variable is set and when the hand moves away from the sensor, it gets reset. This can be observed on Bridge Control Panel (BCP).

Figure 5-17. Firmware Flow

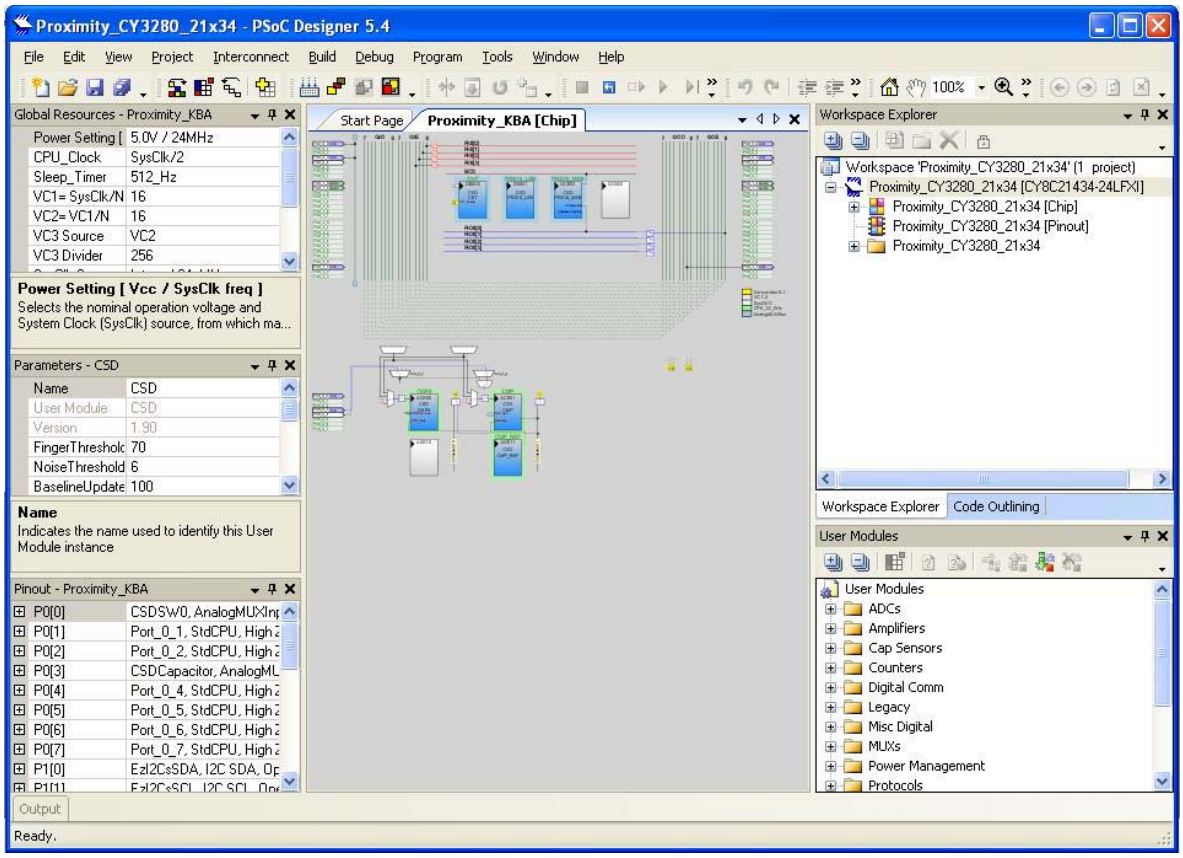



### 5.3.1 Loading Proximity Sensing Project

1. Open PSoC Designer™
2. In the **Start** page, go to **File > Open Project/Workspace**
3. Navigate to the project directory `<Install_Directory>\CY3280-BK1\<version>\Firmware\`
4. Move the Firmware folder to a writable directory and then open it
5. Open the folder **Proximity_CY3280_21x34**
6. Double-click **Proximity_CY3280_21x34.app**

The project opens in the **Chip Editor** view. All project files are in the **Workspace Explorer**.

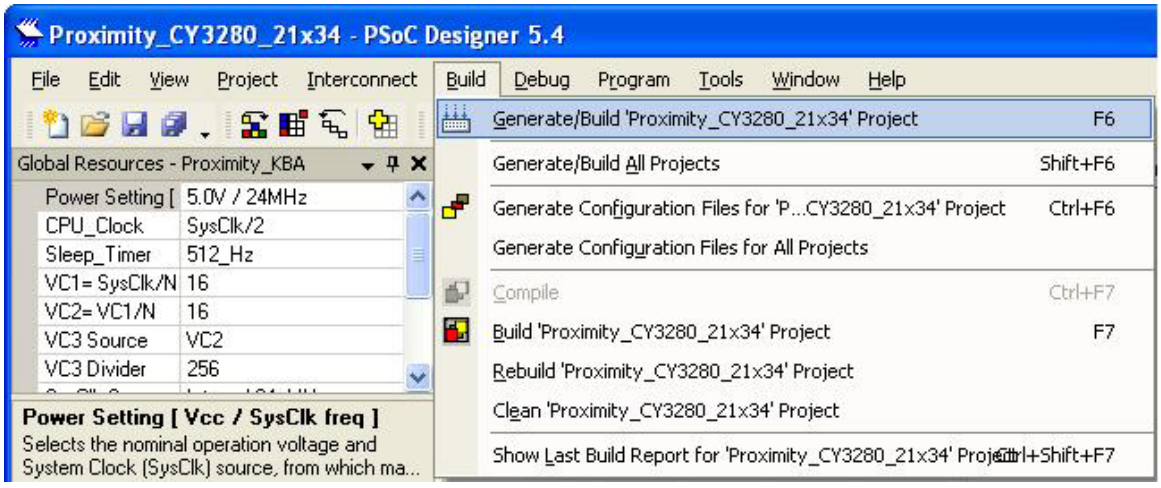
Figure 5-18. PSoC Designer Chip Editor View




## 5.3.2 Building Proximity Sensing Project

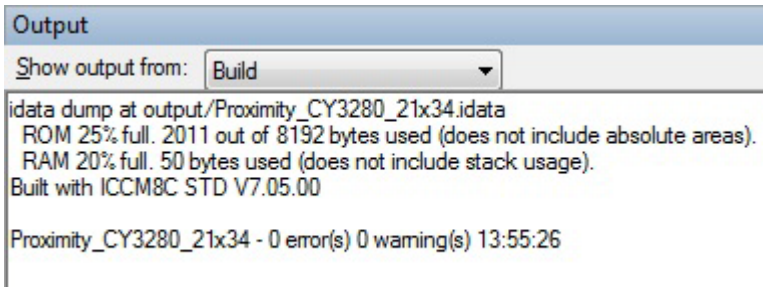
Select **Build > Generate/Build Proximity_CY3280_21x34 Project**.

Figure 5-19. Build Project




PSoC Designer builds the project and displays comments in the Output window. When you see the message that the project is built with 0 errors and 0 warnings, you are ready to program the device.

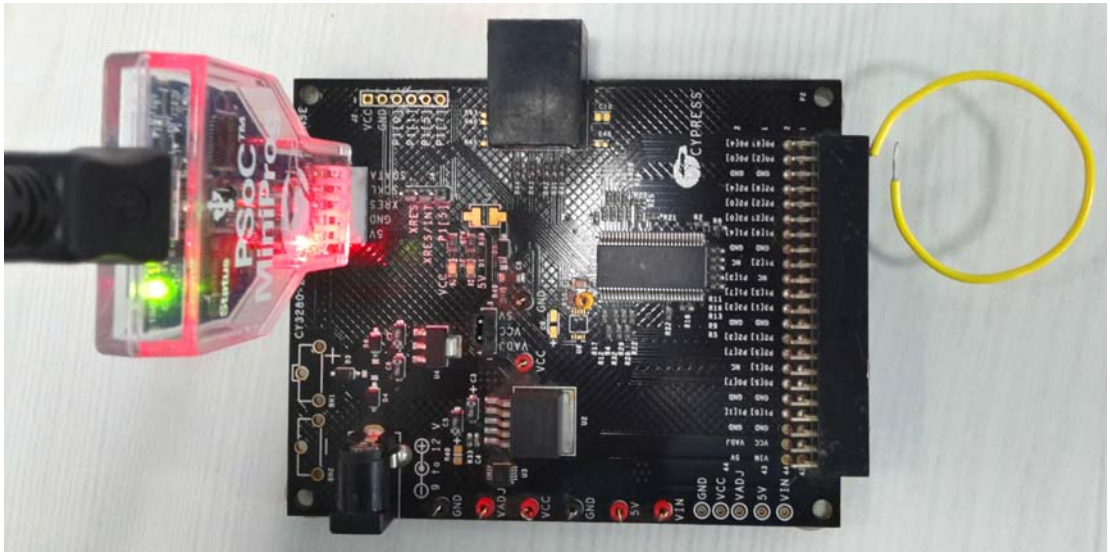
Figure 5-20. Output Window




### 5.3.3 Setting up the Board

1. In the CY3280-21x34 board, place the jumper on header J1 to short pins 2 and 3. This setting allows the CapSense controller to be powered from ISSP connector J3.
2. In the CY3280-21x34 board, place the jumper on header J4 to short pins 1 and 2. This setting routes the XRES pin of the CapSense controller to pin 3 of the ISSP connector J3.
3. Connect your computer to the CY3280-21x34 Universal CapSense Controller board's ISSP connector J3 using MiniProg1 and a USB cable. Connect a wire loop (10-cm circumference) to P0[0] on the P2 connector of the CY3280-21x34 kit as shown in the Figure 5-21.
   **Note:** MiniProg3 can be used as an alternative to MiniProg1 (to program) the CY3240 I2USB board (I2C USB bridge).

Figure 5-21. MiniProg1 Connection



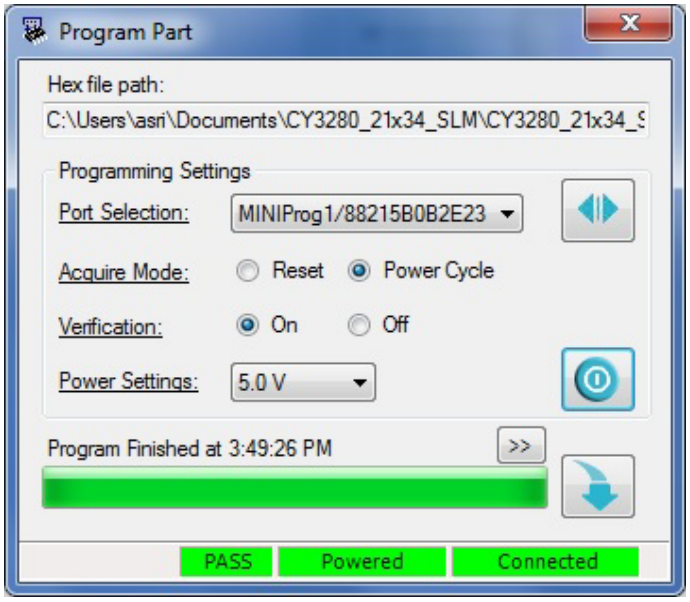
### 5.3.4 Programming Proximity Sensing Project

1. Open **Program Part** in PSoC Designer by selecting **Program > Program Part**.
2. In the **Program Part** window:
   a. Select MiniProg3 in the Port Selection box.
   b. Set Acquire Mode to Power Cycle.
   c. Set Verification to ON. This ensures that the downloaded checksum matches the actual checksum.
   d. Set Power Settings to 5.0 V.

e. Click the program arrow to program the device.

3. Wait until programming is completed

Figure 5-22. Program Part View

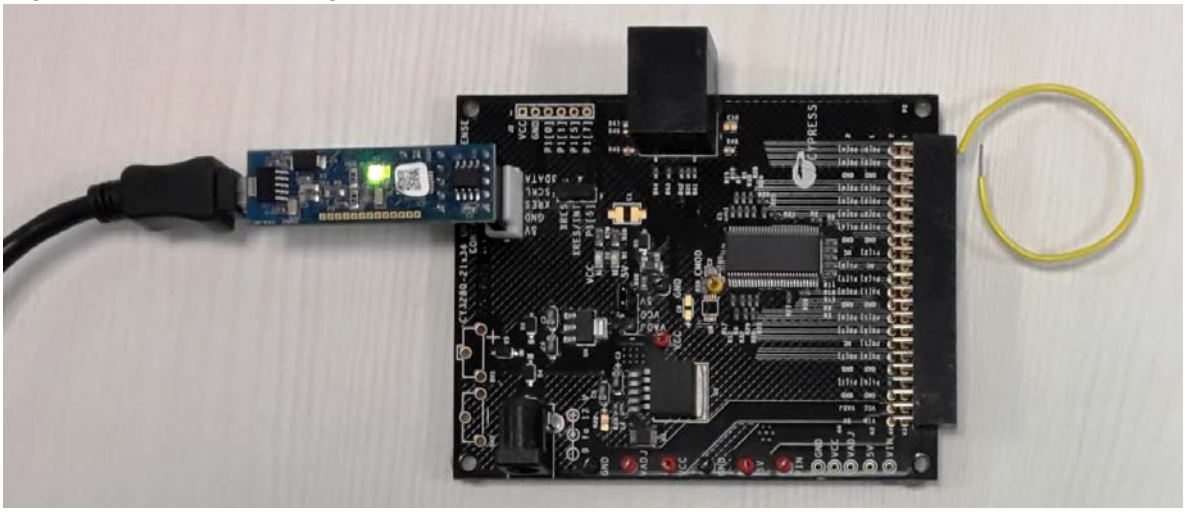



## 5.3.5 Verify Proximity Sensing Project and Read Data over I2C

Follow these steps to set up the Bridge Control Panel for reading the CapSense parameters.

1. Connect your computer to the CY3280-21x34 Universal CapSense Controller board's ISSP connector J3 using the CY3240 I2USB (I2C-USB bridge) and a USB cable, as shown in Figure 5-23.

Figure 5-23. Connect Using CY3240 I2USB



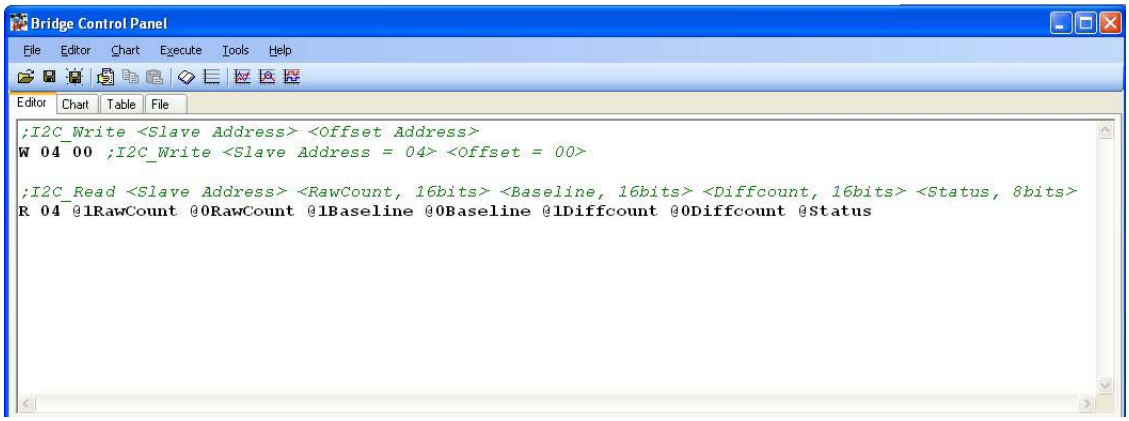
2. Go to **Start > Cypress > Open Bridge Control Panel.**

   **Note** Bridge Control Panel is installed as part of the PSoC Designer installation process.

3. Select the MiniProg3 device from the **Connected I2C/SPI-USB converters:** window.
4. Power the CY3280-21x34 CapSense Controller board at 5 V.

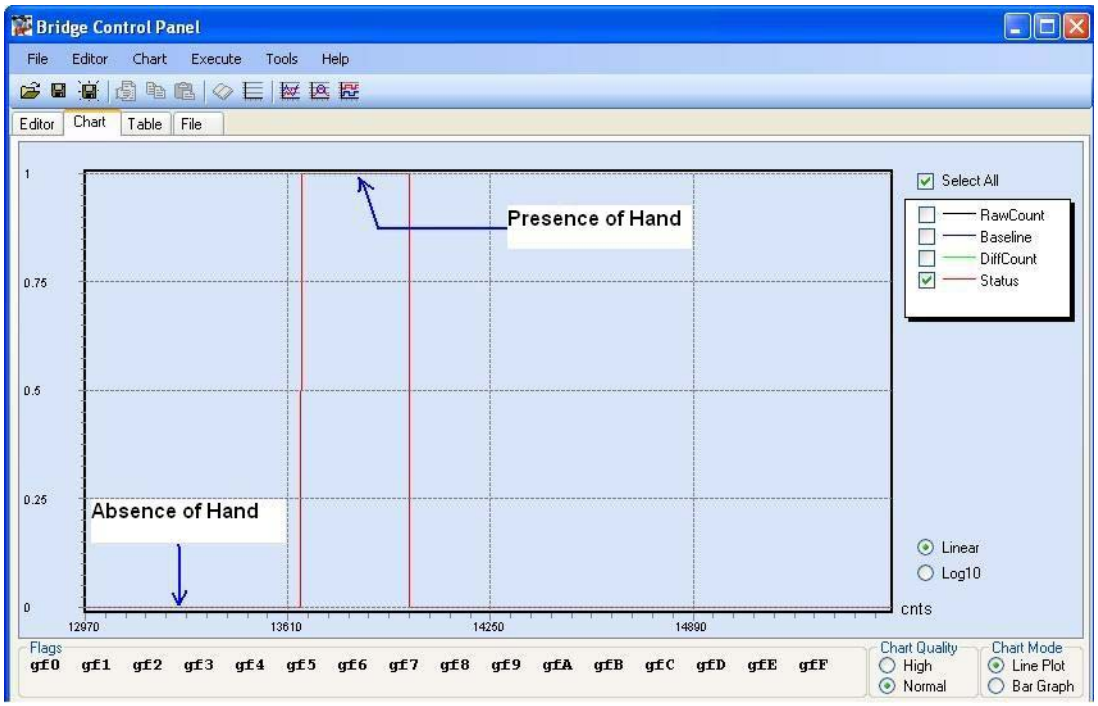
5. Select **File > Open File. Load CY3280-21x34-ProxDet.iic** from `<Install_Directory>\CY3280-BK1\<version>\Firmware\CY3240_I2USB_Configuration files`.
6. Select **Charts > Variable Settings**. Load *CY3280-21x34-ProxDet.ini* from `<Install_Directory>\CY3280-BK1\<version>\Firmware\CY3240_I2USB_Configuration files`
7. Click **OK** to return to the main window.

Figure 5-24. Bridge Control Panel View



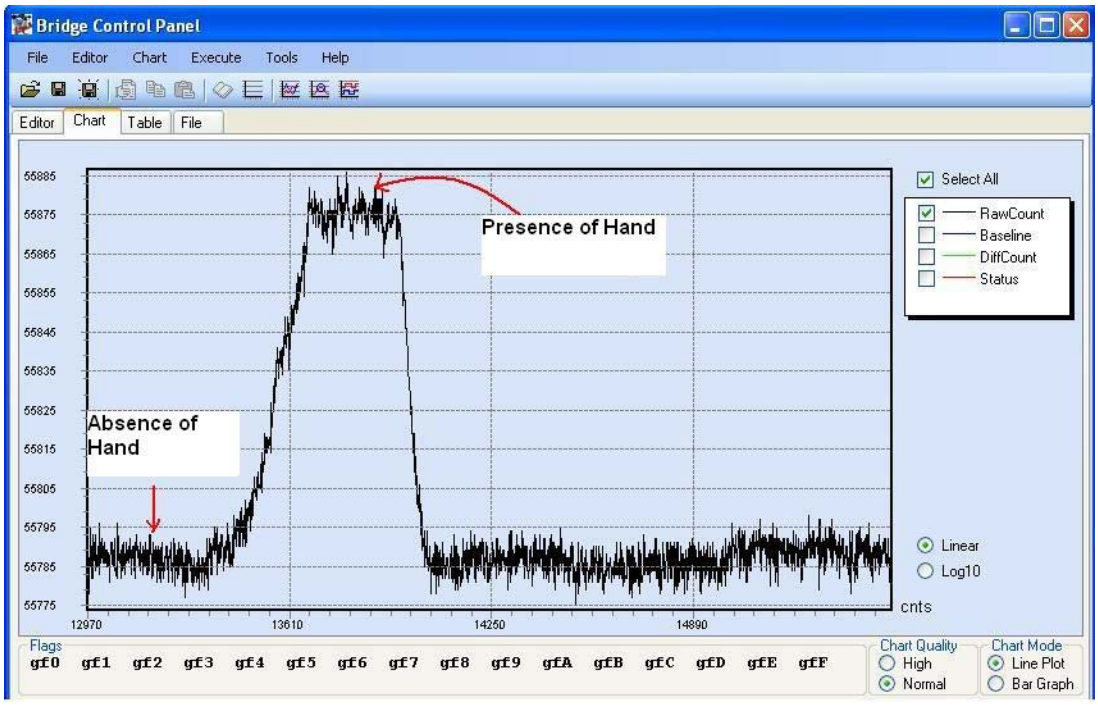

8. Keep the cursor on the first command (w 04 0) in the Editor window and press Enter.
9. Keep the cursor on the second command line in the Editor window and click **Repeat**.
10. Click the **Chart** tab on the BCP and select the plot **Status** listed in the top right corner.
11. Bring the hand towards the wire loop and observe in the BCP that the status variable becomes '1' as shown in Figure 5-25.

Figure 5-25. Status Variable on Bridge Control Panel




12. Deselect the Status plot and select the plot RawCount to see the profile of Raw counts shown in Figure 5-26.

Figure 5-26. Raw Count Profile



### 5.3.6 Proximity Tuning Steps

Use the following steps to tune the CapSense system for proximity detection.

1. Determining Proximity Distance
   For reliable proximity detection, the SNR needs to be 5:1. Follow these steps to determine the proximity distance.
   a. Find the noise count.
   b. Calculate the signal count that is required to achieve a 5:1 SNR (Signal Count = 5*Noise Count).
   c. Bring the hand towards the wire sensor until the signal count reaches the value calculated in Step (b). The present distance between the wire sensor and the hand is called the proximity distance.
   **Note:** Refer to *Section 4.1.1, "Signal, Noise, and SNR"* in the CY8C21x34/B CapSense Design Guide for more information about SNR calculation.
2. Determining CapSense Sigma Delta (without Prescaler) User Module (UM) parameters for proximity detection. The following steps can be used to determine the CapSense Sigma Delta (CSD) UM parameters for proximity detection.
   a. Find the peak Difference Count from the BCP when there is no hand present.
   b. Find the Peak Difference Count from the BCP when the hand is present at the proximity distance calculated above.
   c. Set the **Finger Threshold** parameter to 60 percent of the Difference Count observed in Step b (when the hand is present).
   d. Set the **Noise Threshold** parameter to 40 percent of the Difference Count observed in Step a (when no hand is present).
   e. Set **Baseline Update Threshold** to 100.
   f. Set **Sensor Autoreset** to **Disabled**.
   g. Set **Hysteresis** to 15 percent of the Difference Count observed in Step b (when the hand is present).
   h. Set **Negative Noise Threshold** equal to **Noise Threshold**.
   i. Set **Scanning Speed** to **Slow**.
   j. Set **Resolution** to **16**.
   k. Set **Ref Value** to **1**.
   l. Leave all the other parameters as their default values.

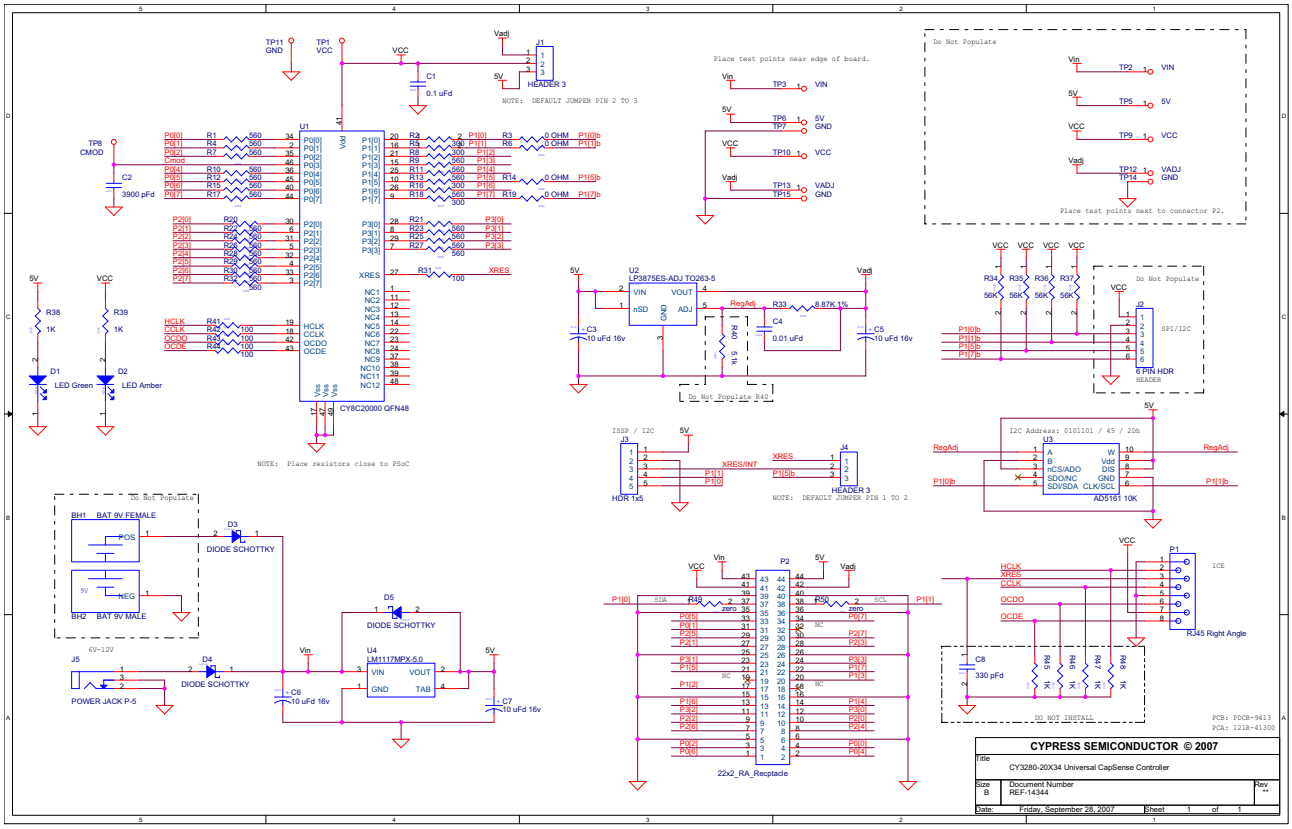
**Note:** Click on the tab **Table** in the BCP to observe the Difference count values.

# A. Appendix

The schematic, board layouts, and bill of materials (BOM) are available on the kit DVD or at the following location: `<Install_directory>:\Cypress\CY3280-BK1\<version>\Hardware`.

## A.1 CY3280-20x34 Universal CapSense Controller Board

### A.1.1 Board Schematic



### A.1.2 Board Layout

Figure A-1. Primary Side

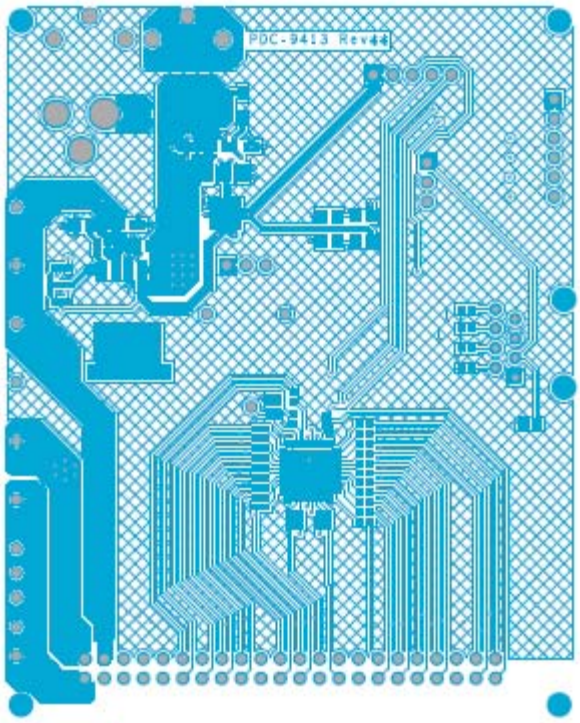
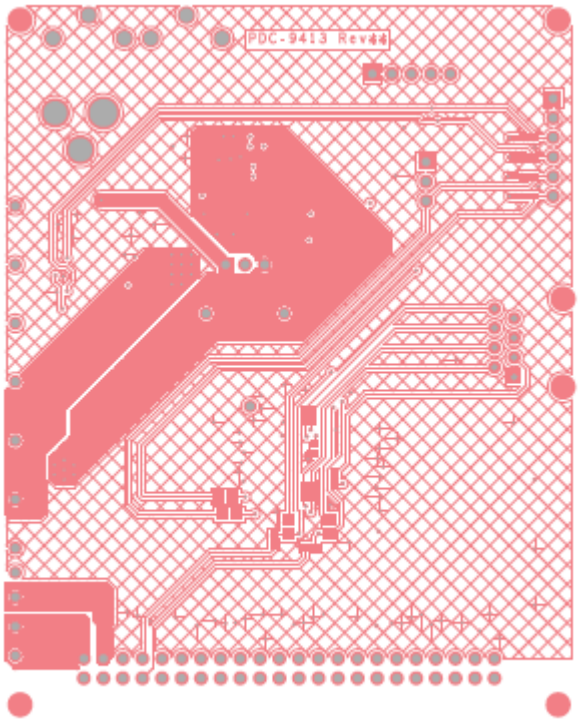


Figure A-2. Secondary Side

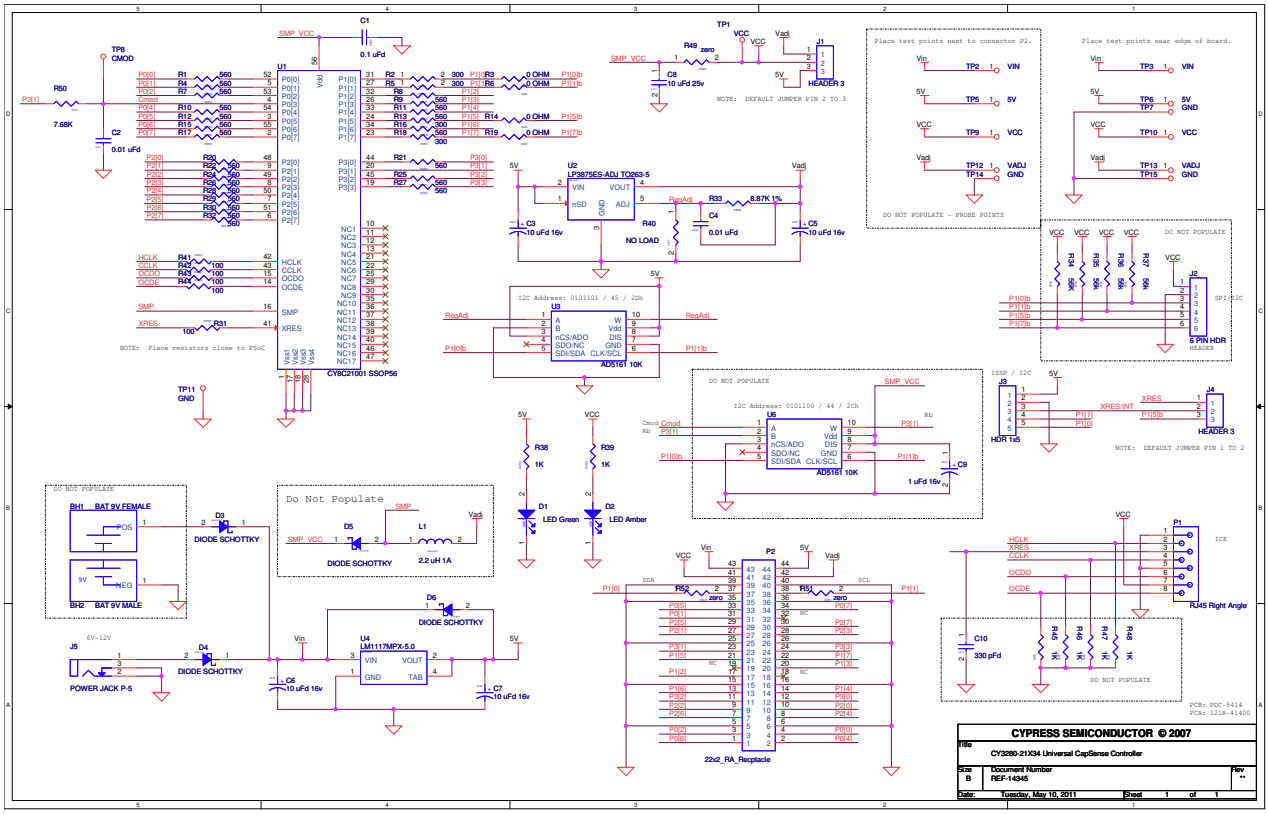


## A.1.3 Bill of Materials

| Item | Qty. | Reference | Part | Manufacturer | Mfr. Part No. |
|---|---|---|---|---|---|
| 1 | 1 | | CY3280-20x34 PCB | Cypress | |
| 2 | 2 | C4,C1 | CAP 10000PF 16V CERAMIC 0402 SMD | Panasonic - ECG | ECJ-0EB1C103K |
| 3 | 1 | C2 | CAP 3900PF 50V CERAMIC 0805 SMD | Panasonic - ECG | ECJ-2VB1H392K |
| 4 | 4 | C3,C5,C6,C7 | CAP 10UF 16V TANTALUM 10% 3216 | AVX | TAJA106K016R |
| 5 | 1 | D1 | LED GREEN Clear 0805 SMD | LITE-ON Inc | LTST-C170GKT |
| 6 | 1 | D2 | LED AMBER Clear 0805 SMD | LITE-ON Inc | LTST-C170AKT |
| 7 | 3 | D3,D4,D5 | DIODE SCHOTTKY 0.5A 20V SOD-123 | Fairchild Semiconductor | MBR0520L |
| 8 | 1 | J3 | CONN HEADER 5POS 0.1 VERT KEYED | Molex | 22-23-2051 |
| 9 | 2 | J1,J4 | CONN HEADER VERT 3POS .100 30AU | AMP Division of TYCO | 87220-3 |
| 10 | 1 | J5 | CONN 2.1MM PWRJACK RT ANGLE PCB | Switchcraft | RAPC722X |
| 11 | 1 | P2 | CONN FMALE 44POS DL .1" R/A GOLD | Sullins Electronics Corp. | PPPC222LJBN-RC |
| 12 | 23 | R1,R4,R7,R8,R9,R10,R11 | RES 560 OHM 1/16W 5% 0402 SMD | Yageo Corporation | RC0402JR-07560RL |
| | | R12,R16,R17,R15, | | | |
| | | R20,R21,R22,R23,R24,R25 | | | |
| | | R26,R27,R28,R29,R30,R32 | | | |
| 13 | 4 | R2,R5,R13,R18 | RES 300 OHM 1/16W 5% 0402 SMD | Yageo Corporation | RC0402JR-07300RL |
| 14 | 4 | R3,R6,R14,R19 | RES ZERO OHM 1/16W 5% 0603 SMD | Yageo Corporation | RC0402JR-070RL |
| 15 | 5 | R31,R41,R42,R43,R44 | RES 100 OHM 1/16W 5% 0402 SMD | Rohm | MCR01MZPJ101 |
| 16 | 1 | R33 | RES 8.87K OHM 1/16W 1% 0402 SMD | Panasonic - ECG | ERJ-2RKF8871X |
| 17 | 2 | R38,R39 | RES 1K OHM 1/10W 5% 0805 SMD | Panasonic - ECG | ERJ-6GEYJ102V |
| 18 | 4 | R34,R35,R36,R37 | RES 56k OHM 1/16W 5% 0402 SMD | Panasonic - ECG | ERJ-2GEJ563X |
| 19 | 2 | R49,R50 | RES ZERO OHM 1/16W 0402 SMD | Panasonic - ECG | ERJ-2GE0R00X |
| 20 | 3 | TP7,TP11,TP15 | TEST POINT 43 HOLE 65 PLATED BLACK | Keystone Electronics | 5001 |
| 21 | 5 | TP1,TP3,TP6,TP10,TP13 | TEST POINT 43 HOLE 65 PLATED RED | Keystone Electronics | 5000 |
| 22 | 1 | TP8 | TEST POINT 43 HOLE 65 PLATED ORANGE | Keystone Electronics | 5003 |
| 23 | 1 | U1 | IC, 48 QFN PSoC OCD | Cypress Semiconductor | CY8C20000 |
| 24 | 1 | U2 | IC REG LDO 1.5A ADJ VOLT TO263-5 | National Semiconductor | LP3875ES-ADJ/ NOPB |
| 25 | 1 | U3 | IC DGTL POT SPI 10K 10-MSOP | Analog Devices Inc | AD5161BRMZ10 |
| 26 | 1 | U4 | IC REG 5.0V 800MA LDO SOT-223 | National Semiconductor | LM1117MPX-5.0 |
| Do Not Populate | | | | | |
| 27 | 1 | BH1 | BATTERY HOLDER 9V Female PC MT | Keystone Electronics | 594 |
| 28 | 1 | BH2 | BATTERY HOLDER 9V Male PC MT | Keystone Electronics | 593 |
| 29 | 1 | C8 | CAP 330PF 100V CERAMIC X7R 0603 | Panasonic - ECG | ECJ-1VB2A331K |
| 30 | 1 | P1 | CONN RJ45 8-8 MOD JACK UNSHIELD RIGHT ANGLE | AMP Division of TYCO | 557785-1 |
| 31 | 1 | R40 | RES 5k OHM 1/8W 5% 0805 SMD | Panasonic - ECG | ERJ-6GEYJ512V |
| 32 | 4 | R45,R46,R47,R48 | RES 1K OHM 1/10W 5% 0402 SMD | Panasonic - ECG | ERJ-2GEJ102X |
| 33 | 1 | J2 | CONN HEADER VERT 6POS .100 TIN | Molex/Waldom Electron-ics | 22-28-4060 |
| 34 | 1 | TP14 | TEST POINT 43 HOLE 65 PLATED BLACK | Keystone Electronics | 5001 |
| 35 | 4 | TP2,TP5,TP9,TP12 | TEST POINT 43 HOLE 65 PLATED RED | Keystone Electronics | 5000 |
| Special Jumper Installation Instructions | | | | | |
| 36 | 1 | | Install jumper across pins 2 and 3 of J1 | Sullins Electronics Corp. | STC02SYAN |
| 37 | 2 | | Install jumper across pins 1 and 2 of J4 | Sullins Electronics Corp. | STC02SYAN |
| Install On Bottom of PCB As Close To Corners As Possible | | | | | |
| 38 | 4 | n/a | BUMPER CLEAR.370X.19" CYLINDER | Richco Plastic Co | RBS-35 |

## A.2 CY3280-21x34 Universal CapSense Controller Board

### A.2.1 Board Schematic



### A.2.2 Board Layout

Figure A-3. Primary Side

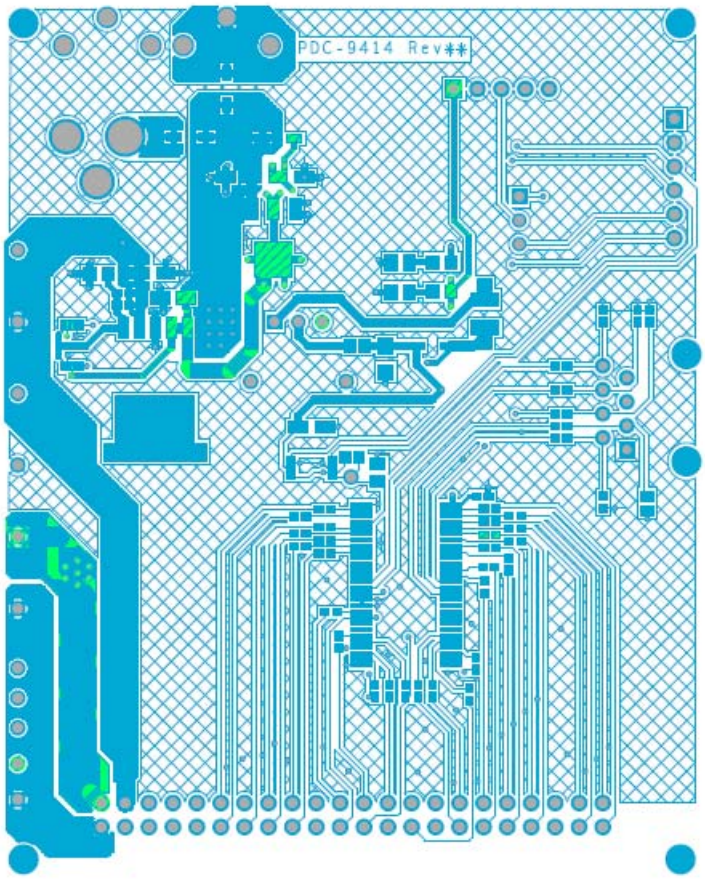
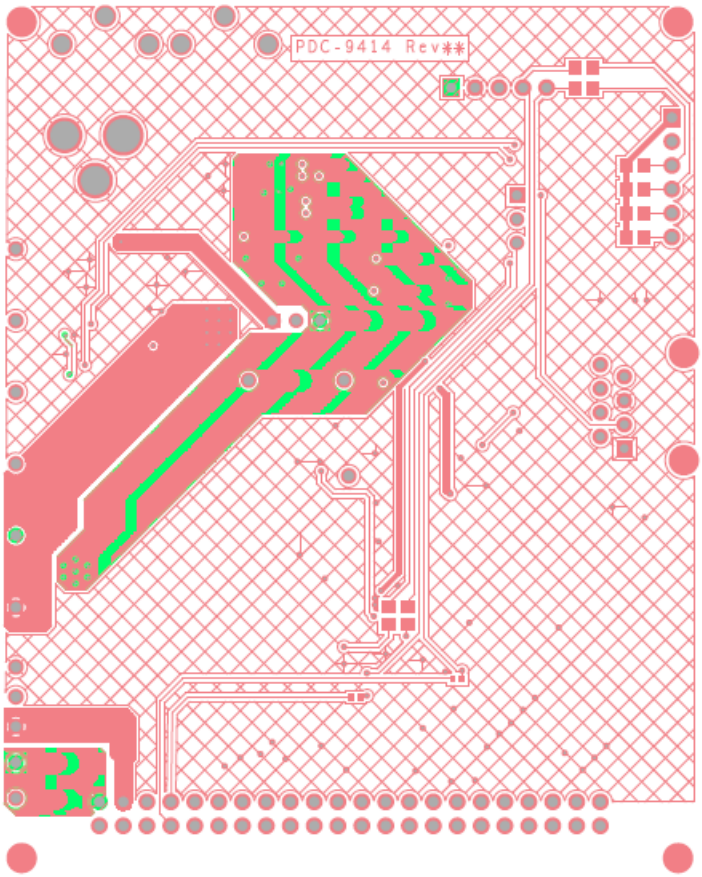


Figure A-4. Secondary Side

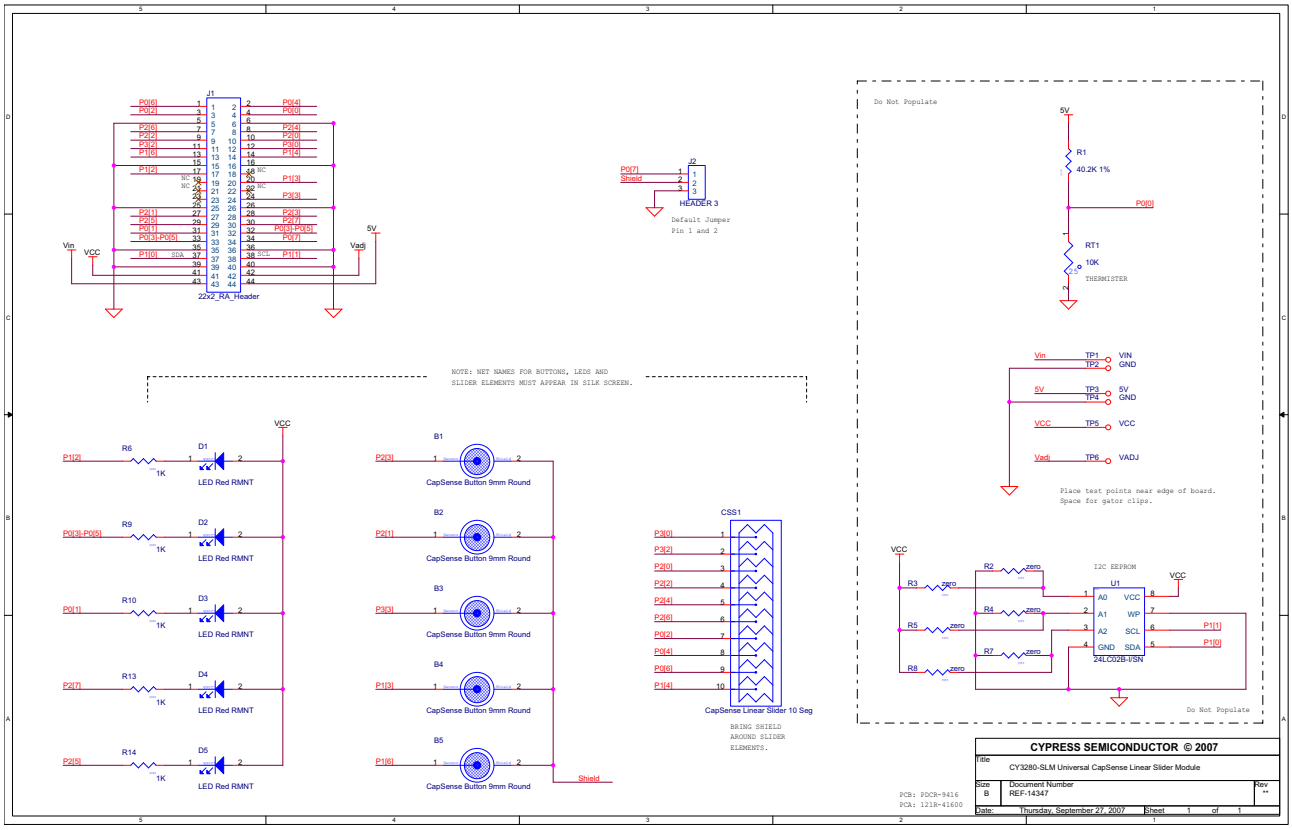


## A.2.3 Bill of Materials

| Item | Qty. | Reference | Part | Manufacturer | Mfr. Part No. |
|---|---|---|---|---|---|
| 1 | 1 | | CY3280-21x34 PCB Rev** | Cypress Semiconductor | PDC-9414** |
| 2 | 2 | C1,C4 | CAP 10000PF 16V CERAMIC 0402 SMD | Panasonic - ECG | ECJ-0EB1C103K |
| 3 | 1 | C2 | CAP 10000PF 50V CERM CHIP 0805 | Panasonic - ECG | ECJ-2VB1H103K |
| 4 | 4 | C3,C5,C6,C7 | CAP 10UF 16V TANTALUM 10% 3216 | AVX | TAJA106K016R |
| 5 | 1 | C8 | CAP CERAMIC 10UF 25V X5R 1206 | Panasonic - ECG | ECJ-3YB1E106M |
| 6 | 1 | D1 | LED GREEN Clear 0805 SMD | LITE-ON Inc | LTST-C170GKT |
| 7 | 1 | D2 | LED AMBER Clear 0805 SMD | LITE-ON Inc | LTST-C170AKT |
| 8 | 4 | D3,D4,D5,D6 | DIODE SCHOTTKY 0.5A 20V SOD-123 | Fairchild Semiconductor | MBR0520L |
| 9 | 2 | J1,J4 | CONN HEADER VERT 3POS .100 30AU | AMP Division of TYCO | 87220-3 |
| 10 | 1 | J3 | CONN HEADER 5POS 0.1 VERT KEYED | Molex | 22-23-2051 |
| 11 | 1 | J5 | CONN 2.1MM PWRJACK RT ANGLE PCB | Switchcraft | RAPC722X |
| 12 | 1 | P2 | CONN FMALE 44POS DL .1" R/A GOLD | Sullins Electronics Corp. | PPPC222LJBN-RC |
| 13 | 22 | R1,R4,R7,R8,R9,R10,R11, R12, R15, R16,R17, R20, R21,R22,R24, R25,R26, R27,R28,R29,R30,R32 | RES 560 OHM 1/16W 5% 0402 SMD | Yageo Corporation | RC0402JR-07560RL |
| 14 | 4 | R2,R5,R13,R18 | RES 300 OHM 1/16W 5% 0402 SMD | Yageo Corporation | RC0402JR-07300RL |
| 15 | 6 | R3,R6,R14,R19,R51,R52 | RES ZERO OHM 1/16W 5% 0402 SMD | Panasonic - ECG | ERJ-2GE0R00X |
| 16 | 5 | R31,R41,R42,R43,R44 | RES 100 OHM 1/16W 5% 0402 SMD | Rohm | MCR01MZPJ101 |
| 17 | 1 | R33 | RES 8.87K OHM 1/16W 1% 0402 SMD | Panasonic - ECG | ERJ-2RKF8871X |
| 18 | 2 | R38,R39 | RES 1K OHM 1/10W 5% 0805 SMD | Panasonic - ECG | ERJ-6GEYJ102V |
| 19 | 1 | R49 | RES ZERO OHM 1/16W 5% 0603 SMD | Panasonic - ECG | ERJ-3GEY0R00V |
| 20 | 4 | R34,R35,R36,R37 | RES 56k OHM 1/16W 5% 0402 SMD | Panasonic - ECG | ERJ-2GEJ563X |
| 21 | 3 | TP7,TP11,TP15, | TEST POINT 43 HOLE 65 Plated BLACK | Keystone Electronics | 5001 |
| 22 | 5 | TP1,TP3,TP6,TP10,TP13 | TEST POINT 43 HOLE 65 Plated RED | Keystone Electronics | 5000 |
| 23 | 1 | TP8 | TEST POINT 43 HOLE 65 Plated ORANGE | Keystone Electronics | 5003 |
| 24 | 1 | U2 | IC REG LDO 1.5A ADJ VOLT TO263-5 | National Semiconductor | LP3875ES-ADJ/NOPB |
| 25 | 1 | U3 | IC DGTL POT SPI 10K 10-MSOP | Analog Devices Inc | AD5161BRMZ10 |
| 26 | 1 | U4 | IC REG 5.0V 800MA LDO SOT-223 | National Semiconductor | LM1117MPX-5.0 |
| 27 | 1 | U5 | IC, 56 SSOP PSoC OCD | Cypress Semiconductor | CY8C21001 |
| 28 | 1 | R50 | RES 7.68K OHM 1/10W 1% 0603 SMD | Panasonic - ECG | ERJ-3EKF7681V |
| Do Not Populate | | | | | |
| 29 | 1 | BH1 | BATTERY HOLDER 9V Female PC MT | Keystone Electronics | 594 |
| 30 | 1 | BH2 | BATTERY HOLDER 9V Male PC MT | Keystone Electronics | 593 |
| 31 | 1 | C9 | CAPACITOR 1.0UF/16V TEH SER SMD | Panasonic - ECG | ECS-H1CY105R |
| 32 | 1 | P1 | CONN RJ45 8-8 MOD JACK UNSHIELD RIGHT ANGLE | AMP Division of TYCO | 557785-1 |
| 33 | 1 | U6 | IC DGTL POT SPI 10K 10-MSOP | Analog Devices Inc | AD5161BRMZ10 |
| 34 | 1 | L1 | INDUCTOR 2.2UH 1000MA 1812 10% | EPCOS Inc | B82432T1222K |
| 35 | 1 | R40 | RES 5.1K 0805 SMD | Panasonic - ECG | ERJ-6GEYJ512V |
| 36 | 1 | C10 | CAP 330PF 100V CERAMIC X7R 0603 | Panasonic - ECG | ECJ-1VB2A331K |
| 37 | 4 | R45,R46,R47,R48 | RES 1.0K OHM 1/16W 5% 0402 SMD | Yageo Corporation | RC0402JR-071KL |
| 38 | 1 | J2 | CONN HEADER VERT 6POS .100 TIN | Molex/Waldom Electronics | 22-28-4060 |
| 39 | 4 | TP2,TP5,TP9,TP12 | TEST POINT 43 HOLE 65 PLATED RED | Keystone Electronics | 5000 |
| 40 | 1 | TP14 | TEST POINT 43 HOLE 65 PLATED BLACK | Keystone Electronics | 5001 |
| Special Jumper Installation Instructions | | | | | |
| 41 | 1 | | Install jumper across pins 2 and 3 of J1 | Sullins Electronics Corp. | STC02SYAN |
| 42 | 2 | | Install jumper across pins 1 and 2 of J4 | Sullins Electronics Corp. | STC02SYAN |
| Install On Bottom of PCB As Close To Corners As Possible | | | | | |
| 43 | 4 | n/a | BUMPER CLEAR.370X.19" CYLINDER | Richco Plastic Co | RBS-35 |

# A.3 CY3280-SLM Universal CapSense Linear Slider

## A.3.1 Board Schematic



### A.3.2 Board Layout

Figure A-5. Primary Side

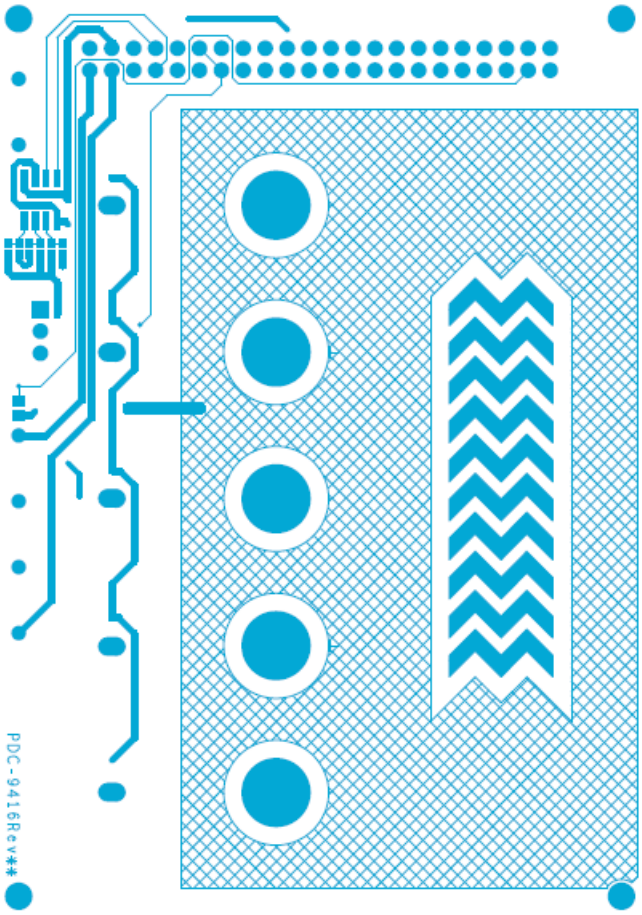
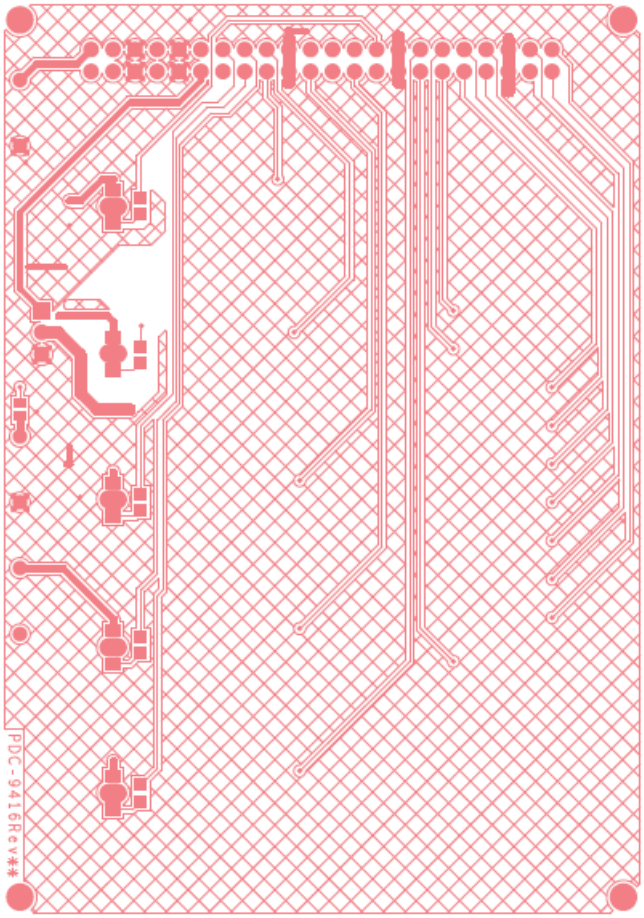


Figure A-6. Secondary Side

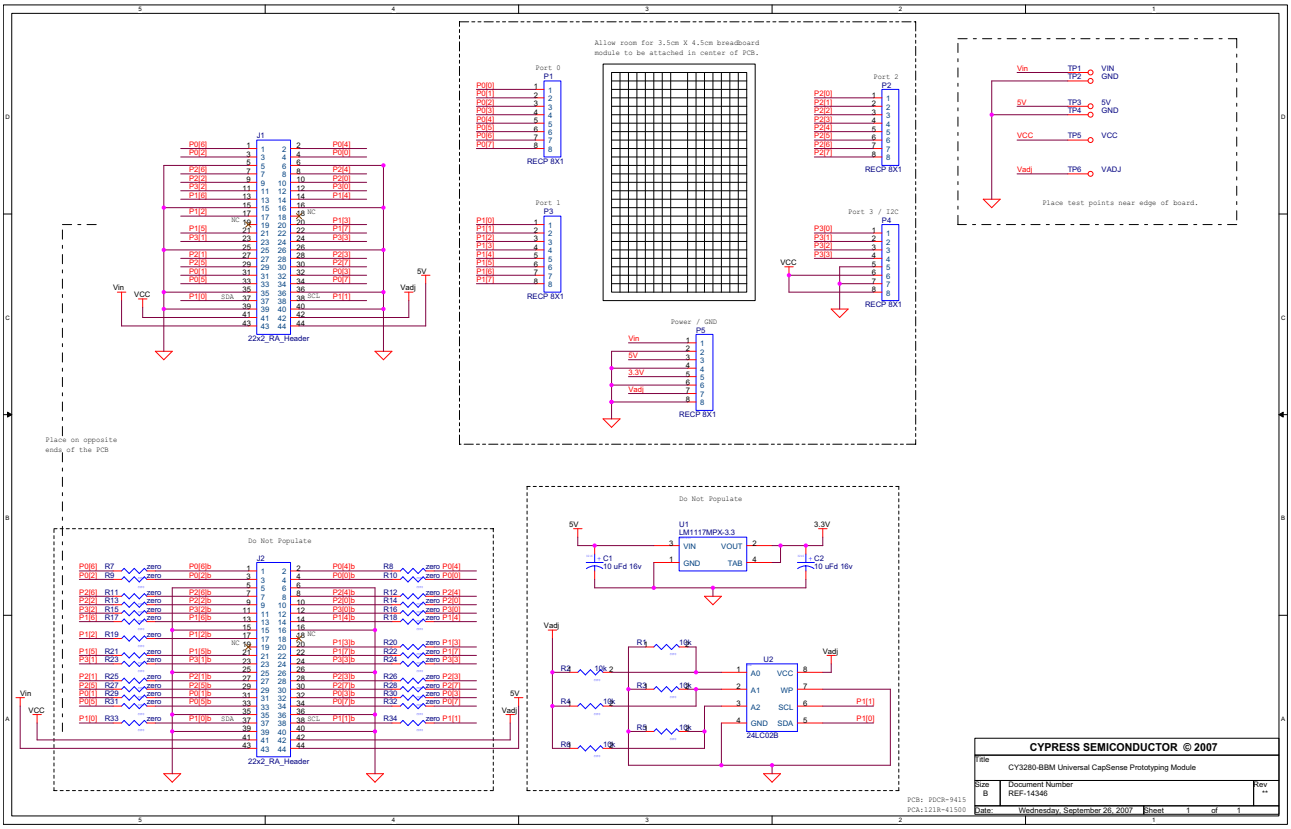


## A.3.3 Bill of Materials

| Item | Qty. | Reference | Part | Manufacturer | Mfr. Part No. |
|---|---|---|---|---|---|
| 1 | 1 | | CY3280-BBM PCB | Cypress | |
| 2 | 5 | B1,B2,B3,B4,B5 | Copper CapSense Pads | Cypress | n/a |
| 3 | 1 | CSS1 | Copper CapSense Slider | Cypress | n/a |
| 4 | 5 | D1,D2,D3,D4,D5 | LED RED CLEAR 1206 REAR MNT SMD | LITE-ON INC | LTST-C230CKT |
| 5 | 1 | J1 | CONN HEADER .100 DUAL R/A 44POS | Sullins Electronics Corp. | PBC22DBAN |
| 6 | 1 | J2 | CONN HEADER VERT 3POS .100 30AU | AMP Division of TYCO | 87220-3 |
| 7 | 5 | R6,R9,R10,R13,R14 | RES 1K OHM 1/10W 5% 0805 SMD | Panasonic - ECG | ERJ-6GEYJ102V |
| Special Jumper Installation Instructions | | | | | |
| 8 | 1 | | Install jumper across pins 2 and 3 of J2 | Sullins Electronics Corp. | STC02SYAN |
| Place on bottom of PCB as close to four corners as possible | | | | | |
| 9 | 4 | | BUMPER CLEAR.370X.19" CYLINDER | Richco Plastic Co | RBS-35 |
| Do Not Populate | | | | | |
| 10 | 1 | U1 | IC EEPROM CMOS SERIAL 256X8 SO-8 | Microchip Technology | 24LC02B-I/SN |
| 11 | 6 | R2,R3,R4,R5,R7,R8 | RES 10K OHM 1/16W 5% 0402 SMD | Panasonic - ECG | ERJ-2GEJ103X |
| 12 | 4 | TP1,TP3,TP5,TP7 | TEST POINT 43 HOLE 65 PLATED RED | Keystone Electronics | 5000 |
| 13 | 2 | TP2,TP4 | TEST POINT 43 HOLE 65 PLATED BLACK | Keystone Electronics | 5001 |
| 14 | 1 | R1 | RES 40.2K OHM 1/10W 1% 0603 SMD | Panasonic - ECG | ERJ-3EKF4022V |
| 15 | 1 | RT1 | THERMISTORS 10K OHM NTC 0805 SMD | Murata | NCP21XV103J03RA |

# A.4 CY3280-BBM Universal CapSense Controller Board

## A.4.1 Board Schematic



## A.4.2 Board Layout

Figure A-7. Primary Side

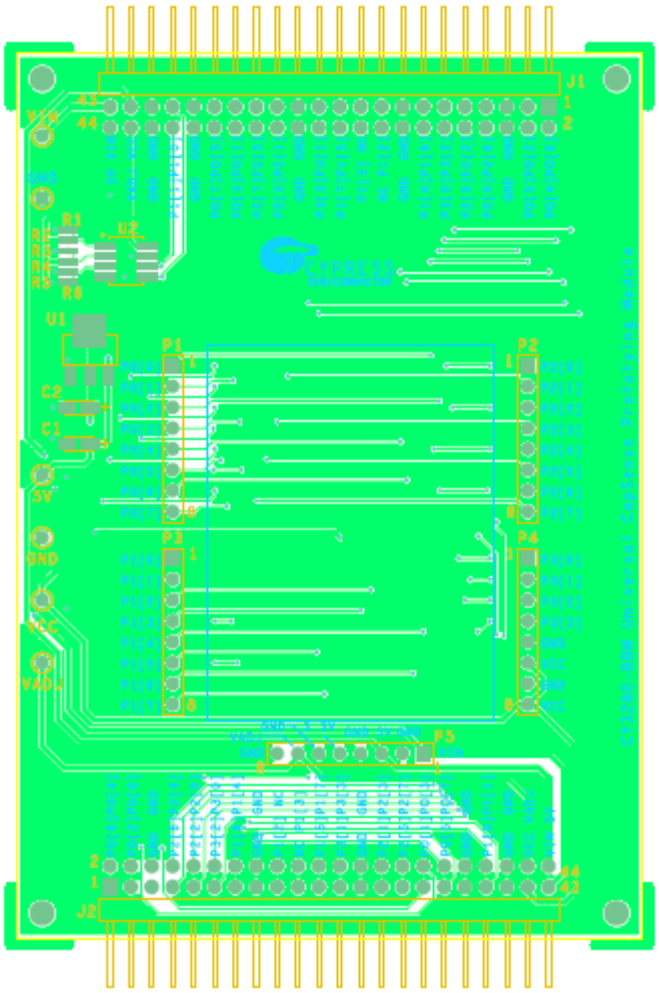
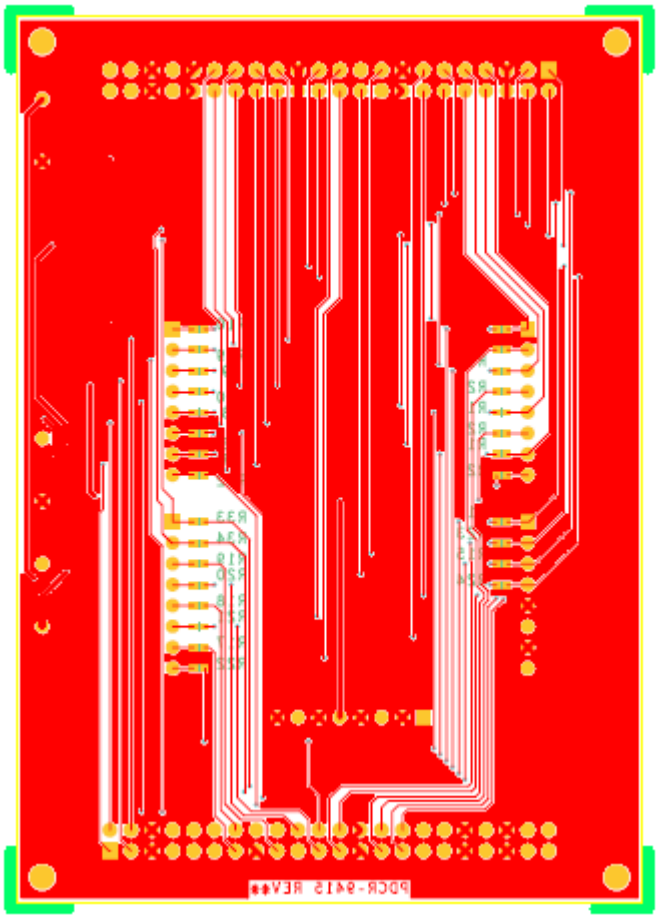


Figure A-8. Secondary Side



## A.4.3 Bill of Materials

| Item | Qty. | Reference | Part | Manufacturer | Mfr. Part No. |
|---|---|---|---|---|---|
| 1 | 1 | | PDCR-9415 CY3280-BBM | Cypress | |
| 2 | 1 | J1 | CONN HEADER .100 DUAL R/A 44POS | Sullins Electronics Corp. | PBC22DBAN |
| 3 | 5 | P1,P2,P3,P4,P5 | CONN RECT 8POS .100" VERT | 3M | 929850-01-08-RA |
| 4 | 4 | TP1,TP3,TP5,TP6 | TEST POINT 43 HOLE 65 PLATED RED | Keystone Electronics | 5000 |
| 5 | 2 | TP2,TP4 | TEST POINT 43 HOLE 65 PLATED BLACK | Keystone Electronics | 5001 |
| 6 | 1 | | TERMINAL STRIP | 3M | 923273-I |
| Do Not Install | | | | | |
| 7 | 2 | C1,C2 | CAP 10UF 16V TANTALUM 10% 3216 | AVX | TAJA106K016R |
| 8 | 1 | J2 | CONN HEADER .100 DUAL R/A 44POS | Sullins Electronics Corp. | PBC22DBAN |
| 9 | 34 | R1,R2,R3,R4,R5,R6,R7,R8, R9,R10,R11,R12,R13,R14,R 15,R16,R17,R18,R19,R20,R 21,R22,R23,R24,R25,R26,R 27,R28,R29,R30,R31,R32,R 33,R34 | RES ZERO OHM 1/16W 0402 SMD | Panasonic - ECG | ERJ-2GE0R00X |
| 10 | 1 | U1 | IC REG 3.3V 800MA LDO SOT-223 | National Semiconductor | LM1117MPX-3.3 |
| 11 | 1 | U2 | IC EEPROM CMOS SERIAL 256X8 SOIC-8 | Microchip Technology | 24LC02B |
| Place on bottom side as near to corners as possible: | | | | | |
| 12 | 4 | | BUMPER CLEAR.370X.19" CYLINDER | Richco Plastic Co | RBS-35 |

# Revision History

## Document Revision History

| Document Title: CY3280-BK1 Universal CapSense® Controller Basic Kit 1 User Guide<br>Document Number: 001-67236 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN#** | **Issue Date** | **Origin of Change** | **Description of Change** |
| ** | 3164704 | 02/08/2011 | KPOL | Initial version of kit guide. |
| *A | 3184766 | 03/07/2011 | KPOL | Updated Kit Operation chapter on page 19:<br>Updated CY3280-20x34 Universal CapSense Controller Board:<br>Updated Hardware Description:<br>Added CMOD.<br>Updated CY3280-21x34 Universal CapSense Controller Board:<br>Updated Hardware Description:<br>Added CMOD.<br>Added board layouts.<br>Minor content updates throughout the document. |
| *B | 3518224 | 02/06/2012 | RKPM | Added Getting Started chapter on page 12.<br>Added Hardware chapter on page 21.<br>Updated kit images. |
| *C | 3612452 | 05/09/2012 | RKPM | Updated Code Examples chapter on page 41:<br>Updated images and file names.<br>Updated “My First CapSense (CY8C21x34) Project” on page 47:<br>Removed “Tuning for Water Proofing”.<br>Updated Appendix chapter on page 60:<br>Updated the schematic, board layout and bill of materials. |
| *D | 4066180 | 07/16/2013 | DCHE | Updated Introduction chapter on page 5:<br>Updated “Additional Learning Resources” on page 6:<br>Updated “Application Notes”:<br>Added an application note.<br>Updated “Code Examples”:<br>Added a code example. |
| *E | 4297467 | 03/04/2013 | DCHE | No technical updates.<br>Completing Sunset Review. |
| *F | 4552678 | 10/27/2014 | DIMA | Updated Code Examples chapter on page 41:<br>Added “Proximity Sensing Project (CY8C21x34)” on page 52.<br>Updated screenshots with the latest installer images. |

| Document Title: CY3280-BK1 Universal CapSense® Controller Basic Kit 1 User Guide<br>Document Number: 001-67236 | | | | |
|---|---|---|---|---|
| **Revision** | **ECN#** | **Issue Date** | **Origin of Change** | **Description of Change** |
| *G | 4665689 | 02/25/2015 | DCHE | Updated Introduction chapter on page 5:<br>Updated “Additional Learning Resources” on page 6:<br>Updated description.<br>Removed “Application Notes”.<br>Removed “Code Examples”.<br>Removed “Datasheets”.<br>Removed “Technical Reference Manuals”.<br>Added “PSoC Designer” on page 7.<br>Added “Code Examples” on page 8.<br>Added “PSoC Designer Help” on page 10.<br>Added “Technical Support” on page 10.<br>Updated to new template. |
| *H | 5204765 | 04/13/2016 | ASRI | Updated hyperlinks across the document.<br>Updated Getting Started chapter on page 12:<br>Updated “Kit Installation” on page 12:<br>Updated description.<br>Removed figure “InstallShield Wizard”.<br>Updated Figure 2-3.<br>Removed figure “Installation Page”.<br>Updated Figure 2-4.<br>Updated “PSoC Designer” on page 15:<br>Updated description.<br>Updated Figure 2-5.<br>Updated to new template. |
| *I | 5318989 | 06/22/2016 | ASRI | Updated cross references<br>Modified board images. Modified the Output Window images in “Code Examples” on page 41. |
| **Distribution**: External<br>**Posting**: None | | | | |