

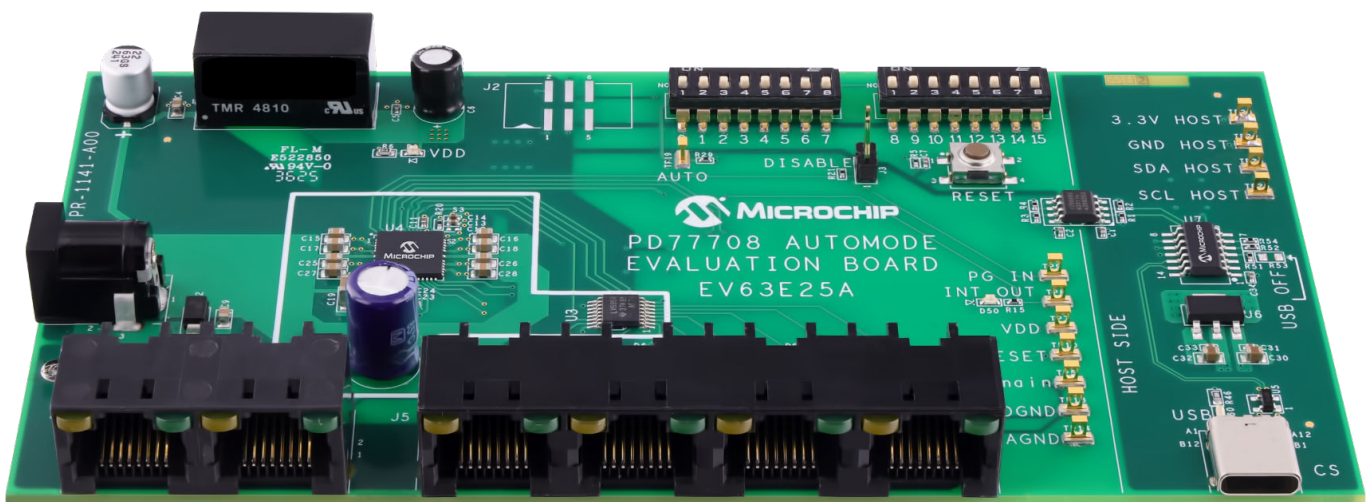
Introduction

The EV63E25A evaluation board (EVB) is based on Microchip's PD77708 PoE manager. The EV63E25A operates in Auto mode using the PD77708 and demonstrates four IEEE® 802.3bt 2-pair ports and two IEEE® 802.3bt 4-pair ports using a single PD77708T4 devices.

The PD77708 device is a part of the seventh generation IEEE 802.3bt compliant Power over Ethernet (PoE) Power Sourcing Equipment (PSE) family from Microchip. This device is a fully integrated eight port PoE controller, with integrated Field Effect Transistor (FET) switches and current sense resistors. The PD77708 chipset supports IEEE 802.3af/at/bt standards, as well as legacy/pre-standard PD detection. The device is available in a 56-pin, 8 mm × 8 mm Quad flat no-lead (QFN) package.

The following figure shows the top view of the evaluation board.

Figure 1. Evaluation Board - Top View



Features

The EVB has the following features.

- Two RJ45 Gang (Contains Six RJ45 Connectors)
- Four 2-pair and Two 4-pair Ports Structured by a single PD77708T4
- Switch Domain USB-C[®] Interface to be Connected to a PC with the Microchip dedicated GUI
- Manual Reset and Disable Port Jumpers
- Six Green Color LED Status Indication, one per port
- Requires only a Single Power Source 46-57 V_{DC}
- 0°C to 40°C Operating Temperature
- RoHS Compliant

The following figures show the system block diagram and the dimensions of the evaluation board.

Figure 2. EV63E25A Evaluation Board Block Diagram

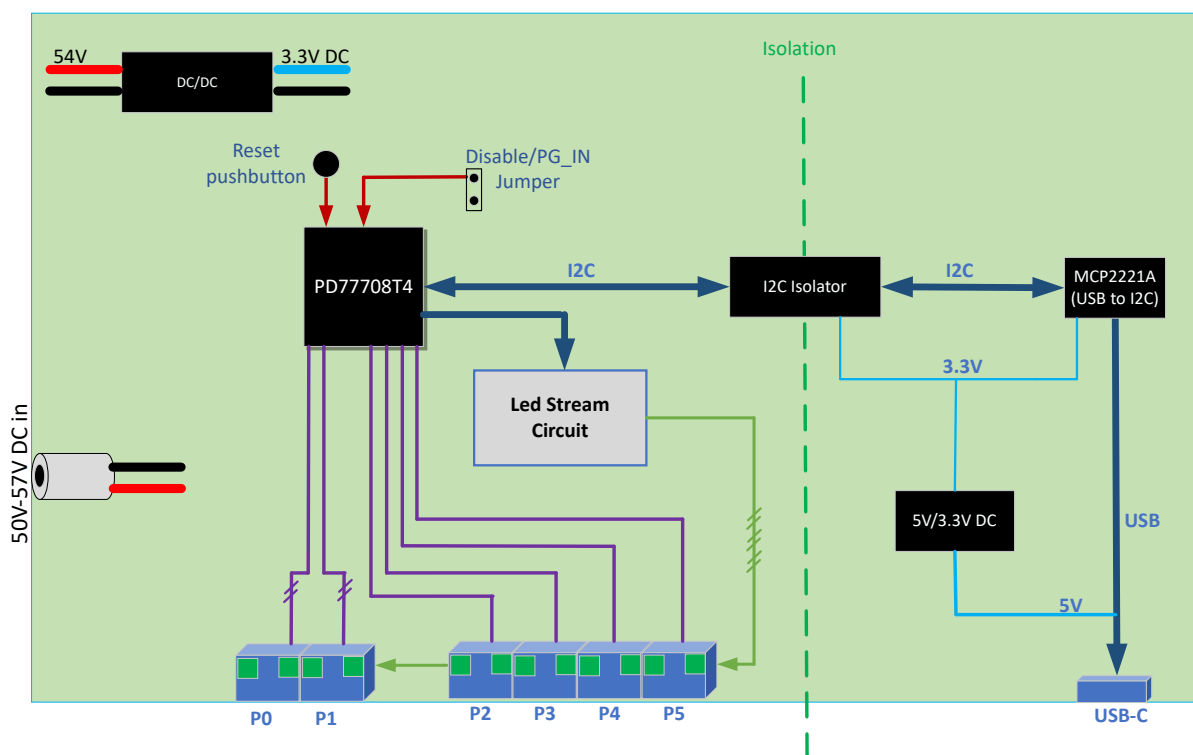
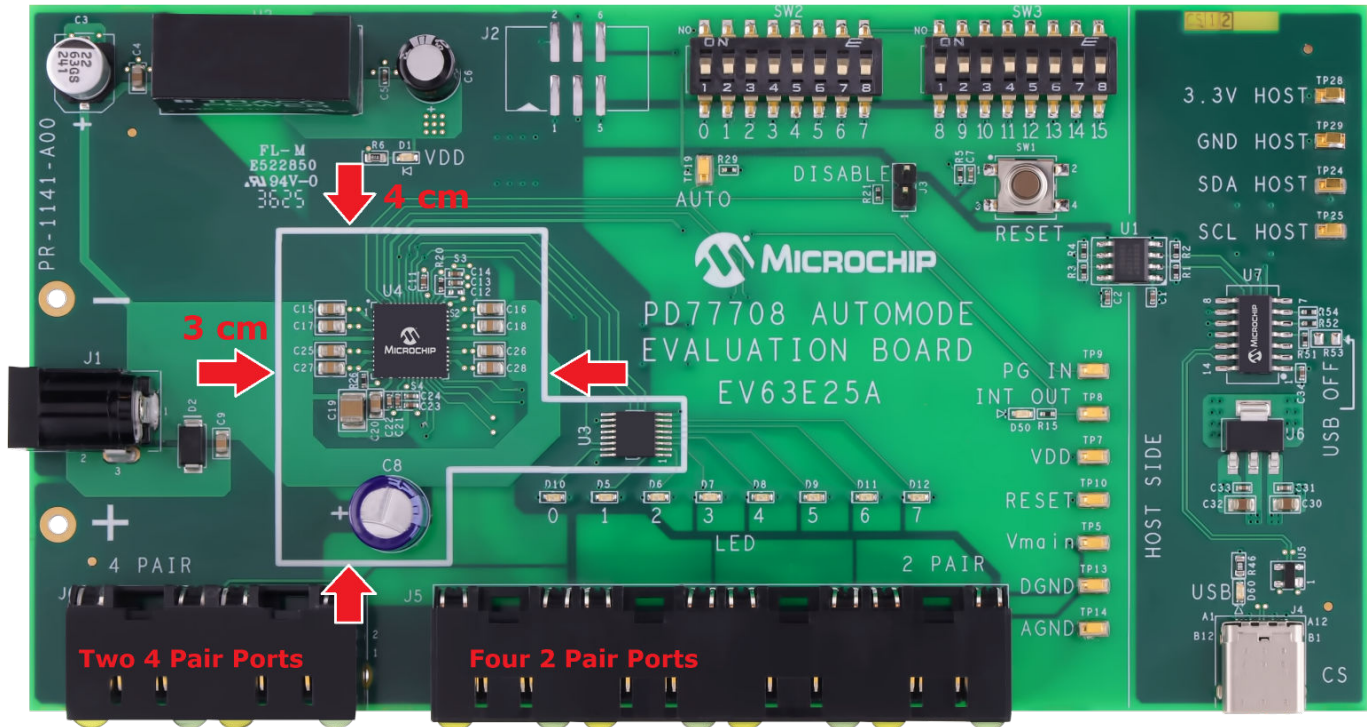


Figure 3. EV63E25A PoE Section Size



Note: Actual PoE application size is 4 cm × 3 cm

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1. Overview

This section provides the basic overview of the EV63E25A evaluation board.

1.1. Power

The EVB is powered by a single source through the DC connector J1. The input voltage level can be selected according to the following IEEE® 802.3 PoE standards:

1. IEEE 802.3af: 44 V_{DC} to 57 V_{DC}
2. IEEE 802.3at: 50 V_{DC} to 57 V_{DC}
3. IEEE 802.3bt:
 - a. 50 V_{DC} to 57 V_{DC} for Type 3
 - b. 52 V_{DC} to 57 V_{DC} for Type 4

The recommended voltage level is 53 V_{DC} to 55 V_{DC}, which covers all the PoE standards. The EVB has three power domains as follows:

1. PoE domain, which is fed directly by the main supply and is the power domain provided by the RJ45
2. 3.3 V_{DC} which feeds the PD77708, LED stream, and I2C isolator, same ground as the PoE domain. This 3.3 V_{DC} is generated by U2 (a DC/DC module).
3. Isolated 5 V_{DC} and 3.3 V_{DC} for serial communication (USB to I²C). This domain is fed by the USB port, and it is marked on the EVB as Host.

Note: The EVB is polarity sensitive. The correct polarity is shown in the following figure.

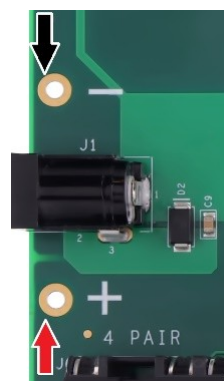
Figure 1-1. DC Connector J1 Polarity



Important: DC input connector J1 is limited to current level up to 4A. If higher current is needed, the 2 via holes next to J1 can be used by soldering a cable to it. The two via holes support up to 8A to feed the whole EVB at full power.

The via holes are marked in the following figure: hole marked red is the V_{main} (+), and the hole marked black is the AGND (-).

Figure 1-2. Power via Holes



1.2. Interface and Control

This section describes the set-up procedures for serial communication, reset push-button, PoE ports disable/power good input, and additional test points.

1.2.1. Serial Communication

The EVB supports serial communication with the PD77708 by I²C. The serial communication is converted to USB by the MCP2221A (U7) from Microchip through a dedicated GUI that allows a user-friendly experience.

To use the USB port, install the MCP2221A driver on your PC. You can download the driver from the Microchip website at www.microchip.com/wwwproducts/en/MCP2221A

The I²C address is set by 4 address pins (A0-A3), which also are used for the LED stream when it is enabled. Therefore, these four pins should be pulled-up or pulled-down with 10K resistors, not connected directly to GND or Vcc. The eight resistors to set the address are R16, R17, R18, R19, R22, R23, R24, R25. These are located on the bottom side of the EVB (next to TP2). The EVB is set to I²C address 0x2F (R16-R19 assembled, R22-R25 not assembled).

A bi-directional isolator (U1) isolates the PD77708's I²C bus from the USB's I2C bus.

The following diagram shows the I²C address setting for the PD77708 controller.

Figure 1-3. I²C Address Setting Diagram

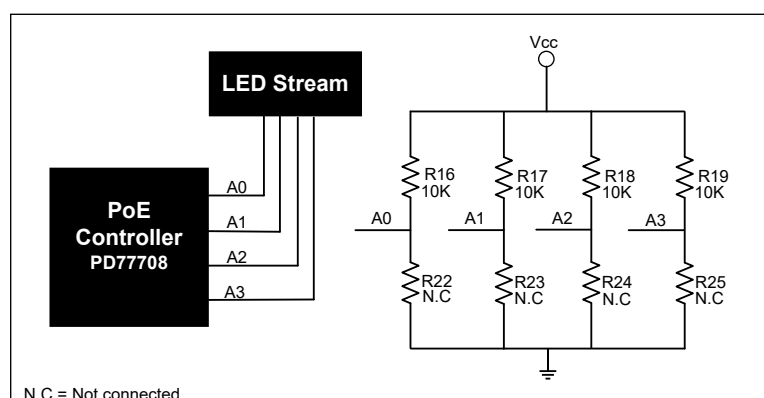


Table 1-1. I²C Address Select

A3 / LED_OE_N	A2 / LED_CS_N	A1 / LED_SCK	A0 / LED_MOSI	I ² C Address
0	0	0	0	0x20
0	0	0	1	0x21
0	0	1	0	0x22
0	0	1	1	0x23
0	1	0	0	0x24
0	1	0	1	0x25
0	1	1	0	0x26
0	1	1	1	0x27
1	0	0	0	0x28
1	0	0	1	0x29
1	0	1	0	0x2A
1	0	1	1	0x2B
1	1	0	0	0x2C
1	1	0	1	0x2D

A3 / LED_OE_N	A2 / LED_CS_N	A1 / LED_SCK	A0 / LED_MOSI	I ² C Address
1	1	1	0	0x2E
1	1	1	1	0x2F

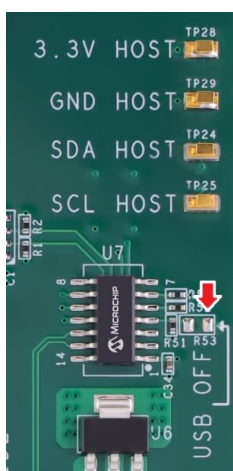
R53 is used to disable the I²C -to-USB conversion. When R53 is installed as a 0Ω resistor, the USB converter (U7) is disabled. This configuration allows the user to connect directly to the I²C bus through the two I²C test points (TP24 and TP25) and control the EVB through I²C .

GND_HOST (TP29) is the GND for the I²C bus.

Note: These four TPs are isolated from the PoE domain, and are related to the USB port.

The following figure shows the R53 and the test points location on the EVB.

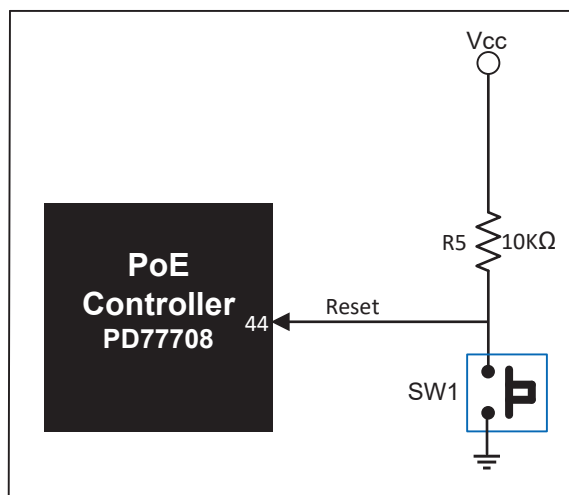
Figure 1-4. Test Points Location



1.2.2. Reset Pushbutton

The pushbutton is connected to the Reset pin of the PD77708 (pin 44), as shown in the following figure. To short the Reset pin to GND, press the SW1 pushbutton. This resets the PoE controller. The Disable/PD_IN is connected to TP9, and is related to the PoE domain.

Figure 1-5. Reset Control Diagram



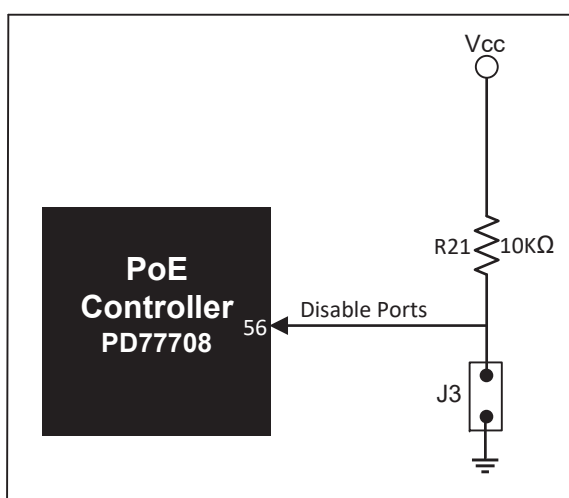
1.2.3. PoE Ports Disable Settings

The jumper J3 is connected to the Disable/PD_IN pin of the PD77708 (Pin 56). When the jumper is installed, the Disable/PD_IN pin is connected to GND, and the ports are disabled.

In normal operations, the host can disable all ports by setting this pin to '0'. The following figure shows the J3 jumper settings.

Reset pin is connected to TP10, and related to the PoE domain.

Figure 1-6. Ports Disable Control Jumper Diagram



1.2.4. EVB Operational Mode Settings

The PD77708 supports 14 pre-defined modes. For more information, refer to modes 1-14 in the following table:

Table 1-2. Operational Modes

PD77708T4						
Level	RB	Voltage Range	Device Power	Legacy	2P/4P	IEEE®802.3
0	GND	0–0.139V	—	Use Saved Default (Configurable saved database)		
1	0.681 kΩ	0.139–0.279V	120W	Disabled	4P	BT
2	1.18	0.279–0.418V	240W	Disabled	4P	BT
3	1.74	0.418–0.557V	360W	Disabled	4P	BT
4	2.37	0.557–0.697V	120W	Enabled	4P	BT
5	3.01	0.697–0.836V	240W	Enabled	4P	BT
6	3.74	0.836–0.976V	360W	Enabled	4P	BT
7	4.64	0.976–1.115V	120W	Disabled	2P	BT
8	5.62	1.115–1.254V	240W	Disabled	2P	BT
9	6.65	1.254–1.394V	360W	Disabled	2P	BT
10	8.06	1.394–1.533V	120W	Enabled	2P	BT
11	9.53	1.533–1.672V	240W	Enabled	2P	BT
12	11.3	1.672–1.812V	360W	Enabled	2P	BT
13	13.3	1.812–1.951V	120W	Disabled	2P	AT
14	15.8	1.951V–2.09V	240W	Disabled	2P	AT
15	OPEN ¹	2.09–2.23V	0W	Disabled	2P	BT

1. Use Factory Default Parameters

- Mode 0 is used when the user wants to use its own saved parameters
- Mode 15 is used when the user wants to use the factory default

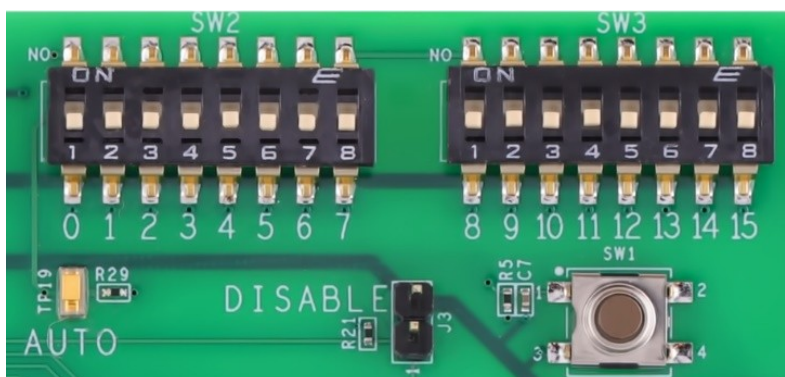
To set the EVB to one of the modes in the table, use SW2 or SW3, each contains 8 dipswitches:

- SW2 sets modes 0-7
- SW3 sets modes 8-15

If none of the modes is selected, then the EVB is set by default to mode 15. The EVB is shipped out in mode 0 is set to ON.

The following figure shows the location of the dip switches on the evaluation board.

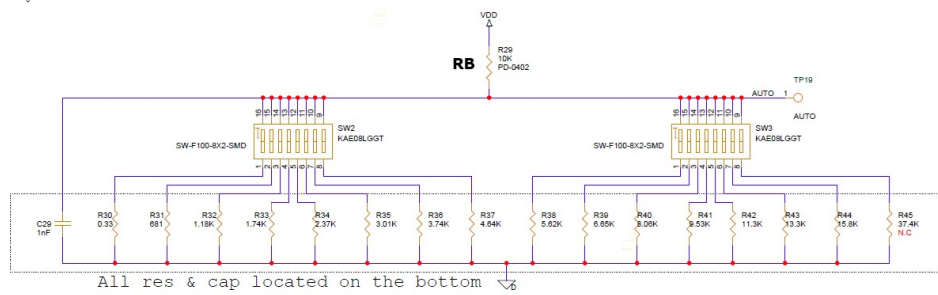
Figure 1-7. Location of Dipswitches on EVB



Note: Only one mode/dipswitch can be set to ON for proper operation. Do not set more than one mode to ON.

The analog level of the auto pin (PD77708 pin 52) can be measured between TP19/AUTO to TP14/AGND.

Figure 1-8. Dipswitches Circuit



1.3. LED Indication

The evaluation board contains status indication LED per logical port and other LEDs for indication. These LEDs and their corresponding functions are listed in the following table.

Table 1-3. LED List

Designation	Function
D1	VDD, 3.3V _{DC} for the PSE domain (Feeds the PD77708, LED stream, I ² C isolation)
D50	INT_OUT (Interruptout, active low)
D60	USB 5V (fed by the USB port, isolated from the PSE domain)
D5-D12	A LED per logical port to provide its status, Marked on the PCB as LED0 to LED7. (The EVB is shipped with port matrix of 6 logical ports, therefore in the current setting only LED 0-5 are active)

The EVB includes LED stream to drive a LED per logical port, U3 is a shift register (74LV595) and each LED is driven by one of its outputs.

Figure 1-9. LED Stream Application

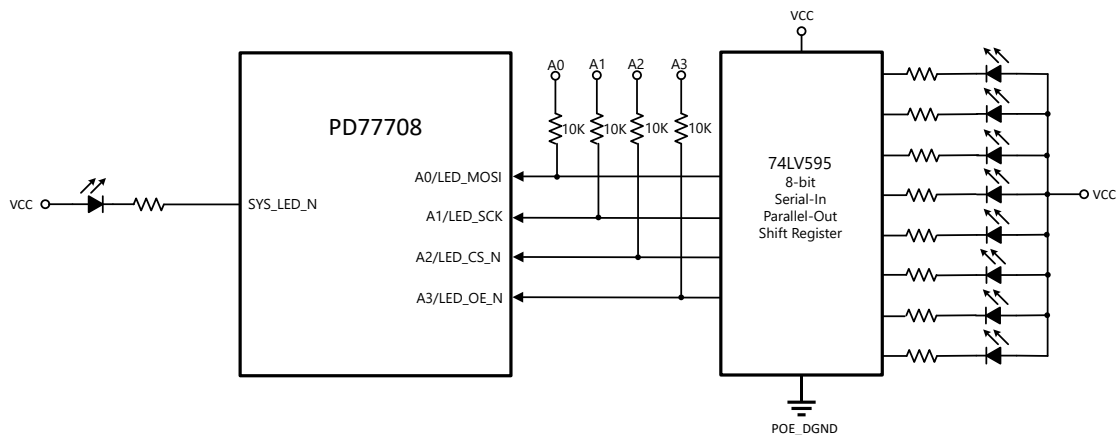
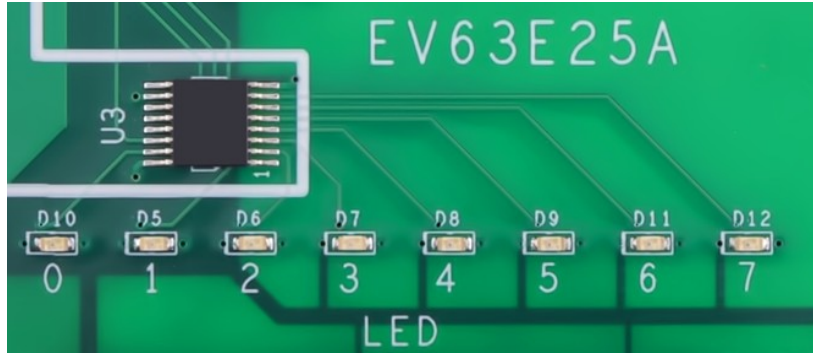


Figure 1-10. LED Stream Location



1.4. RJ45 Connectors Polarity

The six ports of the EVB are divided into two RJ45 gangs:

- Four ports of 2-pair up to 30W
- Two ports of 4-pair up to 90W

The polarity of the port is listed in the following tables:

Table 1-4. J5/RJ45 Connector 2-Pair Port (Logical Ports 0-7)

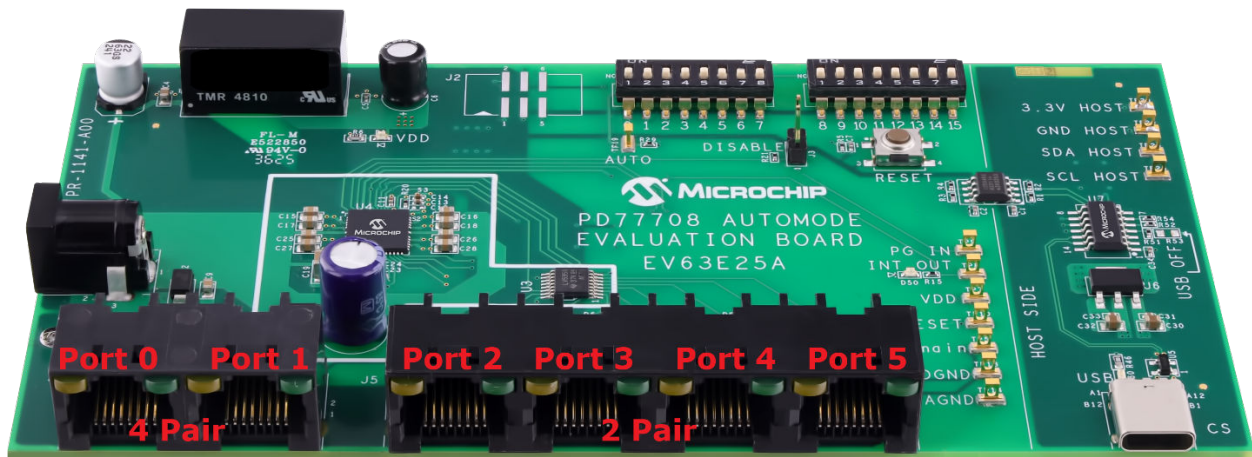
Pin Number (Each RJ45 Port)	Polarity
1, 2	Negative Alt A
3, 6	Positive Alt A
4, 5	N.A.
7, 8	N.A.

Table 1-5. J6/RJ45 Connector 4-Pair Port (Logical Ports 0-1)

Pin Number (Each RJ45 Port)	Polarity
1, 2	Negative Alt A
3, 6	Positive Alt A
4, 5	Positive Alt B
7, 8	Negative Alt B

See the following figure for port numbering.

Figure 1-11. Port Numbering



2. Installation and Setting

This section describes the steps required to install and operate the EVB. Take the following precautions before starting the installation:

- Ensure that the 52 V_{DC}- 57V_{DC} power supply of the board is turned off before plugging in the DC connector.
- Turn the main power supply on only after the DC connector is plugged in.
- Ensure the correct polarity of the power supply cable. The polarity of the power supply cable is as shown in [Figure 1-1](#).

2.1. Port Matrix

Ensure that the ports matrix is configured according to the following table

Table 2-1. Port Matrix Configuration

Logical Port/LED	Physical Port A	Physical Port B	Setting
0	0	1	4 Pair
1	2	3	4 Pair
2	4	0xF	2 Pair
3	5	0xF	2 Pair
4	6	0xF	2 Pair
5	7	0xF	2 Pair
6	0xF	0xF	Not Defined
7	0xF	0xF	Not Defined

Note: Setting the dipswitch SW2 or SW3 to a different mode other than 0, will change the port matrix, according to [Table 1-2](#).

2.2. Schematics

Contact Microchip for the full-board schematics and PCB file.

3. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 3-1. Revision History

Revision	Date	Description
A	January 2026	Initial Revision

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