PIC24FJ256GA705 Family Silicon Errata and Data Sheet Clarification

The PIC24FJ256GA705 family devices that you have received conform functionally to the current Device Data Sheet (DS30010118**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24FJ256GA705 family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A3**).

Data Sheet clarifications and corrections start on Page 7, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24FJ256GA705 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)	Part Number	Device ID(1)	Revision ID for Silicon Revision(2)
		A3			A3
PIC24FJ64GA705	0x7507	0x03	PIC24FJ256GA704	0x750D	0x03
PIC24FJ128GA705	0x750B		PIC24FJ64GA702	0x7506	
PIC24FJ256GA705	0x750F		PIC24FJ128GA702	0x750A	
PIC24FJ64GA704	0x7505		PIC24FJ256GA702	0x750E	
PIC24FJ128GA704	0x7509				

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC24FJ256GA705 Family Flash Programming Specification"* (DS30010102) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A3
I^2C	Address Hold	1.	In Slave mode when AHEN = 1 (Address Hold Enable), if ACKDT (Acknowledge Data bit) is set at the beginning of address reception, clock stretching will not happen after the 8th clock.	X
Reset	Trap Conflict	2.	The TRAPR bit is not getting set when a hard trap conflict occurs.	X
I^2C	Data Hold	3.	In Slave mode when DHEN = 1 (Data Hold Enable), if ACKDT (Acknowledge Data bit) is set at the beginning of data reception, then a slave interrupt will not occur after the 8th clock.	X
Primary XT and HS Oscillator (POSC)	Primary Oscillator Start-up Timer (OST)	4.	OST may indicate oscillator is ready for use too early.	X
Power	Retention Sleep	5.	When the device wakes up from Retention Sleep mode (RETEN bit (RCON<12>) = 1, $\overline{\text{LPCFG}}$ bit (FPOR<2>) = 0), a device Reset may occur. The BOR, POR and EXTR bits in the RCON register are set erroneously for this Reset.	X
Power	Power BOR	6.	The main BOR may not function on some devices.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A3**).

1. Module: I^2C

In Slave mode when AHEN = 1 (Address Hold Enable), if the ACKDT bit (Acknowledge Data) is set at the beginning of address reception, clock stretching will not happen after the 8th clock.

Work around

In Slave mode, user software should clear ACKDT on receiving the Start bit.

Affected Silicon Revisions

A3							
X							

2. Module: Reset

If a lower priority address error trap occurs while a higher priority oscillator failure trap is being processed, the TRAPR bit (RCON<15>) is not set. A Trap Conflict Reset does not occur as expected and the device may stop executing code.

Work around

None. However, a $\overline{\text{MCLR}}$/POR Reset will recover the device.

Affected Silicon Revisions

A3							
X							

3. Module: I^2C

In Slave mode when DHEN = 1 (Data Hold Enable), if the ACKDT bit (Acknowledge Data) is set at the beginning of data reception, then the slave interrupt will not occur after the 8th clock.

Work around

In Slave mode, user software should clear ACKDT on receiving the Start bit.

Affected Silicon Revisions

A3							
X							

4. Module: Primary XT and HS Oscillator (POSC)

The Primary Oscillator Start-up Timer (OST) may indicate the oscillator is ready for use too early. Clocking the device before the oscillator is ready may result in incorrect execution and exceptions. This issue exists when the POSC is requested at power-on, during clock switching, when waking from Sleep or when a peripheral module requests the POSC directly. This issue affects XT and HS modes only.

Work around

Make sure that the Primary Oscillator clock is ready before using it by following these steps:

1. Running on a non-POSC source, request the POSC clock using a peripheral such as REFO.
2. Provide a delay to stabilize the POSC.
3. Switch to the POSC source.

Example 1 shows a work around for the device power-on and Example 2 explains the work around when the device wakes from Sleep.

EXAMPLE 1: USING POSC AT POWER-ON

```
#pragma config FNOSC = FRC            // Oscillator Selection bits (Fast RC oscillator (FRC))
// Clock Switching Enabled (Failsafe Clock Monitor can be enabled or disabled)
#pragma config FCKSM = CSECMD
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
int     main()
{
    // configure REFO to request POSC
    REFOCONLbits.ROSEL = 2;           // POSC
    REFOCONLbits.ROOUT = 0;           // disable output
    REFOCONLbits.ROEN = 1;            // enable module

    // wait for POSC stable clock
    // this delay may vary depending on different application conditions
    // such as voltage, temperature, layout, XT or HS mode and components
    {   // delay for 9 ms
        unsigned int delayms = 9;
        while(delayms--) asm volatile("repeat #(8000000/1000/2) \n nop");
    }

    // switch to POSC = 2
    __builtin_write_OSCCONH(2);
    __builtin_write_OSCCONL(1);
    while(OSCCONbits.OSWEN == 1);     // wait for switch
```

EXAMPLE 2: USING POSC WHEN WAKING FROM SLEEP

```
// Clock Switching Enabled (Failsafe Clock Monitor can be enabled or disabled)
#pragma config FCKSM = CSECMD
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
    // switch to FRC = 0 before entering sleep
    __builtin_write_OSCCONH(0);
     __builtin_write_OSCCONL(1);
    while(OSCCONbits.OSWEN == 1);     // wait for switch

    // enter sleep mode
    Sleep();

    // configure REFO to request POSC
    REFOCONLbits.ROSEL = 2;           // POSC
    REFOCONLbits.ROOUT = 0;           // disable output
    REFOCONLbits.ROEN = 1;            // enable module

    // wait for POSC stable clock
    // this delay may vary depending on different application conditions
    // such as voltage, temperature, layout, XT or HS mode and components
    {   // delay for 9 ms
        unsigned int delayms = 9;
        while(delayms--) asm volatile("repeat #(8000000/1000/2) \n nop");
    }

    // switch to POSC = 2
    __builtin_write_OSCCONH(2);
    __builtin_write_OSCCONL(1);
    while(OSCCONbits.OSWEN == 1);     // wait for switch
```

Affected Silicon Revisions

A3							
X							

5. Module: Power

When the device wakes up from Retention Sleep mode (RETEN bit (RCON<12>) = 1, LPCFG bit (FPOR<2>) = 0), occasionally a device reset may occur. The BOR, POR and EXTR bits in the RCON register are set erroneously for this Reset.

Work around

To provide a consistent behavior when the device wakes up from Retention Sleep mode, a software RESET instruction (RESET) should be inserted following the SLEEP instruction. In this case, a Reset will be always be generated when the device wakes up from Retention Sleep. Example 3 shows the software RESET instruction implementation:

EXAMPLE 3: SOFTWARE RESET AFTER SLEEP INSTRUCTION

```
// ENTER SLEEP MODE.
asm volatile (“pwrsav #0”);
// SOFTWARE RESET RIGHT AFTER SLEEP.
asm volatile(“reset”);
```

Affected Silicon Revisions

A3							
X							

6. Module: Power

The main BOR may not occur when the operating voltage drops below the BOR trip voltage.

Work around

Ensure the device operating voltage does not violate the specified values. Use an external supervisor circuit to reset the device if the operating voltage can be outside the specified values.

Affected Silicon Revisions

A3							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS30010118**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Referenced Sources

The referenced sources have been updated. The changes to the references are shown in **bold**.

- "CPU with Extended Data Space (EDS)" (DS39732)
- **"PIC24F Data Memory" (DS30009717) has been removed**
- "Direct Memory Access Controller (DMA)" (DS39742)
- "PIC24F Flash Program Memory" (DS30009715)
- "Data Memory with Extended Data Space (EDS)" (DS39733)
- "Reset" (DS39712)
- "Interrupts" (DS70000600)
- "Oscillator" (DS39700)
- **"Power-Saving Features with Deep Sleep (DS39727)**
- "I/O Ports with Peripheral Pin Select (PPS)" (DS39711)
- "Timers" (DS39704)
- "Input Capture with Dedicated Timer" (DS70000352)
- "Output Compare with Dedicated Timer" (DS70005159)
- "Capture/Compare/PWM/Timer (MCCP and SCCP)" (DS33035)
- **"Serial Peripheral Interface (SPI) with Audio Codec Support" (DS70005136)**
- "Inter-Integrated Circuit (I^2C)" (DS70000195)
- **"Universal Asynchronous Receiver Transmitter (UART)" (DS70000582)**
- "Enhanced Parallel Master Port (EPMP)" (DS39730)
- "RTCC with Timestamp" (DS70005193)
- "32-Bit Programmable Cyclic Redundancy Check (CRC)" (DS30009729)
- "Configurable Logic Cell (CLC)" (DS33949)
- "12-Bit A/D Converter with Threshold Detect" (DS39739)
- "Scalable Comparator Module" (DS39734)
- "Dual Comparator Module" (DS39710)
- "Charge Time Measurement Unit (CTMU) and CTMU Operation with Threshold Detect" (DS30009743)
- "High-Level Integration with Programmable High/Low-Voltage Detect (HLVD)" (DS39725)
- "Watchdog Timer (WDT)" (DS39697)
- "CodeGuard™ Intermediate Security" (DS70005182)
- "High-Level Device Integration" (DS39719)
- "Programming and Diagnostics" (DS39716)
- **"Comparator Voltage Reference Module" (DS39709)**

2. Module: Device Overview

In Table 1-3, the RC0 row has been added:

Pin Function	Pin Number/Grid Locater				I/O	Input Buffer	Description
	28-Pin SOIC SSOP, SPDIP	28-Pin QFN, UQFN	44-Pin TQFP	48-Pin QFN/TQFP			
RC0	—	—	25	27	I/O	DIG/ST	PORTC Digital I/Os

3. Module: Power-Saving Features

In Table 10-1, the values have been updated. The changes are shown in **bold**.

TABLE 10-1: LOW POWER SLEEP MODES

RETEN	VREGS	MODE	Relative Power
0	**1**	Sleep	**A Few µA Range**
0	**0**	Fast Wake-up	**100 µA Range**
1	**1**	Retention Sleep	**Less than 1 µA**
1	**0**	Fast Retention	**A Few µA Range**

4. Module: Capture/Compare/PWM/Timer Modules (MCCP)

In Table 16-2 and Register 16-1, the following note has been added:

Note 1: Center-Aligned PWM mode is only available on MCCP modules. This feature is disabled on SCCP modules.

5. Module: Serial Peripheral Interface

In Register 17-1, MODE<32,16> now includes FIFO DEPTH information. The addition is shown in **bold**.

bit 11-10 MODE<32,16>: Serial Word Length bits(1,4)

AUDEN = 0:

MODE32	MODE16	COMMUNICATION‘	FIFO DEPTH
1	x	32-Bit	**8**
0	1	16-Bit	**16**
0	0	8-Bit	**32**

6. Module: Serial Peripheral Interface

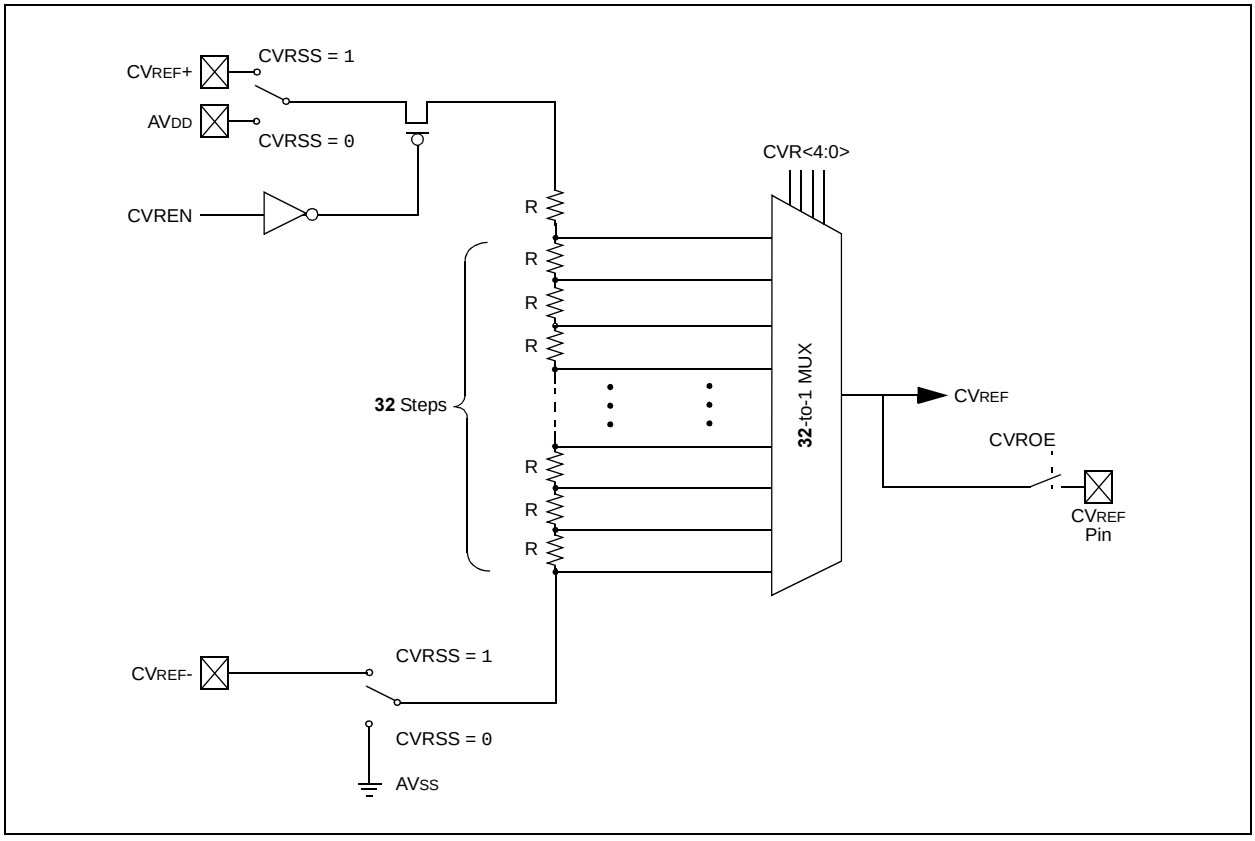
In Register 17-5, the following note has been added:

Note 4: See MODE bits of SPIxCON1L.

7. Module: Comparator Voltage Reference

All voltage references have been corrected to 32 distinct voltage levels. In Figure 26-1, the values for the CVR voltage levels have been corrected. The corrected values are shown in **bold.**

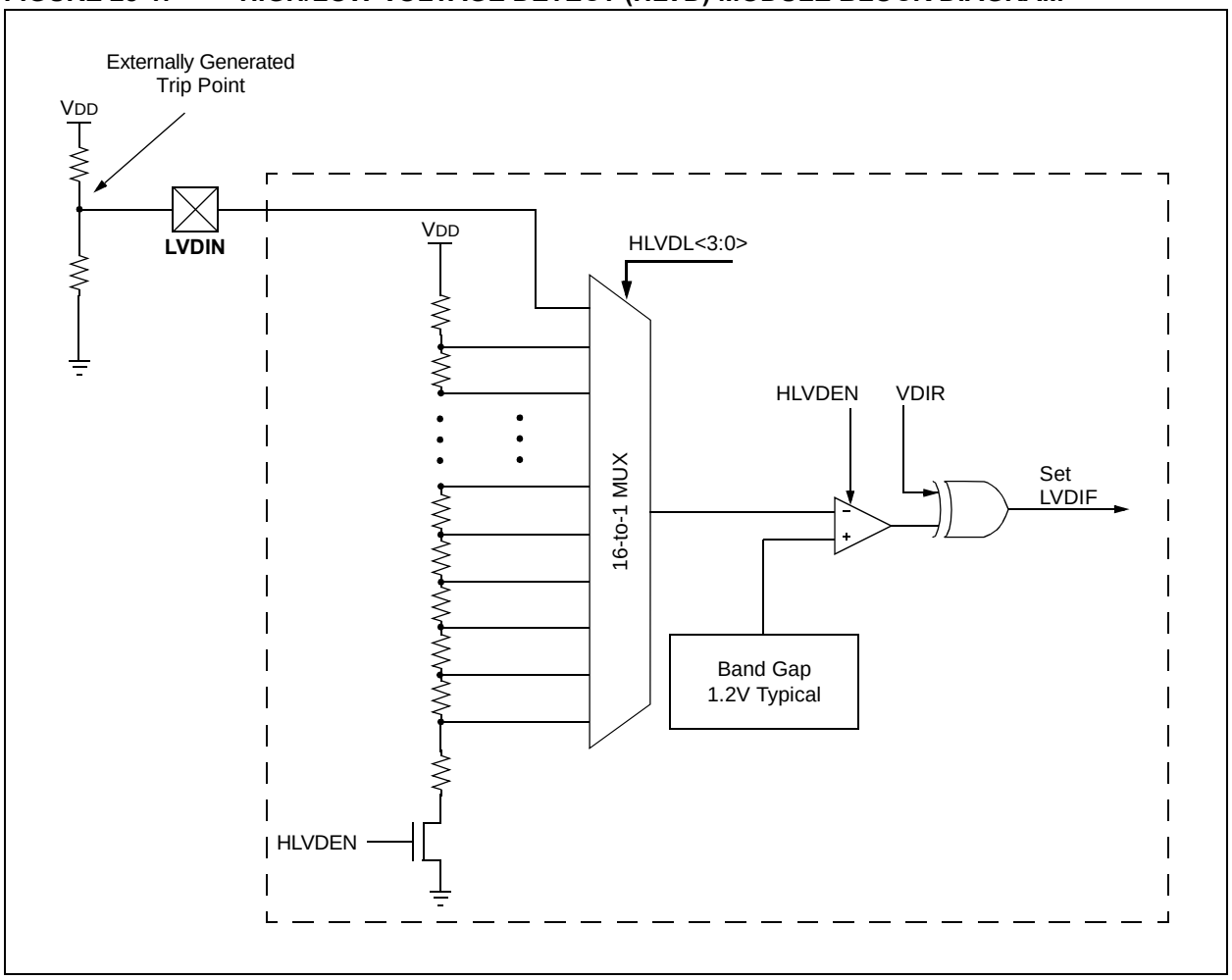
FIGURE 26-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



8. Module: High/Low-Voltage Detect (HLVD)

Figure 28-1 has been corrected with the proper voltage information. The corrected text is shown in **bold**.

FIGURE 28-1: HIGH/LOW-VOLTAGE DETECT (HLVD) MODULE BLOCK DIAGRAM



9. Module: High/Low-Voltage Detect (HLVD)

In Register 28-1, the bit description for HLVDL<3:0> has been corrected as shown in **bold**.

bit 3-0 HLVDL<3:0>: High/Low-Voltage Detection Limit bits

1111 = External analog input is used (input comes from the **LVDIN** pin)
1110 = Trip Point 1(1)
1101 = Trip Point 2(1)
1100 = Trip Point 3(1)
•
•
•
0100 = Trip Point 11(1)
00xx = Unused

10. Module: Electrical Characteristics

In Table 32-12, the DC101 row has been corrected as shown in **bold**.

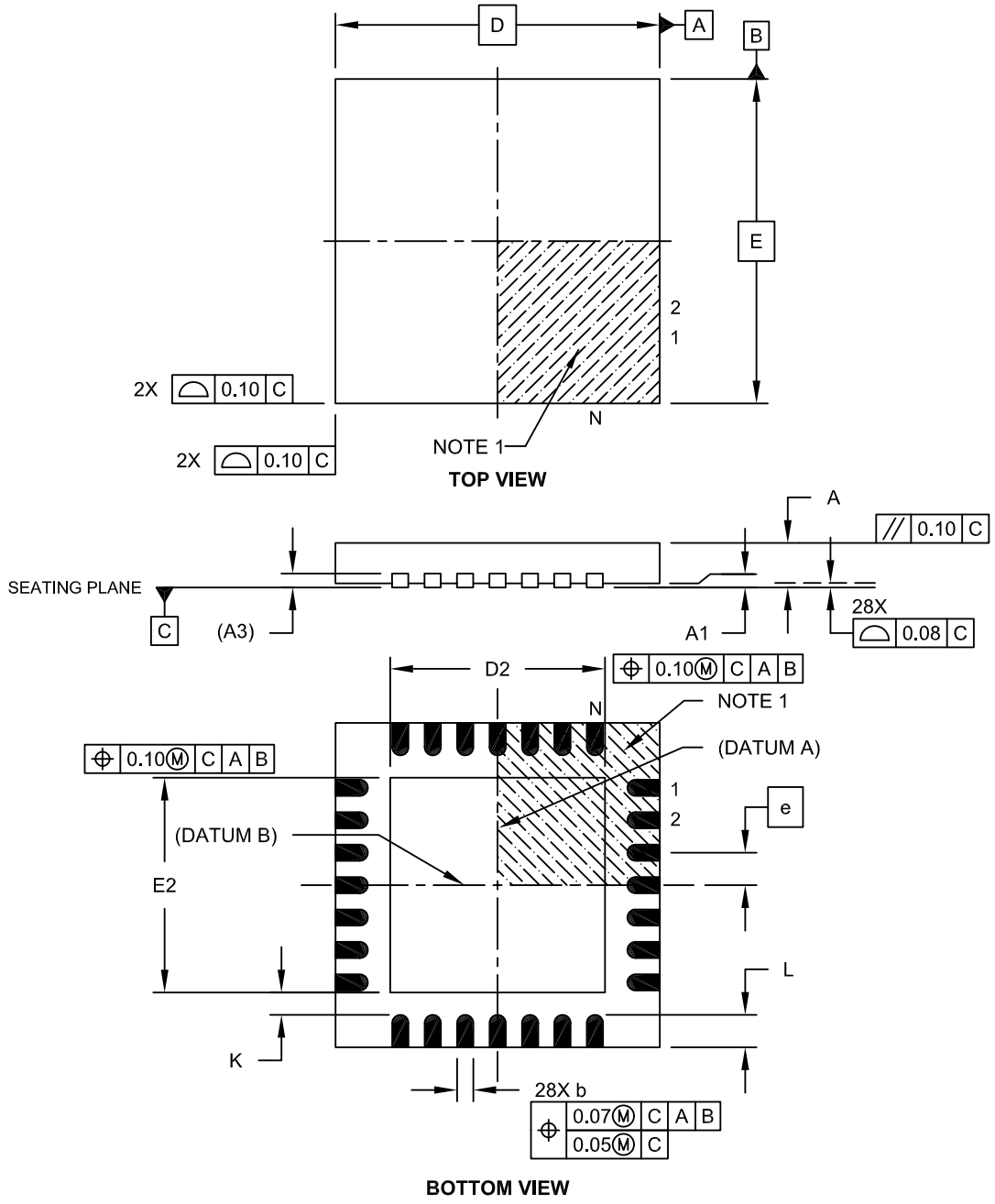
Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)								
Param No.	Symbol	Characteristic		Min	Typ	Max	Units	Conditions
DC101	VTHL	HLVD Voltage on **LVDIN** Pin Transition	HLVDL<3:0> = 1111	—	1.20	—	V	

11. Module: Packaging Information

Replaced the 28-Lead M6 package drawings with the correct MV package drawings as shown below.

28-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 4x4x0.5 mm Body [UQFN]

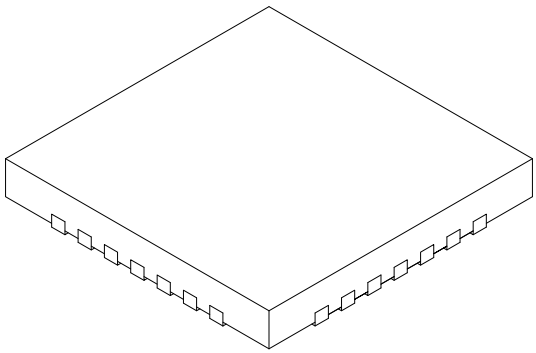
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-152A Sheet 1 of 2

28-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) – 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.40 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.127 REF	
Overall Width	E		4.00 BSC	
Exposed Pad Width	E2	2.55	2.65	2.75
Overall Length	D		4.00 BSC	
Exposed Pad Length	D2	2.55	2.65	2.75
Contact Width	b	0.15	0.20	0.25
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

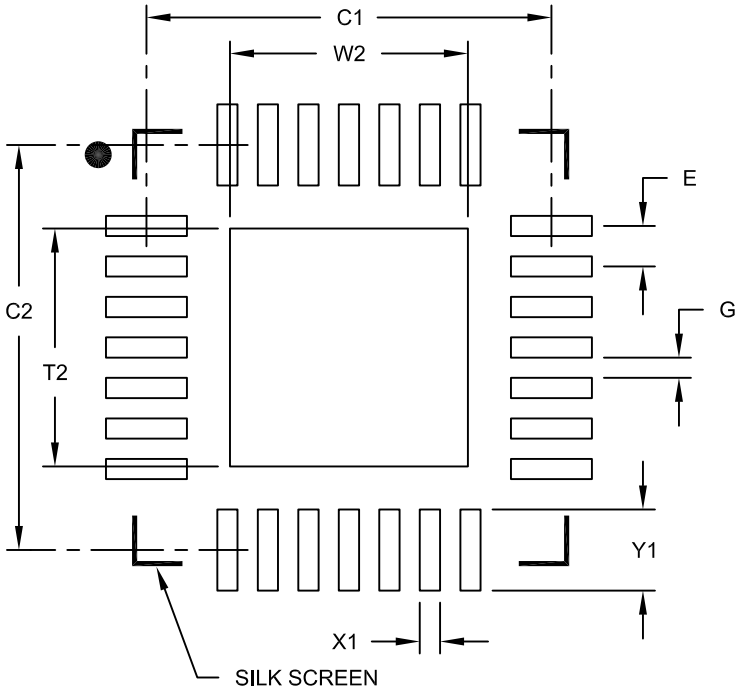
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-152A Sheet 2 of 2

28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) - 4x4 mm Body [UQFN]
With 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	W2			2.35
Optional Center Pad Length	T2			2.35
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X28)	X1			0.20
Contact Pad Length (X28)	Y1			0.80
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2152A

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (10/2016)

Initial release of this document; issued for Revision A3.

Rev B Document (12/2016)

Added silicon errata issue 5 (Power).

Rev C Document (6/2017)

Added silicon errata issue 6 (Power).

Added data sheet clarifications 1 (Referenced Sources), 2 (Device Overview), 3 (Power-Saving Features), 4 (Capture/Compare/PWM/Timer Modules (MCCP)), 5 (Serial Peripheral Interface), 6 (Serial Peripheral Interface), 7 (Comparator Voltage Reference), 8 (High/Low-Voltage Detect (HLVD)), 9 (High/Low-Voltage Detect (HLVD)), 10 (Electrical Characteristics) and 11 (Packaging Information.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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