SY21113D

High Efficiency, 500kHz, 3A, 18V Input Synchronous Step Down Regulator

General Description

The SY21113D is a high efficiency 500kHz synchronous step-down DC/DC converter capable of delivering 3A current. The SY21113D operates over a wide input voltage range from 4.5V to 18V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Low output voltage ripple and small external inductor and capacitor sizes are achieved with 500kHz switching frequency. It adopts the instant PWM architecture to achieve fast transient responses for high step down applications

Ordering Information

SY21113 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY21113DAIC	TSOT23-8	--

Features

- Low $R_{DS(ON)}$ for Internal Switches (Top/Bottom): 80mΩ/40mΩ
- 4.5-18V Input Voltage Range
- 3A Output Current Capability
- 500 kHz Switching Frequency
- Instant PWM Architecture to Achieve Fast Transient Responses
- Cycle-by-cycle Current Limitation
- Hiccup Mode Short Circuit Protection
- Power Good Indicator
- Programmable Soft-start Time to Limit the Inrush Current
- ±1.5% 0.6V Reference
- Thermal Shut Down With Auto-recovery
- RoHS Compliant and Halogen Free
- TSOT23-8 Package

Applications

- Set Top Box
- Portable TV
- Access Point Router
- DSL Modem
- LCD TV

Typical Applications

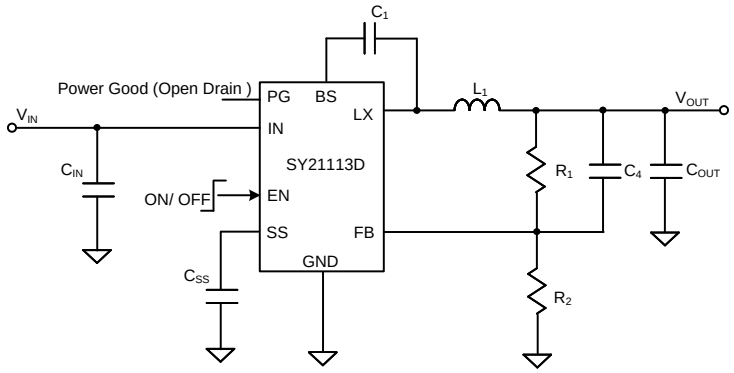


Figure1. Schematic Diagram

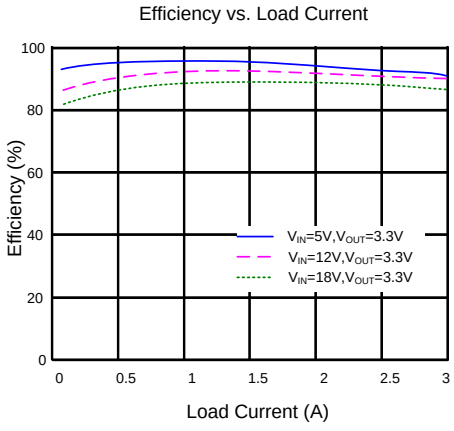
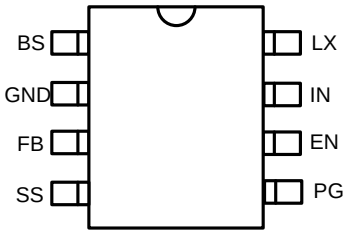


Figure2. Efficiency vs. Load Current

Pinout (top view)



TSOT23-8

Top Mark: **YN*xyz*, (**Device code: YN, ***x=year code, y=week code, z= lot number code*****)**

Pin Name	Pin Number	Pin Description
BS	1	Boot-strap pin. Supply high side gate driver. Decouple this pin to the LX pin with a 0.1μF ceramic capacitor.
GND	2	Ground pin.
FB	3	Output feedback pin. Connect this pin to the center point of the output resistor divider (as shown in Figure1) to program the output voltage: $V_{OUT}=0.6\times(1+R_1/R_2)$
SS	4	Soft-start programming pin. Connect a capacitor from this pin to the ground to program the soft-start time. $t_{SS}(ms)=C_{SS}(nF)\times0.6V/4\mu A$. The typical soft-start time is 800μs.
PG	5	Power good Indicator. Low output if the output is within 90% of the regulation voltage; Open-drain output otherwise.
EN	6	Enable control. Pulled high to turn on. Do not leave it floating.
IN	7	Input pin. Decouple this pin to the GND pin with at least a 1μF ceramic capacitor.
LX	8	Inductor pin. Connect this pin to the switching node of the inductor.

Block Diagram

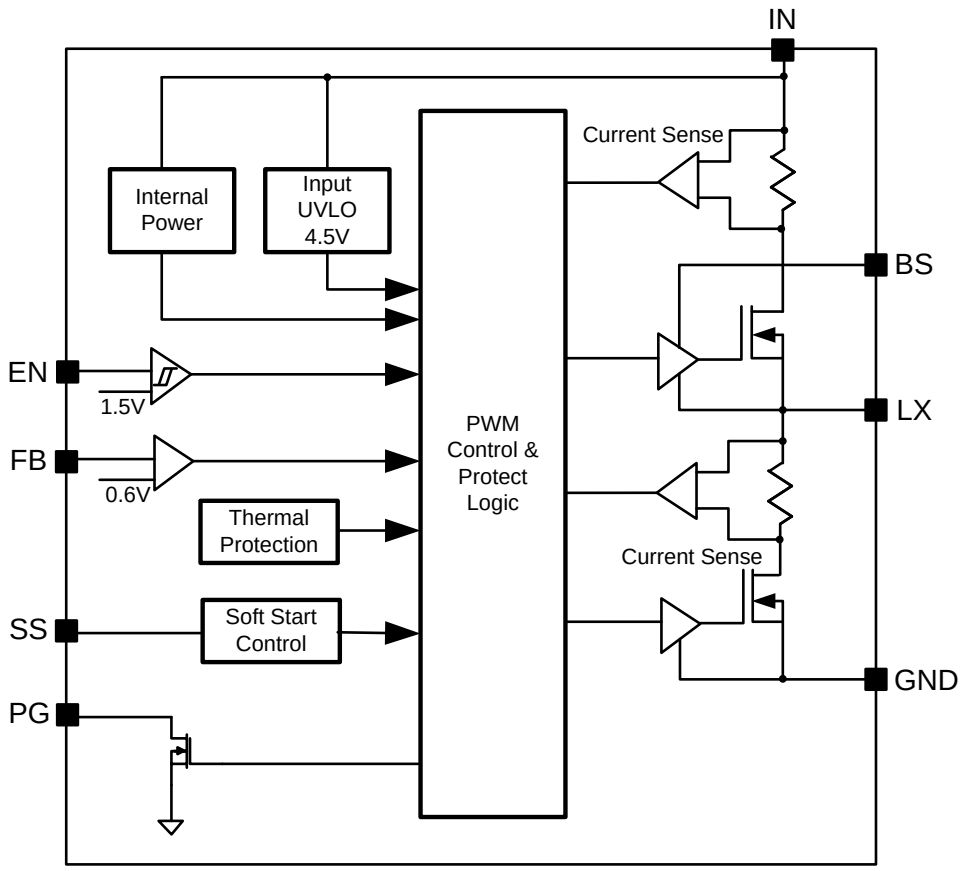


Figure3. Block Diagram

Absolute Maximum Ratings (Note 1)

IN, LX, PG, EN ---------- 19V
FB, SS, BS-LX ---------- 4V
Power Dissipation, P_D @ T_A = 25°C, TSOT23-8 ---------- 1.5W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 66°C/W
θ_{JC} ---------- 15°C/W
Junction Temperature Range ---------- 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
Dynamic LX voltage in 10ns duration---------- IN+3V to GND-4V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4.5V to 18V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, I_{OUT} = 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		18	V
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF}×105%		100		μA
Shutdown Current	I_{SHDN}	EN=0		5	10	μA
Feedback Reference Voltage	V_{REF}		0.591	0.6	0.609	V
FB Input Current	I_{FB}	V_{FB}=3.3V	-50		50	nA
Top FET RON	$R_{DS(ON)1}$			80	90	mΩ
Bottom FET RON	$R_{DS(ON)2}$			40	50	mΩ
Bottom FET Valley Current Limit	I_{LIM}		3.4	4.2	5	A
Top FET Peak Current Limit **(Note 4)**	$I_{LIM,TOP}$		4.5	6	7.5	A
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
Input UVLO Threshold	V_{UVLO}				4.5	V
UVLO Hysteresis	V_{HYS}			0.3		V
Min ON Time			50	80	120	ns
Min OFF Time			140	170	220	ns
Switching Frequency				500		kHz
Soft-start Charging Current	I_{SS}			4		μA
Soft-start Time	t_{SS}			800		μs
Power Good Threshold	V_{PG}	V_{FB} rising (Good)	88	90	92	%V_{REF}
Power Good Hysteresis	$V_{PG,HYS}$			2		%V_{REF}
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C

Note 1: Stresses beyond "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

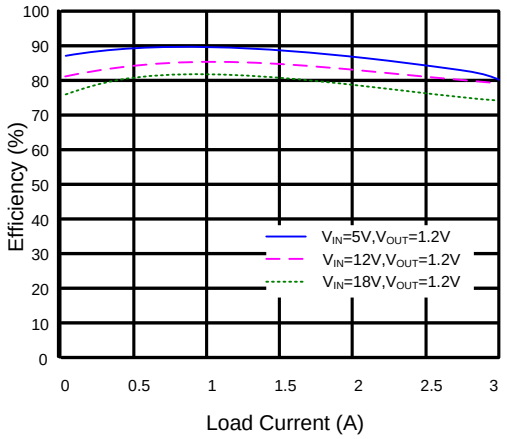
Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a two-layer Silergy evaluation board.

Note 3: The device is not guaranteed to function outside its operating conditions.

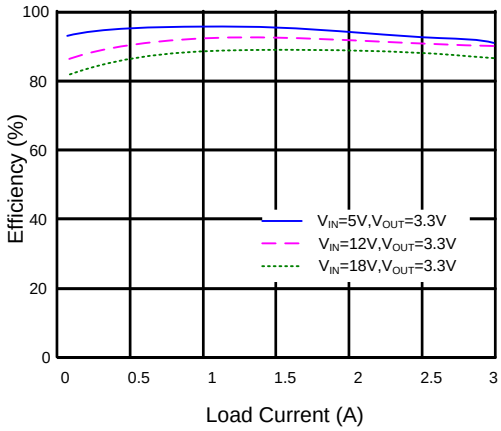
Note 4: The values are guaranteed by design.

Typical Performance Characteristics

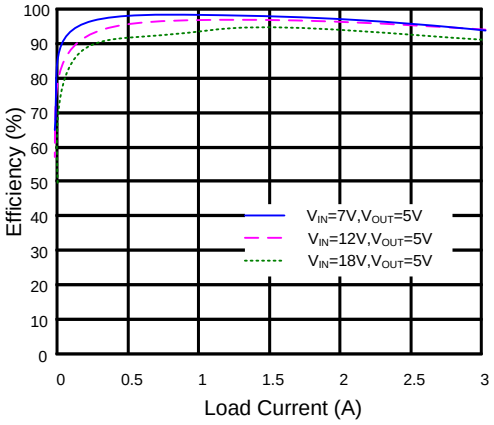
Efficiency vs. Load Current



Efficiency vs. Load Current

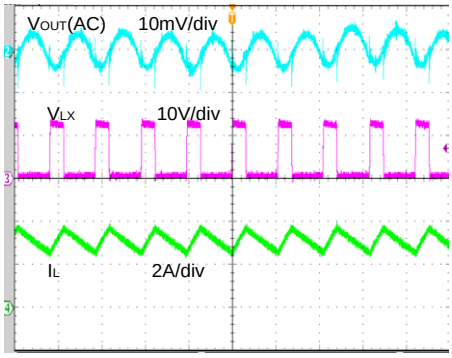


Efficiency vs. Load Current



Output Ripple

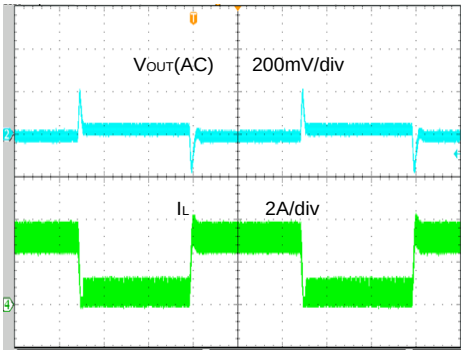
(V_{IN}=12V, V_{OUT}=3.3V, I_{LOAD}=3A)



Time (2μs/div)

Load Transient

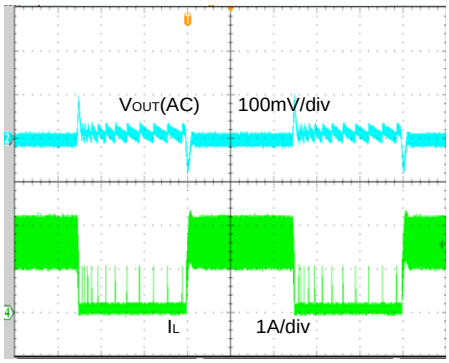
(V_{IN}=12V, V_{OUT}=3.3V, I_{LOAD}=0.3-3A)



Time (200μs/div)

Load Transient

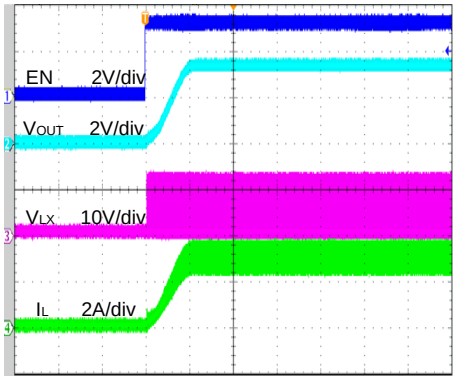
(V_{IN}=12V, V_{OUT}=3.3V, I_{LOAD}=0-1.5A)



Time (200μs/div)

Startup

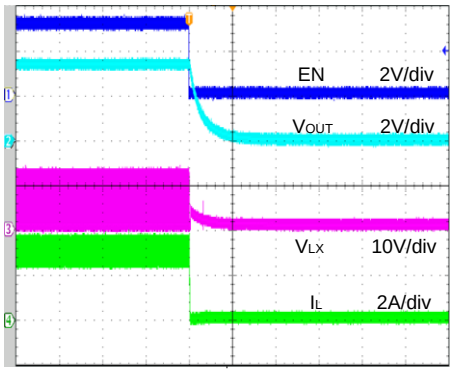
(V_{IN}=12V, V_{OUT}=3.3V, I_{LOAD}=3A)



Time (2ms/div)

Shutdown

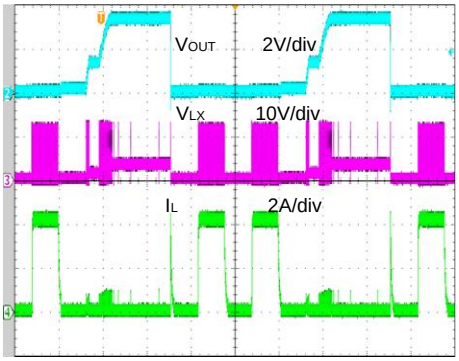
(V_{IN}=12V, V_{OUT}=3.3V, I_{LOAD}=3A)



Time (200μs/div)

Short Circuit Protection

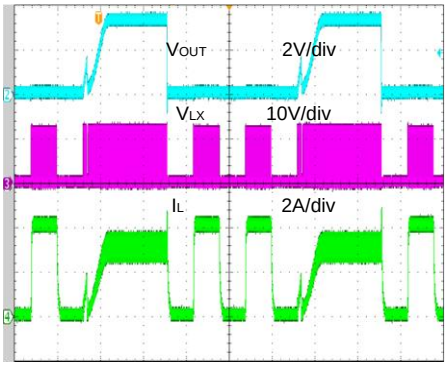
(V_{IN}=12V, V_{OUT}=3.3V, Open to Short)



Time (4ms/div)

Short Circuit Protection

(V_{IN}=12V, V_{OUT}=3.3V, 3A to Short)



Time (4ms/div)

Operation

The SY21113D is a synchronous Buck regulator that integrates the PWM control, top and bottom switches on the same die to minimize the switching transition loss and conduction loss. With ultra low $R_{DS(ON)}$ power switches and proprietary PWM control, the SY21113D can achieve the highest efficiency and the highest switch frequency simultaneously to minimize the external inductor and capacitor sizes, and thus achieves the minimum solution footprint.

The SY21113D provides protection functions such as cycle-by-cycle current limit, thermal shutdown protection with auto-recovery and hiccup mode short circuit protection.

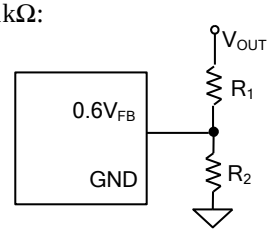
Applications Information

Because of the high integration in the SY21113D, the application circuit based on this regulator is rather simple. Only the input capacitor C_{IN}, the output capacitor C_{OUT}, the output inductor L and the feedback resistors (R_1 and R_2) need to be selected for the targeted applications specifications.

Feedback Resistor Dividers R_1 and R_2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If V_{OUT} is 3.3V, R_1=100kΩ is chosen, then using the following equation, R_2 can be calculated to be 22.1kΩ:

$$R_2 = \frac{0.6V}{V_{OUT}-0.6V} R_1$$



Input Capacitor C_{IN}:

The ripple current through the input capacitor is calculated as:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{D(1-D)}$$

To minimize the potential noise problem, a typical X5R or better grade ceramic capacitor should be placed really close to the IN and the GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and the IN/GND pins. In this case, a 10μF low ESR ceramic capacitor is recommended.

Output Capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X5R or better grade ceramic capacitor greater than 22μF capacitance.

Output Inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{f_{SW} \times I_{OUT,MAX} \times 40\%}$$

Where fsw is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY21113D is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

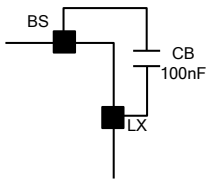
2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mΩ to achieve a good overall efficiency.

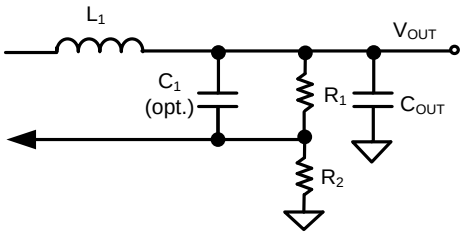
External Bootstrap Capacitor

This capacitor provides the gate driver voltage for the internal high side MOSEFET. A 100nF low ESR ceramic capacitor connected between the BS pin and the LX pin is recommended.



Load Transient Considerations:

The SY21113D integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a 22pF ceramic capacitor in parallel with R_1 may further speed up the load transient responses and is thus recommended for applications with large load transient step requirements.



Soft-start:

The SY21113D provides programmable soft-start time feature. The soft-start time is 800μs typically when the SS pin is floating. Connect a capacitor across the SS pin and the GND to program the soft-start time.

$t_{SS}(ms)=C_{SS}(nF)\times 0.6V/4\mu A$

Layout Design:

The layout design of the SY21113D is relatively simple. For the best efficiency and minimum noise problem, the following components should be placed close to the IC: C_{IN}, L_1, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connecting to the GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to the pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with the LX pin must be minimized to avoid the potential noise problem.

4) The components R_1 and R_2 and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull-down 1MΩ resistor between the EN and the GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

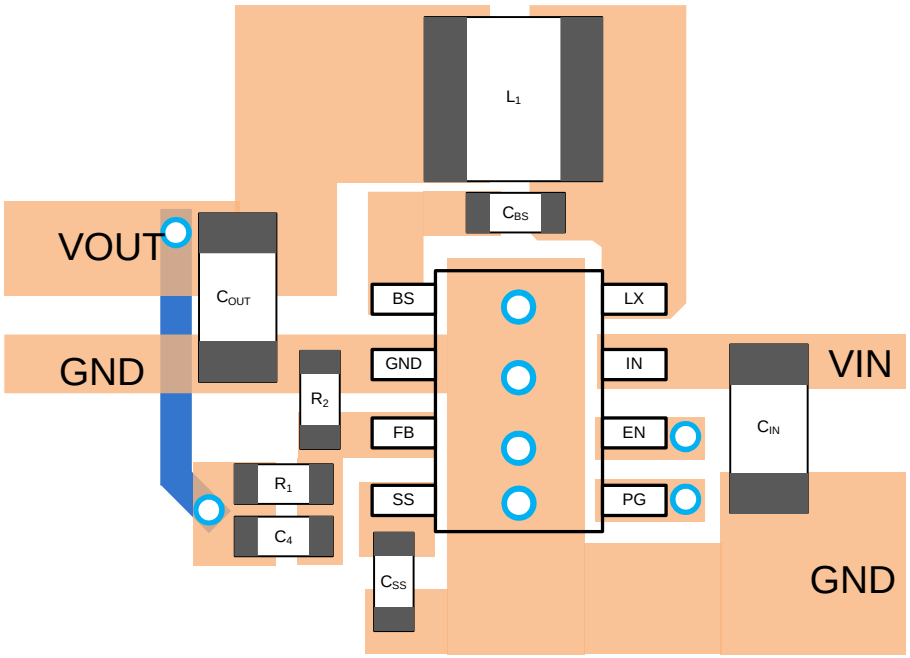
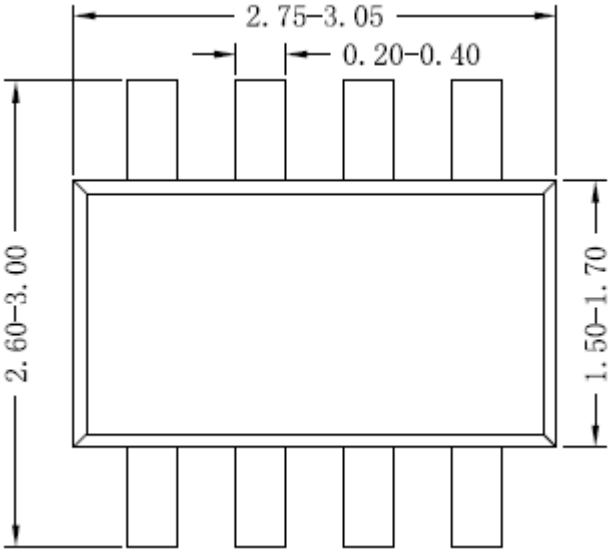
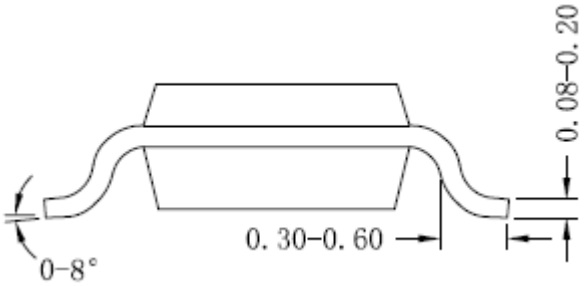


Figure4. PCB Layout Suggestion

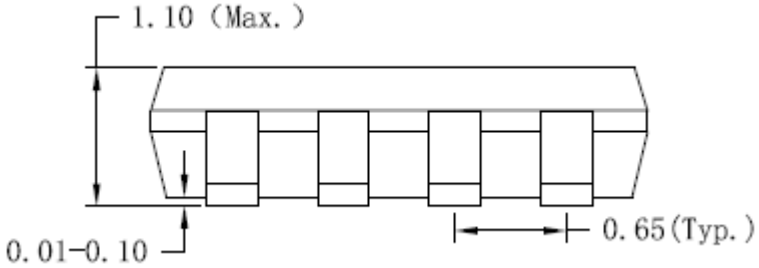
TSOT23-8 Package Outline Drawing



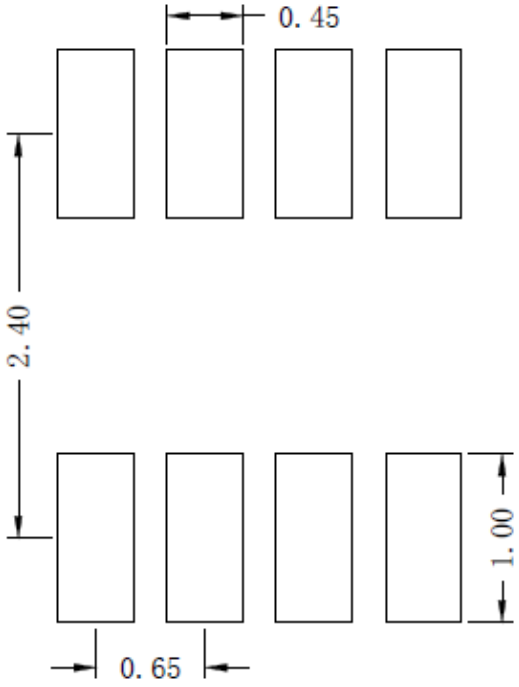
Top view



Side view A



Side view B

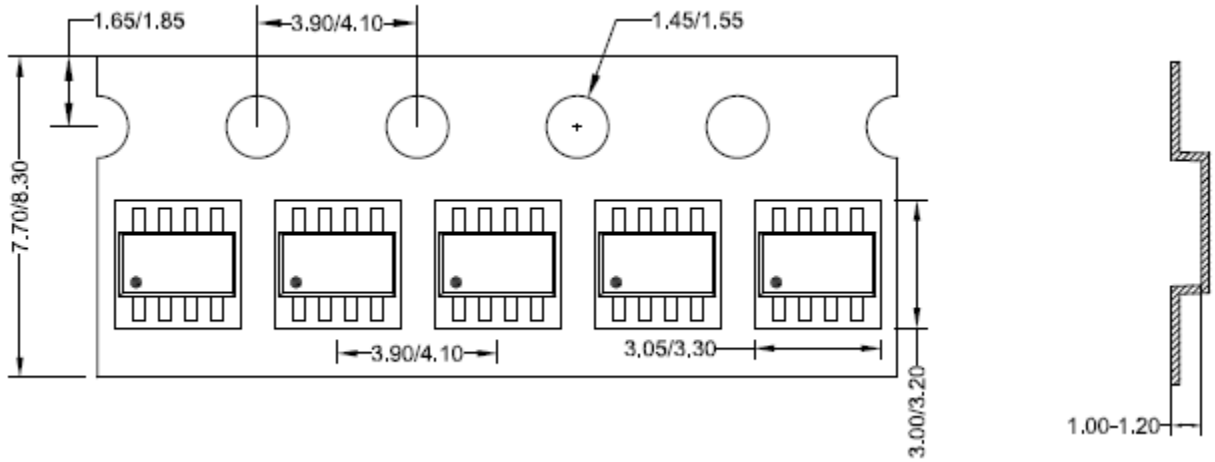


Recommended PCB layout
(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr**

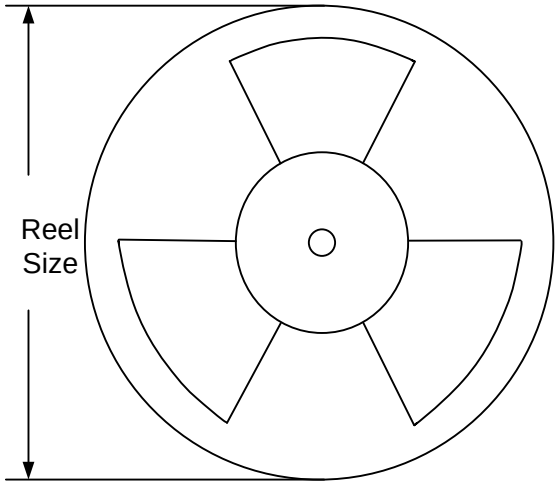
Taping & Reel Specification

1. TSOT23-8 taping orientation



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
TSOT23-8	8	4	7	400	160	3000

3. Others: NA

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