Title Page

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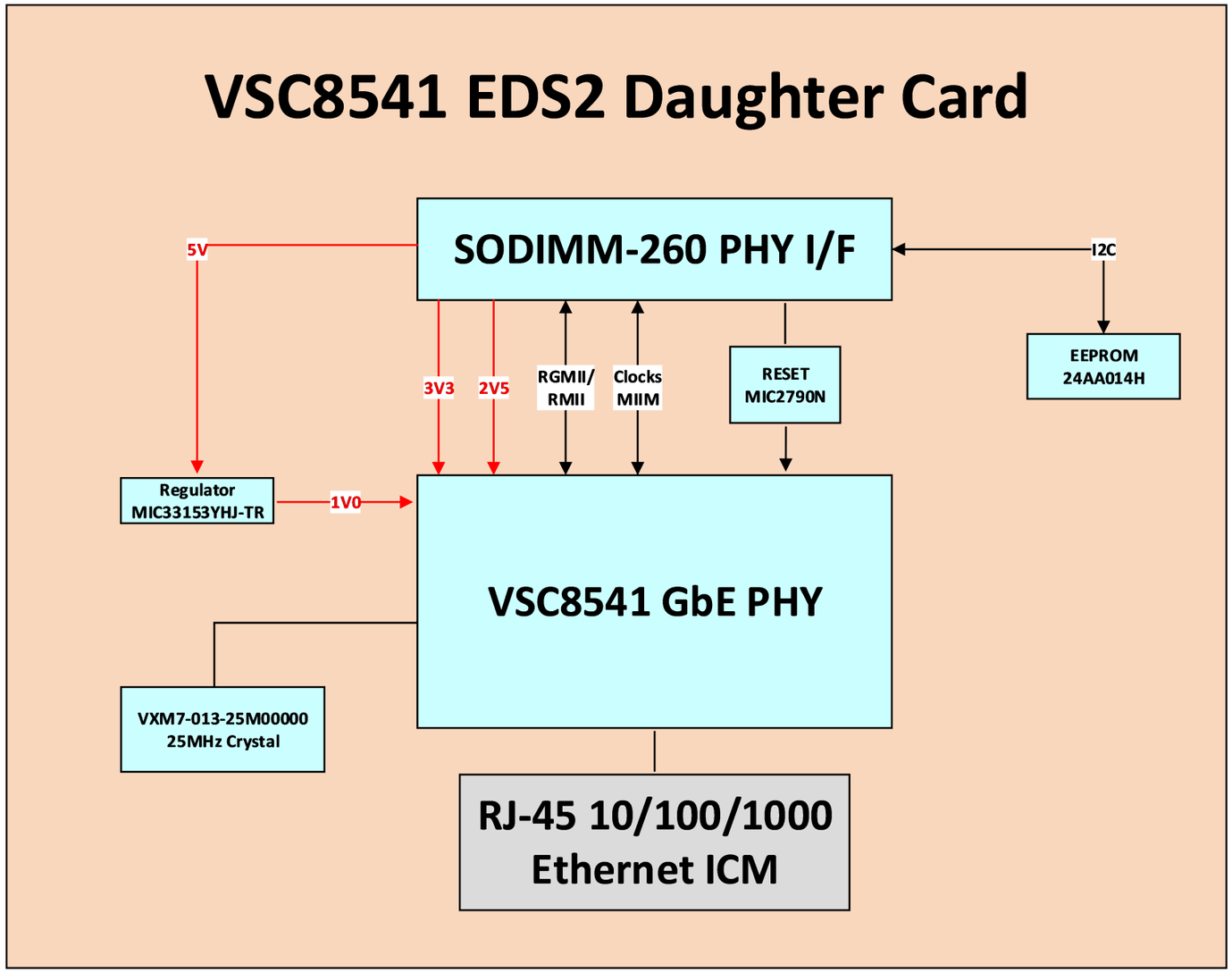
Revision History

Revision	Date	Revision Summary	Author
A0	09/12/2024	Intial draft	Alexys Antell
B0	02/24/2025	Fixing strapping population, silk errors, and reset lines.	Alexys Antell
C0	05/13/2025	Addressing TX_CLK driving issue	Alexys Antell
R1	05/13/2025	Released	Alexys Antell



Notes

#	Description
1	This daughter card supports VDDIO at 3.3V or 2.5V
2	This daughter card supports VDDMAC at 3.3V or 2.5V

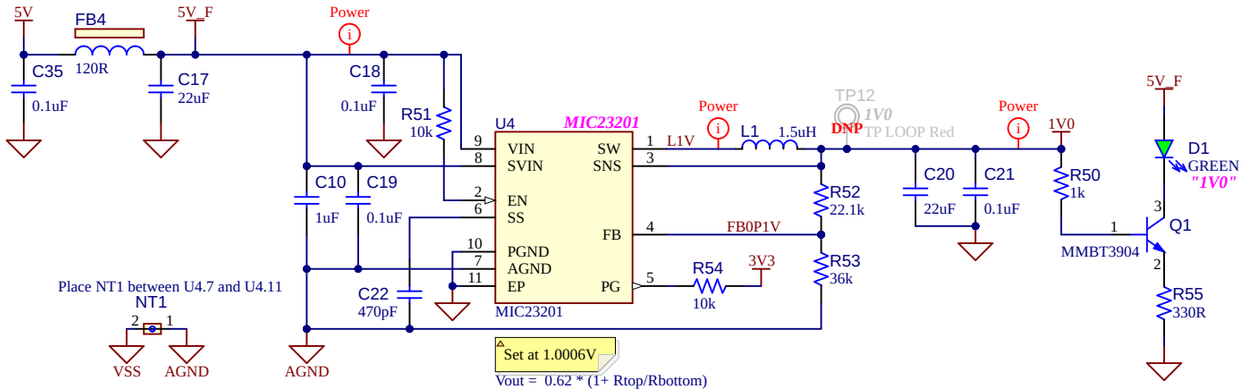
Default Selections

1	Resistors: 1%, 100mW, 0402
2	Capacitors: X7R, 50V, 0402

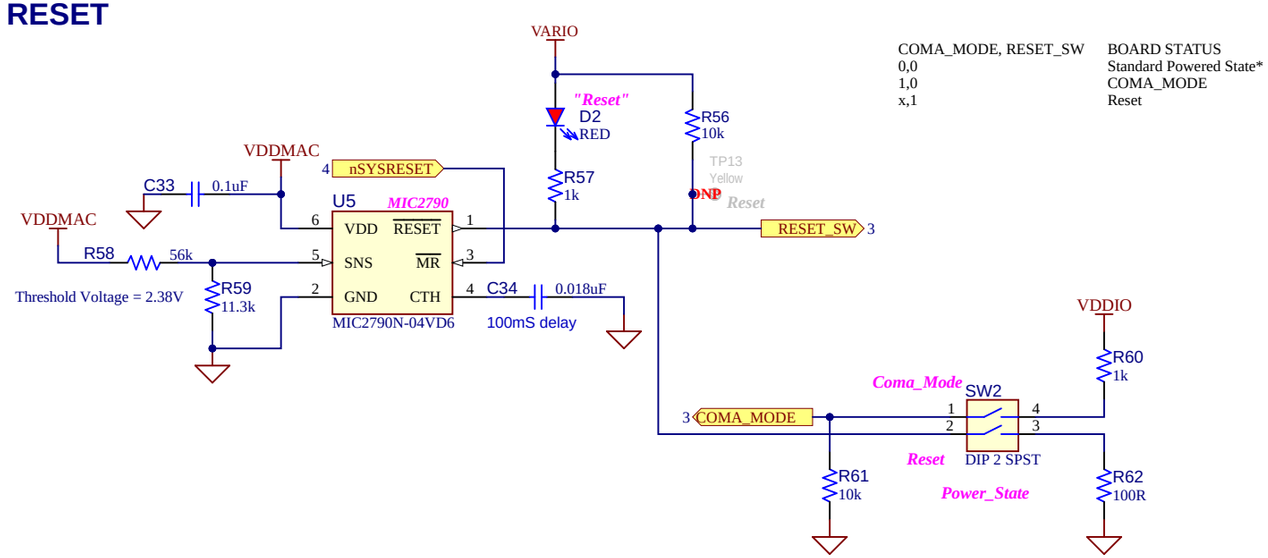
Project Owner: Alexys Antell		MICROCHIP	
PCB Layout Contact: Alexys Antell			
PartNumber: EV13K40A	Project Title: *VSC8541 EDS2 Daughter Card*	Variant: Standard	
Sheet Title: Title Page			Designed with Altium
Size: B	SCH #: 02-01275 / PCB #: 04-12339	Rev: 1 / Rev: 1	Date: 5/28/2025 / Sheet 1 of 5
File: 1_Title-Page_UNG10097_C0.SchDoc			Altium.com

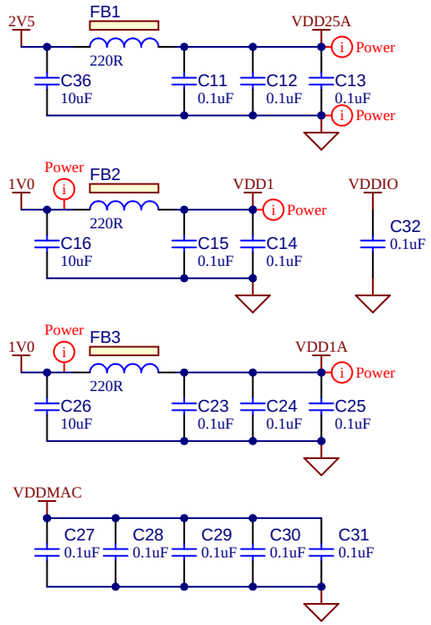
Power

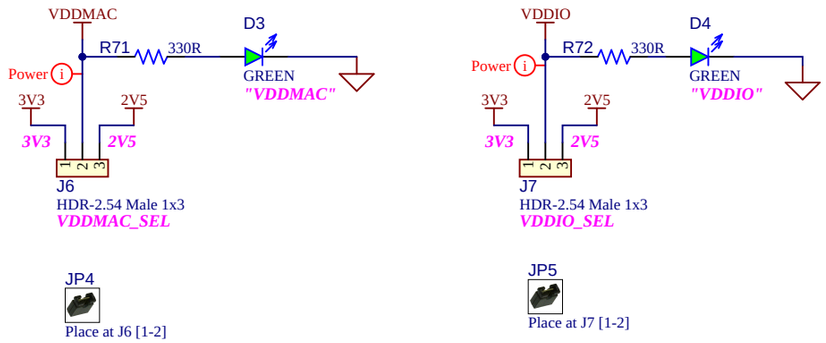
1V0



RESET







Project Owner: Alexys Antell			
PCB Layout Contact: Alexys Antell			
PartNumber: EV13K40A	Project Title: VSC8541 EDS2 Daughter Card	Variant: Standard	
Sheet Title: Power			
Size: B	SCH #: 02-01275	Rev: 1	Date: 5/28/2025
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File: 2_Power_UNG10097_C0.SchDoc			

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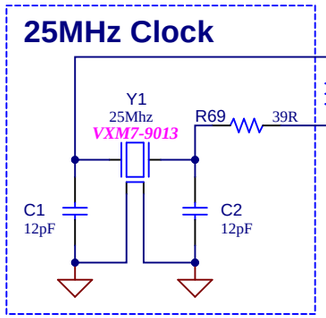
VSC8541-Clock-Straps

25MHz Clock



BOOT STRAPPING

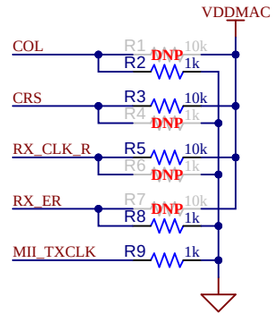
COL	MASTER/SLAVE MODE
0	Disabled*
1	Enabled

CRS	MDI/MDIX MODE
0	Disabled
1	Enabled*

RX_CLK_R	DEVICE OPERATION
0	Managed
1	Unmanaged*

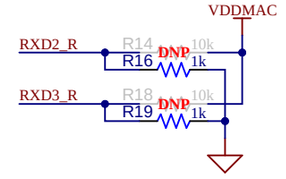
RX_ER	FORCED 1000BASE-T MODE
0	Disabled*
1	Enabled

MII_TXCLK	INTERFACE MODE
0	RGMII/RMII*
1	GMII/MII (Not Used)



LINK ADVERTISING

RXD2_R, RXD3_R	LINK ADVERTISMENT
0,0	10/100/100 FDX/HDX, autoneg ON*
0,1	10/100 FDX/HDX, autoneg ON
1,0	100BTX, HDX Forced, autoneg OFF
1,1	10BT, HDX Forced. autoneg OFF



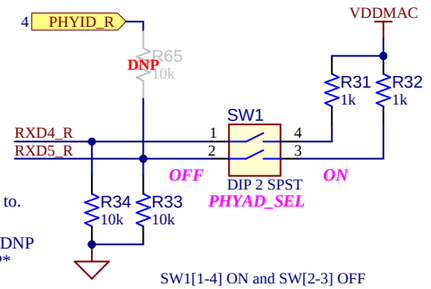
PHY ADDRESSING

RXD5_R, RXD4_R	PHY ADDRESS
0,0	PHYAD0
0,1	PHYAD1*
1,0	PHYAD2
1,1	PHYAD3

NOTE: PHYAD[3:0] = 0x1 and x=PHYID

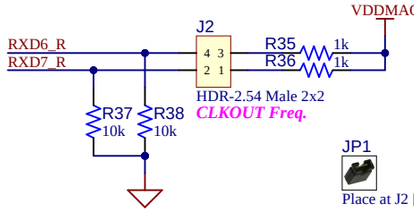
NOTE 2: The PHY Adresses will need to be configured to that of which port that the card is connected to. (IE Port 1 - PHYAD0, Port 2 = PHYAD1, etc.)

NOTE 3: When using U3 to set PHYAD1, R32 and R33 DNP
When using SW1 to set PHYAD1, R65 is DNP*



SW1[1-4] ON and SW[2-3] OFF

CLKOUT FREQUENCY

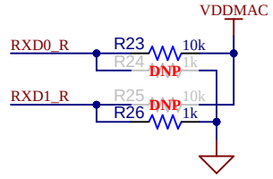


RXD7_R, RXD6_R	CLKOUT Frequency
00	25Mhz
01	50MHz*
10	125MHz
11	Reserved

*CLKOUT must be configured to be 50MHz for RMII Mode

RGMII CLOCK DELAY

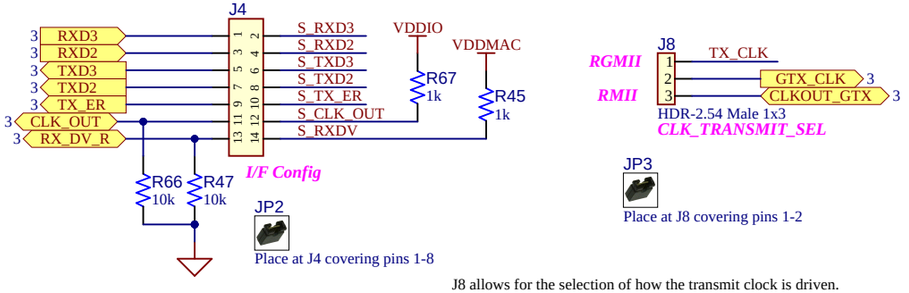
RXD0_R, RXD1_R	RX_CLK & TX_CLK DELAY SETTING
0,0	000 - 0.2 ns
0,1	101 - 1.1 ns
1,0	100 - 2.0 ns*
1,1	110 - 2.6 ns



Project Owner: Alexys Antell			
PCB Layout Contact: Alexys Antell			
PartNumber: EV13K40A	Project Title: VSC8541 EDS2 Daughter Card	Variant: Standard	
Sheet Title: VSC8541-Clock-Straps			Designed with Altium
Size: B	SCH #: 02-01275	Rev: 1	Date: 5/28/2025
	PCB #: 04-12339	Rev: 1	Sheet 3 of 5
File: 3_VSC8541-Clock-Straps_UNG10097_C0.SchDoc			Altium.com

SODIMM Edge Connector

RGMII/RMII Configuration



*RGMII: Populate 2x4 shunt across pins 1-2, 3-4, 5-6, and 7-8.

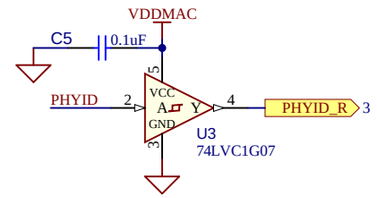
RMII: Populate 2x4 shunt across pins 9-10, 11-12, and 13-14.

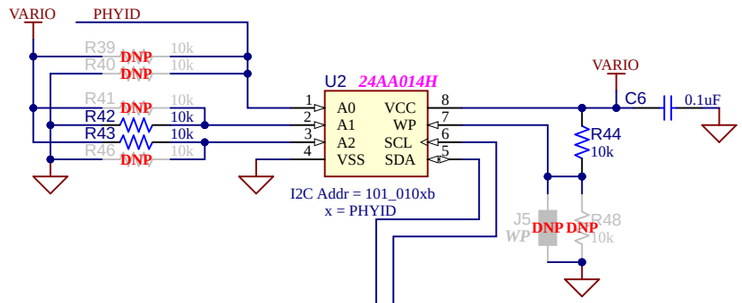
J8 allows for the selection of how the transmit clock is driven.

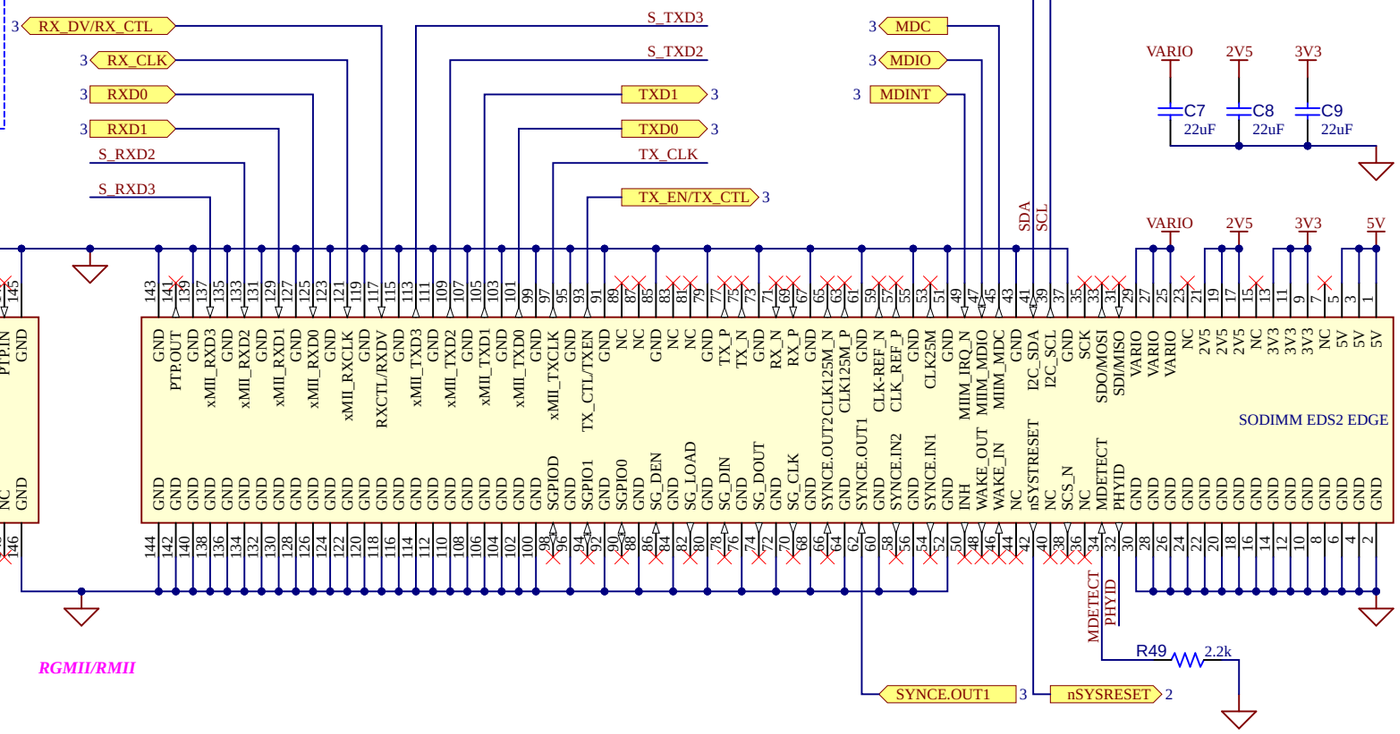
*RGMII Mode: U1[37] must be driven by the host. Shunt pins 1-2

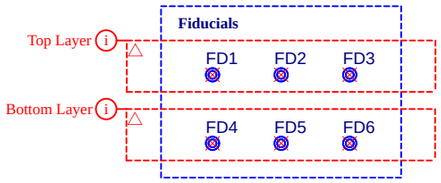
RMII Mode: U1[37] must be driven by clkout (IE. U1[54]). Shunt pins 2-3

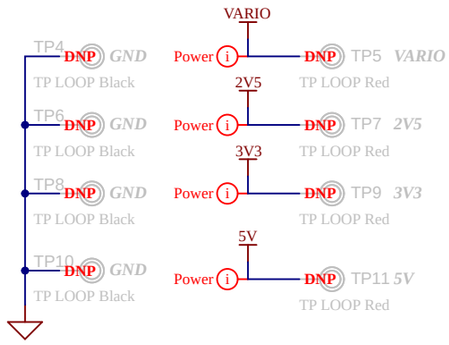
NOTE: When using U3 to set PHYAD1, R32 and R33 must be removed
U3 is not used by default











LABEL1

[ASSY# / REV]
SN: [SERIAL]
[DATE yyyy.mm.dd]

PCBA LABEL 18X6mm

Project Owner: Alexys Antell			
PCB Layout Contact: Alexys Antell			
PartNumber: EV13K40A	Project Title: VSC8541 EDS2 Daughter Card	Variant: Standard	
Sheet Title: SODIMM Edge Connector			
Size: B	SCH #: 02-01275	Rev: 1	Date: 5/28/2025
	PCB #: 04-12339	Rev: 1	Sheet 4 of 5
File: 5_SODIMM-Edge-Connector_UNG10097_C0.SchDoc			

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Ethernet-Port

RJ-45 ICM

Project Owner: Alexys Antell			
PCB Layout Contact: Alexys Antell			
PartNumber: EV13K40A	Project Title: *VSC8541 EDS2 Daughter Card*	Variant: Standard	
Sheet Title: Ethernet-Port			Designed with Altium — Altium.com
Size: B	SCH #: 02-01275	Rev: 1	Date: 5/28/2025
	PCB #: 04-12339	Rev: 1	Sheet 5 of 5
File: 4_Copper-Port_UNG10097_C0.SchDoc			