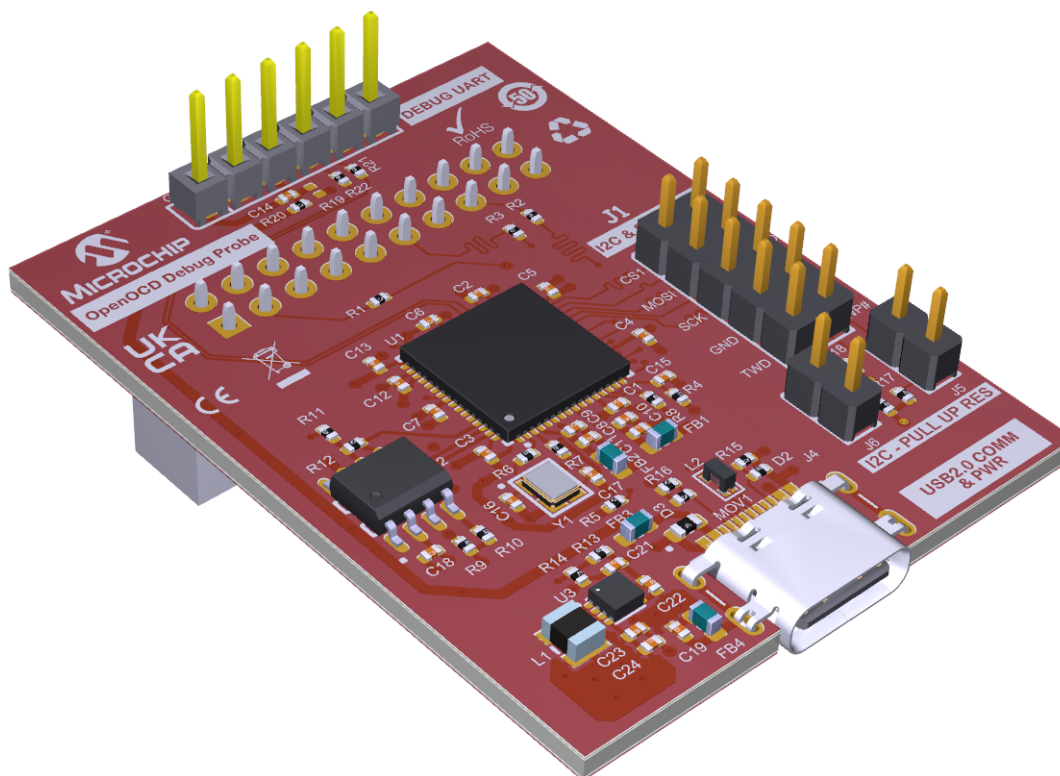


Scope

This user guide provides detailed information on the overall design and features of the OpenOCD Debug Probe (DV22S07A).

Figure 1. OpenOCD Debug Probe



Reference Document

The following document is recommended as a supplemental reference resource:

- FTDI FT4232 data sheet, available on [this page](#).

1. Kit Content

The OpenOCD Debug Probe kit includes the following:

- The OpenOCD board inside an ESD bag
- One 20 cm 1x6 female-to-female ribbon cable for serial connection to the target board FTDI port
- One short ribbon adapter: IDC 2x10 male to IDC 2x10 female for flexible adaptation to the target board JTAG port

2. Product Overview

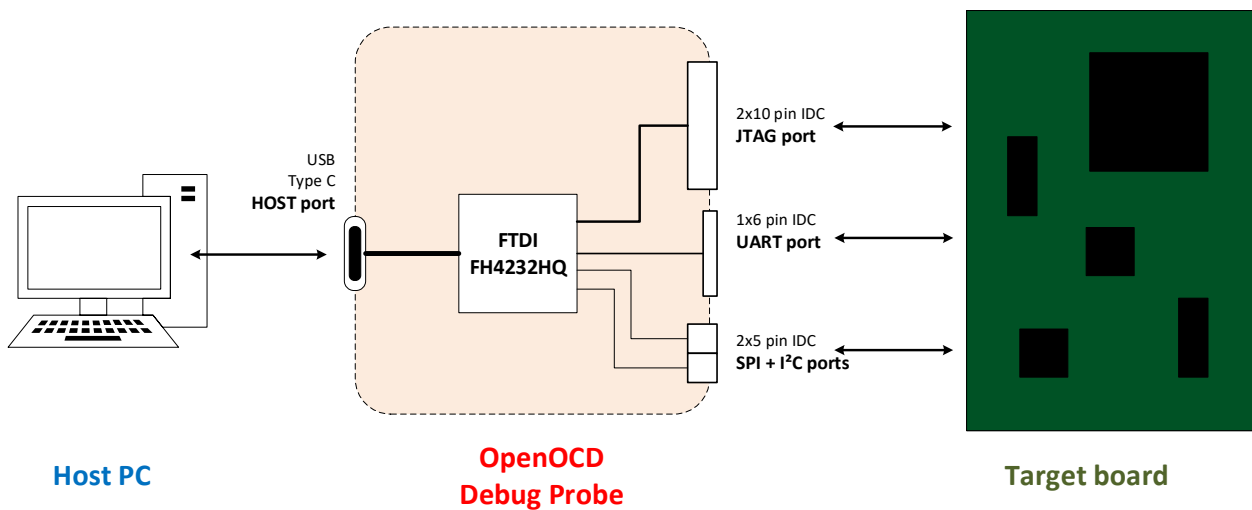
The OpenOCD Debug Probe is an implementation of the FTDI FT4232 product. The probe connects to and is powered by a host PC via a standard USB Type-C cable (not provided).

The on-board FT4232HQ chip provides bidirectional conversion between the host PC and the following dedicated debug channels:

- One JTAG port
- One UART port
- One I²C port with optional on-board pull-ups
- One SPI port

The user may use either one or several ports at a time, depending on the relevant target board and application.

Figure 2-1. OpenOCD Diagram



WARNING The OpenOCD Debug Probe does not have level shifters and can only be used with 3.3V JTAG logic.

2.1. Specifications

Table 2-1. OpenOCD Debug Probe Specifications

Characteristic	Specification
Board identification	OpenOCD Debug Probe
Board supply voltage	USB-powered
Temperature	Operating: 0°C to +70°C
Relative humidity	0 to 90% (non-condensing)
Main board dimensions	48 mm × 36 mm × 18.5 mm
RoHS status	RoHS 3-compliant
China RoHS status	EFUP50
REACH status	REACH-compliant

2.2. Power Source

The OpenOCD Debug Probe is powered via the USB Type-C connector (J4), which also acts as a data transmission link with the host PC.

On-board power management (USB 5Vcc to system 3.3Vcc) is handled via a MIC23150 buck converter.

3. Port Descriptions

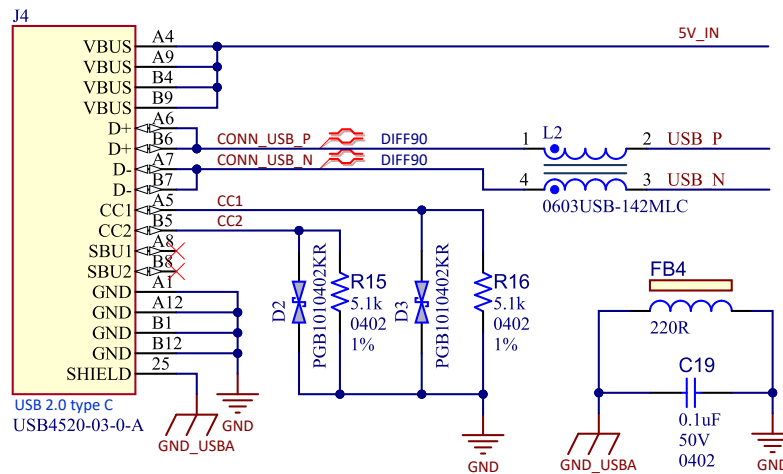
3.1. On-Board Connectors

Table 3-1. OpenOCD Debug Probe Interface Connectors

Connector	Type	Interfaces with
J1	2x5 pin IDC male header	Target SPI + I ² C
J2	2x10 pin IDC female header with orientation notch	Target JTAG
J3	1x6 pin IDC male header	Target UART
J4	USB 2.0 Type-C	Host PC
J5	1x2 pin IDC male header	Jumper for optional pull-up on I ² C clock
J6	1x2 pin IDC male header	Jumper for optional pull-up on I ² C data

3.2. From USB Port to Host PC

Figure 3-1. USB-C Port



3.3. JTAG Debug Port

Figure 3-2. JTAG Port

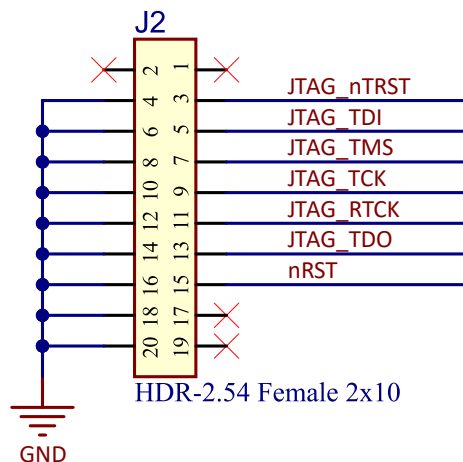


Table 3-2. J2, JTAG Port Pinout

Pin	Signal	Function
3	JTAG_nTRST	Target reset
5	JTAG_TDI	Target data input
7	JTAG_TDO	Target data output
9	JTAG_TCK	Target clock
11	JTAG_RTCK	Target return clock
13	JTAG_TDO	Target data output
15	nRST	System reset
1, 2, 17, 19	-	Not connected
4, 6, 8, 10, 12, 14, 16, 18, 20	GND	System ground

3.4. UART Communication Port

Figure 3-3. UART Port

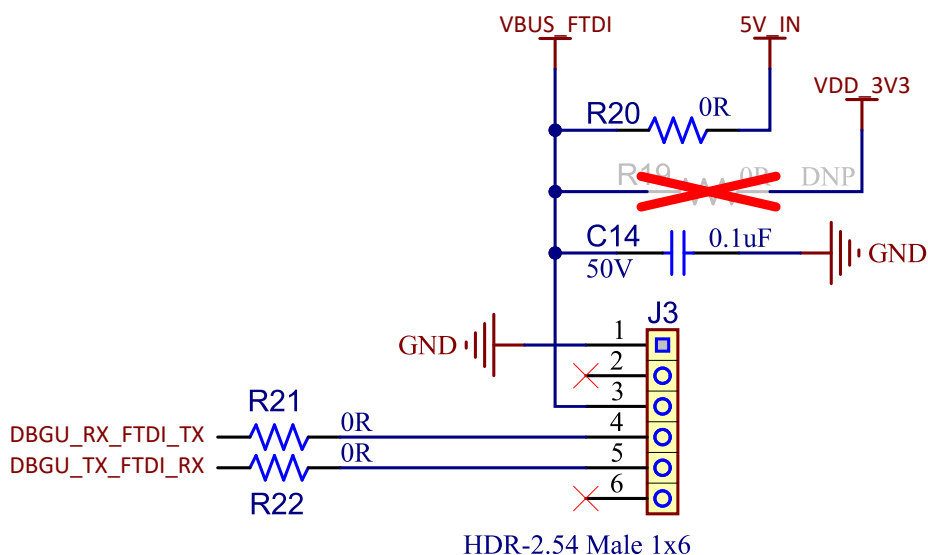


Table 3-3. J2, UART Port Pinout

Pin	Signal	Function
1	GND	System ground
2	-	Not connected
3	Vdd	5Vcc from USB, provides 5Vcc to target
4	UART Tx	Transmission signal
5	UART Rx	Reception signal
6	-	Not connected

3.5. SPI/I²C Debug Ports

Figure 3-4. SPI-I²C Ports

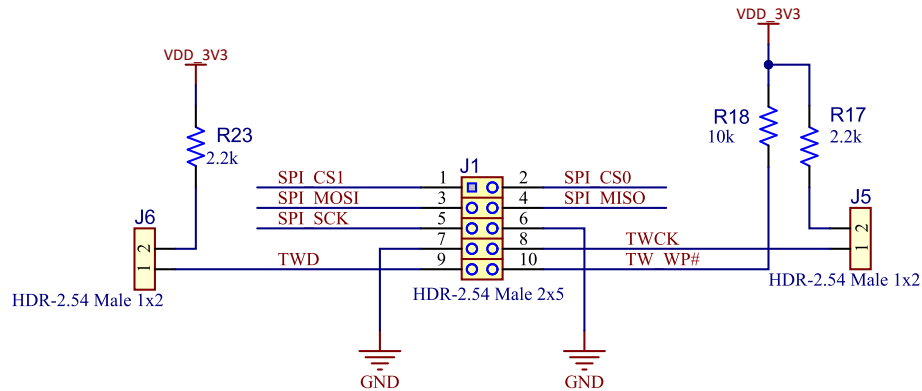


Table 3-4. J1, SPI and I²C Port Pinout

Pin	Signal	Function
1	SPI_CS1	SPI chip select 1
2	SPI_CS0	SPI chip select 0
3	SPI_MISO	SPI MISO (host in/client out)
4	SPI_MOSI	SPI MISO (host out/client in)
5	SPI_SCK	SPI clock
6	GND	System ground
7	GND	System ground
8	TWCK	I ² C clock
9	TWD	I ² C data
10	TW_WP#	I ² C write protect

4. Installation and Operation

Refer to www.microchip.com/en-us/development-tool/DV22S07A.

5. Appendix. Schematics and Layouts

This appendix contains the following schematics and layouts:

- OpenOCD Debug Probe Schematic
- OpenOCD PCBA Top
- OpenOCD PCBA Bottom

Figure 5-1. OpenOCD Debug Probe Schematic

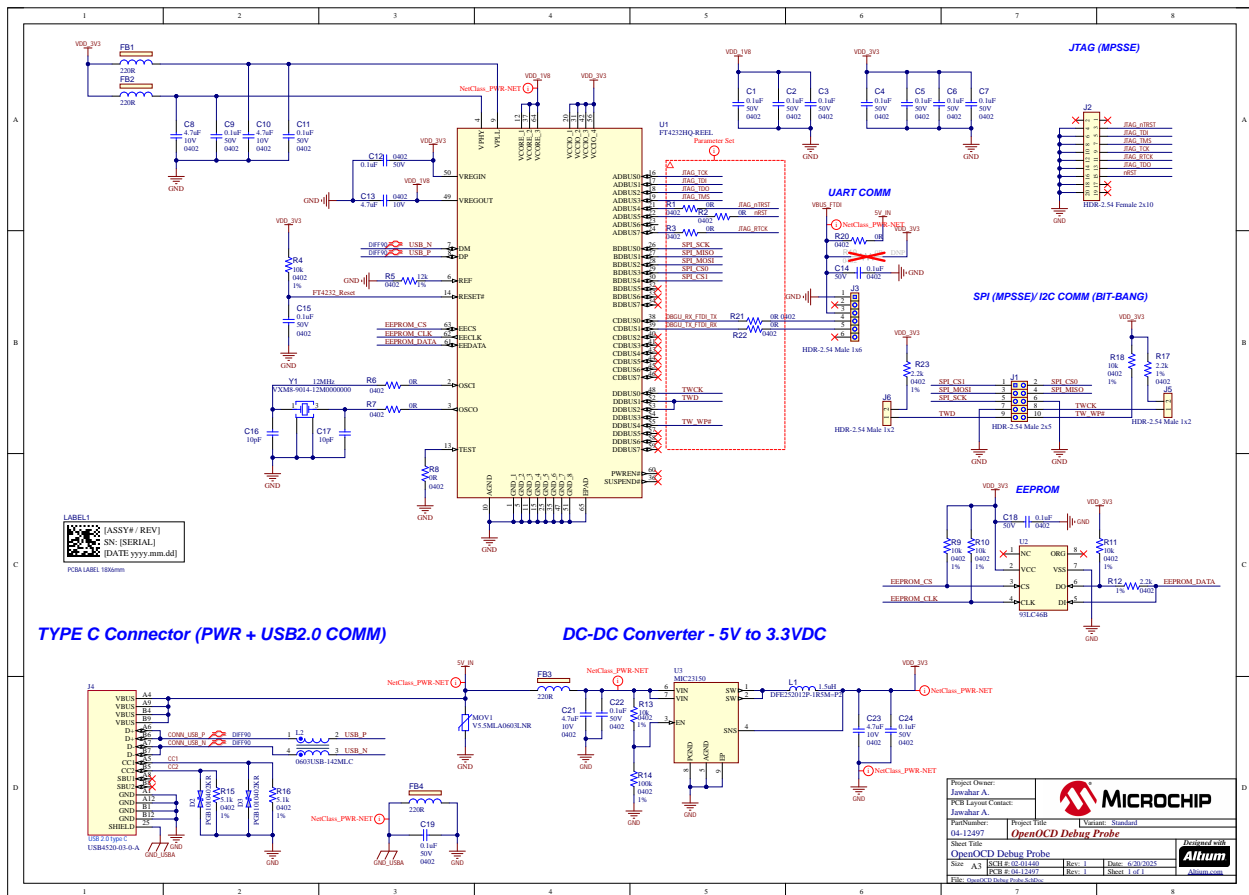


Figure 5-2. OpenOCD PCBA Top

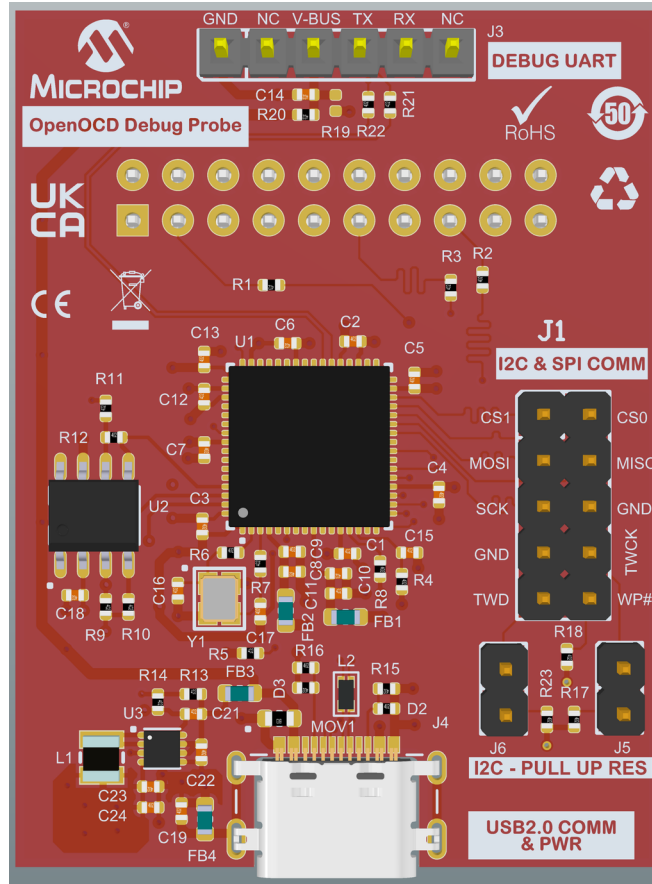
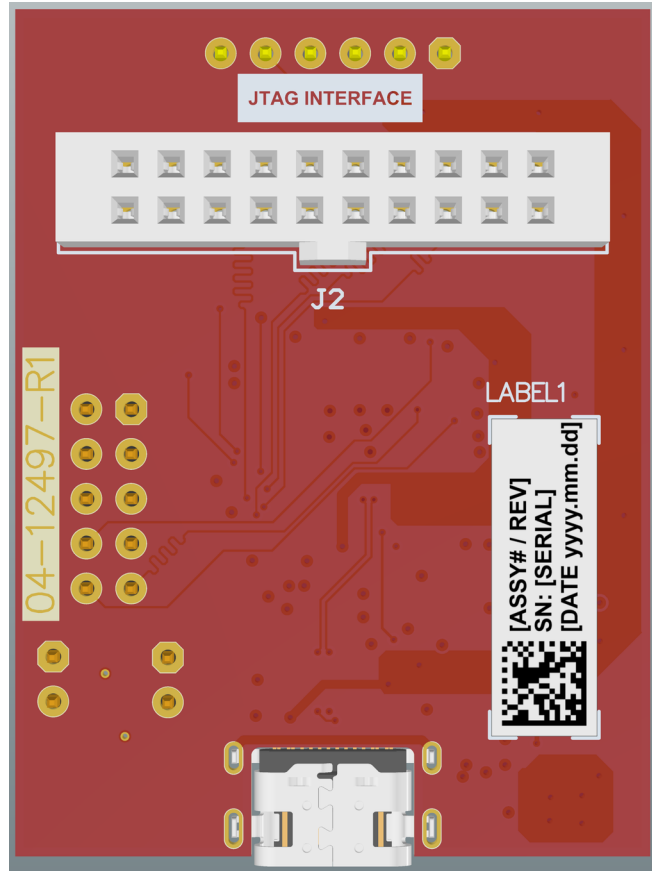


Figure 5-3. OpenOCD PCBA Bottom



6. Revision History

6.1. DS50004043A - 01/2026

First issue.

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