

FDMA1032CZ

20V Complementary PowerTrench® MOSFET

General Description

This device is designed specifically as a single package solution for a DC/DC 'Switching' MOSFET in cellular handset and other ultra-portable applications. It features an independent N-Channel & P-Channel MOSFET with low on-state resistance for minimum conduction losses. The gate charge of each MOSFET is also minimized to allow high frequency switching directly from the controlling device. The MicroFET 2x2 package offers exceptional thermal performance for its physical size and is well suited to switching applications.



Features

■ Q1: N-Channel

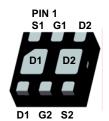
3.7 A, 20V. $R_{DS(ON)} = 68 \text{ m}\Omega$ @ $V_{GS} = 4.5V$ $R_{DS(ON)} = 86 \text{ m}\Omega$ @ $V_{GS} = 2.5V$

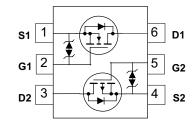
■ Q2: P-Channel

-3.1 A, -20V. R_{DS(ON)} = 95 m Ω @ V_{GS} = -4.5V R_{DS(ON)} = 141 m Ω @ V_{GS} = -2.5V

- Low profile 0.8 mm maximum in the new package MicroFET 2x2 mm
- HBM ESD protection level > 2 kV (Note 3)
- RoHS Compliant
- Free from halogenated compounds and antimony oxides







MicroFET 2x2 Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter		Q1	Q2	Units
V _{DS}	Drain-Source Voltage		20	-20	V
V _{GS}	Gate-Source Voltage		±12	±12	V
1	Drain Current - Continuous	(Note 1a)	3.7	-3.1	A
I _D	– Pulsed		6	-6	
P _D	Power Dissipation for Single Operation (Note 1a)		1.4		W
	(Note 1b)		0.7		
T _J , T _{STG}	Operating and Storage Junction Temperature Range		-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	86 (Single Operation)	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1b)	173 (Single Operation)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1c)	69 (Dual Operation)] 'C/V
R _{0,JA}	Thermal Resistance, Junction-to-Ambient	(Note 1d)	151 (Dual Operation)]

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
032	FDMA1032CZ	7"	8mm	3000 units

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Symbol	Parameter	Test Conditions	Type	Min	Тур	Max	Units
Off Cha	racteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \qquad I_{D} = 250 \mu\text{A} \\ V_{GS} = 0 \text{ V}, \qquad I_{D} = -250 \mu\text{A}$	Q1 Q2	20 –20			V
<u>ΔBV_{DSS}</u> ΔT _J	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, Referenced to 25°C I_D = -250 μ A, Referenced to 25°C	Q1 Q2		15 –12		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16 \text{ V}, \qquad V_{GS} = 0 \text{ V}$ $V_{DS} = -16 \text{ V}, \qquad V_{GS} = 0 \text{ V}$	Q1 Q2			1 –1	μΑ
I _{GSS}	Gate-Body Leakage	$V_{GS} = \pm 12 \text{ V}, \qquad V_{DS} = 0 \text{ V}$	All			±10	μА
On Chai	racteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS},$ $I_{D} = 250 \mu A$ $V_{DS} = V_{GS},$ $I_{D} = -250 \mu A$	Q1 Q2	0.6 -0.6	1.0 –1.0	1.5 –1.5	V
$\Delta V_{GS(th)} \over \Delta T_J$	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C I_D = -250 μA, Referenced to 25°C	Q1 Q2		-4 4		mV/°C
R _{DS(on)}	Static Drain-Source On-Resistance	$V_{GS} = 4.5 \text{ V}, I_D = 3.7 \text{ A}$ $V_{GS} = 2.5 \text{ V}, I_D = 3.3 \text{ A}$ $V_{GS} = 4.5 \text{ V}, I_D = 3.7 \text{ A}, T_J = 125^{\circ}\text{C}$	Q1		37 50 53	68 86 90	mΩ
		$V_{GS} = -4.5V$, $I_D = -3.1$ A $V_{GS} = -2.5$ V, $I_D = -2.5$ A $V_{GS} = -4.5$ V, $I_D = -3.1$ A, $T_J = 125^{\circ}$ C	Q2		60 88 87	95 141 140	mΩ
g fs	Forward Transconductance	$V_{DS} = 10 \text{ V}, \qquad I_{D} = 3.7 \text{ A} $ $V_{DS} = -10 \text{ V}, \qquad I_{D} = -3.1 \text{ A}$	Q1 Q2		16 –11		S
Dynami	c Characteristics						
	Input Capacitance	Q1 V _{DS} = 10 V, V _{GS} = 0 V, f = 1.0 MHz	Q1 Q2		340 540		pF
C _{oss}	Output Capacitance	Q2	Q1 Q2		80 120		pF
C _{rss}	Reverse Transfer Capacitance	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz}$	Q1 Q2		60 100		pF
Switchir	ng Characteristics (Note	; 2)					
$t_{\text{d(on)}}$	Turn-On Delay Time	Q1 V _{DD} = 10 V, I _D = 1 A,	Q1 Q2		8 13	16 24	ns
t _r	Turn-On Rise Time	V_{GS} = 4.5 V, R_{GEN} = 6 Ω	Q1 Q2		8 11	16 20	ns
$t_{\text{d(off)}}$	Turn-Off Delay Time	$\begin{bmatrix} Q2 \\ V_{DD} = -10 \text{ V}, I_{D} = -1 \text{ A}, \end{bmatrix}$	Q1 Q2		14 37	26 59	ns
t _f	Turn-Off Fall Time	V_{GS} = -4.5 V, R_{GEN} = 6 Ω	Q1 Q2		3 36	6 58	ns
Q _g	Total Gate Charge	Q1 $V_{DS} = 10 \text{ V}, I_{D} = 3.7 \text{ A}, V_{GS} = 4.5 \text{ V}$	Q1 Q2		4 7	6 10	nC
Q _{gs}	Gate-Source Charge	Q2	Q1 Q2		0.7 1.1		nC
Q_{gd}	Gate-Drain Charge	$V_{DS} = -10 \text{ V}, I_{D} = -3.1 \text{ A},$ $V_{GS} = -4.5 \text{ V}$	Q1 Q2		1.1 2.4		nC

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Туре	Min	Тур	Max	Units
Drain-S	ource Diode Character	istics and Maximum Ratings	6				
Is	Maximum Continuous Source-	-Drain Diode Forward Current	Q1			1.1	Α
			Q2			-1.1	
V _{SD}	Source-Drain Diode Forward	$V_{GS} = 0 \text{ V}, I_S = 1.1 \text{ A}$ (Note 2)	Q1		0.7	1.2	V
	Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -1.1 \text{ A}$ (Note 2)	Q2		-0.8	-1.2	
t _{rr}	Diode Reverse Recovery	Q1	Q1		11		ns
	Time	$I_F = 3.7 \text{ A}, dI_F/dt = 100 \text{ A/}\mu\text{s}$	Q2		25		
Q _{rr}	Diode Reverse Recovery	Q2	Q1		2		nC
	Charge	$I_F = -3.1 \text{ A, } dI_F/dt = 100 \text{ A/}\mu\text{s}$	Q2		9		

- 1. $R_{\theta,JA}$ is determined with the device mounted on a 1 in² oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta,JC}$ is guaranteed by design while $R_{\theta,JA}$ is determined by the user's board design.

 (a) $R_{\theta,JA} = 86$ °C/W when mounted on a 1 in² pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB. For single operation.

 - (b) $R_{\theta JA}$ = 173 °C/W when mounted on a minimum pad of 2 oz copper. For single operation.
 - (c) $R_{\theta JA}$ = 69 °C/W when mounted on a 1 in² pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB. For dual operation.
 - (d) $R_{\theta JA}$ = 151 °C/W when mounted on a minimum pad of 2 oz copper. For dual operation.



- 2. Pulse Test : Pulse Width < 300 us, Duty Cycle < 2.0%
- 3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics Q1 (N-Channel)

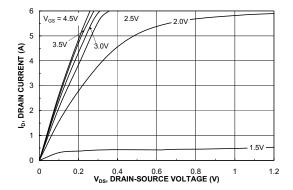


Figure 1. On-Region Characteristics.

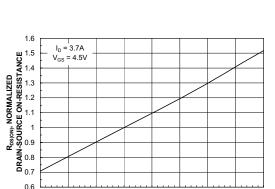


Figure 3. On-Resistance Variation with Temperature.

-50

0 25 50 75 100 T_J, JUNCTION TEMPERATURE (°C)

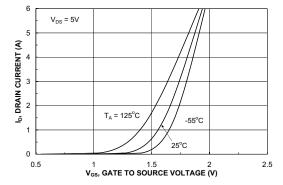


Figure 5. Transfer Characteristics.

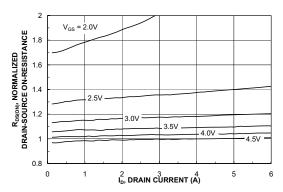


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

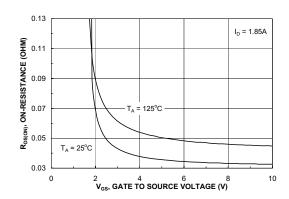


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

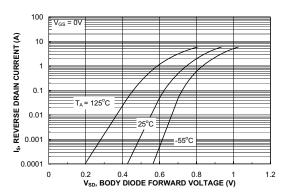
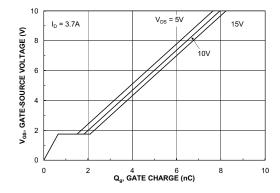


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

f = 1MHz V_{GS} = 0 V

Typical Characteristics Q1 (N-Channel)



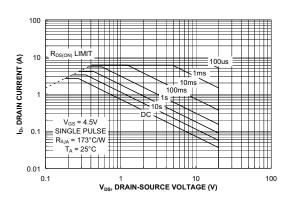
100 C_{rss} C_{oss} C_{ss} 20 V_{Ds}, DRAIN TO SOURCE VOLTAGE (V)

500

400

Figure 7. Gate Charge Characteristics.

Figure 8. Capacitance Characteristics.



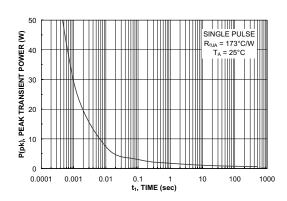


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

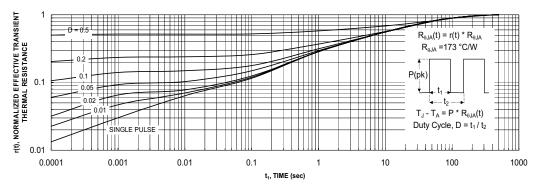


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

Typical Characteristics: Q2 (P-Channel)

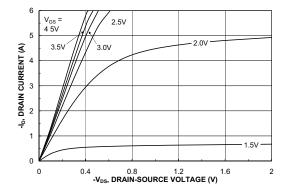


Figure 12. On-Region Characteristics.

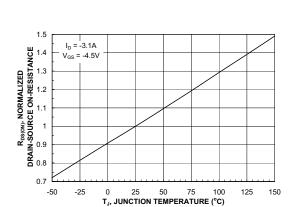


Figure 14. On-Resistance Variation with Temperature.

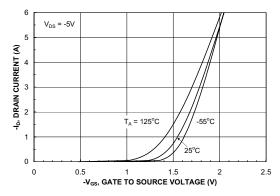


Figure 16. Transfer Characteristics.

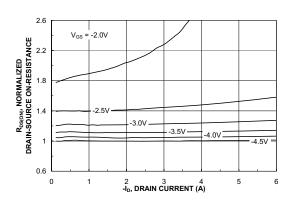


Figure 13. On-Resistance Variation with Drain Current and Gate Voltage.

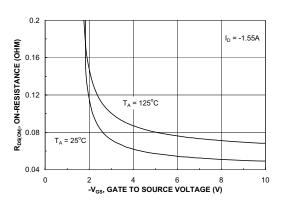


Figure 15. On-Resistance Variation with Gate-to-Source Voltage.

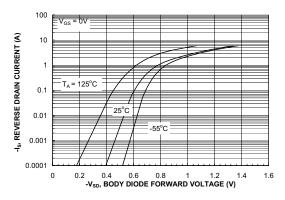
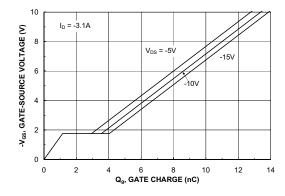


Figure 17. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: Q2 (P-Channel)



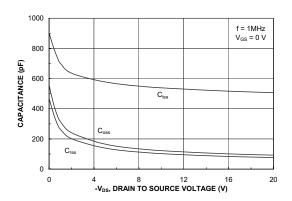
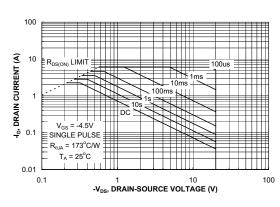


Figure 18. Gate Charge Characteristics.





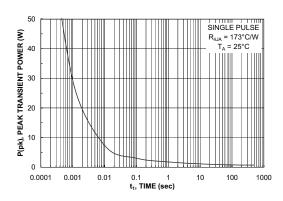


Figure 20. Maximum Safe Operating Area.

Figure 21. Single Pulse Maximum Power Dissipation.

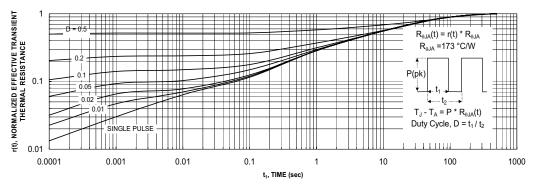
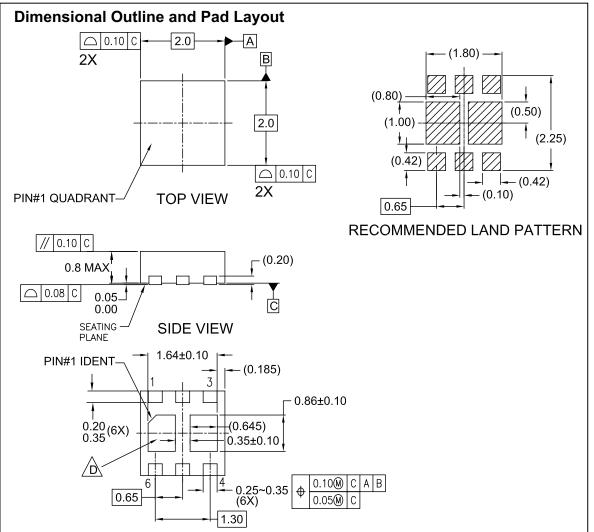


Figure 22. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.



BOTTOM VIEW

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION VCCC EXCEPT AS NOTED.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- NON-JEDEC DUAL DAP
- E. DRAWING FILE NAME : MLP06J rev3





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