Datasheet

Vela IF820

Version 2.2

Revision History

Version	Date	Notes	Contributors	Approver
1.0	10 Oct 2023	Initial release	Li Yuan Chang Mark Duncombe Rikki Horrigan Ryan Erickson	Jonathan Kaye
1.1	22 Jan 2024	Updates to pin tables in MHF4 Connector Variant Module Pin Definition and Integrated Antenna Variant Module Pin Definition	Li Yuan Chang Mark Duncombe Rikki Horrigan Ryan Erickson	Jonathan Kaye
1.2	7 May 2024	Add recommendation for 32.768KHz crystal. HCI UART IOs are required.	Li Yuan Chang Ryan Erickson	Jonathan Kaye
2.0	13 June 2024	Ezurio rebranding. Added crystal connection diagram to 10.4 Reference Schematic Design	Ryan Erickson Sue White	Jonathan Kaye
2.1	1 July 2024	Fix the antenna gain in Certified Antennas in Table 25	Li Yuan Chang	Jonathan Kaye
2.2	15 Oct 2024	Updates to Bluetooth Qualification	Dave Drogowski	Jonathan Kaye

Contents

Tables

1 Scope

This document describes the key hardware aspects of the Ezurio Vela IF820 Series wireless modules providing high-speed 4-wire UART interface for Bluetooth® / Bluetooth® LE connections. This document is intended to assist device manufacturers and related parties with the integration of this radio into their host devices. Data in this document is drawn from several sources and includes information found in the Infineon CYW20820 data sheet issued on September 26, 2022, along with other documents provided by Infineon.

Note: **The information in this document is subject to change.** Please contact Ezurio to obtain the most recent version of this document.

2 General Description

Ensure your estate of Classic Bluetooth devices don't get left behind in a growing environment of Bluetooth LE-only wireless options. Our Vela IF820 series being dual mode allows a single module to cover legacy Classic Bluetooth and migration to Bluetooth LE with a single part. This innovative series is based on **Infineon Technologies AIROC™ CYW20820** silicon. This range of flexible modules, adapters and DVKs marries all the benefits of the CYW20820 hardware, software, and tools offerings with our added value application software, services, certification, and support capabilities. The Vela IF820 series provides OEMs with multiple software development options suited to their resources and skillsets, with close attention to providing forward-looking replacement products for some of Ezurio's legacy Bluetooth product portfolio.

The Vela IF820 includes multiple small form factor PCB modules to suit any host board footprint and targets both hosted and hostless applications. They're accompanied by low cost, easy to use development kits and the addition of a certified, packaged USB Adapter to add Classic Bluetooth and Bluetooth LE connectivity to a variety of additional products in your Bluetooth portfolio. Together, Infineon and Ezurio drive down your total cost of ownership, design complexity and risk, while ensuring you the fastest time to market for your next dual mode Bluetooth IoT design.

Table 1: Product ordering information

Part	Description
453-00171R	Vela IF820 - Dual Mode Bluetooth Module, Integrated Antenna (Infineon CYW20820) - Tape / Reel
453-00171C	Vela IF820 - Dual Mode Bluetooth Module, Integrated Antenna (Infineon CYW20820) – Cut / Tape
453-00172R	Vela IF820 - Dual Mode Bluetooth Module, MHF4 Connector (Infineon CYW20820) - Tape / Reel
453-00172C	Vela IF820 - Dual Mode Bluetooth Module, MHF4 Connector (Infineon CYW20820) – Cut / Tape
453-00171-K1	Vela IF820 - Development Kit with integrated chip antenna
453-00172-K1	Vela IF820 - Development Kit with MHF4 Connector
450-00185	Vela IF820 - Dual Mode Bluetooth USB Adapter with integrated antenna variant (Infineon CYW20820)

3 Features Summary

The Ezurio Vela IF820 series device features are described in Table 2.

Table 2: Vela IF820 series wireless module features

Feature	Description
Variants	• Integrated antenna variant • MHF4 connector variant • USB Adapter
Bluetooth subsystem	• Complies with Bluetooth® core specification version 5.4 • Includes support for basic data rate (BR), EDR 2 Mbps and 3 Mbps, extended synchronous connection-oriented • Bluetooth® LE 1MPHY & 2 MPMY • Up to 10dBm EIRP output power • Excellent receiver sensitivity (-94dBm for Bluetooth® LE 1 Mbps)
Microcontroller (MCU)	• Powerful Arm® Cortex®-M4 core with a maximum speed of 96 MHz • Bluetooth® stack in ROM allowing standalone operation without any external MCU • 256-KB on-chip flash • 176-KB on-chip RAM Bluetooth® stack, peripheral drivers, security functions built into ROM (1 MB) allowing application to efficiently use on-chip flash • AES-128 and true random number generator (TRNG) • Security functions in ROM including elliptic curve digital signature algorithm (ECDSA) signature verification • Over-the-air (OTA) firmware updates
Peripherals	• Up to 22 GPIOs • I2C, I2S, UART, and PCM interfaces • Two Quad-SPI interfaces • Auxiliary ADC with up to 28 analog channels • Programmable key scan 20 ´ 8 matrix • Three-axis quadrature signal decoder • General-purpose timers and pulse width modulation (PWM) • Real-time clock (RTC) and watchdog timer (WDT)
Power management	• On-chip power-on reset (POR) • Integrated buck (DC-DC) and low drop out (LDO) regulators • On-chip software-controlled power management unit • On-chip 32 kHz low power oscillator (LPO) with optional external 32 kHz crystal oscillator support

4 Specifications

Table 3: Vela IF820 Specifications

Feature		Description
Physical Interface		54-pin LGA package for integrated antenna variant 44-pin LGA package for MHF4 connector variant
Bluetooth/BLE Interface		Host Controller Interface (HCI) using high speed UART
Main Chip		Infineon CYW20820
Input Voltage Requirements		3V Typ, 2.6V Min, 3.3V Max
I/O Signalling Voltage		Set to 3V or 1.8V, by the power domains connected to VDDIO
Operating Temperature		-40° to +85°C (-40° to +185°F)
Operating Humidity		Less than 85% RH (non-condensing)
Storage Temperature		-40° to +85°C (-40° to +185°F)
Storage Humidity		Less than 60% RH (non-condensing)
MSL (Moisture Sensitivity Level)		4 (module) N/A (USB Adapter)
Maximum Electrostatic Discharge		4kV Indirect application (In compliance with EN 301489)
Size – mm		Integrated Antenna variant: 9.3mm x 12.5mm x 2.15 mm MHF4 Connector variant: 7.5mm x 7.5mm x 2.15 mm USB Adapter: 18.39mm x 50.74mm x 11mm
Weight – g (oz.)		0.0003g (Integrated Antenna) 0.0001g (MHF4)
Bluetooth Media		Frequency Hopping Spread Spectrum (FHSS)
Bluetooth Standards		Bluetooth 5.4
Bluetooth Data Rates Supported		1, 2, 3 Mbps
Bluetooth Modulation	**GFSK@ 1 Mbps** **Pi/4-DQPSK@ 2 Mbps (EDR)**	8-DPSK@ 3 Mbps (EDR) BLE 1 Mbps, 2Mbps
Regulatory Certifications		FCC, IC, CE, UKCA, RCM, Japan, and Korea, Bluetooth SIG
Compliance		**ACMA** AS/NZS 2772.2:2016 Amd 1:2018 AS/NZS 4268:2017+Amd 1:2021 **CE** EN 62479:2010 EN 50663:2017 EN 300 328 V2.2.2 EN 62368-1 **EMC** ICES-003 Issue 7, Class B EN 301 489-1 V2.2.3 EN 301 489-17 V3.2.4 **FCC** FCC Part 15, Subpart B, Class B 47 CFR FCC Part 2.1091 47 CFR FCC Part 15.247 **Japan** Article 2 Paragraph 1 Item 19 **Korea** TBD
Certifications		***Bluetooth*® SIG Qualification**
		One Year Warranty
All specifications are subject to change without notice		

5 Block Diagram

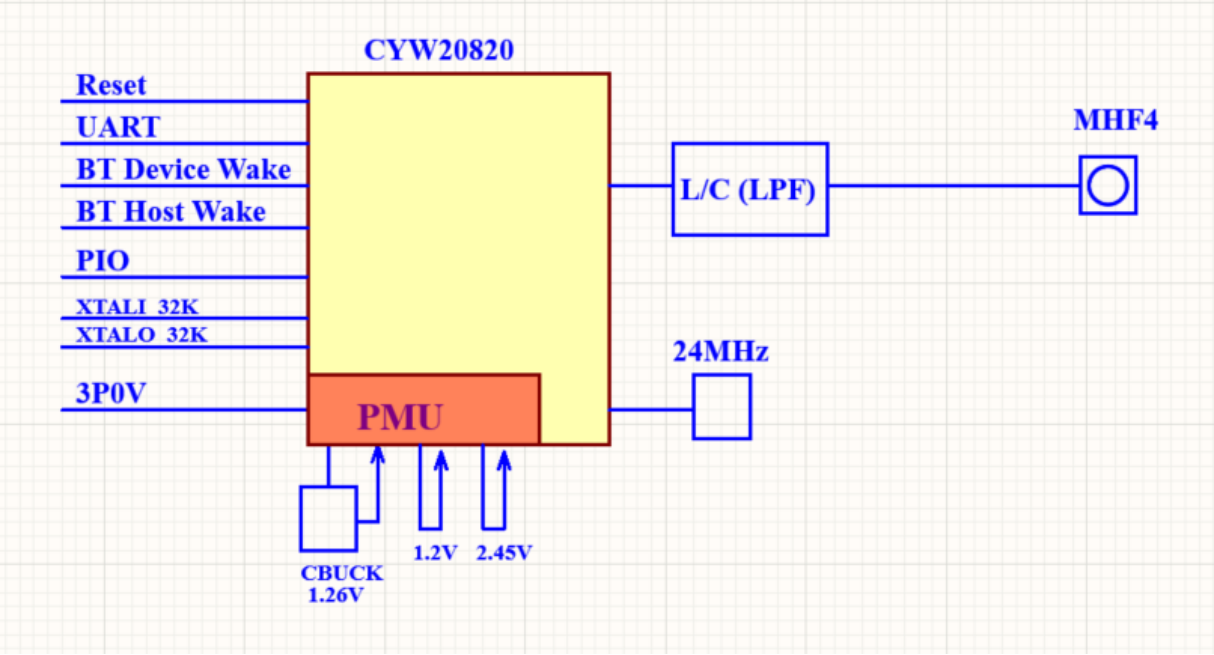


Figure 1: MHF4 connector variant diagram

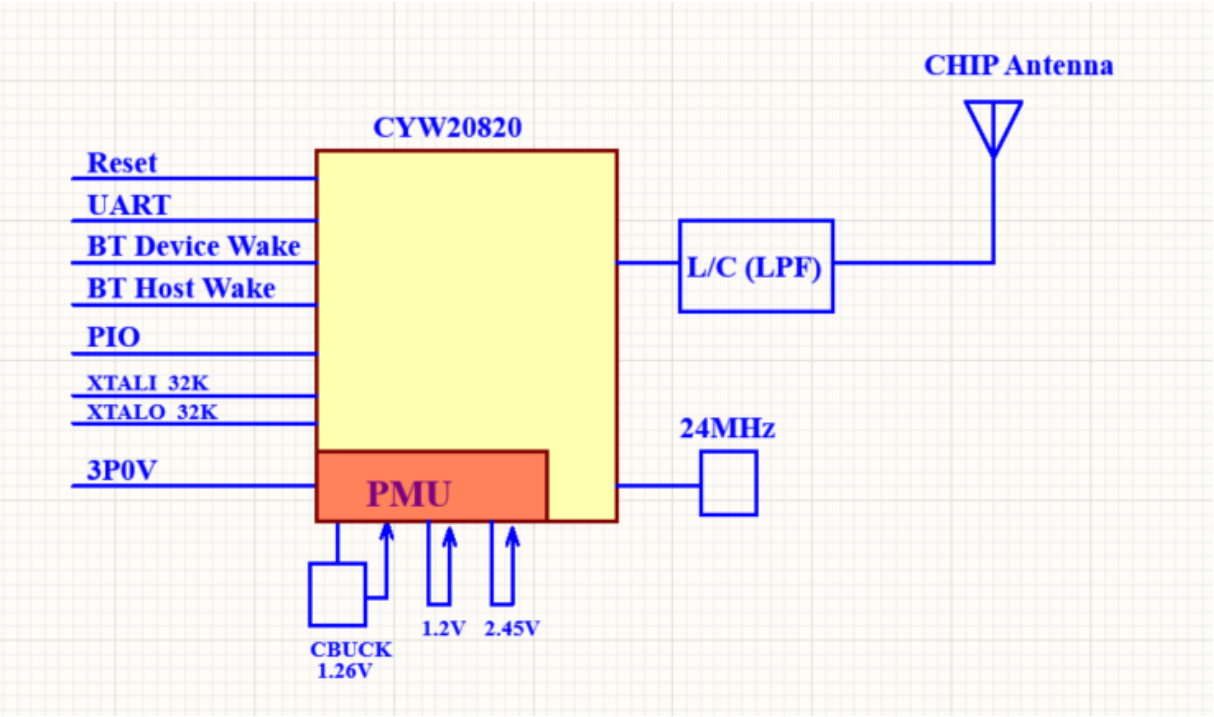


Figure 2: Integrated antenna variant diagram.

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 4 summarizes the absolute maximum ratings and Table 5 lists the recommended operating conditions for the Vela IF820 series wireless module. Absolute maximum ratings are those values beyond which damage to the device can occur. Operating this device outside of the listed maximum ratings and operating conditions may damage the device and void the warranty.

Note: Maximum rating for signals follows the supply domain of the signals.

Table 4: Absolute maximum ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
3P0V	Power supply for Internal Regulators	-0.5		3.45	V
VDDIO	DC supply voltage for digital I/O	-0.5		3.45	V

6.2 Recommended Operating Conditions

Table 5: Recommended operating conditions

Symbol (Domain)	Parameter	Min	Typ	Max	Unit
3P0V	Power supply for Internal Regulators	2.6	3.0	3.3	V
VDDIO	DC supply voltage for digital I/O	1.71	1.8/3.0	3.3	V
T-ambient	Ambient temperature	-40	25	85	°C

6.3 General DC Electrical Characteristics

Table 6 list the general DC electrical characteristics over recommended operating conditions (unless otherwise specified).

Table 6: General DC electrical characteristics (For 1.8V or 3V operation VIO)

Symbol	Parameter	Min	Typ	Max	Unit
VIL	Input low voltage (VDDIO = 3V)	—	—	0.8	V
VIH	Input high voltage (VDDIO = 3V)	2.4	—	—	
VIL	Input low voltage (VDDIO = 1.8V)	—	—	0.4	
VIH	Input high voltage (VDDIO = 1.8V)	1.4	—	—	
VOL	output low voltage	—	—	0.4	
VOH	output high voltage	VDDIO-0.4V	—	—	
IIL	input low current	—	—	1	uA
IIH	input high current	—	—	1	
IOL	output low current (VDDIO = 3V, VOL = 0.4V)	—	—	4	mA
IOL	output low current (VDDIO = 3V, VOL = 1.8V)	—	—	2	
IOH	output high current (VDDIO = 3V, VOH = 2.6V)	—	—	8	
IOH	output high current (VDDIO = 1.8V, VOH = 1.4V)	—	—	4	
CIN	Input capacitance	—	—	0.4	pF

7 RF Characteristics

7.1 Bluetooth Radio Characteristics

Table 7 through Table 10 describe the Bluetooth Basic Rate (BR) / BLE transmitter performance, Basic Rate (BR) / BLE receiver performance, Enhanced Data Rate (EDR) receiver performance, and current consumption conditions at 25°C.

Table 7: Basic Rate (BR) transmitter performance temperature at 25°C (3V)

Test Parameter		Min	Typ	Max	Bluetooth Spec.	Unit
RF Output Power[4] (test at MHF4 connector)	BR	–	6	7.5	0 ~ +20	dBm
	EDR 2M	–	1.5	2.5		
	EDR 3M	–	0.5	1.5		
Max EIRP (Integrated antenna variant)				10		dBm
Frequency Range		2.4	–	2.480	2.4 ≤ f ≤ 2.480	GHz

Table 8: Basic Rate (BR) receiver performance at (3V)

Test Parameter		Min	Typ	Max	Bluetooth Spec.	Unit
Sensitivity (1DH5)	BER ≤ 0.1%	–	-90	-87	≤ -70	dBm
Maximum Input	BER ≤ 0.1%	–	–	-20	≥ -20	dBm

Table 9: Enhanced Data Rate (EDR) receiver performance (3V)

Test Parameter		Min	Typ	Max	Bluetooth Spec.	Unit
Sensitivity (BER ≤ 0.01%)	π/4-DQPSK	–	-92.5	-89.5	≤ -70	dBm
	8-DPSK	–	-86	-83	≤ -70	dBm

Table 10: Bluetooth LE RF Specifications (3V)

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range	–	2402	–	2480	MHz
Rx sensitivity[3]	GFSK, 30.8% PER, 1Mbps	–	-94	-91	dBm
	GFSK, 30.8% PER, 2Mbps	–	-90	-87	dBm
RF Output Power[4] (test at MHF4 connector)	1M	–	6	7.5	dBm
	2M		6	7.5	dBm
Max EIRP (Integrated antenna variant)				10	dBm

Note[3]: Dirty TX is Off.

Note[4]: The Bluetooth LE TX power cannot exceed 10 dBm EIRP specification limit. The front-end losses and antenna gain/loss must be factored in so as not to exceed the limit.

7.2 Bluetooth Current Consumption

Table 11: Bluetooth current consumption, VBAT=3V VDDIO=3V, MHF4 connector variant

Operating Mode	Data Rate	Module 3V	Unit
TX	DH1	13.5	mA
	DH3	13.5	
	DH5	13.5	
	2DH1	20.2	
	2DH3	20	

Operating Mode	Data Rate	Module 3V	Unit
	2DH5	20.1	
	3DH1	19.8	
	3DH3	20	
	3DH5	20.1	
	LE1M	13.3	
	LE2M	13.3	
RX	DH5	6.2	mA
	LE1M	6.4	
	LE2M	7.4	

Table 12: Bluetooth current consumption, VBAT=3V VDDIO=3V, Integrated antenna variant

Operating Mode	Data Rate	Module 3V	Unit
TX	DH1	14.4	mA
	DH3	14.5	
	DH5	14.5	
	2DH1	19.9	
	2DH3	20.4	
	2DH5	20.4	
	3DH1	20.2	
	3DH3	20.1	
	3DH5	20.1	
	LE1M	16.4	
	LE2M	16.3	
RX	DH5	6.2	mA
	LE1M	6.4	
	LE2M	7.4	

Note: Current consumption is measured at average of the TX-on time

8 Host Interface Specifications

8.1 High-Speed UART Specifications

Table 13: UART timing specifications

Reference	Characteristics	Min	Typ	Max	Units
1	Delay time, UART_CTS_N LOW to UART_TXD valid.	—	—	1.5	Bit periods
2	Setup time, UART_CTS_N HIGH before midpoint of stop bit.		—	0.67	
3	Delay time, midpoint of stop bit to UART_RTS_N HIGH.	—	—	1.33	

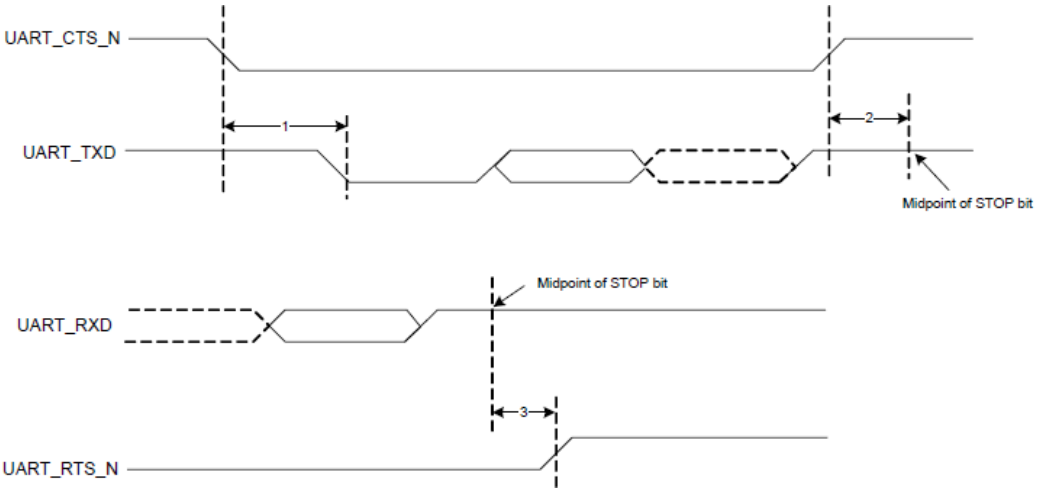


Figure 3: UART timing diagram

8.2 SPI Timing

Table 14: SPI mode 0 and 2

Reference	Characteristics	Min	Max	Units
1	Time from master assert SPI_CSN to first clock edge	45	—	ns
2	Setup time for MOSI data lines	6	1/2 SCK	
3	Idle time between subsequent SPI transactions	1 SCK	—	

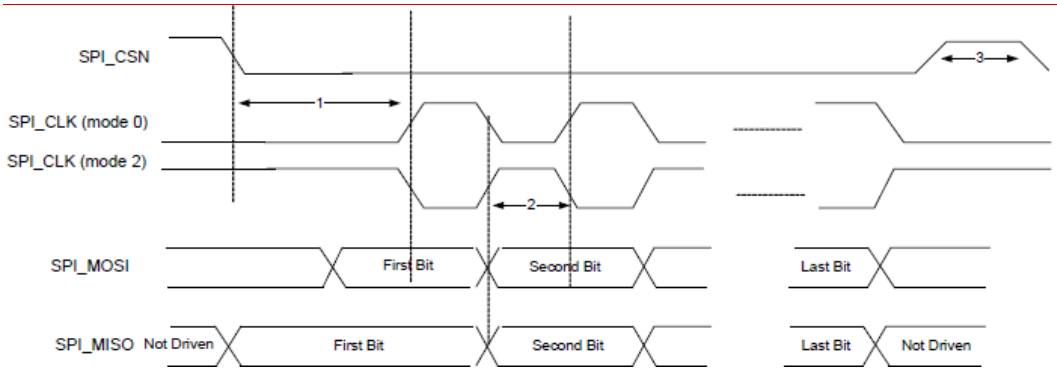


Figure 4: SPI timing, mode 0 and 2

Table 15: SPI mode 1 and 3

Reference	Characteristics	Min	Max	Units
1	Time from master assert SPI_CSN to first clock edge	45	—	ns
2	Setup time for MOSI data lines	6	1/2 SCK	
3	Idle time between subsequent SPI transactions	1 SCK	—	

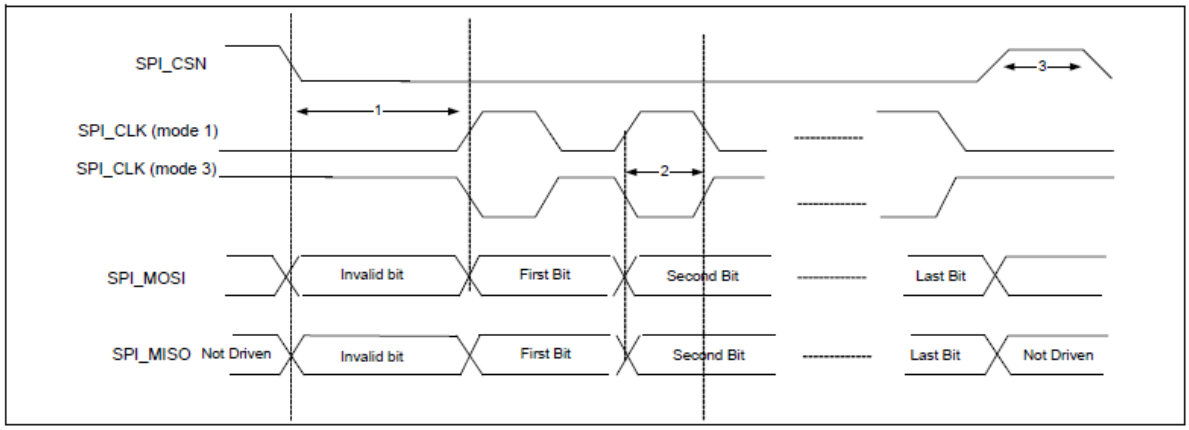


Figure 5: SPI timing, mode 1 and 3

8.3 I²C Timing

Table 16: I2C interface timing specifications (up to 1 MHz)

Reference	Characteristics	Min	Max	Units
1	Clock frequency	—	100 400 800 1000	KHz
2	START condition setup time	650	—	us
3	START condition hold time	280	—	
4	Clock low time	650	—	
5	Clock high time	280		
6	Data input hold time[1]	0	—	
7	Data input setup time	100	—	
8	STOP condition setup time	280		
9	Output valid from clock	—	400	
10	Bus free time[2]	650	—	

Notes: 1. As a transmitter, 125 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2. Time that the CBUS must be free before a new transaction can start.

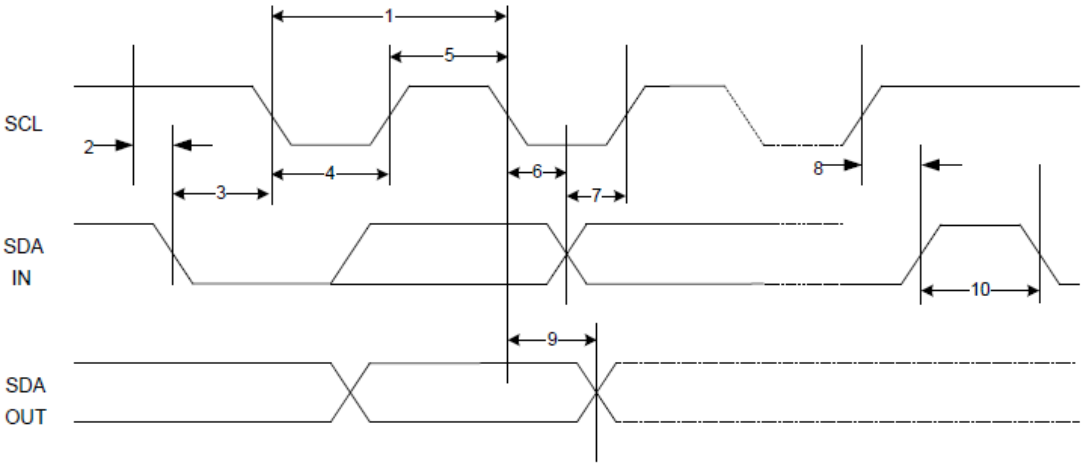


Figure 6: I²C interface timing diagram

8.4 I²S Timing

Table 17: Timing for I2S transmitters and receivers

	Transmitter				Receiver				Notes
	Lower limit		Upper limit		Lower limit		Upper limit		
	Min	Max	Min	Max	Min	Max	Min	Max	
Clock Period T	T_{tr}	-	-	-	T_r	-	-	-	[3]
Master mode: Clock generated by transmitter or receiver									
HIGH t_{HC}	0.35 x T_{tr}	-	-	-	0.35 x T_{tr}	-	-	-	[4]
LOW t_{LC}	0.35 x T_{tr}	-	-	-	0.35 x T_{tr}	-	-	-	[4]
Slave mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}	-	0.35 x T_{tr}	-	-	-	0.35 x T_{tr}	-	-	[3]
LOW t_{LC}	-	0.35 x T_{tr}	-	-	-	0.35 x T_{tr}	-	-	[3]
Rise time t_{RC}	-	-	0.15 x T_{tr}	-	-	-	-	-	[4]
Transmitter									
Delay t_{dtr}	-	-	-	0.8 x T	-	-	-	-	[5]
Hold time t_{htr}	0	-	-	-	-	-	-	-	[4]
Receiver									
Setup time t_{sr}	-	-	-	-	0.2 x T_{tr}	-	-	-	[6]
Hold time t_{hr}	-	-	-	-	0.2 x T_{tr}	-	-	-	[6]

Notes: [3] The system clock period T must be greater than Ttr and Tr because both the transmitter and receiver must be able to handle the data transfer rate.

[4] At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, tHC and tLC are specified with respect to T.

[5] In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than 0.35Tr, any clock that meets the requirements can be used.

[6] Because the delay (tdtr) and the maximum transmitter speed (defined by Ttr) are related, a fast transmitter driven by a slow clock edge can result in tdtr not exceeding tRC which means thtr becomes zero or negative. Therefore, the transmitter must guarantee that thtr is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than tRCmax, where tRCmax is not less than 0.15Ttr.

[7] To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.

[8] The data setup and hold time must not be less than the specified receiver setup and hold time.

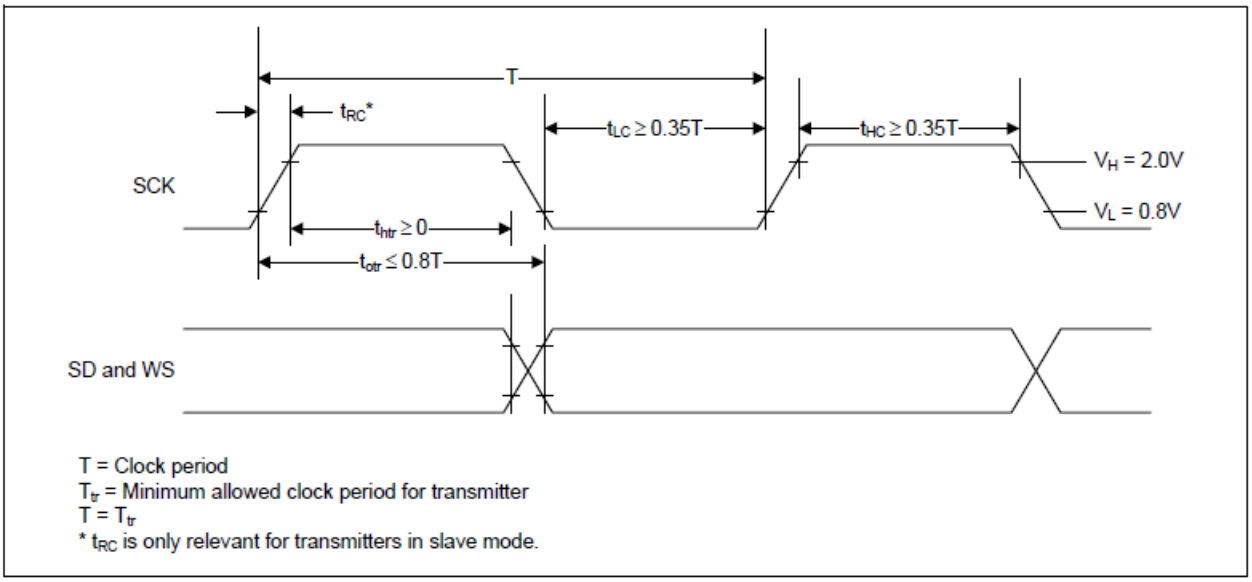


Figure 7: I²S transmitter timing

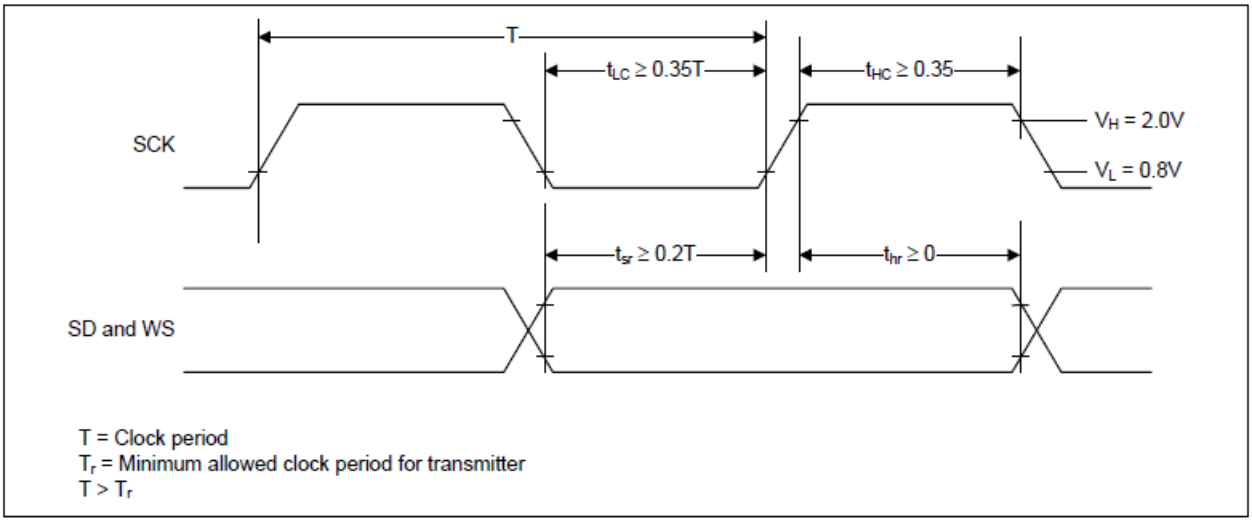


Figure 8: 2S receiver timing

9 MHF4 Connector Variant Footprint and Pin Definitions

Note: The following footprint and pin definitions apply to the Vela IF820. There are two module footprints, depending on which variant of the module is used. *It is important to ensure you are using the correct version on your design.*

9.1 MHF4 Connector Variant Mechanical Definition

Module dimensions of MHF4 connector variant module is 7.5 x 7.5 x 2.15 mm. Detail drawings are shown in Figure 9.

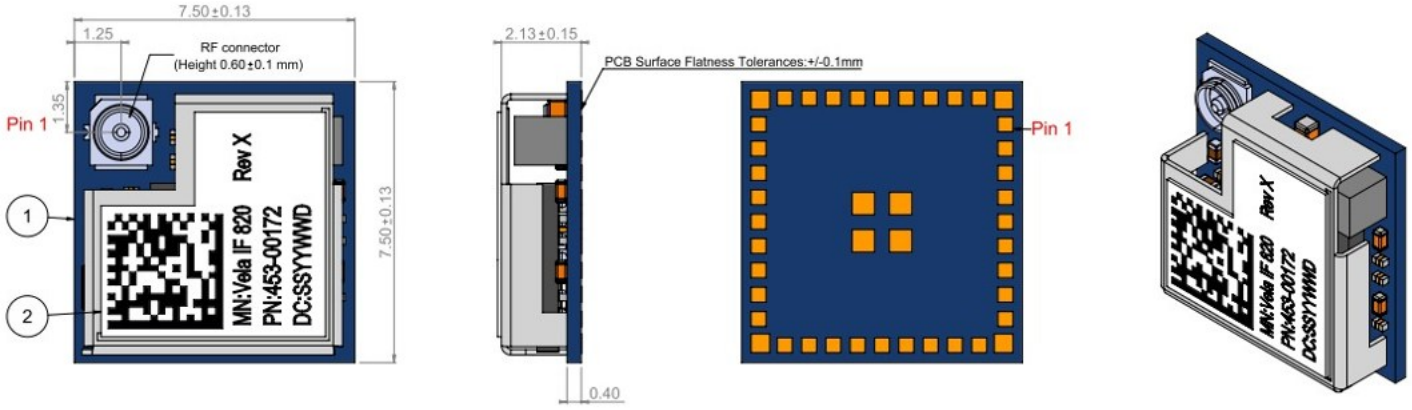


Figure 9: Mechanical Details – MHF4 Variant (453-00172)

9.2 MHF4 Connector Variant Module Footprint

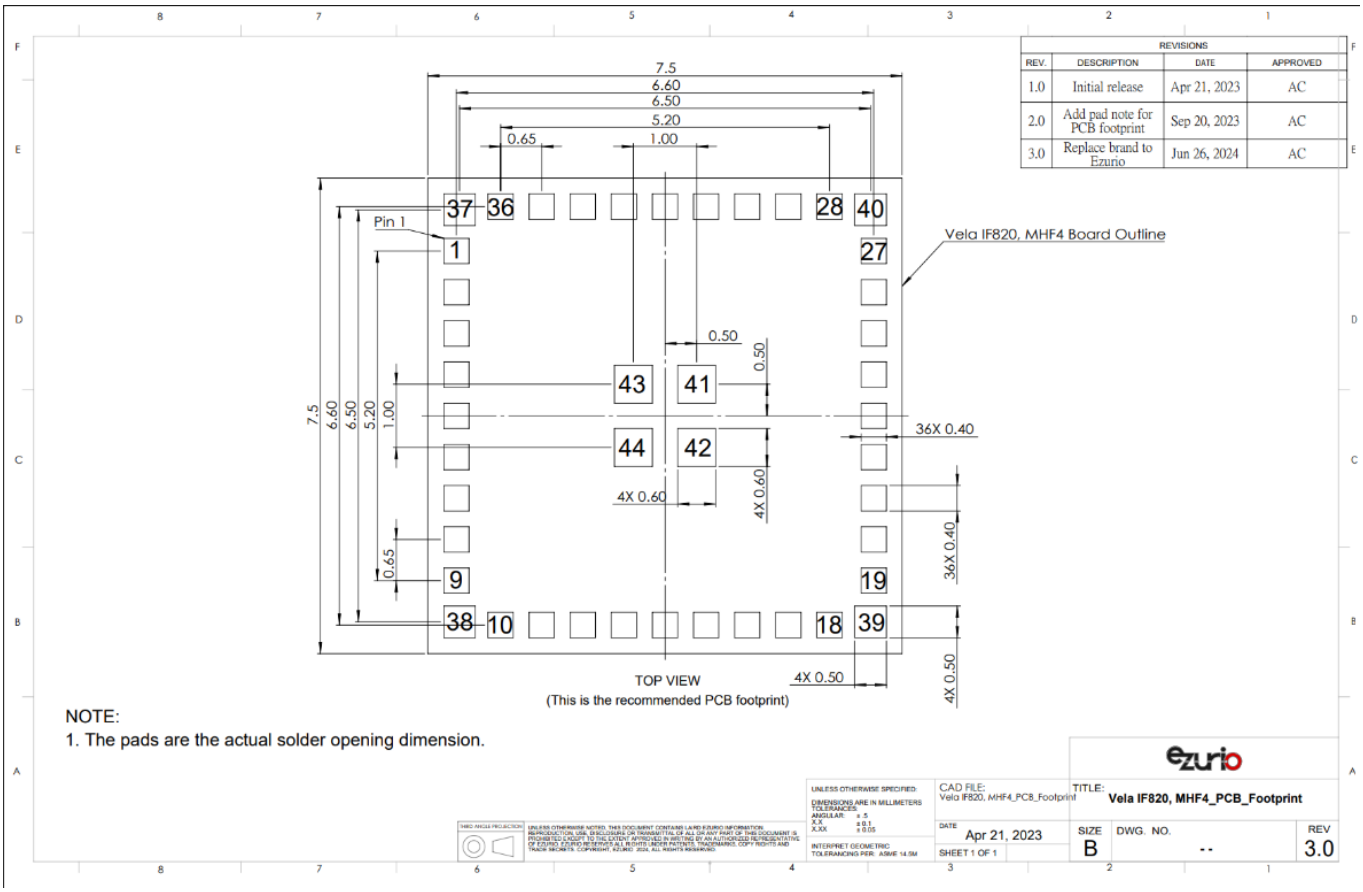


Figure 10: MHF4 connector variant module pinout (top view)

9.3 MHF4 Connector Variant Module Pin Definition

Table 18: Pin definitions of MHF4 connector variant module

Pin #	Name	EZ-Serial FW Default Function	Pin When Not Used	I/O	Voltage Ref.	Description
1	BT_DEV_WAKE	NA	floating	I	VDDIO	A signal from the host to the CYW20820 indicating that the host requires attention.
2	BT_HOST_WAKE	BT_HOST_WAKE[1]	floating	O	VDDIO	A signal from the CYW20820 device to the host indicating that the Bluetooth® device requires attention.
3	GND			-	-	NA
4	P28	I2C CLK	floating	I/O	VDDIO	Recommended functions for P28 • PWM2 • SCL3 (master and slave) • Optical control output: QOC2 • A/D converter input 11 • Current: 16 mA sink P28 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
5	P4	GPIO for USER LED	floating	I/O	VDDIO	Recommended functions for P4 • Keyboard scan input (row): KSI4 • Quadrature: QDY0 • SPI_1: MOSI (master only) P4 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
6	P2	SWDCLK	floating	I/O	VDDIO	Recommended functions for P2 • Keyboard scan input (row): KSI2 • Quadrature: QDX0 • SPI_1: MOSI (master only) • UART1_RTS_N P2 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
7	P15	SPI_CS	floating	I/O	VDDIO	Recommended functions for P15 • Keyboard scan output (column): KSO7 • A/D converter input 20 P15 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
8	P5	GPIO for Hardware Interrupt	floating	I/O	VDDIO	Recommended functions for P5 • Keyboard scan input (row): KSI5 • Quadrature: QDY1 • Peripheral UART: puart_tx • SPI_1: MISO (slave only) • I2C: SDA

[1]BT_HOST_WAKE is an output from the IF820. With EZ-Serial it is used for low power operation. When the IF820 is awake and ready to accept commands, this pin will be high, otherwise it will be low.

Pin #	Name	EZ-Serial FW Default Function	Pin When Not Used	I/O	Voltage Ref.	Description
						P5 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
9	P8	GPIO for Analog	floating	I/O	VDDIO	Recommended functions for P8 • Keyboard scan output (column): KSO0 • A/D converter input 27 • External T/R switch control: ~tx_pd P8 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
10	VDDIO			I	VDDIO	1.71V to 3.3V is recommended to supply for digital I/O
11	GND			-	-	NA
12	XTALI_32K	XTALI_32K	floating[2]	I	VDDIO	Low-power oscillator input
13	XTALO_32K	XTALO_32K	floating[2]	O	VDDIO	Low-power oscillator output
14	P3	SWDIO	floating	I/O	VDDIO	Recommended functions for P3 • Keyboard scan input (row): KSI3 • Quadrature: QDX1 • UART1_CTS_N • SPI_1: SPI_CLK (master only) P3 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
15	P6	SPI_SCK	floating	I/O	VDDIO	Recommended functions for P6 • Keyboard scan input (row): KSI6 • Quadrature: QDZ0 • Peripheral UART: puart_rts • PWM2 P6 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
16	P17	SPI_MISO	floating	I/O	VDDIO	Recommended functions for P17 • Keyboard scan output (column): KSO9 • A/D converter input 18 P17 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
17	P9	SPI_MOSI	floating	I/O	VDDIO	Recommended functions for P9 • Keyboard scan output (column): KSO1 • A/D converter input 26 • External T/R switc0h control: tx_pd P9 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
18	P12	LP_MODE	floating	I/O	VDDIO	Recommended functions for P12 • Keyboard scan output (column): KSO4

[2] highly recommend placing external 32.768kHz crystal. Using the external crystal guarantees the lowest power and highest timing accuracy.

Pin #	Name	EZ-Serial FW Default Function	Pin When Not Used	I/O	Voltage Ref.	Description
						• A/D converter input 23 P12 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
19	P13	CYSPP/SPP	floating	I/O	VDDIO	Recommended functions for P13 • Keyboard scan output (column): KSO5 • A/D converter input 22 • PWM3 P13 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
20	P1	CP_ROLE	floating	I/O	VDDIO	Recommended functions for P1 • Keyboard scan input (row): KSI1 • A/D converter input 28 • Peripheral UART: puart_rts • SPI_1: MISO (slave only) • UART1_RXD Can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
21	P11	P_UART_RTS[3]	floating	I/O	VDDIO	Recommended functions for P11 • Keyboard scan output (column): KSO3 • A/D converter input 24 P11 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
22	P10	P_UART_CTS[4]	floating	I/O	VDDIO	Recommended functions for P10 • Keyboard scan output (column): KSO2 • A/D converter input 25 • External PA ramp control: PA_Ramp P10 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
23	P27	Connection Indication GPIO[5]	floating	I/O	VDDIO	Recommended functions for P27 • Keyboard scan output (column): KSO19 • PWM1 • SPI_1: MOSI (master only) • Optical control output: QOC1 • Current: 16 mA sink P27 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
24	RST	RST_L	floating	I	VDDIO	Active-low system reset with internal pull-up resistor. **NOTE - Required for flashing EZ-Serial and HCI firmware.**

[3] EZ-Serial (Optional) - Requires enabling RTS/CTS in EZ-Serial
[4] EZ-Serial (Optional) - Requires enabling RTS/CTS in EZ-Serial
[5] Connection Indicator pin in EZ-Serial FW

Pin #	Name	EZ-Serial FW Default Function	Pin When Not Used	I/O	Voltage Ref.	Description
25	P0	GPIO for user button	floating	I/O	VDDIO	Recommended functions for P0 • Keyboard scan input (row): KSI0 • A/D converter input 29 • Peripheral UART: puart_tx • SPI_1: MOSI (master only) • UART1_TXD P0 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
26	P37	P_UART_RXD[6]	floating	I/O	VDDIO	Recommended functions for P37 • A/D converter input 2 • Quadrature: QDZ1 • SPI_1: MISO (slave only) • Auxiliary clock output: ACLK1 • I2C: SCL P37 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
27	P32	P_UART_TXD[7]	floating	I/O	VDDIO	Recommended functions P32 • A/D converter input 7 • Quadrature: QDX0 • Auxiliary clock output: ACLK0 • Peripheral UART: puart_tx P32 Can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
28	P14	GPIO10 for peripheral RST_L	floating	I/O	VDDIO	Recommended functions for P14 • Keyboard scan output (column): KSO6 • A/D converter input 21 • PWM2 P14 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
29	P29	I2C DATA	floating	I/O	VDDIO	Recommended functions for P29 • PWM3 • SDA3 (master and slave) • Optical control output: QOC3 • A/D converter input 10 • Current: 16 mA sink P29 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
30	P26	GPIO for PWM	floating	I/O	VDDIO	Recommended functions for P26 • Keyboard scan output (column): KSO18 • PWM0

[6] REQUIRED for EZ-Serial Command/Data mode

[7] REQUIRED for EZ-Serial Command/Data mode

Pin #	Name	EZ-Serial FW Default Function	Pin When Not Used	I/O	Voltage Ref.	Description
						• SPI_1: SPI_CS (slave only) • Optical control output: QOC0 • Current: 16 mA sink P26 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
31	3P0V			I	3V	Power supply input
32	GND			-	-	Ground
33	BT_UART_RTS	HCI_UART_RTS	Required pin	O, PU	VDDIO	Request to send (RTS) for HCI UART interface. **NOTE - Required for flashing EZ-Serial and HCI firmware.**
34	BT_UART_TXD	HCI_UART_TXD	Required pin	O, PU	VDDIO	UART serial output. Serial data output for the HCI UART interface. **NOTE - Required for flashing EZ-Serial and HCI firmware.**
35	BT_UART_RXD	HCI_UART_RXD	Required pin	I	VDDIO	UART serial input. Serial data input for the HCI UART interface. **NOTE - Required for flashing EZ-Serial and HCI firmware.**
36	BT_UART_CTS	HCI_UART_CTS	Required pin	I, PU	VDDIO	Clear to send (CTS) for HCI UART interface. **NOTE - Required for flashing EZ-Serial and HCI firmware.**
37	GND			-	-	Ground
38	GND			-	-	Ground
39	GND			-	-	Ground
40	GND			-	-	Ground
41	GND			-	-	Ground
42	GND			-	-	Ground
43	GND			-	-	Ground
44	GND			-	-	Ground

9.4 Reference Schematic Design

Note: It is recommended to put a 100nF bypass capacitor in the 3P0V (pin31) and VDDIO (pin10).

Highly recommend placing external 32.768kHz crystal. Using the external crystal guarantees the lowest power and highest timing accuracy.

BT_UART signals (x4) are required for flashing EZ-Serial and HCI firmware.

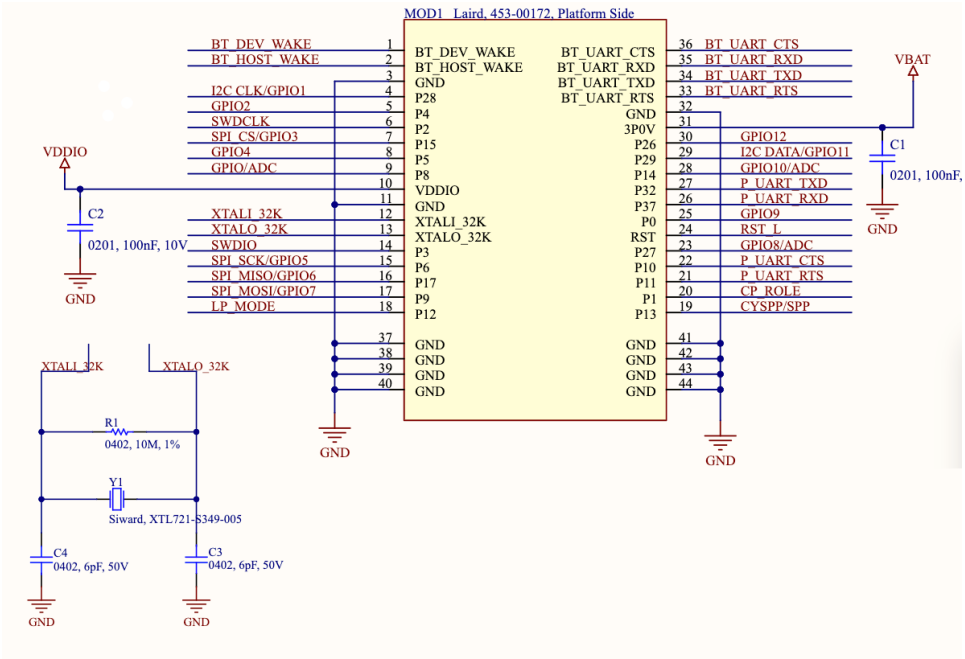


Figure 11: MHF4 connector variant schematic

9.5 Supermux I/O Function Defined Table

Table 19: GPIO Supermux input functions

Input		
SWDCK	SPI2_CS	SCL2
SWDIO	SPI2_MOSI	SDA2
SPI1_CLK	SPI2_MISO	PCM_IN
SPI1_CS	SPI2_IO2	PCM_CLK
SPI1_MOSI	SPI2_IO3	PCM_SYNC
SPI1_MISO	SPI2_INT	I2S_DI
SPI1_IO2	puart_rx	I2S_WS
SPI1_IO3	puart_cts_n	I2S_CLK
SPI1_INT	SCL	PDM_IN_Ch_1
SPI2_CLK	SDA	PDM_IN_Ch 2

Table 20: GPIO Supermux output functions

Output			
do_P# (data out of GPIO. For example: P0)	kso4	kso19	SCL2
do_PCM_IN	kso5	do_P# pwm0	puart_tx (uart2_tx)
do_PCM_OUT	kso6	do_P# pwm1	puart_rts_n (uart2_rts_n)
do_PCM_CLK	kso7	do_P# pwm2	SPI1_CLK
do_PCM_SYNC	kso8	do_P# pwm3	SPI1_CS
do_I2S_DO	kso9	do_P# pwm4	SPI1_MOSI
do_I2S_DI	kso10	do_P# pwm5	SPI1_MISO
do_I2S_WS	kso11	aclk0	SPI1_IO2
do_I2S_CLK	kso12	aclk1	SPI1_IO3
do_CLK_REQ	kso13	HID_OFF	SPI2_CLK
IR_TX	kso14	pa_ramp	SPI2_CS
kso0	kso15	tx_pd	SPI2_MOSI
kso1	kso16	~tx_pd	SPI2_MISO
kso2	kso17	SWDIO	SPI2_IO2
kso3	kso18	SDA2	SPI2_IO3

10 Integrated Antenna Variant Footprint and Pin Definitions

10.1 Integrated Antenna Variant Mechanical Definition

Module dimensions of integrated antenna variant module is 12.5 x 9.3 x 2.15 mm. Detail drawings are shown in Figure 9.

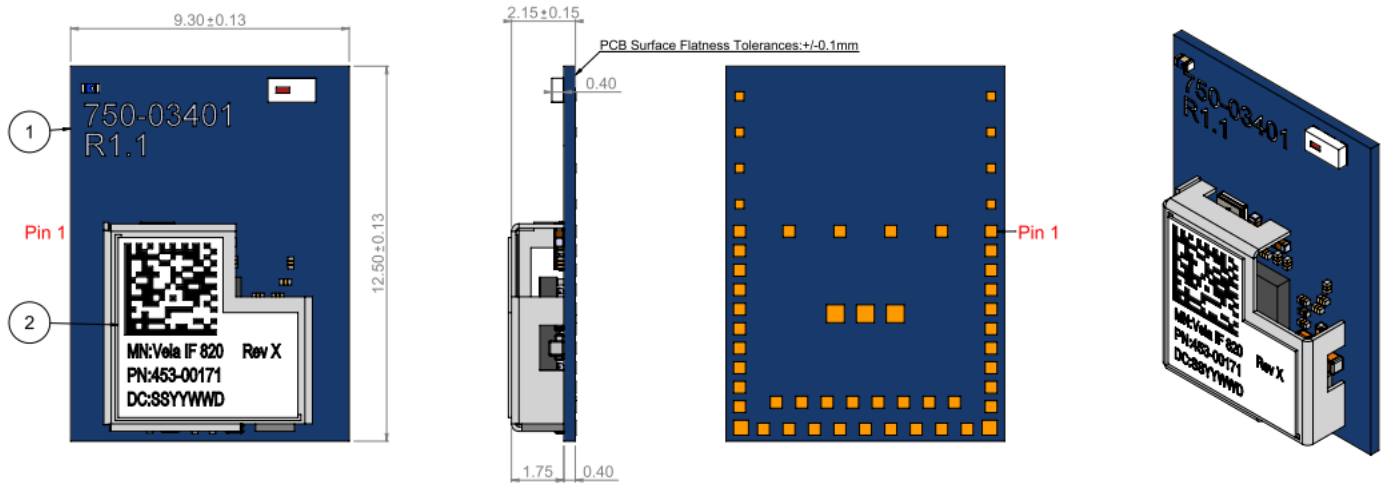


Figure 12: Mechanical Details – Integrated Antenna Variant (453-00171)

10.2 Integrated Antenna Variant Module Footprint

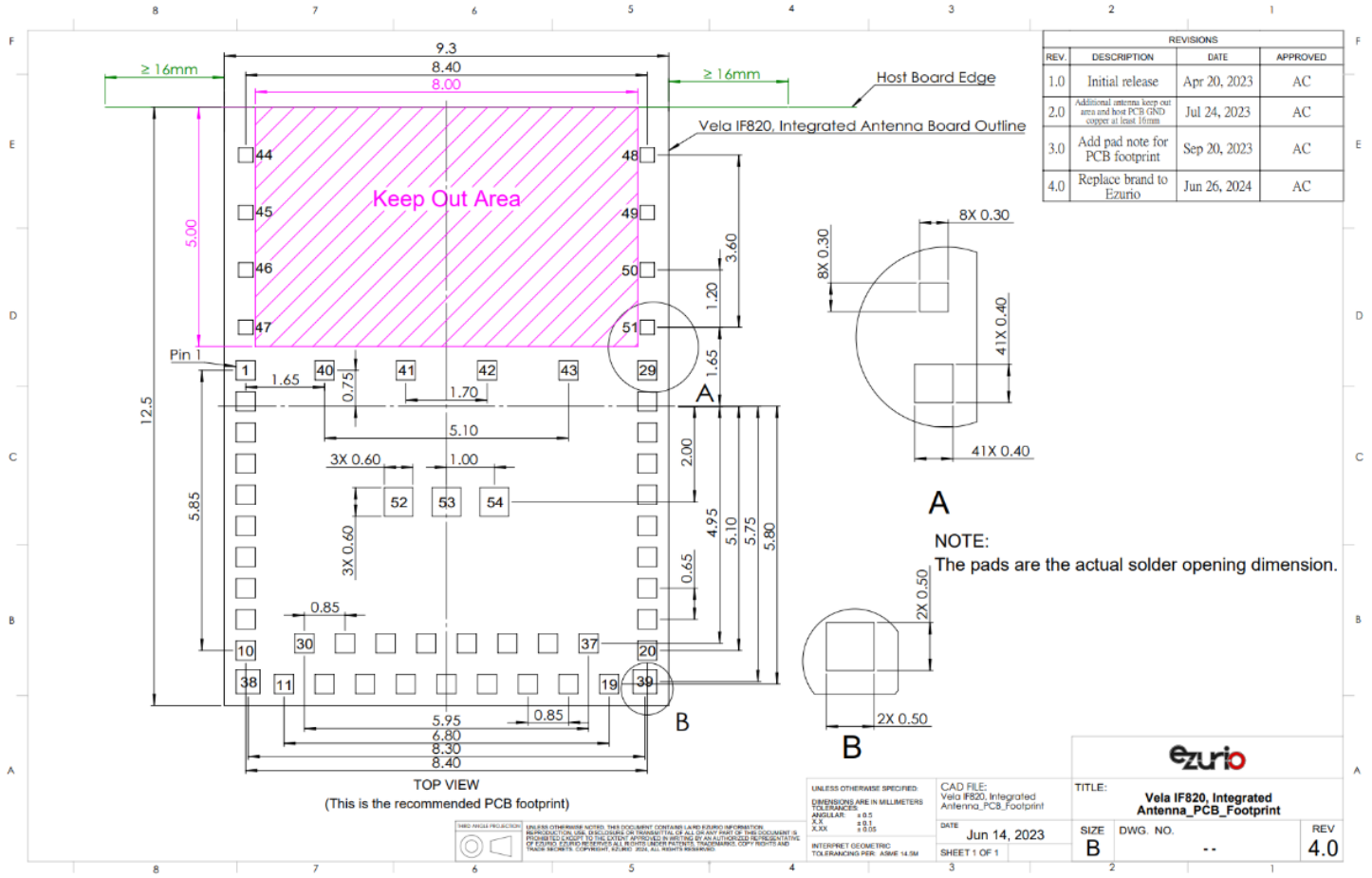


Figure 13: Integrated antenna variant module pinout (top view)

10.3 Integrated Antenna Variant Module Pin Definition

Table 21: Pin definitions of Vela IF820 chip Antenna module

Pin #	Name	EZ-Serial FW Default Function	Pin When Not Used	I/O	Voltage Ref.	Description
1	GND			-	-	Ground
2	VDDIO			I	VDDIO	1.71V to 3.3V is recommended to supply for digital I/O
3	GND			-	-	Ground
4	XTALI_32K	XTALI_32K	floating[8]	I	VDDIO	Low-power oscillator input
5	XTALO_32K	XTALO_32K	floating[9]	O	VDDIO	Low-power oscillator output
6	P15	SPI_CS	floating	I/O	VDDIO	Recommended functions for P15

[8] highly recommend to implement 32.768KHz crystal, if not, link issue may be occurred.
[9] highly recommend to implement 32.768KHz crystal, if not, link issue may be occurred.

Pin #	Name	EZ-Serial FW Default Function	Pin When Not Used	I/O	Voltage Ref.	Description
						• Keyboard scan output (column): KSO7 • A/D converter input 20 P15 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
7	P8	GPIO for Analog	floating	I/O	VDDIO	Recommended functions for P8 • Keyboard scan output (column): KSO0 • A/D converter input 27 • External T/R switch control: ~tx_pd P8 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
8	P2	SWDCLK	floating	I/O	VDDIO	Recommended functions for P2 • Keyboard scan input (row): KSI2 • Quadrature: QDX0 • SPI_1: MOSI (master only) • UART1_RTS_N P2 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
9	P3	SWDIO	floating	I/O	VDDIO	Recommended functions for P3 • Keyboard scan input (row): KSI3 • Quadrature: QDX1 • UART1_CTS_N • SPI_1: SPI_CLK (master only) P3 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
10	P6	SPI_SCK	floating	I/O	VDDIO	Recommended functions for P6 • Keyboard scan input (row): KSI6 • Quadrature: QDZ0 • Peripheral UART: puart_rts • PWM2 P6 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
11	P17	SPI_MISO	floating	I/O	VDDIO	Recommended functions for P17 • Keyboard scan output (column): KSO9 • A/D converter input 18 P17 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
12	P13	CYSPP/SPP[10]	floating	I/O	VDDIO	Recommended functions for P13 • Keyboard scan output (column): KSO5 • A/D converter input 22 • PWM3 P13 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
13	P9	SPI_MOSI	floating	I/O	VDDIO	Recommended functions for P9 • Keyboard scan output (column): KSO1

[10] CYSPP Input/output CYSPP mode control. Assert (LOW) for CYSPP data mode, de-assert (HIGH) for command mode.

Pin #	Name	EZ-Serial FW Default Function	Pin When Not Used	I/O	Voltage Ref.	Description
						• A/D converter input 26 • External T/R switc0h control: tx_pd P9 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
14	P10	P_UART_CTS[11]	floating	I/O	VDDIO	Recommended functions for P10 • Keyboard scan output (column): KSO2 • A/D converter input 25 • External PA ramp control: PA_Ramp P10 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
15	P37	P_UART_RXD[12]	floating	I/O	VDDIO	Recommended functions for P37 • A/D converter input 2 • Quadrature: QDZ1 • SPI_1: MISO (slave only) • Auxiliary clock output: ACLK1 • I2C: SCL P37 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
16	P11	P_UART_RTS[13]	floating	I/O	VDDIO	Recommended functions for P11 • Keyboard scan output (column): KSO3 • A/D converter input 24 P11 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
17	P32	P_UART_TXD[14]	floating	I/O	VDDIO	Recommended functions P32 • A/D converter input 7 • Quadrature: QDX0 • Auxiliary clock output: ACLK0 • Peripheral UART: puart_tx P32 Can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
18	P14	GPIO for peripheral RST_L	floating	I/O	VDDIO	Recommended functions for P14 • Keyboard scan output (column): KSO6 • A/D converter input 21 • PWM2 P14 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
19	P5	GPIO for Hardware Interrupt	floating	I/O	VDDIO	Recommended functions for P5 • Keyboard scan input (row): KSI5 • Quadrature: QDY1 • Peripheral UART: puart_tx • SPI_1: MISO (slave only) • I2C: SDA

[11] P_UART_CTS (optional) - requires enabling RTS/CTS in the EZ-Serial FW
[12] REQUIRED for EZ-Serial command/data mode
[13] P_UART_RTS (optional) - requires enabling RTS/CTS in the EZ-Serial FW
[14] REQUIRED for EZ-Serial command/data mode

Pin #	Name	EZ-Serial FW Default Function	Pin When Not Used	I/O	Voltage Ref.	Description
						P5 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
20	P28	I2C_CLK	floating	I/O	VDDIO	Recommended functions for P28 • PWM2 • SCL3 (master and slave) • Optical control output: QOC2 • A/D converter input 11 • Current: 16 mA sink P28 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
21	GND			-	-	Ground
22	3P0V			I	3V	Power supply input
23	GND			-	-	Ground
24	BT_UART_RTS	HCI_UART_RTS[15]	floating	O, PU	VDDIO	Request to send (RTS) for HCI UART interface. **NOTE - Required for flashing EZ-Serial and HCI firmware.**
25	BT_UART_TXD	HCI_UART_TXD[16]	floating	O, PU	VDDIO	UART serial output. Serial data output for the HCI UART interface. **NOTE - Required for flashing EZ-Serial and HCI firmware.**
26	BT_UART_RXD	HCI_UART_RXD[17]	floating	I	VDDIO	UART serial input. Serial data input for the HCI UART interface. **NOTE - Required for flashing EZ-Serial and HCI firmware.**
27	BT_UART_CTS	HCI_UART_CTS[18]	floating	I, PU	VDDIO	Clear to send (CTS) for HCI UART interface. **NOTE - Required for flashing EZ-Serial and HCI firmware.**
28	BT_DEV_WAKE	NA	floating	I	VDDIO	A signal from the host to the CYW20820 indicating that the host requires attention.
29	BT_HOST_WAKE	BT_HOST_WAKE[19]	floating	O	VDDIO	A signal from the CYW20820 device to the host indicating that the Bluetooth® device requires attention.
30	P12	LP_MODE	floating	I/O	VDDIO	Recommended functions for P12 • Keyboard scan output (column): KSO4 • A/D converter input 23

[15] HCI_UART_RTS REQUIRED for firmware loading/upgrades.

[16] HCI_UART_TXD REQUIRED for firmware loading/upgrades.

[17] HCI_UART_RXD REQUIRED for firmware loading/upgrades.

[18] HCI_UART_CTS REQUIRED for firmware loading/upgrades.

[19] BT_HOST_WAKE is an output from the IF820. With EZ-Serial it is used for low power operation. When the IF820 is awake and ready to accept commands, this pin will be high, otherwise it will be low.

Pin #	Name	EZ-Serial FW Default Function	Pin When Not Used	I/O	Voltage Ref.	Description
						P12 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
31	P1	CP_ROLE	floating	I/O	VDDIO	Recommended functions for P1 • Keyboard scan input (row): KSI1 • A/D converter input 28 • Peripheral UART: puart_rts • SPI_1: MISO (slave only) • UART1_RXD Can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
32	P0	GPIO for user button	floating	I/O	VDDIO	Recommended functions for P0 • Keyboard scan input (row): KSI0 • A/D converter input 29 • Peripheral UART: puart_tx • SPI_1: MOSI (master only) • UART1_TXD P0 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
33	P27	Connection Indication GPIO[20]	floating	I/O	VDDIO	Recommended functions for P27 • Keyboard scan output (column): KSO19 • PWM1 • SPI_1: MOSI (master only) • Optical control output: QOC1 • Current: 16 mA sink P27 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
34	RST	RST_L	floating	I	VDDIO	Active-low system reset with internal pull-up resistor. **NOTE - Required for flashing EZ-Serial and HCI firmware.**
35	P29	I2C_DATA	floating	I/O	VDDIO	Recommended functions for P29 • PWM3 • SDA3 (master and slave) • Optical control output: QOC3 • A/D converter input 10 • Current: 16 mA sink P29 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
36	P26	GPIO for PWM	floating	I/O	VDDIO	Recommended functions for P26 • Keyboard scan output (column): KSO18 • PWM0 • SPI_1: SPI_CS (slave only) • Optical control output: QOC0 • Current: 16 mA sink

[20] Connection Indicator pin in EZ-Serial FW

Pin #	Name	EZ-Serial FW Default Function	Pin When Not Used	I/O	Voltage Ref.	Description
						P26 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
37	P4	GPIO for USER LED	floating	I/O	VDDIO	Recommended functions for P4 • Keyboard scan input (row): KSI4 • Quadrature: QDY0 • SPI_1: MOSI (master only) P4 can also be remapped using Supermux I/O functions as defined in Table 19 and Table 20.
38	GND			-	-	Ground
39	GND			-	-	Ground
40	GND			-	-	Ground
41	GND			-	-	Ground
42	GND			-	-	Ground
43	GND			-	-	Ground
44	GND			-	-	Ground
45	GND			-	-	Ground
46	GND			-	-	Ground
47	GND			-	-	Ground
48	GND			-	-	Ground
49	GND			-	-	Ground
50	GND			-	-	Ground
51	GND			-	-	Ground
52	GND			-	-	Ground
53	GND			-	-	Ground
54	GND			-	-	Ground

10.4 Reference Schematic Design

Note: It is recommended to put bypass capacitors 100nF in the 3P0V (pin22) and VDDIO (pin2).

Highly recommend to implement 32.768KHz crystal (pin4, pin5), Using the external crystal guarantees the lowest power and highest timing accuracy.

BT_UART signals (x4) are required for flashing EZ-Serial and HCI firmware.

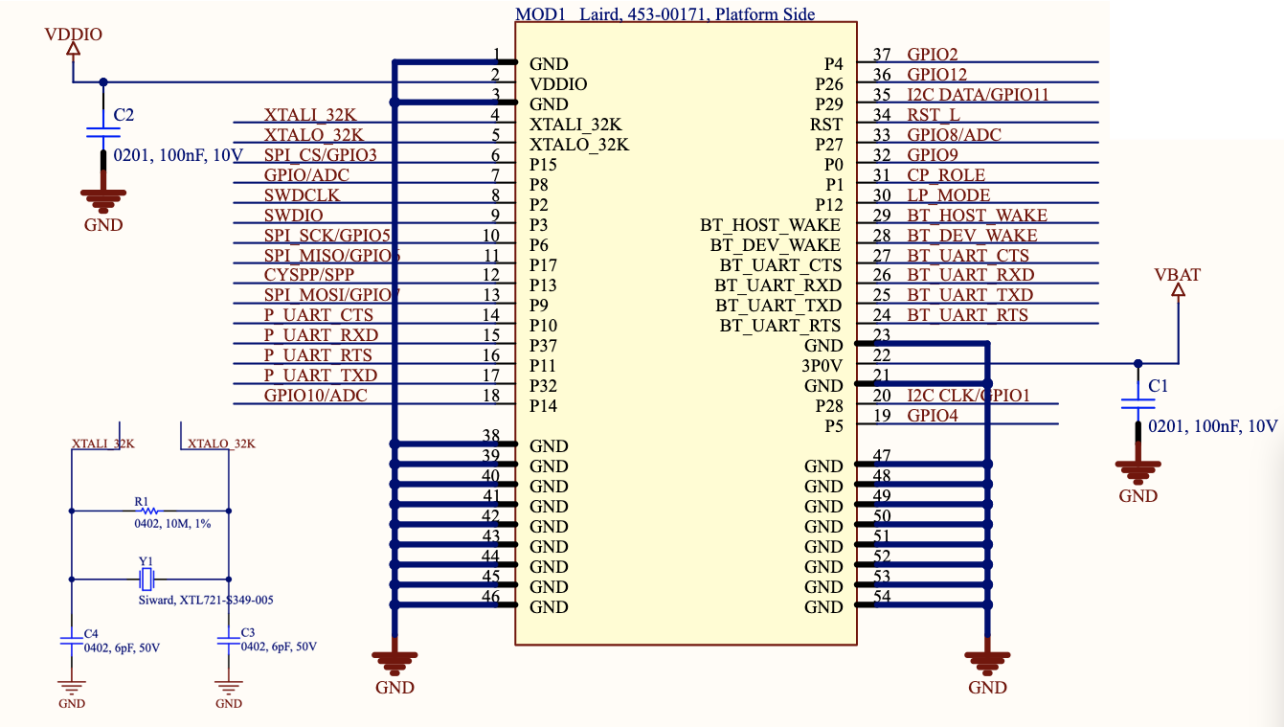


Figure 14: Integrated antenna variant schematic

11 Flashing Firmware – EZ Serial or HCI Firmware

Vela IF820 firmware programming is done via the HCI UART.

There are two tools to flash a Vela IF820 module detailed in the following link:-

https://github.com/LairdCP/Vela_IF820_Firmware/releases

if820_flasher_gui is a graphical user interface for flashing Vela IF820 DVKs and dongles, it will auto detect any Vela IF820 DVKs and dongles currently connected to your PC. It cannot be used for flashing a loose module.

if820_flasher_cli is a command line tool for flashing Vela IF820 DVK, dongle and loose modules. Like the GUI it will auto detect a DVK or dongle but you can also specify a com port for a loose module. When specifying a com port the Flasher CLI bypasses the DVK probe auto detect. You can use the -c option in the IF820 Flasher GUI to specify a com port

When flashing a loose module via a particular com port the following should be noted

- Flashing uses BT_UART_TXD, BT_UART_RXD, BT_UART_CTS, BT_UART_RTS
- Flow control is mandatory.
- Reset line is also required to be able to enter programming mode.
- UART settings are 1152008N1
- CTS needs to be low during a reset to enter programming mode.
- The GUI can only be used to flash DVKs and dongles. You must use the CLI for loose modules.

12 RF Layout Design Guidelines

12.1 General Consideration

The following is a list of RF layout design guidelines and recommendation when installing an Ezurio radio into your device.

- Do not run antenna cables directly above or directly below the radio.
- Do not place any parts or run any high-speed digital lines below the radio.
- If there are other radios or transmitters located on the device (such as a Bluetooth radio), place the devices as far apart from each other as possible. Also, make sure there is at least 25 dB isolation between these two antennas.
- Ensure that there is the maximum allowable spacing separating the antenna connectors on the Ezurio radio from the antenna. In addition, do not place antennas directly above or directly below the radio.
- Ezurio recommends the use of a double-shielded cable for the connection between the radio and the antenna elements.
- Be sure to put a 100nF capacitor on EACH power pin. Also, place that capacitor to the pin as close as possible to make sure the internal PMU working correctly.

Use proper electro-static-discharge (ESD) procedures when installing the Ezurio radio module. To avoid negatively impacting Tx power and receiver sensitivity, do not cover the antennas with metallic objects or components.

12.2 Layout Recommendations for Integrated Antenna Variant

The following are recommended for layout of the integrated antenna variant of the Vela IF820:

1. Align module edge with PCB edge.
2. To maintain antenna radiation efficiency, keep at least 15mm width of the GND plane to the sides the module.

Please see Figure 15 for a layout example.

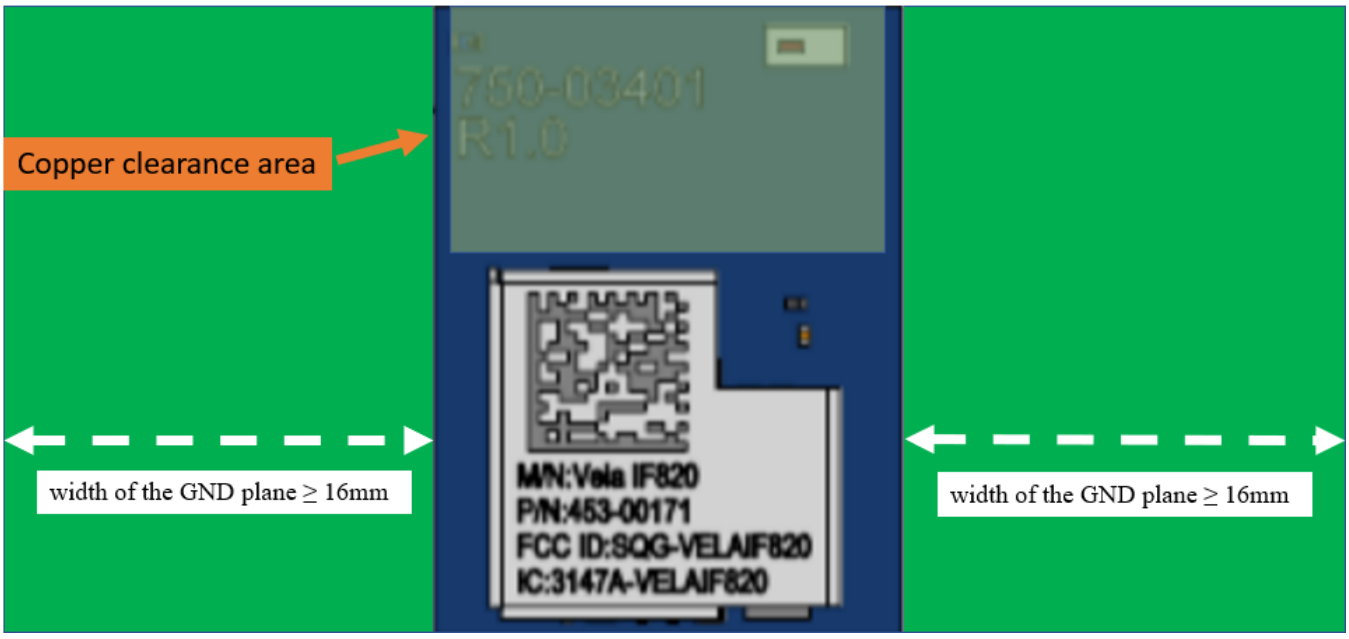


Figure 15: Integrated antenna variant layout suggestion example

13 Application Note for Surface Mount Modules

13.1 Introduction

Ezurio's surface mount modules are designed to conform to all major manufacturing guidelines. This application note is intended to provide additional guidance beyond the information that is presented in the user manual. This application note is considered a living document and will be updated as new information is presented.

The modules are designed to meet the needs of several commercial and industrial applications. They are easy to manufacture and conform to current automated manufacturing processes.

Vela IF820 part numbers – 453-00171**R** and 453-00172**R** are shipped as Tape / Reel, with a reel containing 1,000 pcs.

13.2 Module Packaging Configuration

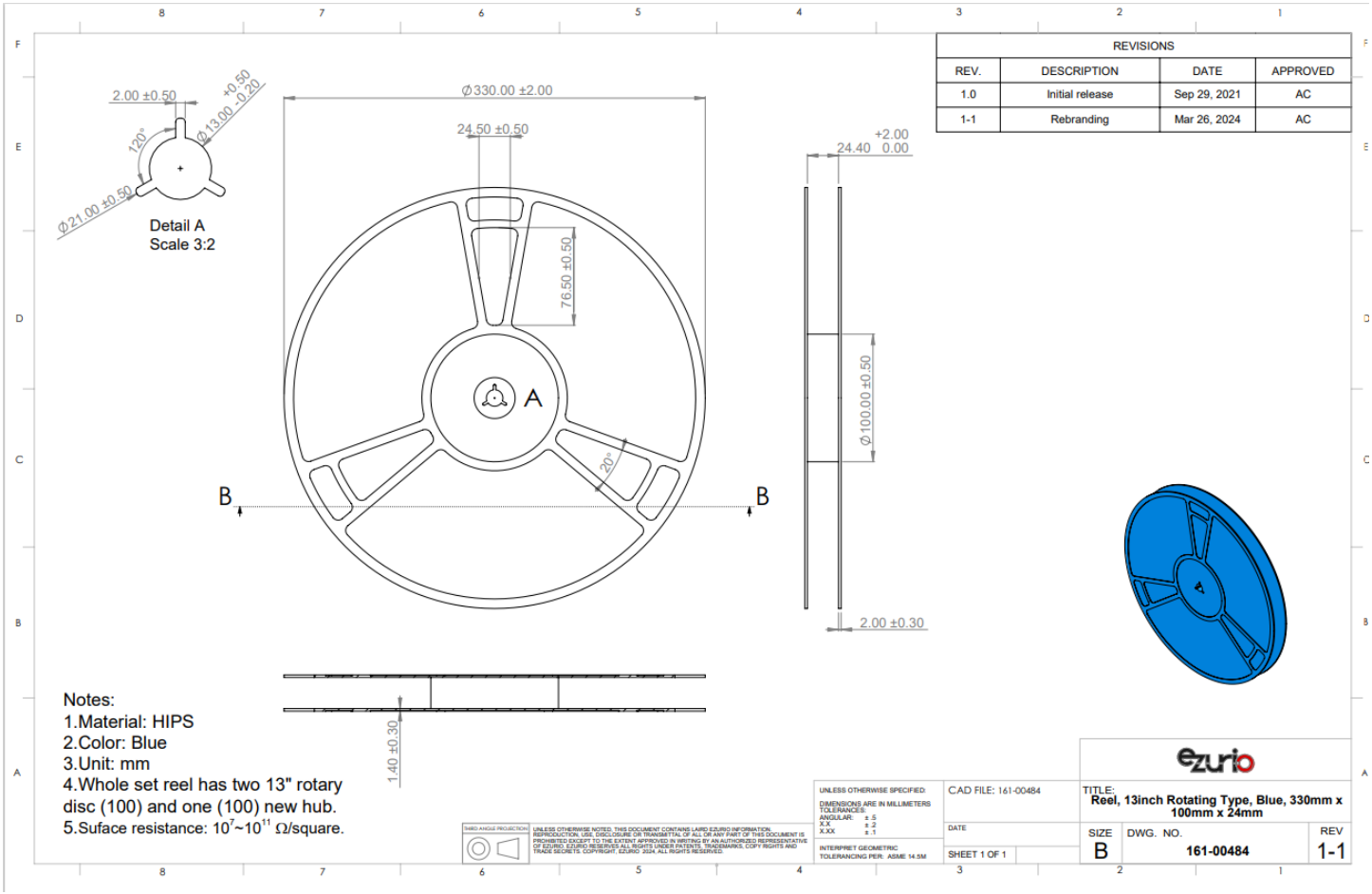


Figure 16: Reel specifications – 1,000 pieces per reel

Figure 17: Carrier Tape specifications for Integrated Antenna Variant

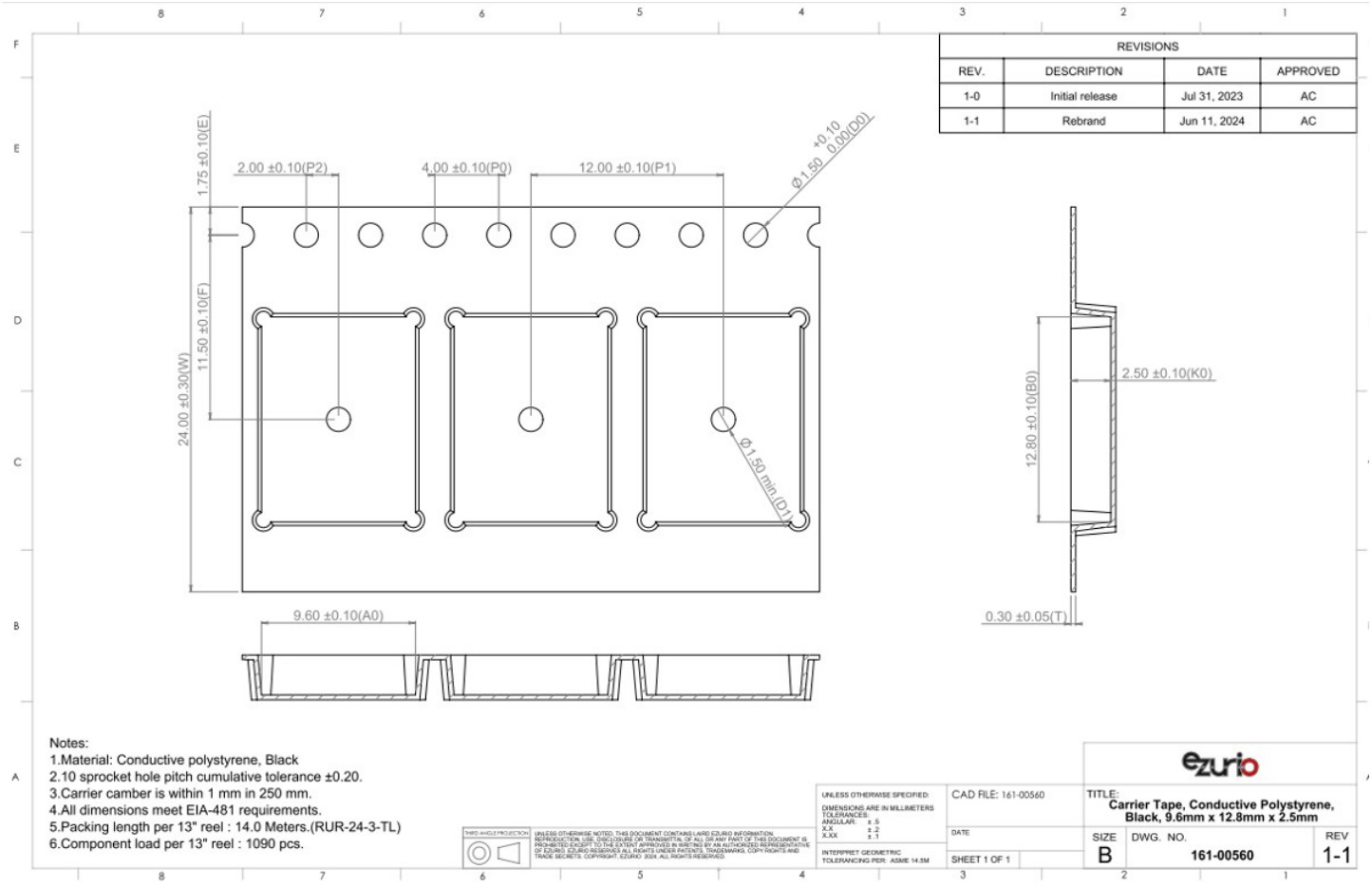
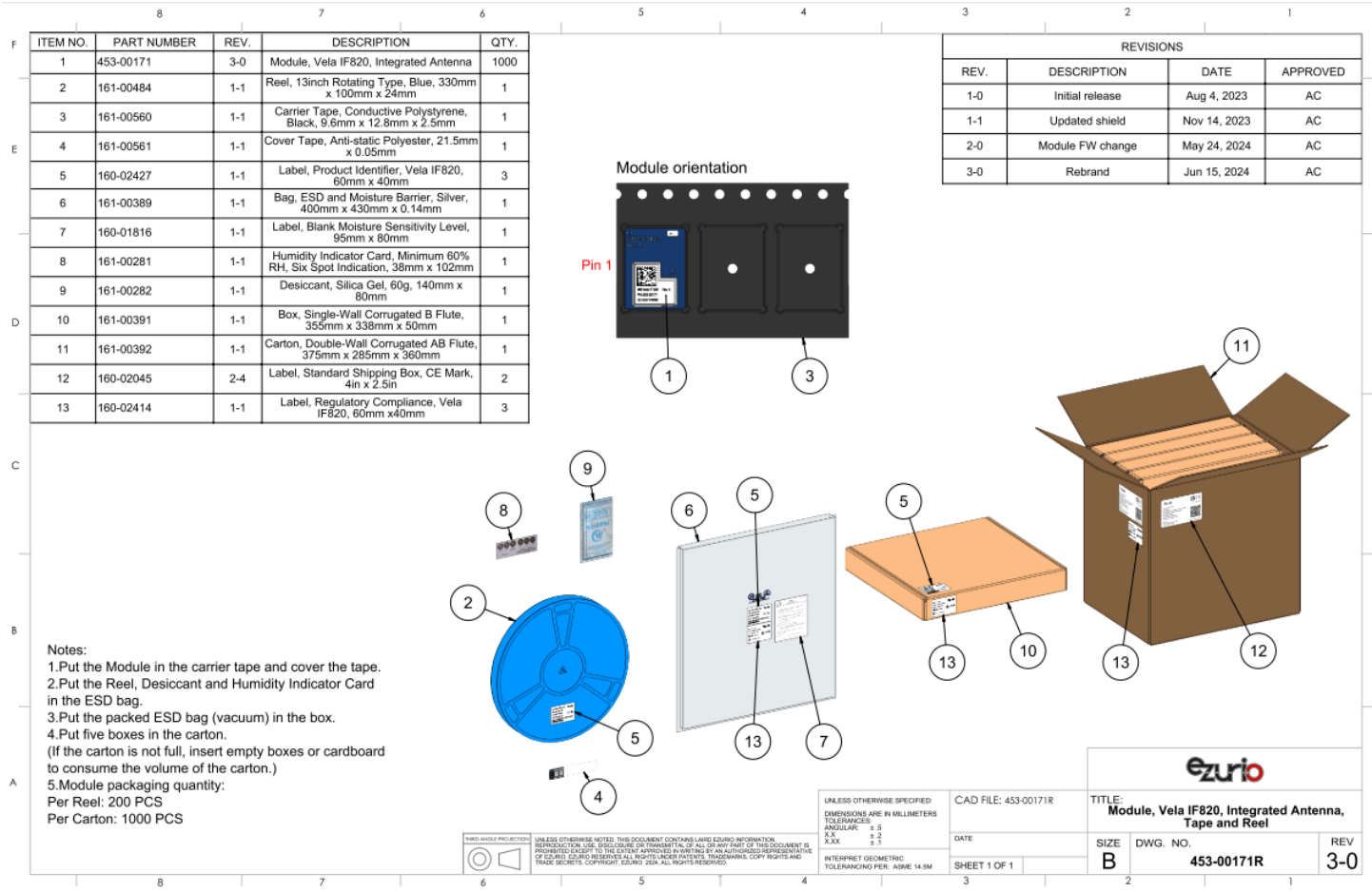


Figure 18: Carrier Tape Specifications for MHF4 Variant



ITEM NO.	PART NUMBER	REV.	DESCRIPTION	QTY.
1	453-00171	3-0	Module, Vela IF820, Integrated Antenna	1000
2	161-00484	1-1	Reel, 13inch Rotating Type, Blue, 330mm x 100mm x 24mm	1
3	161-00560	1-1	Carrier Tape, Conductive Polystyrene, Black, 9.6mm x 12.8mm x 2.5mm	1
4	161-00561	1-1	Cover Tape, Anti-static Polyester, 21.5mm x 0.05mm	1
5	160-02427	1-1	Label, Product Identifier, Vela IF820, 60mm x 40mm	3
6	161-00389	1-1	Bag, ESD and Moisture Barrier, Silver, 400mm x 430mm x 0.14mm	1
7	160-01816	1-1	Label, Blank Moisture Sensitivity Level, 95mm x 80mm	1
8	161-00281	1-1	Humidity Indicator Card, Minimum 60% RH, Six Spot Indication, 38mm x 102mm	1
9	161-00282	1-1	Desiccant, Silica Gel, 60g, 140mm x 80mm	1
10	161-00391	1-1	Box, Single-Wall Corrugated B Flute, 355mm x 338mm x 50mm	1
11	161-00392	1-1	Carton, Double-Wall Corrugated AB Flute, 375mm x 285mm x 360mm	1
12	160-02045	2-4	Label, Standard Shipping Box, CE Mark, 4in x 2.5in	2
13	160-02414	1-1	Label, Regulatory Compliance, Vela IF820, 60mm x40mm	3

REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
1-0	Initial release	Aug 4, 2023	AC
1-1	Updated shield	Nov 14, 2023	AC
2-0	Module FW change	May 24, 2024	AC
3-0	Rebrand	Jun 15, 2024	AC

Figure 19: Vela IF820 Packaging Process for Integrated Antenna Variant

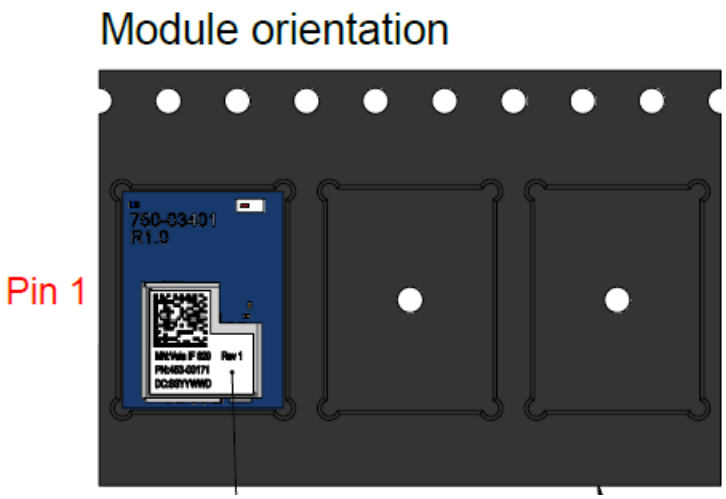
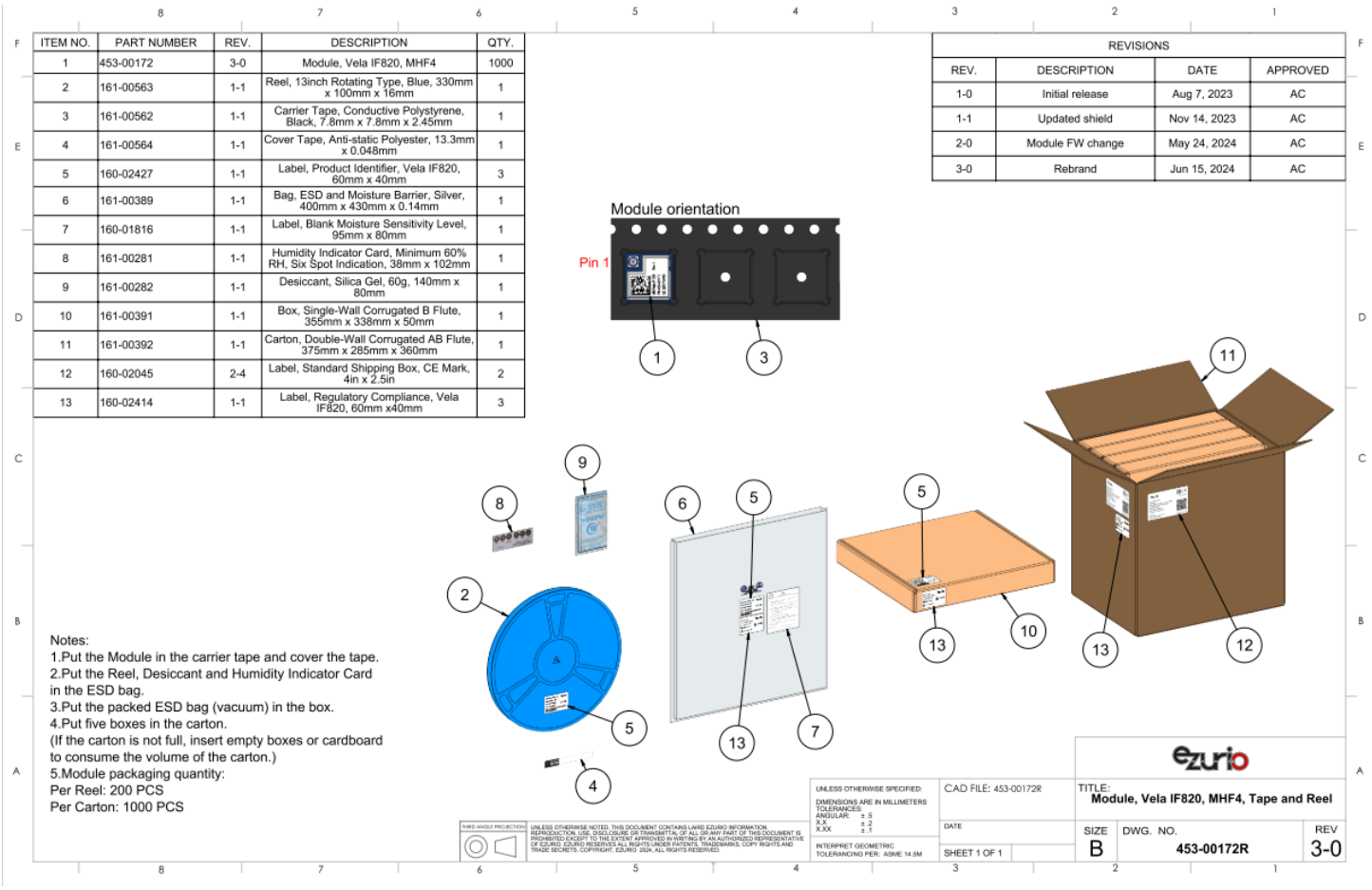


Figure 20: Module Orientation in Carrier Tape Pocket, Integrated Antenna Variant



ITEM NO.	PART NUMBER	REV.	DESCRIPTION	QTY.
1	453-00172	3-0	Module, Vela IF820, MHF4	1000
2	161-00563	1-1	Reel, 13inch Rotating Type, Blue, 330mm x 100mm x 16mm	1
3	161-00562	1-1	Carrier Tape, Conductive Polystyrene, Black, 7.8mm x 7.8mm x 2.45mm	1
4	161-00564	1-1	Cover Tape, Anti-static Polyester, 13.3mm x 0.048mm	1
5	160-02427	1-1	Label, Product Identifier, Vela IF820, 60mm x 40mm	3
6	161-00389	1-1	Bag, ESD and Moisture Barrier, Silver, 400mm x 430mm x 0.14mm	1
7	160-01816	1-1	Label, Blank Moisture Sensitivity Level, 95mm x 80mm	1
8	161-00281	1-1	Humidity Indicator Card, Minimum 60% RH, Six Spot Indication, 38mm x 102mm	1
9	161-00282	1-1	Desiccant, Silica Gel, 60g, 140mm x 80mm	1
10	161-00391	1-1	Box, Single-Wall Corrugated B Flute, 355mm x 338mm x 50mm	1
11	161-00392	1-1	Carton, Double-Wall Corrugated AB Flute, 375mm x 285mm x 360mm	1
12	160-02045	2-4	Label, Standard Shipping Box, CE Mark, 4in x 2.5in	2
13	160-02414	1-1	Label, Regulatory Compliance, Vela IF820, 60mm x40mm	3

REVISIONS			
REV.	DESCRIPTION	DATE	APPROVED
1-0	Initial release	Aug 7, 2023	AC
1-1	Updated shield	Nov 14, 2023	AC
2-0	Module FW change	May 24, 2024	AC
3-0	Rebrand	Jun 15, 2024	AC

Figure 21: Vela IF820 Packaging Process for MHF4 Variant

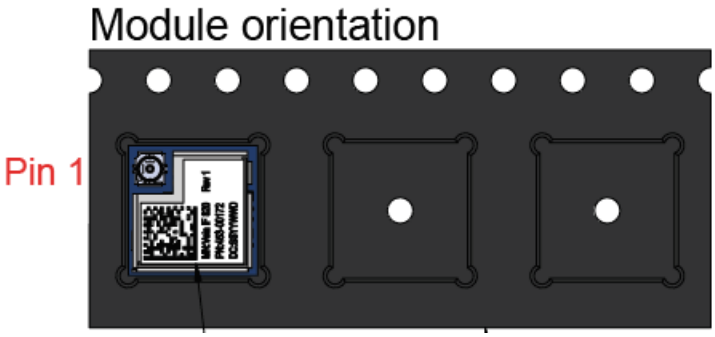


Figure 22: Module Orientation in Carrier Tape Pocket, MHF4 Variant

13.3 Module Shipping

All modules are shipped in tape and reel package and sealed in ESD Bags.

13.4 Labeling

The following labels are placed on the anti-static bag. The Vela IF820 solder-down modules are classified as MSL4 devices.

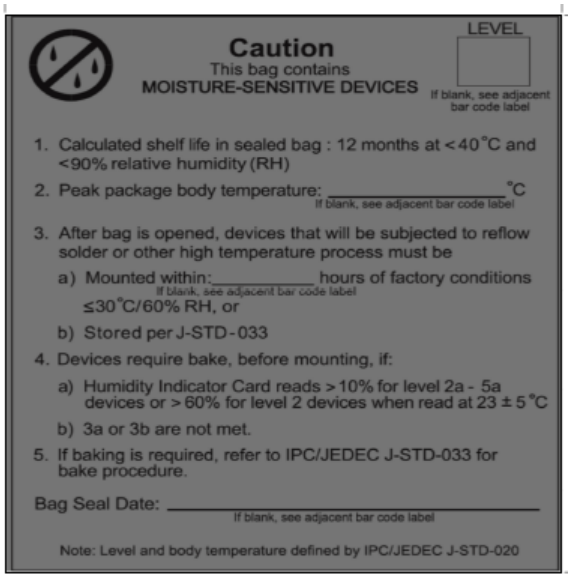


Figure 23: Moisture Sensitivity Level Label

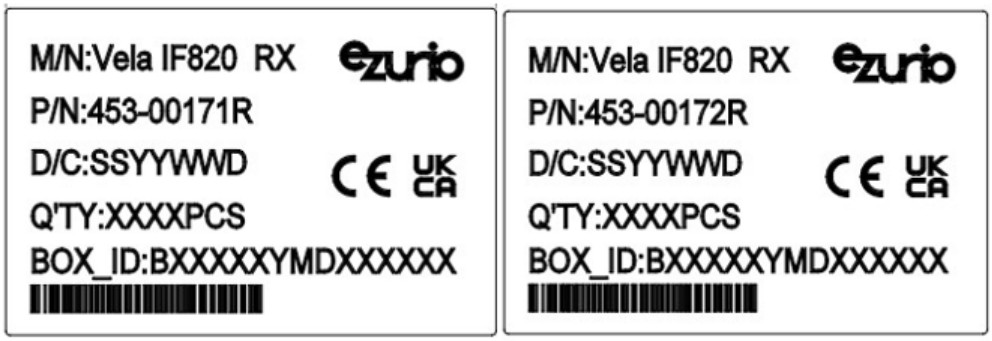


Figure 24: Product Identifier Label

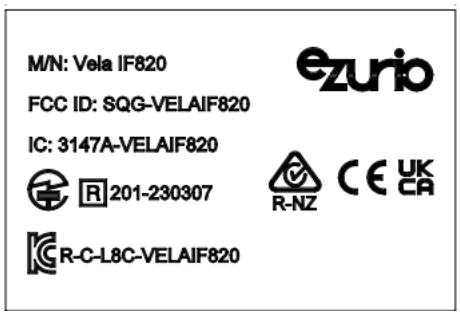


Figure 25: Regulatory Compliance Label

The following labels are placed on the pizza box.

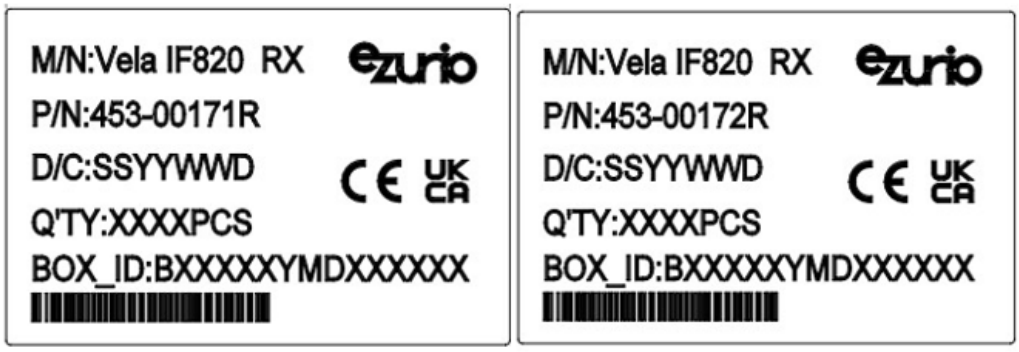


Figure 26: Product Identifier Label

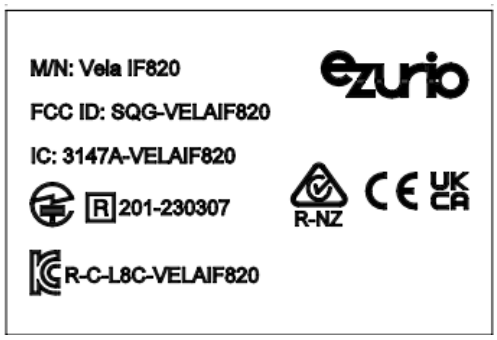


Figure 27: Regulatory Compliance Label

The following labels are placed on the master shipping carton.

Figure 28: Standard Shipping Carton Label

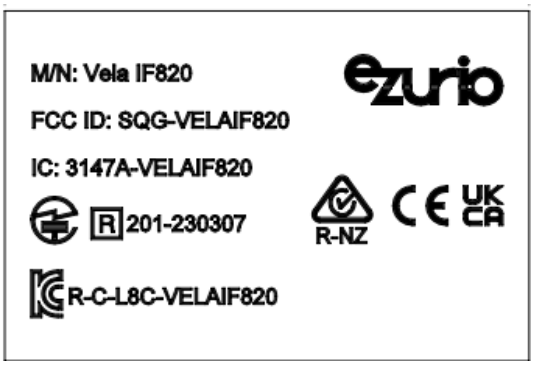


Figure 29: Regulatory Compliance Label

13.5 Required Storage Conditions

13.5.1 Prior to Opening the Dry Packing

The following are required storage conditions ***prior* to opening the dry packing**:

- Normal temperature: 5~40˚C
- Normal humidity: 80% (Relative humidity) or less
- Storage period: One year or less

Note: Humidity means relative humidity.

13.5.2 After Opening the Dry Packing

The following are required storage conditions ***after* opening the dry packing** (to prevent moisture absorption):

- Storage conditions for one-time soldering:
  - Temperature: 5-25°C
  - Humidity: 60% or less
  - Period: 72 hours or less after opening
- Storage conditions for two-time soldering
  - Storage conditions following opening and prior to performing the 1st reflow:
    - Temperature: 5-25°C
    - Humidity: 60% or less
    - Period: A hours or less after opening
  - Storage conditions following completion of the 1st reflow and prior to performing the 2nd reflow
    - Temperature: 5-25°C
    - Humidity: 60% or less
    - Period: B hours or less after completion of the 1st reflow

---

Note: Should keep A+B within 72 hours.

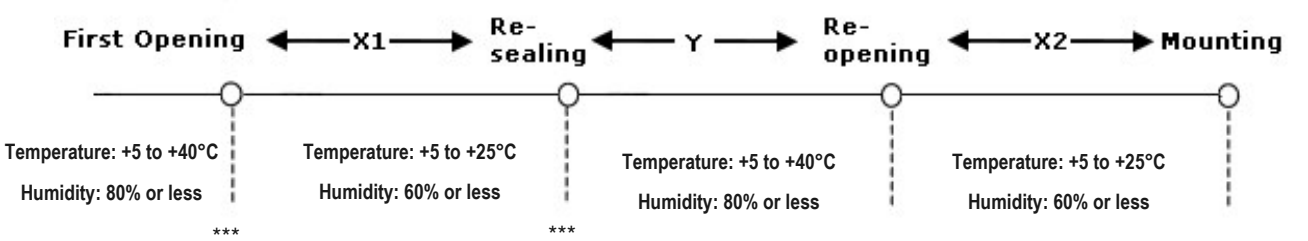
13.5.3 Temporary Storage Requirements after Opening

The following are temporary storage requirements after opening:

- Only re-store the devices *once* prior to soldering.
- Use a dry box or place desiccant (with a blue humidity indicator) with the devices and perform dry packing again using vacuumed heat-sealing.

The following indicate the required storage period, temperature, and humidity for this temporary storage:

- Storage temperature and humidity:



*** - External atmosphere temperature and humidity of the dry packing

- Storage period:
  - X1+X2 – Refer to After Opening the Dry Packing storage requirements. Keep is X1+X2 within 72 hours.
  - Y – Keep within two weeks or less.

13.6 Baking Conditions

Baking conditions and processes for the module follow the J-STD-033 standard which includes the following:

- The calculated shelf life in a sealed bag is 12 months at <40℃ and <80% relative humidity.
- Once the packaging is opened, the SiP must be mounted (per MSL4/Moisture Sensitivity Level 4) within 72 hours at <30˚C and <60% relative humidity.
- If the SiP is not mounted within 72 hours or if, when the dry pack is opened, the humidity indicator card displays >10% humidity, then the product must be baked for 48 hours at 125 ˚C (±5 ˚C).

13.7 Surface Mount Conditions

The following soldering conditions are recommended to ensure device quality.

13.7.1 Soldering

Note: When soldering, the stencil thickness should be ≥ 0.1 mm.

Convection reflow or IR/Convection reflow (one-time soldering or two-time soldering in air or nitrogen environment)

- Measuring point – IC package surface
- Temperature profile:

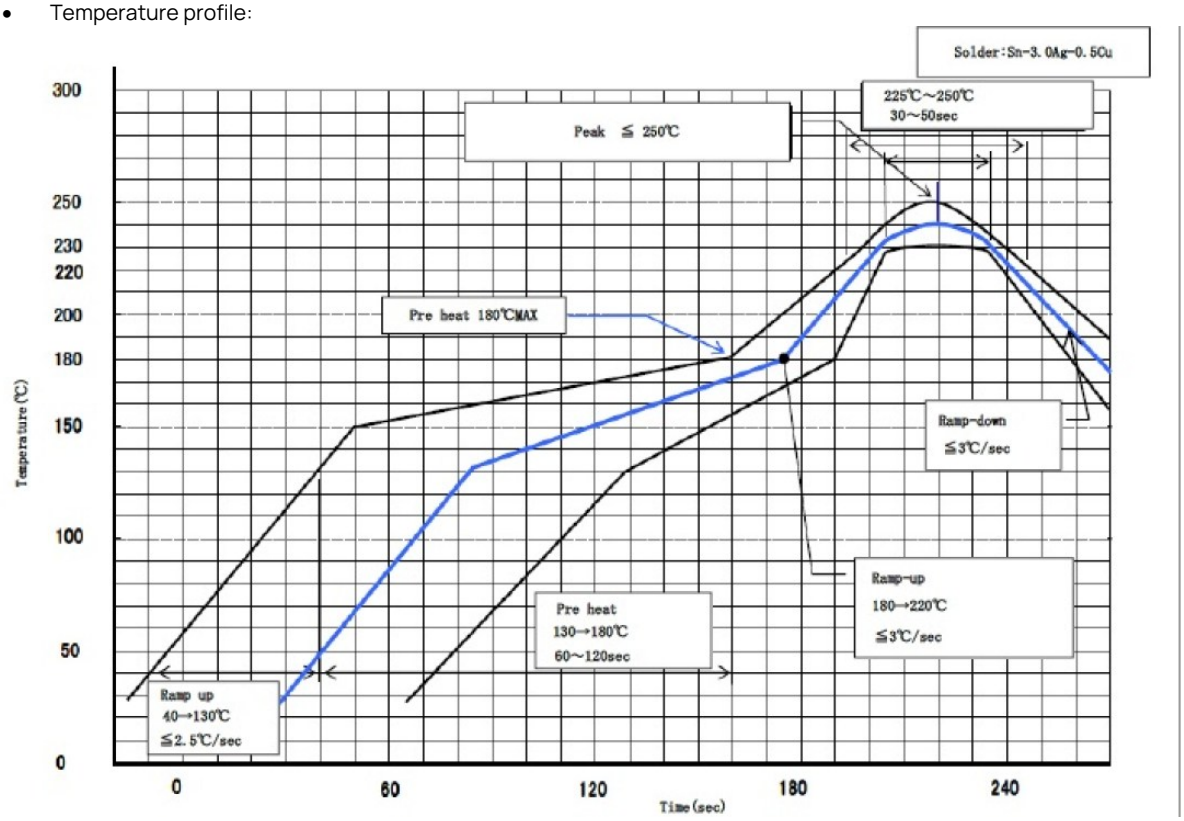


Figure 30: Temperature profile

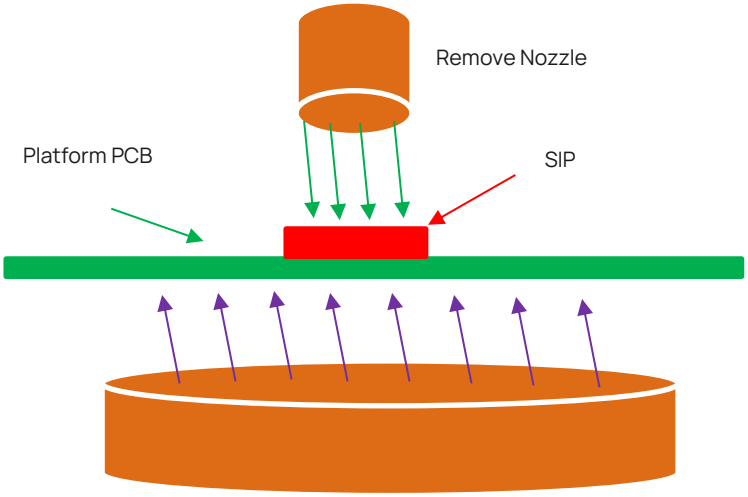
- Ramp-up: 40-130 °C. Less than 2.5 °C/sec
- Pre heat: 130-180 °C 60-120 sec, 180 °C MAX
- Ramp-up: 180-220 °C. Less than 3 °C/sec
- Peak Temperature: MAX 250 °C
  - 225 °C ~ 250 °C, 30 ~ 50 sec
- Ramp-down: Less than 3 °C/sec

13.7.2 Cautions When Removing the SIP from the Platform for RMA

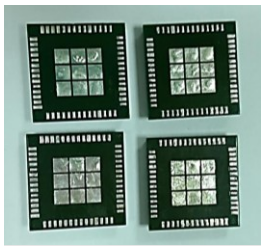
- Bake the platform before removing the SIP from the platform. Reference baking conditions.
- Remove the SIP by using a hot air gun. This process should be carried out by a skilled technician.

Suggestion conditions:

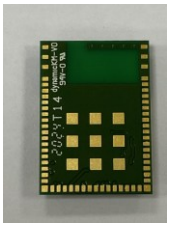
- One-side component platform:
  - Set the hot plate at 280 °C.
  - Put the platform on the hot plate for 8~10 seconds.
  - Remove the SIP from platform.
- Two-side components platform:
  - Use two hot air guns
  - On the bottom side, use a pre-heated nozzle (temperature setting of 200~250 °C) at a suitable distance from the platform PCB.
  - On the top side, apply a remove nozzle (temperature setting of 330 °C). Heat the SIP until it can be removed from platform PCB.



- Remove the residue solder under the bottom side of SIP. (Note: Alternate module pictured as an example)



(Not accepted for RMA)



(Accepted for RMA analysis)

Example SIP with residue solder on the bottom ***Example Module, no residue solder***

- Remove and clean the residue flux as needed.

13.7.3 Precautions for Use

- Opening/handing/removing must be done on an anti-ESD treated workbench. All workers must also have undergone anti-ESD treatment.
- The devices should be mounted within one year of the date of delivery.
- The Vela IF820 modules are MSL 4 rated.

14 Reliability Test

14.1 Climatic And Dynamic Reliability Test

Table 22: Climatic and Dynamic Reliability Test Results for Vela IF820 Modules

Test Item	Specification	Standard	Test Result
Thermal Shock	Temperature: -40 ~ 85℃ Ramp time: Less than 10 seconds. Dwell Time: 10 minutes Number of Cycles: 350 times	*JESD22-A106 *IEC 60068-2-14 for dwell time and number of cycles	Pass
Vibration Non-Operating Unpackaged device	Vibration Wave Form: Sine Waveform Vibration frequency / Displacement: 20-80 Hz/1.5mm Vibration frequency / Acceleration: 80-2000 Hz/20g Cycle Time: 4 min/cycle Number of Cycles: 4 cycle/axis Vibration Axes: X, Y and Z (Rotate each axis on vertical vibration table)	JEDEC 22-B103B (2016)	Pass
Mechanical Shock Non-Operating Unpackaged device	Pulse shape: Half-sine waveform Impact acceleration: 1500 g Pulse duration: 0.5 ms Number of shocks: 30 shocks (5 shocks for each face) Orientation: Bottom, top, left, right, front, and rear faces	JEDEC 22-B110B.01 (2019)	Pass

14.2 Reliability MTBF Prediction

Table 23: MTBF Predictions for Vela IF820 Modules

Ezurio Part Number	Environment	Standard	Test Result 45 ℃ (Hours)
453-00171R 453-00171C	Ground, Fixed, Uncontrolled	Telcordia Issue 3	7,920,607
453-00172R 453-00172C	Ground, Fixed, Uncontrolled	Telcordia Issue 3	8,084,775
450-00185	Ground, Fixed, Uncontrolled	Telcordia Issue 3	1,114,640.34
453-00171R 453-00171C	Mobile, Fixed, Uncontrolled	Telcordia Issue 3	2,970,228
453-00172R 453-00172C	Mobile, Fixed, Uncontrolled	Telcordia Issue 3	3,031,791
450-00185	Mobile, Fixed, Uncontrolled	Telcordia Issue 3	181,815.09
Ezurio Part Number	**Environment**	**Standard**	**Test Result 85 ℃ (Hours)**
453-00171R 453-00171C	Ground, Fixed, Uncontrolled	Telcordia Issue 3	1,839,958
453-00172R 453-00172C	Ground, Fixed, Uncontrolled	Telcordia Issue 3	1,8537,738
450-00185	Ground, Fixed, Uncontrolled	Telcordia Issue 3	2,549,301.59
453-00171R 453-00171C	Mobile, Fixed, Uncontrolled	Telcordia Issue 3	689,984
453-00172R 453-00172C	Mobile, Fixed, Uncontrolled	Telcordia Issue 3	696,652
450-00185	Mobile, Fixed, Uncontrolled	Telcordia Issue 3	440,892.82

15 Regulatory

Full regulatory information on the Vela IF820, including the Regulatory Information Guide, grants, and test reports are available on the Vela IF820 product page (coming soon).

The Vela IF820 holds current certifications in the following countries:

Table 24: Vela IF820 Certifications

Country/Region	Regulatory ID
USA (FCC)	SQG-VELAIF820
EU (ETSI)	N/A (No ID Number Required)
UKCA	N/A (No ID Number Required)
Canada (ISED)	3147A-VELAIF820
Japan (MIC)	201-230307
Australia (RCM)	N/A
New Zealand (RCM)	N/A
Korea	R-C-L8C-VELAIF820

15.1 Certified Antennas for the Vela IF820

Table 25: Certified Antennas for Vela IF820 Modules

Model	MPN	Manufacturer	Type	Connector	Peak Gain (2400 – 2500 MHz)
NanoBlue	EBL2400A1-10MH4L	Ezurio (Laird Connectivity)Ezurio	PCB Antenna	IPEX MHF4	2 dBi
FlexPIFA	001-0022	Ezurio (Laird Connectivity)Ezurio	Planar Inverted-F Type	IPEX MHF4	2 dBi
EDA-8709-2G4C1-B27-CY	EDA-8709-2G4C1-B27-CY (Ezurio Part#0600-00057)	MAG.LAYERS	Dipole	IPEX MHF4	2.32 dBi
mFlexPIFA	EFA2400A3S-10MH4L	Ezurio (Laird Connectivity)Ezurio	Planar Inverted-F Type	IPEX MHF4	2 dBi
AD1608	AD1608-A2455AAT/LF	ACX	Chip Antenna	N/A	1.0 dBi

16 Ordering Information

Table 26: Vela IF820 Ordering Part Numbers

Part	Description
453-00171R	Vela IF820 - Dual Mode Bluetooth Module, Integrated Antenna (Infineon CYW20820) - Tape / Reel
453-00171C	Vela IF820 - Dual Mode Bluetooth Module, Integrated Antenna (Infineon CYW20820) – Cut / Tape
453-00172R	Vela IF820 - Dual Mode Bluetooth Module, MHF4 Connector (Infineon CYW20820) - Tape / Reel
453-00172C	Vela IF820 - Dual Mode Bluetooth Module, MHF4 Connector (Infineon CYW20820) – Cut / Tape
453-00171-K1	Vela IF820 - Development Kit with integrated chip antenna
453-00172-K1	Vela IF820 - Development Kit with MHF4 Connector
450-00185	Vela IF820 - Dual Mode Bluetooth USB Adapter with integrated antenna variant (Infineon CYW20820)

16.1 General Comments

This is a preliminary datasheet. Please check with Ezurio for the latest information before commencing a design. If in doubt, ask. For additional information visit Vela IF820 product page.

17 Bluetooth Qualification Process

17.1 Overview

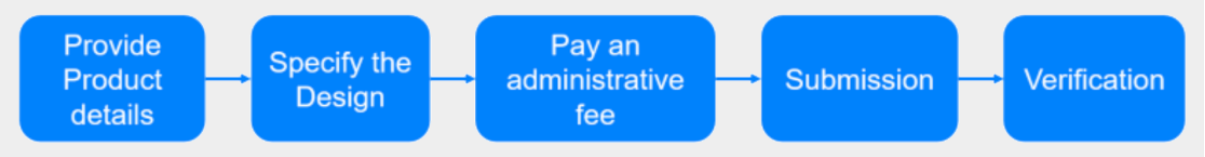
The Bluetooth Qualification Process promotes global product interoperability and reinforces the strength of the Bluetooth® brand and ecosystem to the benefit of all Bluetooth SIG members. The Bluetooth Qualification Process helps member companies ensure their products that incorporate Bluetooth technology comply with the Bluetooth Patent & Copyright License Agreement and the Bluetooth Trademark License Agreement (collectively, the Bluetooth License Agreement) and Bluetooth Specifications.

The Bluetooth Qualification Process is defined by the Qualification Program Reference Document (QPRD) v3.

To demonstrate that a product complies with the Bluetooth Specification(s), each member must for each of its products:

- Identify the product, the design included in the product, the Bluetooth Specifications that the design implements, and the features of each implemented specification
- Complete the Bluetooth Qualification Process by submitting the required documentation for the product under a user account belonging to your company

The Bluetooth Qualification Process consists of the phases shown below:



To complete the Qualification Process the company developing a Bluetooth End Product shall be a member of the Bluetooth SIG. To start the application please use the following link: Apply for Adopter Membership

17.2 Scope

This guide is intended to provide guidance on the Bluetooth Qualification Process for End Products that reference multiple existing designs, that have not been modified, (refer to Section 3.2.2.1 of the Qualification Program Reference Document v3).

For a Product that includes a new Design created by combining two or more unmodified designs that have DNs or QDIDs into one of the permitted combinations in Table 3.1 of the QPRDv3, a Member must also provide the following information:

- DNs or QDIDs for Designs included in the new Design
- The desired Core Configuration of the new Design (if applicable, see Table 3.1 below)
- The active TCRL Package version used for checking the applicable Core Configuration (including transport compatibility) and evaluating test requirements

Any included Design must not implement any Layers using withdrawn specification(s).

When creating a new Design using Option 2a, the Inter-Layer Dependency (ILD) between Layers included in the Design will be checked based on the latest TCRL Package version used among the included Designs.

For the purposes of this document, it is assumed that the member is combining unmodified Core-Controller Configuration and Core-Host Configuration designs, to complete a Core-Complete Configuration.

17.3 Qualification Steps When Referencing multiple existing designs, (unmodified) – Option 2a in the QPRDv3

For this qualification option, follow these steps:

1. To start a listing, go to: https://qualification.bluetooth.com/
2. Select **Start the Bluetooth Qualification Process**.
3. Product Details to be entered:
    - Project Name (this can be the product name or the Bluetooth Design name).
    - Product Description
    - Model Number

- Product Publication Date (the product publication date may not be later than 90 days after submission)
- Product Website (optional)
- Internal Visibility (this will define if the product will be visible to other users prior to publication)
- If you have multiple End Products to list then you can select 'Import Multiple Products', firstly downloading and completing the template, then by 'Upload Product List'. This will populate Qualification Workspace with all your products.

4. Specify the Design:
   - Do you include any existing Design(s) in your Product? Answer Yes, I do.
   - Enter the multiple DNs or QDIDs used in your, (for Option 2a two or more DNs or QDIDs must be referenced)
   - Select 'I'm finished entering DN's
   - Once the DNs or QDIDs are selected they will appear on the left-hand side, indicating the layers covered by the design (should show Core-Controller and Core Host Layers covered).
   - What do you want to do next? Answer, 'Combine unmodified Designs'.
   - The Qualification Workspace Tool will indicate that a new Design will be created and what type of Core-Complete configuration is selected.
   - An active TCRL will be selected for the design.
   - Perform the Consistency Check, which should result in no inconsistencies
   - If there are any inconsistencies these will need to be resolved before proceeding
   - Save and go to Test Plan and Documentation
5. Test Plan and Documentation
   a. As no modifications have been made to the combined designs the tool should report the following message:
   'No test plan has been generated for your new Design. Test declarations and test reports do not need to be submitted. You can continue to the next step.'
   b. Save and go to Product Qualification fee
6. Product Qualification Fee:
   - It's important to make sure a Prepaid Product Qualification fee is available as it is required at this stage to complete the Qualification Process.
   - Prepaid Product Qualification Fee's will appear in the available list so select one for the listing.
   - If one is not available select 'Pay Product Qualification Fee', payment can be done immediately via credit card, or you can pay via Invoice. Payment via credit will release the number immediately, if paying via invoice the number will not be released until the invoice is paid.
   - Once you have selected the Prepaid Qualification Fee, select 'Save and go to Submission'
7. Submission:
   - Some automatic checks occur to ensure all submission requirements are complete.
   - To complete the listing any errors must be corrected
   - Once you have confirmed all design information is correct, tick all of the three check boxes and add your name to the signature page.
   - Now select 'Complete the Submission'.
   - You will be asked a final time to confirm you want to proceed with the submission, select 'Complete the Submission'.
   - Qualification Workspace will confirm the submission has been submitted. The Bluetooth SIG will email confirmation once the submission has been accepted, (normally this takes 1 working day).
8. Download Product and Design Details (SDoC):
   a. You can now download a copy of the confirmed listing from the design listing page and save a copy in your Compliance Folder

For further information, please refer to the following webpage:
https://www.bluetooth.com/develop-with-bluetooth/qualification-listing/

17.4 Example Design Combinations

The following gives an example of a design possible under option 2a:

Ezurio Controller Subsystem + AIROC™ Bluetooth Host Software Stack (Ezurio Vela IF820-based design)

Design Name	Owner	Declaration ID	QD ID	Link to listing on the SIG website
Vela IF820	Ezurio	D063148	217016	https://qualification.bluetooth.com/ListingDetails/192311
AIROC™ Bluetooth Host Software Stack	Infineon	D065385	223736	https://qualification.bluetooth.com/ListingDetails/194929

17.5 Qualify More Products

If you develop further products based on the same design in the future, it is possible to add them free of charge. The new product must not modify the existing design i.e add ICS functionality, otherwise a new design listing will be required.

To add more products to your design, select 'Manage Submitted Products' in the Getting Started page, Actions, Qualify More Products. The tool will take you through the updating process.

18 453-00171 Integrated Chip Antenna Performance

The following are details and plots of the measured radiation performance of the chip antenna on the Vela IF820 module with integrated antenna (part numbers 453-00171R and 453-00171C).

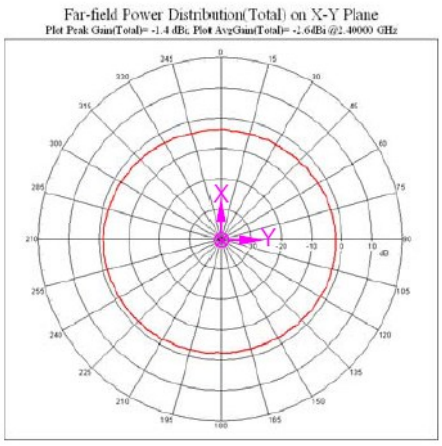
18.1 Summary of Antenna Performance

Unit in dBi	XY-plane		XZ-plane		YZ-plane		Efficiency
	Peak	Avg.	Peak	Avg.	Peak	Avg.	
@2400MHz	-1.4	-2.6	-2.1	-5	0.1	-2.8	45%
@2440MHz	-1.5	-2.3	-1.2	-4.3	0.6	-2.3	51%
@2480MHz	-2.1	-2.7	-1.8	-4.4	0.2	-2.7	48%

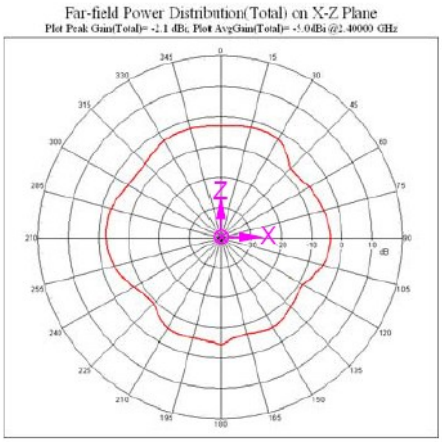
Note: The result is measured with Ezurio DVK part # 453-00171-K1.

1 2.4GHz Radiated Performance

XY-plane



XZ-plane



YZ-plane

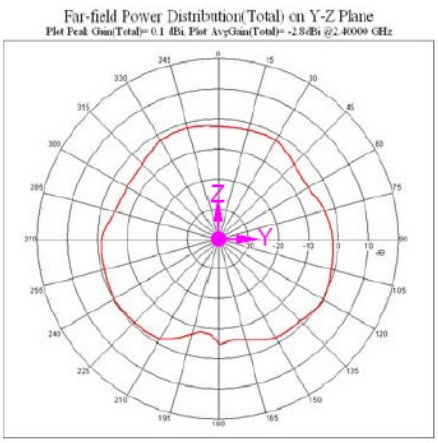
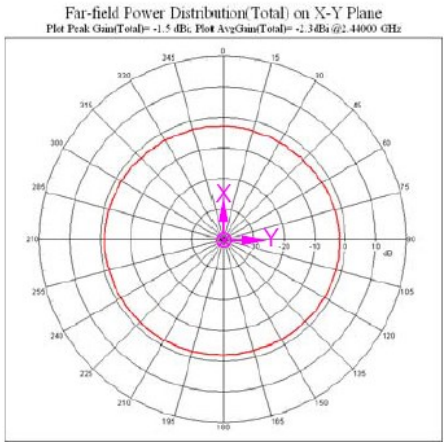
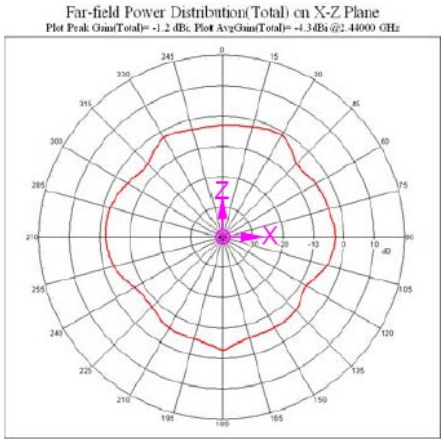


Figure 31: 2400 MHz radiation pattern

XY-plane



XZ-plane



YZ-plane

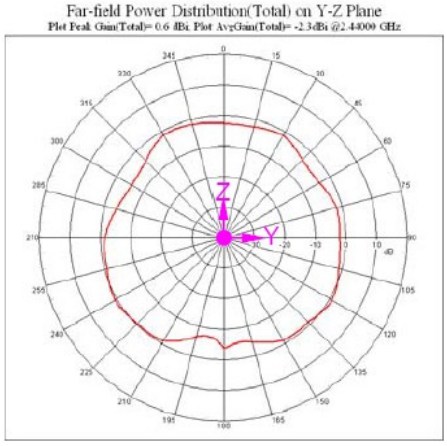
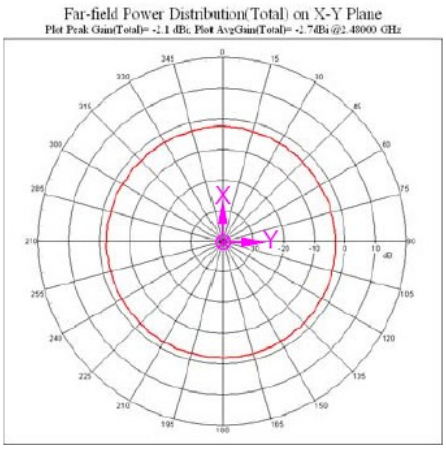
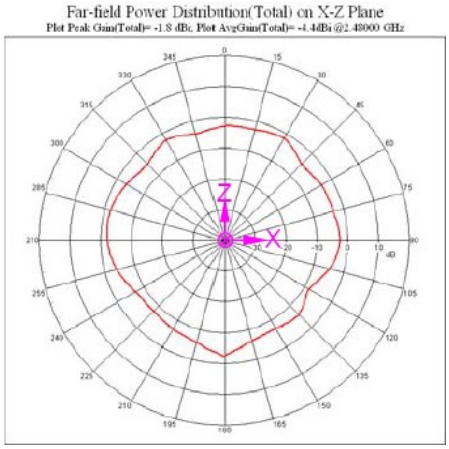


Figure 32: 2440 MHz radiation pattern

XY-plane



XZ-plane



YZ-plane

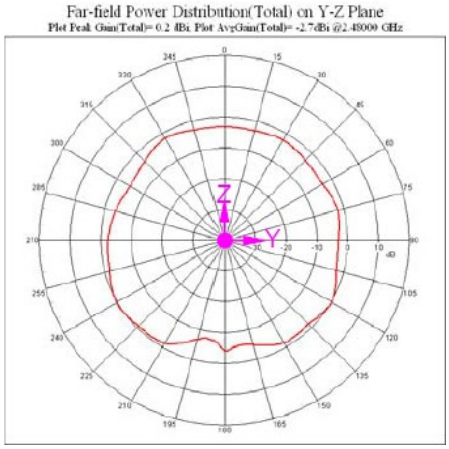


Figure 33: 2480 MHz radiation pattern

19 453-00185 USB Adapter Integrated Antenna Performance

The following are details and plots of the measured radiation performance of the integrated antenna on the Vela IF820 USB adapter (part number 453-00185).

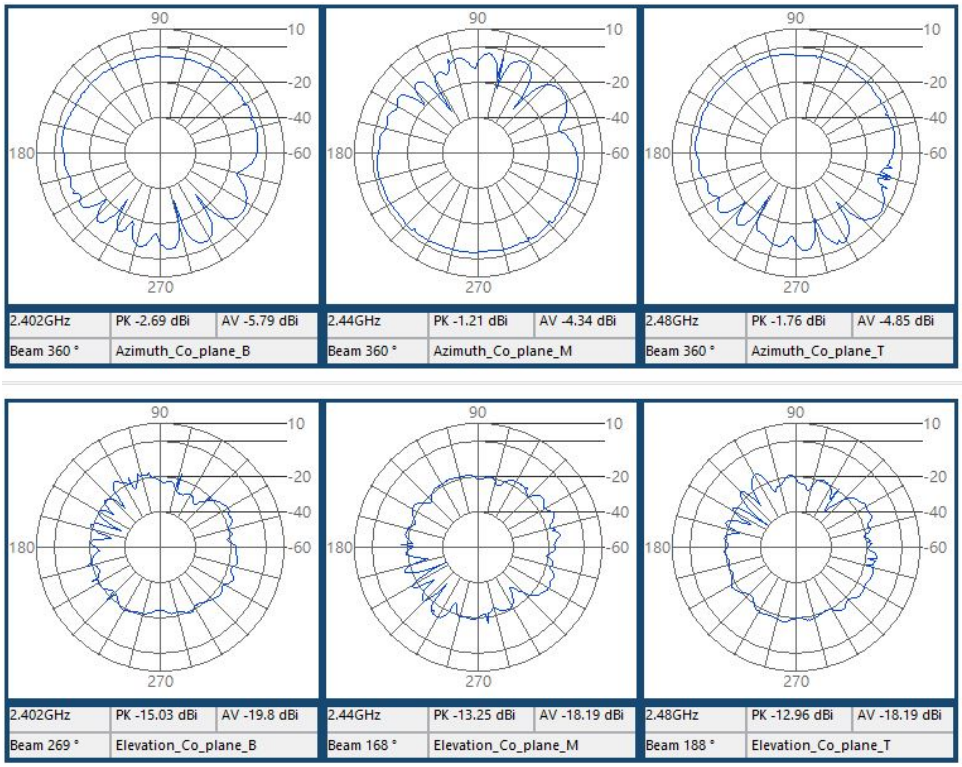
19.1 Summary of Antenna Performance

Unit in dBi	XY-plane		XZ-plane		YZ-plane	
	Peak	Avg.	Peak	Avg.	Peak	Avg.
@2400MHz	-2.69	-5.79	-4.47	-9.66	-4.92	-8.14
@2440MHz	-1.21	-4.34	-3.39	-8.67	-2.62	-5.35
@2480MHz	-1.76	-4.85	-3.71	-9.47	-2.27	-5.82

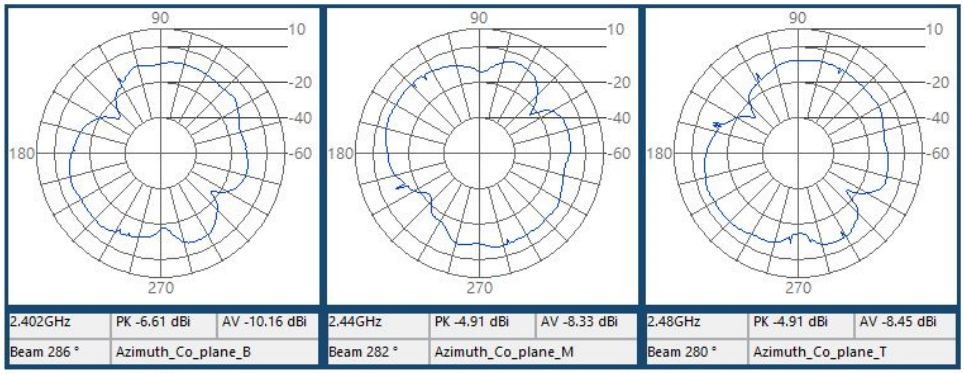
Note: The result is measured with USB adapter (part # 450-00185).

19.2 2.4GHz Radiated Pattern

19.2.1 X-Axis



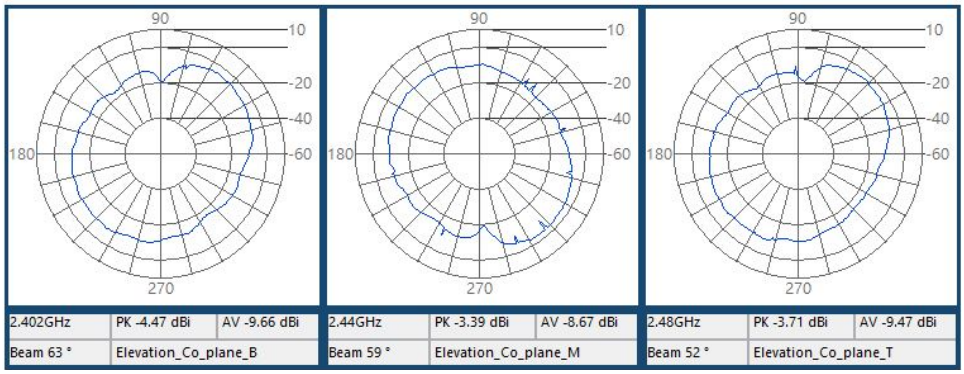
19.2.2 Y-axis



2.402GHz	PK -6.61 dBi	AV -10.16 dBi
Beam 286 °	Azimuth_Co_plane_B	

2.44GHz	PK -4.91 dBi	AV -8.33 dBi
Beam 282 °	Azimuth_Co_plane_M	

2.48GHz	PK -4.91 dBi	AV -8.45 dBi
Beam 280 °	Azimuth_Co_plane_T	

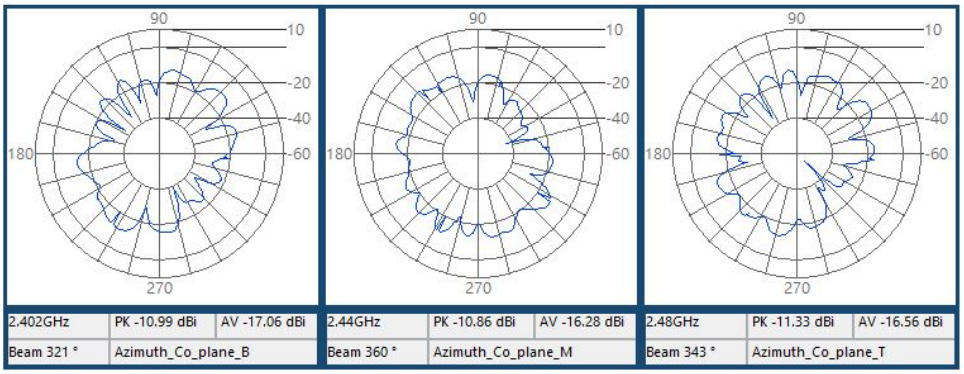


2.402GHz	PK -4.47 dBi	AV -9.66 dBi
Beam 63 °	Elevation_Co_plane_B	

2.44GHz	PK -3.39 dBi	AV -8.67 dBi
Beam 59 °	Elevation_Co_plane_M	

2.48GHz	PK -3.71 dBi	AV -9.47 dBi
Beam 52 °	Elevation_Co_plane_T	

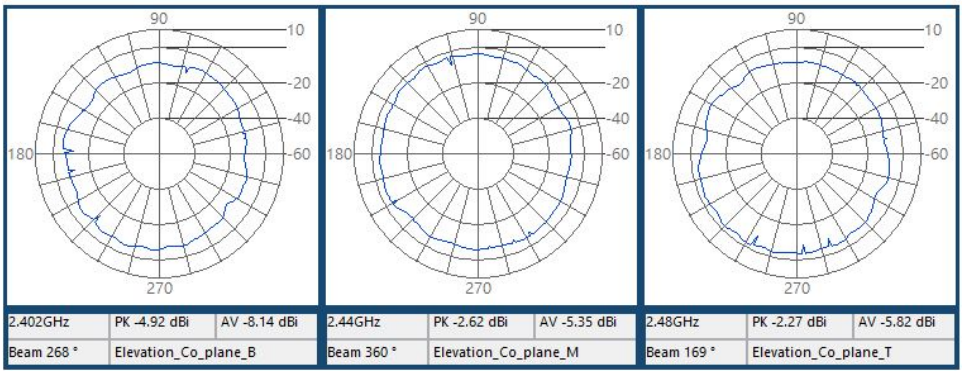
2 Z-axis



2.402GHz	PK -10.99 dBi	AV -17.06 dBi
Beam 321 °	Azimuth_Co_plane_B	

2.44GHz	PK -10.86 dBi	AV -16.28 dBi
Beam 360 °	Azimuth_Co_plane_M	

2.48GHz	PK -11.33 dBi	AV -16.56 dBi
Beam 343 °	Azimuth_Co_plane_T	



2.402GHz	PK -4.92 dBi	AV -8.14 dBi
Beam 268 °	Elevation_Co_plane_B	

2.44GHz	PK -2.62 dBi	AV -5.35 dBi
Beam 360 °	Elevation_Co_plane_M	

2.48GHz	PK -2.27 dBi	AV -5.82 dBi
Beam 169 °	Elevation_Co_plane_T	

20 Additional Information

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