



## KL16 Sub-Family Data Sheet

Supports the following:

MKL16Z32VFM4, MKL16Z64VFM4,  
MKL16Z128VFM4, MKL16Z32VFT4,  
MKL16Z64VFT4, MKL16Z128VFT4,  
MKL16Z32VLH4, MKL16Z64VLH4,  
MKL16Z128VLH4

### Features

- Operating Characteristics
  - Voltage range: 1.71 to 3.6 V
  - Flash write voltage range: 1.71 to 3.6 V
  - Temperature range (ambient): -40 to 105°C
- Performance
  - Up to 48 MHz ARM® Cortex-M0+ core
- Memories and memory interfaces
  - 128 KB program flash memory
  - 16 KB RAM
- Clocks
  - 32 kHz to 40 kHz or 3 MHz to 32 MHz crystal oscillator
  - Multi-purpose clock source
- System peripherals
  - Nine low-power modes to provide power optimization based on application requirements
  - 4-channel DMA controller, supporting up to 63 request sources
  - COP Software watchdog
  - Low-leakage wakeup unit
  - SWD interface and Micro Trace buffer
  - Bit Manipulation Engine (BME)
- Security and integrity modules
  - 80-bit unique identification (ID) number per chip
- Human-machine interface
  - Low-power hardware touch sensor interface (TSI)
  - General-purpose input/output
- Analog modules
  - 16-bit SAR ADC
  - 12-bit DAC
  - Analog comparator (CMP) containing a 6-bit DAC and programmable reference input
- Timers
  - Six channel Timer/PWM (TPM)
  - Two 2-channel Timer/PWM (TPM)
  - Periodic interrupt timers
  - 16-bit low-power timer (LPTMR)
  - Real-time clock
- Communication interfaces
  - Two 16-bit SPI modules
  - Two I2C modules
  - I2S (SAI) module
  - One low power UART module
  - Two UART modules

## KL16P64M48SF5



Freescale reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

# Table of Contents

1	Ordering parts.....	3	5.3	Switching specifications.....	20
1.1	Determining valid orderable parts.....	3	5.3.1	Device clock specifications.....	20
2	Part identification.....	3	5.3.2	General switching specifications.....	21
2.1	Description.....	3	5.4	Thermal specifications.....	21
2.2	Format.....	3	5.4.1	Thermal operating requirements.....	21
2.3	Fields.....	3	5.4.2	Thermal attributes.....	21
2.4	Example.....	4	6	Peripheral operating requirements and behaviors.....	22
3	Terminology and guidelines.....	4	6.1	Core modules.....	22
3.1	Definition: Operating requirement.....	4	6.1.1	SWD electricals .....	22
3.2	Definition: Operating behavior.....	4	6.2	System modules.....	23
3.3	Definition: Attribute.....	5	6.3	Clock modules.....	24
3.4	Definition: Rating.....	5	6.3.1	MCG specifications.....	24
3.5	Result of exceeding a rating.....	6	6.3.2	Oscillator electrical specifications.....	25
3.6	Relationship between ratings and operating requirements.....	6	6.4	Memories and memory interfaces.....	28
3.7	Guidelines for ratings and operating requirements.....	6	6.4.1	Flash electrical specifications.....	28
3.8	Definition: Typical value.....	7	6.5	Security and integrity modules.....	29
3.9	Typical value conditions.....	8	6.6	Analog.....	29
4	Ratings.....	8	6.6.1	ADC electrical specifications.....	29
4.1	Thermal handling ratings.....	8	6.6.2	CMP and 6-bit DAC electrical specifications.....	34
4.2	Moisture handling ratings.....	8	6.6.3	12-bit DAC electrical characteristics.....	36
4.3	ESD handling ratings.....	8	6.7	Timers.....	39
4.4	Voltage and current operating ratings.....	9	6.8	Communication interfaces.....	39
5	General.....	9	6.8.1	SPI switching specifications.....	39
5.1	AC electrical characteristics.....	9	6.8.2	Inter-Integrated Circuit Interface (I2C) timing.....	43
5.2	Nonswitching electrical specifications.....	10	6.8.3	UART.....	44
5.2.1	Voltage and current operating requirements.....	10	6.8.4	I2S/SAI switching specifications.....	45
5.2.2	LVD and POR operating requirements.....	11	6.9	Human-machine interfaces (HMI).....	49
5.2.3	Voltage and current operating behaviors.....	11	6.9.1	TSI electrical specifications.....	49
5.2.4	Power mode transition operating behaviors.....	12	7	Dimensions.....	49
5.2.5	Power consumption operating behaviors.....	13	7.1	Obtaining package dimensions.....	49
5.2.6	EMC radiated emissions operating behaviors.....	19	8	Pinout.....	50
5.2.7	Designing with radiated emissions in mind.....	20	8.1	KL16 Signal Multiplexing and Pin Assignments.....	50
5.2.8	Capacitance attributes.....	20	8.2	KL16 pinouts.....	52

# 1 Ordering parts

## 1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to [freescale.com](http://freescale.com) and perform a part number search for the following device numbers: PKL16 and MKL16

## 2 Part identification

### 2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

### 2.2 Format

Part numbers for this device have the following format:

Q KL## A FFF R T PP CC N

### 2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	<ul style="list-style-type: none"> <li>M = Fully qualified, general market flow</li> <li>P = Prequalification</li> </ul>
KL##	Kinetis family	<ul style="list-style-type: none"> <li>KL16</li> </ul>
A	Key attribute	<ul style="list-style-type: none"> <li>Z = Cortex-M0+</li> </ul>
FFF	Program flash memory size	<ul style="list-style-type: none"> <li>32 = 32 KB</li> <li>64 = 64 KB</li> <li>128 = 128 KB</li> </ul>
R	Silicon revision	<ul style="list-style-type: none"> <li>(Blank) = Main</li> <li>A = Revision after main</li> </ul>

*Table continues on the next page...*

## Terminology and guidelines

Field	Description	Values
T	Temperature range (°C)	<ul style="list-style-type: none"><li>• V = -40 to 105</li></ul>
PP	Package identifier	<ul style="list-style-type: none"><li>• FM = 32 QFN (5 mm x 5 mm)</li><li>• FT = 48 QFN (7 mm x 7 mm)</li><li>• LH = 64 LQFP (10 mm x 10 mm)</li></ul>
CC	Maximum CPU frequency (MHz)	<ul style="list-style-type: none"><li>• 4 = 48 MHz</li></ul>
N	Packaging type	<ul style="list-style-type: none"><li>• R = Tape and reel</li></ul>

## 2.4 Example

This is an example part number:

MKL16Z128VFM4

## 3 Terminology and guidelines

### 3.1 Definition: Operating requirement

An *operating requirement* is a specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip.

#### 3.1.1 Example

This is an example of an operating requirement:

Symbol	Description	Min.	Max.	Unit
V <sub>DD</sub>	1.0 V core supply voltage	0.9	1.1	V

### 3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

### 3.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
$I_{WP}$	Digital I/O weak pullup/ pulldown current	10	130	$\mu\text{A}$

### 3.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

#### 3.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
$C_{IN\_D}$	Input capacitance: digital pins	—	7	$\text{pF}$

### 3.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

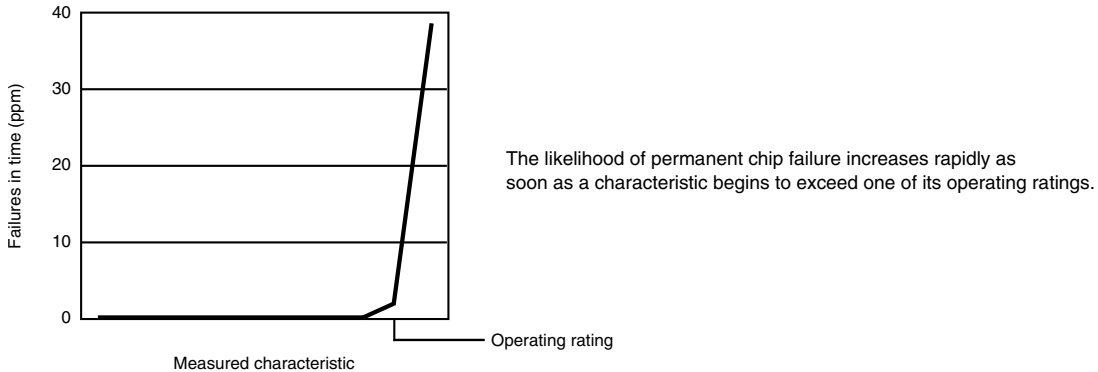
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

#### 3.4.1 Example

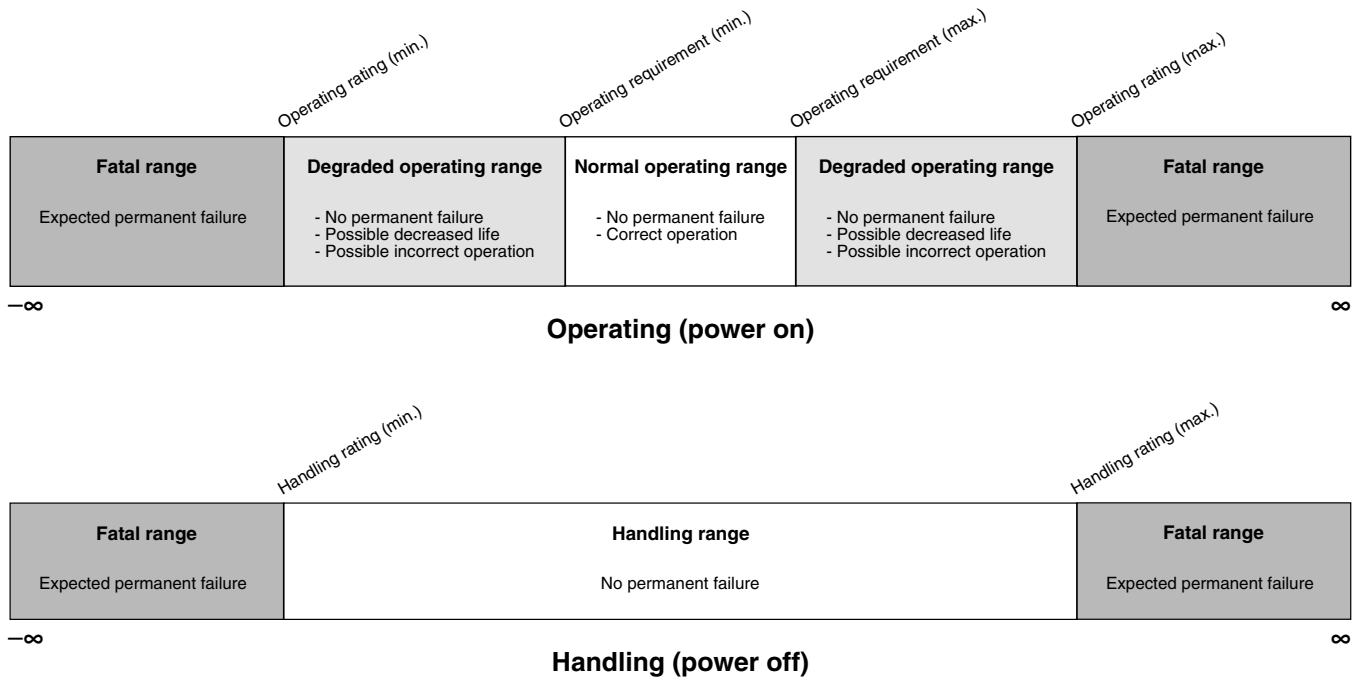
This is an example of an operating rating:

Symbol	Description	Min.	Max.	Unit
$V_{DD}$	1.0 V core supply voltage	-0.3	1.2	V

### 3.5 Result of exceeding a rating



### 3.6 Relationship between ratings and operating requirements



### 3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip’s ratings.
- During normal operation, don’t exceed any of the chip’s operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

### 3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

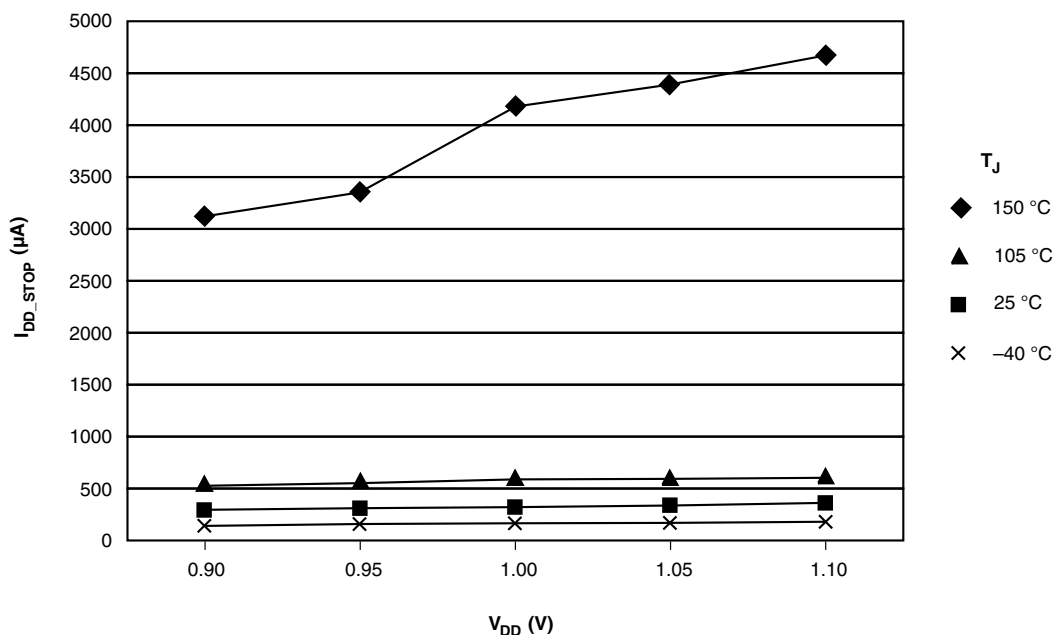
#### 3.8.1 Example 1

This is an example of an operating behavior that includes a typical value:

Symbol	Description	Min.	Typ.	Max.	Unit
$I_{WP}$	Digital I/O weak pullup/pulldown current	10	70	130	$\mu\text{A}$

#### 3.8.2 Example 2

This is an example of a chart that shows typical values for various voltage and temperature conditions:



## 3.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

**Table 1. Typical value conditions**

Symbol	Description	Value	Unit
$T_A$	Ambient temperature	25	°C
$V_{DD}$	3.3 V supply voltage	3.3	V

## 4 Ratings

### 4.1 Thermal handling ratings

**Table 2. Thermal handling ratings**

Symbol	Description	Min.	Max.	Unit	Notes
$T_{STG}$	Storage temperature	-55	150	°C	1
$T_{SDR}$	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

### 4.2 Moisture handling ratings

**Table 3. Moisture handling ratings**

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.



## 4.3 ESD handling ratings

Table 4. ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
$V_{HBM}$	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
$V_{CDM}$	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
$I_{LAT}$	Latch-up current at ambient temperature of 105 °C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

## 4.4 Voltage and current operating ratings

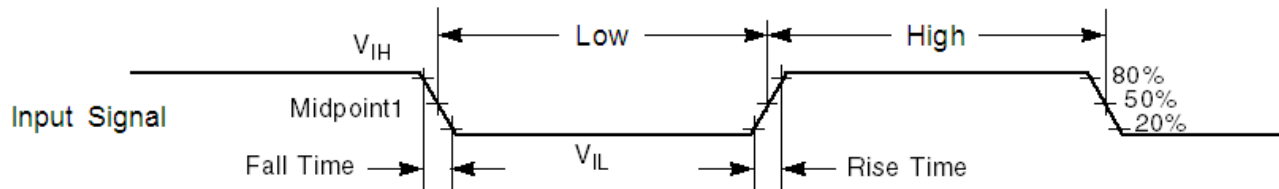
Table 5. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
$V_{DD}$	Digital supply voltage	-0.3	3.8	V
$I_{DD}$	Digital supply current	—	120	mA
$V_{IO}$	IO pin input voltage	-0.3	$V_{DD} + 0.3$	V
$I_D$	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA
$V_{DDA}$	Analog supply voltage	$V_{DD} - 0.3$	$V_{DD} + 0.3$	V

## 5 General

### 5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is  $V_{IL} + (V_{IH} - V_{IL})/2$ .

**Figure 1. Input signal measurement reference**

All digital I/O switching characteristics, unless otherwise specified, assume the output pins have the following characteristics.

- $C_L=30$  pF loads
- Slew rate disabled
- Normal drive strength

## 5.2 Nonswitching electrical specifications

### 5.2.1 Voltage and current operating requirements

**Table 6. Voltage and current operating requirements**

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DD}$	Supply voltage	1.71	3.6	V	
$V_{DDA}$	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	$V_{DD}$ -to- $V_{DDA}$ differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	$V_{SS}$ -to- $V_{SSA}$ differential voltage	-0.1	0.1	V	
$V_{IH}$	Input high voltage	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	$0.7 \times V_{DD}$	—	V
		• $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$	$0.75 \times V_{DD}$	—	V
$V_{IL}$	Input low voltage	• $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$	—	$0.35 \times V_{DD}$	V
		• $1.7\text{ V} \leq V_{DD} \leq 2.7\text{ V}$	—	$0.3 \times V_{DD}$	V
$V_{HYS}$	Input hysteresis	$0.06 \times V_{DD}$	—	V	
$I_{CIO}$	IO pin negative DC injection current — single pin	-3	—	mA	1
$I_{Ccont}$	Contiguous pin DC injection current — regional limit, includes sum of negative injection currents of 16 contiguous pins	• Negative current injection	-25	—	mA

Table continues on the next page...

**Table 6. Voltage and current operating requirements (continued)**

Symbol	Description	Min.	Max.	Unit	Notes
V <sub>ODPU</sub>	Open drain pullup voltage level	V <sub>DD</sub>	V <sub>DD</sub>	V	2
V <sub>RAM</sub>	V <sub>DD</sub> voltage required to retain RAM	1.2	—	V	

- All I/O pins are internally clamped to V<sub>SS</sub> through a ESD protection diode. There is no diode connection to V<sub>DD</sub>. If V<sub>IN</sub> greater than V<sub>IO\_MIN</sub> (= V<sub>SS</sub>-0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as  $R = (V_{IO\_MIN} - V_{IN})/|I_{CIO}|$ .
- Open drain outputs must be pulled to V<sub>DD</sub>.

## 5.2.2 LVD and POR operating requirements

**Table 7. V<sub>DD</sub> supply LVD and POR operating requirements**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V <sub>POR</sub>	Falling V <sub>DD</sub> POR detect voltage	0.8	1.1	1.5	V	—
V <sub>LVDH</sub>	Falling low-voltage detect threshold — high range (LVDV = 01)	2.48	2.56	2.64	V	—
	Low-voltage warning thresholds — high range					1
V <sub>LW1H</sub>	• Level 1 falling (LVWV = 00)	2.62	2.70	2.78	V	
V <sub>LW2H</sub>	• Level 2 falling (LVWV = 01)	2.72	2.80	2.88	V	
V <sub>LW3H</sub>	• Level 3 falling (LVWV = 10)	2.82	2.90	2.98	V	
V <sub>LW4H</sub>	• Level 4 falling (LVWV = 11)	2.92	3.00	3.08	V	
V <sub>HYSH</sub>	Low-voltage inhibit reset/recover hysteresis — high range	—	±60	—	mV	—
V <sub>LVDL</sub>	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	—
	Low-voltage warning thresholds — low range					1
V <sub>LW1L</sub>	• Level 1 falling (LVWV = 00)	1.74	1.80	1.86	V	
V <sub>LW2L</sub>	• Level 2 falling (LVWV = 01)	1.84	1.90	1.96	V	
V <sub>LW3L</sub>	• Level 3 falling (LVWV = 10)	1.94	2.00	2.06	V	
V <sub>LW4L</sub>	• Level 4 falling (LVWV = 11)	2.04	2.10	2.16	V	
V <sub>HYSL</sub>	Low-voltage inhibit reset/recover hysteresis — low range	—	±40	—	mV	—
V <sub>BG</sub>	Bandgap voltage reference	0.97	1.00	1.03	V	—
t <sub>LPO</sub>	Internal low power oscillator period — factory trimmed	900	1000	1100	µs	—

- Rising thresholds are falling threshold + hysteresis voltage

## 5.2.3 Voltage and current operating behaviors

**Table 8. Voltage and current operating behaviors**

Symbol	Description	Min.	Max.	Unit	Notes
$V_{OH}$	Output high voltage — Normal drive pad (except RESET_b) <ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OH} = -5\text{ mA}</math></li> <li>• <math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OH} = -2.5\text{ mA}</math></li> </ul>	$V_{DD} - 0.5$	—	V	1, 2
		$V_{DD} - 0.5$	—	V	
$V_{OH}$	Output high voltage — High drive pad (except RESET_b) <ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OH} = -20\text{ mA}</math></li> <li>• <math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OH} = -10\text{ mA}</math></li> </ul>	$V_{DD} - 0.5$	—	V	1, 2
		$V_{DD} - 0.5$	—	V	
$I_{OHT}$	Output high current total for all ports	—	100	mA	
$V_{OL}$	Output low voltage — Normal drive pad <ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OL} = 5\text{ mA}</math></li> <li>• <math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OL} = 2.5\text{ mA}</math></li> </ul>	—	0.5	V	1
		—	0.5	V	
$V_{OL}$	Output low voltage — High drive pad <ul style="list-style-type: none"> <li>• <math>2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}</math>, <math>I_{OL} = 20\text{ mA}</math></li> <li>• <math>1.71\text{ V} \leq V_{DD} \leq 2.7\text{ V}</math>, <math>I_{OL} = 10\text{ mA}</math></li> </ul>	—	0.5	V	1
		—	0.5	V	
$I_{OLT}$	Output low current total for all ports	—	100	mA	
$I_{IN}$	Input leakage current (per pin) for full temperature range	—	1	$\mu\text{A}$	3
$I_{IN}$	Input leakage current (per pin) at 25 °C	—	0.025	$\mu\text{A}$	3
$I_{IN}$	Input leakage current (total all pins) for full temperature range	—	65	$\mu\text{A}$	3
$I_{OZ}$	Hi-Z (off-state) leakage current (per pin)	—	1	$\mu\text{A}$	
$R_{PU}$	Internal pullup resistors	20	50	k $\Omega$	4

1. The reset pin only contains an active pull down device when configured as the RESET signal or as a GPIO. When configured as a GPIO output, it acts as a pseudo open drain output.
2. PTB0, PTB1, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTX\_PCRn[DSE] control bit. All other GPIOs are normal drive only.
3. Measured at  $V_{DD} = 3.6\text{ V}$
4. Measured at  $V_{DD}$  supply voltage =  $V_{DD}$  min and  $V_{input} = V_{SS}$

## 5.2.4 Power mode transition operating behaviors

All specifications except  $t_{POR}$  and  $V_{LLSx} \rightarrow \text{RUN}$  recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- FEI clock mode

POR and VLLS<sub>x</sub>→RUN recovery use FEI clock mode at the default CPU and system frequency of 21 MHz, and a bus and flash clock frequency of 10.5 MHz.

**Table 9. Power mode transition operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t <sub>POR</sub>	After a POR event, amount of time from the point V <sub>DD</sub> reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	—	—	300	μs	1
	• VLLS0 → RUN	—	106	120	μs	
	• VLLS1 → RUN	—	105	117	μs	
	• VLLS3 → RUN	—	47	54	μs	
	• LLS → RUN	—	4.5	5.0	μs	
	• VLPS → RUN	—	4.5	5.0	μs	
	• STOP → RUN	—	4.5	5.0	μs	

1. Normal boot (FTFA\_FOFT[LPBOOT]=11).

## 5.2.5 Power consumption operating behaviors

**Table 10. Power consumption operating behaviors**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DDA</sub>	Analog supply current	—	—	See note	mA	1
I <sub>DD_RUNCO_CM</sub>	Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus disabled, LPTMR running using 4 MHz internal reference clock, CoreMark benchmark code executing from flash • at 3.0 V	—	6.1	—	mA	2
I <sub>DD_RUNCO</sub>	Run mode current in compute operation - 48 MHz core / 24 MHz flash / bus clock disabled, code of while(1) loop executing from flash • at 3.0 V	—	3.8	5.9	mA	3
I <sub>DD_RUN</sub>	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash • at 3.0 V	—	4.6	6.1	mA	3

Table continues on the next page...

**Table 10. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DD_RUN</sub>	Run mode current - 48 MHz core / 24 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash <ul style="list-style-type: none"> <li>at 3.0 V <ul style="list-style-type: none"> <li>at 25 °C</li> <li>at 70 °C</li> <li>at 125 °C</li> </ul> </li> </ul>	—	6.0	6.5	mA	3, 4
I <sub>DD_WAIT</sub>	Wait mode current - core disabled / 48 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled <ul style="list-style-type: none"> <li>at 3.0 V</li> </ul>	—	2.7	5.7	mA	3
I <sub>DD_WAIT</sub>	Wait mode current - core disabled / 24 MHz system / 24 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled <ul style="list-style-type: none"> <li>at 3.0 V</li> </ul>	—	2.1	5.5	mA	3
I <sub>DD_PSTOP2</sub>	Stop mode current with partial stop 2 clocking option - core and system disabled / 10.5 MHz bus <ul style="list-style-type: none"> <li>at 3.0 V</li> </ul>	—	2.2	4.1	mA	3
I <sub>DD_VLPRCO_CM</sub>	Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, LPTMR running with 4 MHz internal reference clock, CoreMark benchmark code executing from flash <ul style="list-style-type: none"> <li>at 3.0 V</li> </ul>	—	732	—	μA	5
I <sub>DD_VLPRCO</sub>	Very-low-power run mode current in compute operation - 4 MHz core / 0.8 MHz flash / bus clock disabled, code of while(1) loop executing from flash <ul style="list-style-type: none"> <li>at 3.0 V</li> </ul>	—	161	367	μA	6
I <sub>DD_VLPR</sub>	Very-low-power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks disabled, code of while(1) loop executing from flash <ul style="list-style-type: none"> <li>at 3.0 V</li> </ul>	—	185	372	μA	6
I <sub>DD_VLPR</sub>	Very-low-power run mode current - 4 MHz core / 0.8 MHz bus and flash, all peripheral clocks enabled, code of while(1) loop executing from flash <ul style="list-style-type: none"> <li>at 3.0 V</li> </ul>	—	256	420	μA	4, 6
I <sub>DD_VLPW</sub>	Very-low-power wait mode current - core disabled / 4 MHz system / 0.8 MHz bus / flash disabled (flash doze enabled), all peripheral clocks disabled <ul style="list-style-type: none"> <li>at 3.0 V</li> </ul>	—	110	355	μA	6

Table continues on the next page...

**Table 10. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DD_STOP</sub>	Stop mode current at 3.0 V					
	at 25 °C	—	301	428	μA	
	at 50 °C	—	311	722		
	at 70 °C	—	342	758		
	at 85 °C	—	382	809		
at 105 °C	—	481	929			
I <sub>DD_VLPS</sub>	Very-low-power stop mode current at 3.0 V					
	at 25 °C	—	2.3	8.4	μA	
	at 50 °C	—	5.2	18.3		
	at 70 °C	—	10.5	26.1		
	at 85 °C	—	19.3	58.5		
at 105 °C	—	42.3	105.1			
I <sub>DD_LLS</sub>	Low-leakage stop mode current at 3.0 V					
	at 25 °C	—	1.7	3.3	μA	
	at 50 °C	—	3.2	34.9		
	at 70 °C	—	5.8	38.5		
	at 85 °C	—	11.6	43.8		
at 105 °C	—	26.8	61.7			
I <sub>DD_VLLS3</sub>	Very-low-leakage stop mode 3 current at 3.0 V					
	at 25 °C	—	1.3	3.0	μA	
	at 50 °C	—	2.3	17.6		
	at 70 °C	—	4.7	19.5		
	at 85 °C	—	8.5	24.1		
at 105 °C	—	19.5	35.3			
I <sub>DD_VLLS1</sub>	Very-low-leakage stop mode 1 current at 3.0V					
	at 25°C	—	0.7	1.3	μA	
	at 50°C	—	1.2	11.7		
	at 70°C	—	2.2	12.6		
	at 85°C	—	4.8	15.3		
at 105°C	—	12.4	22.6			
I <sub>DD_VLLS0</sub>	Very-low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 0) at 3.0 V					
	at 25 °C	—	310	844	nA	
	at 50 °C	—	778	3861		
	at 70 °C	—	1928	13055		
	at 85 °C	—	3906	15457		
at 105 °C	—	10097	23116			

Table continues on the next page...

**Table 10. Power consumption operating behaviors (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I <sub>DD_VLLS0</sub>	Very-low-leakage stop mode 0 current (SMC_STOPCTRL[PORPO] = 1) at 3.0 V					7
	at 25 °C	—	139	747	nA	
	at 50 °C	—	600	3418		
	at 70 °C	—	1674	11143		
	at 85 °C	—	3554	13683		
	at 105 °C	—	9580	20463		

1. The analog supply current is the sum of the active or disabled current for each of the analog modules on the device. See each module's specification for its supply current.
2. MCG configured for PEE mode. CoreMark benchmark compiled using IAR 6.40 with optimization level high, optimized for balanced.
3. MCG configured for FEI mode.
4. Incremental current consumption from peripheral activity is not included.
5. MCG configured for BLPI mode. CoreMark benchmark compiled using IAR 6.40 with optimization level high, optimized for balanced.
6. MCG configured for BLPI mode.
7. No brownout

**Table 11. Low power mode peripheral adders — typical value**

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
I <sub>IREFSTEN4MHZ</sub>	4 MHz internal reference clock (IRC) adder. Measured by entering STOP or VLPS mode with 4 MHz IRC enabled.	56	56	56	56	56	56	μA
I <sub>IREFSTEN32KHZ</sub>	32 kHz internal reference clock (IRC) adder. Measured by entering STOP mode with the 32 kHz IRC enabled.	52	52	52	52	52	52	μA
I <sub>EREFSTEN4MHZ</sub>	External 4 MHz crystal clock adder. Measured by entering STOP or VLPS mode with the crystal enabled.	250	262	266	268	272	274	uA
I <sub>EREFSTEN32KHZ</sub>	External 32 kHz crystal clock adder by means of the OSC0_CR[EREFSTEN and EREFSTEN] bits. Measured by entering all modes with the crystal enabled.	440	490	540	560	570	580	nA
	VLLS1	440	490	540	560	570	580	
	VLLS3	490	490	540	560	570	680	
	LLS	510	560	560	560	610	680	
	VLPS	510	560	560	560	610	680	
	STOP	510	560	560	560	610	680	
I <sub>CMP</sub>	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	μA

Table continues on the next page...



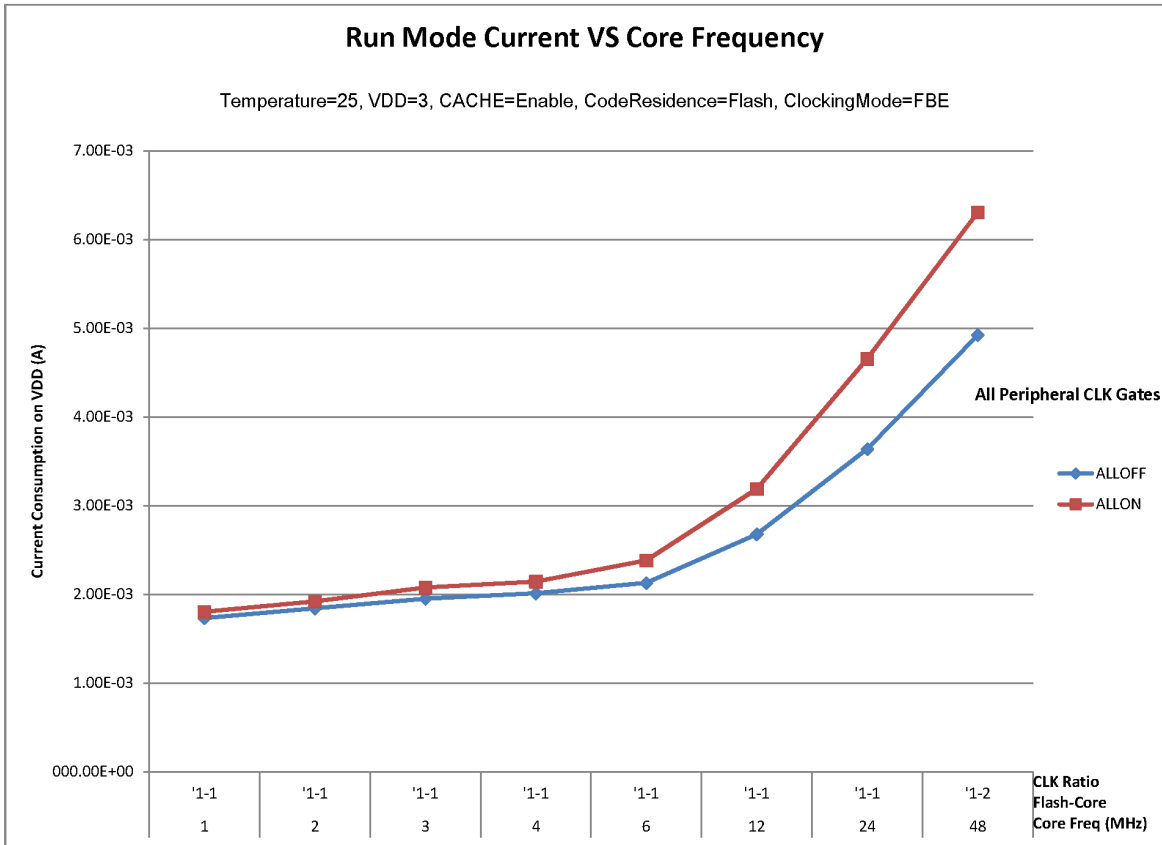
**Table 11. Low power mode peripheral adders — typical value (continued)**

Symbol	Description	Temperature (°C)						Unit
		-40	25	50	70	85	105	
$I_{RTC}$	RTC peripheral adder measured by placing the device in VLLS1 mode with external 32 kHz crystal enabled by means of the RTC_CR[OSCE] bit and the RTC ALARM set for 1 minute. Includes ERCLK32K (32 kHz external crystal) power consumption.	432	357	388	475	532	810	nA
$I_{UART}$	UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption.							
	MCGIRCLK (4 MHz internal reference clock)	66	66	66	66	66	66	$\mu$ A
	OSCERCLK (4 MHz external crystal)	259	271	275	277	281	283	
$I_{TPM}$	TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents.							
	MCGIRCLK (4 MHz internal reference clock)	86	86	86	86	86	86	$\mu$ A
	OSCERCLK (4 MHz external crystal)	275	288	290	295	300	306	
$I_{BG}$	Bandgap adder when BGEN bit is set and device is placed in VLPx, LLS, or VLLSx mode.	45	45	45	45	45	45	$\mu$ A
$I_{ADC}$	ADC peripheral adder combining the measured values at $V_{DD}$ and $V_{DDA}$ by placing the device in STOP or VLPS mode. ADC is configured for low-power mode using the internal clock and continuous conversions.	366	366	366	366	366	366	$\mu$ A

### 5.2.5.1 Diagram: Typical $I_{DD\_RUN}$ operating behavior

The following data was measured under these conditions:

- MCG in FBE for run mode, and BLPE for VLPR mode
- No GPIOs toggled
- Code execution from flash with cache enabled
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA



**Figure 2. Run mode supply current vs. core frequency**

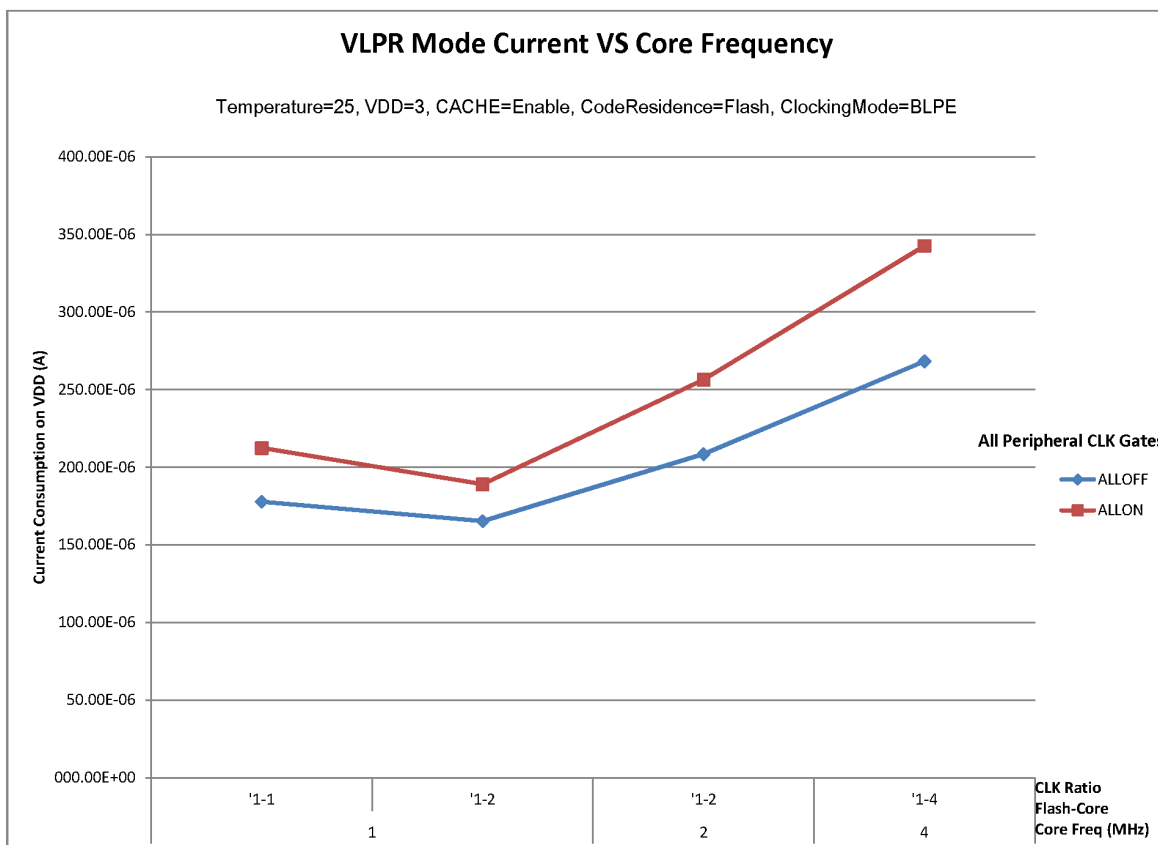


Figure 3. VLPR mode current vs. core frequency

### 5.2.6 EMC radiated emissions operating behaviors

Table 12. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V <sub>RE1</sub>	Radiated emissions voltage, band 1	0.15–50	16	dBμV	1, 2
V <sub>RE2</sub>	Radiated emissions voltage, band 2	50–150	18	dBμV	
V <sub>RE3</sub>	Radiated emissions voltage, band 3	150–500	11	dBμV	
V <sub>RE4</sub>	Radiated emissions voltage, band 4	500–1000	13	dBμV	
V <sub>RE_IEC</sub>	IEC level	0.15–1000	M	—	2, 3

1. Determined according to IEC Standard 61967-1, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 1: General Conditions and Definitions* and IEC Standard 61967-2, *Integrated Circuits - Measurement of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*. Measurements were made while the microcontroller was running basic application code. The reported

## General

emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

2.  $V_{DD} = 3.3\text{ V}$ ,  $T_A = 25\text{ }^\circ\text{C}$ ,  $f_{OSC} = 8\text{ MHz}$  (crystal),  $f_{SYS} = 48\text{ MHz}$ ,  $f_{BUS} = 24\text{ MHz}$
3. Specified according to Annex D of IEC Standard 61967-2, *Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method*

## 5.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to [www.freescale.com](http://www.freescale.com).
2. Perform a keyword search for “EMC design.”

## 5.2.8 Capacitance attributes

Table 13. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
$C_{IN}$	Input capacitance	—	7	pF

## 5.3 Switching specifications

### 5.3.1 Device clock specifications

Table 14. Device clock specifications

Symbol	Description	Min.	Max.	Unit
Normal run mode				
$f_{SYS}$	System and core clock	—	48	MHz
$f_{BUS}$	Bus clock	—	24	MHz
$f_{FLASH}$	Flash clock	—	24	MHz
$f_{LPTMR}$	LPTMR clock	—	24	MHz
VLPR and VLPS modes <sup>1</sup>				
$f_{SYS}$	System and core clock	—	4	MHz
$f_{BUS}$	Bus clock	—	1	MHz
$f_{FLASH}$	Flash clock	—	1	MHz
$f_{LPTMR}$	LPTMR clock <sup>2</sup>	—	24	MHz
$f_{ERCLK}$	External reference clock	—	16	MHz
$f_{LPTMR\_ERCLK}$	LPTMR external reference clock	—	16	MHz

Table continues on the next page...

**Table 14. Device clock specifications (continued)**

Symbol	Description	Min.	Max.	Unit
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	—	16	MHz
$f_{TPM}$	TPM asynchronous clock	—	8	MHz
$f_{UART0}$	UART0 asynchronous clock	—	8	MHz

1. The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.
2. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

### 5.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

**Table 15. General switching specifications**

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2
GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
Port rise and fall time	—	36	ns	3

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. 75 pF load

## 5.4 Thermal specifications

### 5.4.1 Thermal operating requirements

**Table 16. Thermal operating requirements**

Symbol	Description	Min.	Max.	Unit
$T_J$	Die junction temperature	-40	125	°C
$T_A$	Ambient temperature	-40	105	°C

## 5.4.2 Thermal attributes

**Table 17. Thermal attributes**

Board type	Symbol	Description	64 LQFP	48 QFN	32 QFN	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	71	83	98	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	53	30	34	°C/W	
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	59	68	82	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	46	24	28	°C/W	
—	$R_{\theta JB}$	Thermal resistance, junction to board	35	12	13	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	21	2.3	2.3	°C/W	3
—	$\Psi_{JT}$	Thermal characterization parameter, junction to package top outside center (natural convection)	6	5	8	°C/W	4

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions – Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions – Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions – Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.
4. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions – Natural Convection (Still Air)*.

## 6 Peripheral operating requirements and behaviors

### 6.1 Core modules

#### 6.1.1 SWD electricals

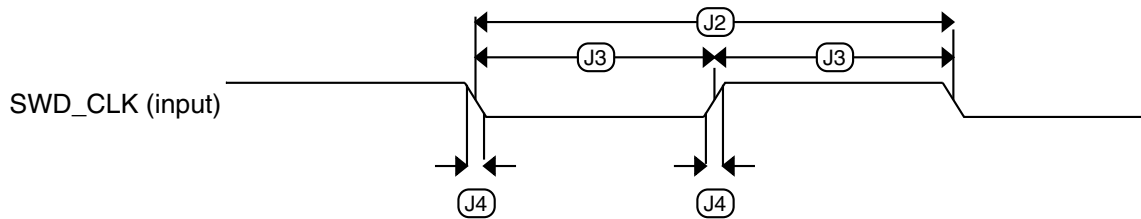
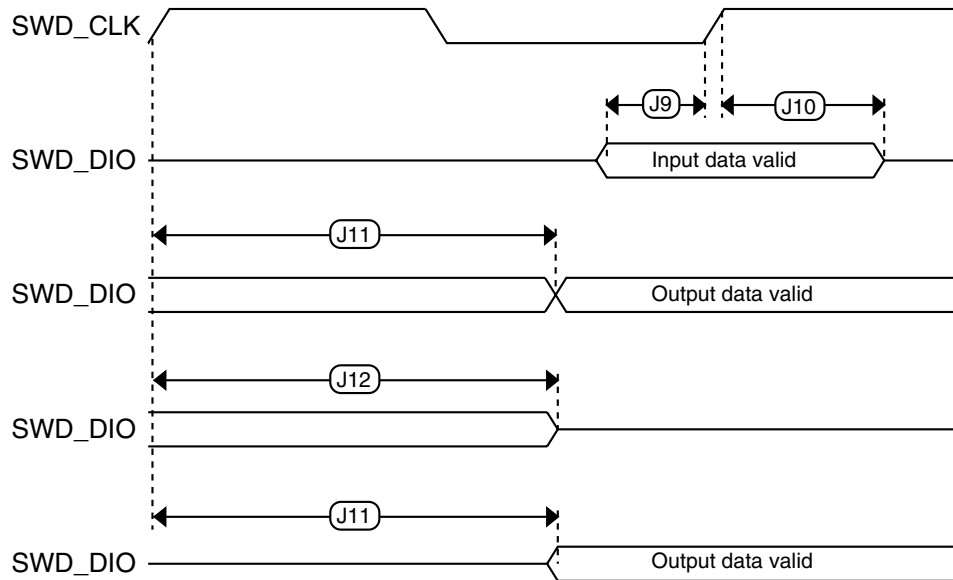
**Table 18. SWD full voltage range electricals**

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation <ul style="list-style-type: none"> <li>• Serial wire debug</li> </ul>	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns

Table continues on the next page...

**Table 18. SWD full voltage range electricals (continued)**

Symbol	Description	Min.	Max.	Unit
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

**Figure 4. Serial wire clock input timing****Figure 5. Serial wire data timing**

## 6.2 System modules

There are no specifications necessary for the device's system modules.

## 6.3 Clock modules

### 6.3.1 MCG specifications

Table 19. MCG specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes	
$f_{ints\_ft}$	Internal reference frequency (slow clock) — factory trimmed at nominal $V_{DD}$ and 25 °C	—	32.768	—	kHz		
$f_{ints\_t}$	Internal reference frequency (slow clock) — user trimmed	31.25	—	39.0625	kHz		
$\Delta f_{dco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using C3[SCTTRIM] and C4[SCFTRIM]	—	± 0.3	± 0.6	% $f_{dco}$	1	
$\Delta f_{dco\_t}$	Total deviation of trimmed average DCO output frequency over voltage and temperature	—	+0.5/-0.7	± 3	% $f_{dco}$	1, 2	
$\Delta f_{dco\_t}$	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70 °C	—	± 0.4	± 1.5	% $f_{dco}$	1, 2	
$f_{intf\_ft}$	Internal reference frequency (fast clock) — factory trimmed at nominal $V_{DD}$ and 25 °C	—	4	—	MHz		
$\Delta f_{intf\_ft}$	Frequency deviation of internal reference clock (fast clock) over temperature and voltage — factory trimmed at nominal $V_{DD}$ and 25 °C	—	+1/-2	± 3	% $f_{intf\_ft}$	2	
$f_{intf\_t}$	Internal reference frequency (fast clock) — user trimmed at nominal $V_{DD}$ and 25 °C	3	—	5	MHz		
$f_{loc\_low}$	Loss of external clock minimum frequency — RANGE = 00	$(3/5) \times f_{ints\_t}$	—	—	kHz		
$f_{loc\_high}$	Loss of external clock minimum frequency — RANGE = 01, 10, or 11	$(16/5) \times f_{ints\_t}$	—	—	kHz		
FLL							
$f_{fill\_ref}$	FLL reference frequency range	31.25	—	39.0625	kHz		
$f_{dco}$	DCO output frequency range	Low range (DRS = 00) $640 \times f_{fill\_ref}$	20	20.97	25	MHz	3, 4
		Mid range (DRS = 01) $1280 \times f_{fill\_ref}$	40	41.94	48	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low range (DRS = 00) $732 \times f_{fill\_ref}$	—	23.99	—	MHz	5, 6
		Mid range (DRS = 01) $1464 \times f_{fill\_ref}$	—	47.97	—	MHz	

Table continues on the next page...



**Table 19. MCG specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$J_{cyc\_fll}$	FLL period jitter <ul style="list-style-type: none"> <li><math>f_{VCO} = 48</math> MHz</li> </ul>	—	180	—	ps	7
$t_{fill\_acquire}$	FLL target frequency acquisition time	—	—	1	ms	8
PLL						
$f_{vco}$	VCO operating frequency	48.0	—	100	MHz	
$I_{pll}$	PLL operating current <ul style="list-style-type: none"> <li>PLL at 96 MHz (<math>f_{osc\_hi\_1} = 8</math> MHz, <math>f_{pll\_ref} = 2</math> MHz, VDIV multiplier = 48)</li> </ul>	—	1060	—	$\mu$ A	9
$I_{pll}$	PLL operating current <ul style="list-style-type: none"> <li>PLL at 48 MHz (<math>f_{osc\_hi\_1} = 8</math> MHz, <math>f_{pll\_ref} = 2</math> MHz, VDIV multiplier = 24)</li> </ul>	—	600	—	$\mu$ A	9
$f_{pll\_ref}$	PLL reference frequency range	2.0	—	4.0	MHz	
$J_{cyc\_pll}$	PLL period jitter (RMS) <ul style="list-style-type: none"> <li><math>f_{vco} = 48</math> MHz</li> <li><math>f_{vco} = 100</math> MHz</li> </ul>	—	120	—	ps	10
$J_{acc\_pll}$	PLL accumulated jitter over 1 $\mu$ s (RMS) <ul style="list-style-type: none"> <li><math>f_{vco} = 48</math> MHz</li> <li><math>f_{vco} = 100</math> MHz</li> </ul>	—	1350	—	ps	10
$D_{lock}$	Lock entry frequency tolerance	$\pm 1.49$	—	$\pm 2.98$	%	
$D_{unl}$	Lock exit frequency tolerance	$\pm 4.47$	—	$\pm 5.97$	%	
$t_{pll\_lock}$	Lock detector detection time	—	—	$150 \times 10^{-6} + 1075(1/f_{pll\_ref})$	s	11

- This parameter is measured with the internal reference (slow clock) being used as a reference to the FLL (FEI clock mode).
- The deviation is relative to the factory trimmed frequency at nominal  $V_{DD}$  and 25 °C,  $f_{ints\_ft}$ .
- These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 0.
- The resulting system clock frequencies must not exceed their maximum specified values. The DCO frequency deviation ( $\Delta f_{dco\_t}$ ) over voltage and temperature must be considered.
- These typical values listed are with the slow internal reference clock (FEI) using factory trim and DMX32 = 1.
- The resulting clock frequency must not exceed the maximum specified clock frequency of the device.
- This specification is based on standard deviation (RMS) of period or frequency.
- This specification applies to any time the FLL reference source or reference divider is changed, trim value is changed, DMX32 bit is changed, DRS bits are changed, or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
- Excludes any oscillator currents that are also consuming power while PLL is in operation.
- This specification was obtained using a Freescale developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary.
- This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

## 6.3.2 Oscillator electrical specifications

### 6.3.2.1 Oscillator DC electrical specifications

**Table 20. Oscillator DC electrical specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{DD}$	Supply voltage	1.71	—	3.6	V	
$I_{DDOSC}$	Supply current — low-power mode (HGO=0) <ul style="list-style-type: none"> <li>• 32 kHz</li> <li>• 4 MHz</li> <li>• 8 MHz (RANGE=01)</li> <li>• 16 MHz</li> <li>• 24 MHz</li> <li>• 32 MHz</li> </ul>	—	500	—	nA	1
		—	200	—	$\mu$ A	
		—	300	—	$\mu$ A	
		—	950	—	$\mu$ A	
		—	1.2	—	mA	
		—	1.5	—	mA	
$I_{DDOSC}$	Supply current — high gain mode (HGO=1) <ul style="list-style-type: none"> <li>• 32 kHz</li> <li>• 4 MHz</li> <li>• 8 MHz (RANGE=01)</li> <li>• 16 MHz</li> <li>• 24 MHz</li> <li>• 32 MHz</li> </ul>	—	25	—	$\mu$ A	1
		—	400	—	$\mu$ A	
		—	500	—	$\mu$ A	
		—	2.5	—	mA	
		—	3	—	mA	
		—	4	—	mA	
$C_x$	EXTAL load capacitance	—	—	—		2, 3
$C_y$	XTAL load capacitance	—	—	—		2, 3
$R_F$	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	M $\Omega$	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	M $\Omega$	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	M $\Omega$	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	M $\Omega$	
$R_S$	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	k $\Omega$	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	k $\Omega$	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	k $\Omega$	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	k $\Omega$	

Table continues on the next page...

**Table 20. Oscillator DC electrical specifications (continued)**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$V_{pp}^5$	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	$V_{DD}$	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	$V_{DD}$	—	V	

1.  $V_{DD}=3.3$  V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3.  $C_x, C_y$  can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
4. When low power mode is selected,  $R_F$  is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

### 6.3.2.2 Oscillator frequency specifications

**Table 21. Oscillator frequency specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$f_{osc\_lo}$	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
$f_{ec\_extal}$	Input clock frequency (external clock mode)	—	—	48	MHz	1, 2
$t_{dc\_extal}$	Input clock duty cycle (external clock mode)	40	50	60	%	
$t_{cst}$	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL or PLL.
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.

## Peripheral operating requirements and behaviors

3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG\_S register being set.

## 6.4 Memories and memory interfaces

### 6.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

#### 6.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

**Table 22. NVM program/erase timing specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{hvpgm4}$	Longword Program high-voltage time	—	7.5	18	$\mu$ s	
$t_{hversscr}$	Sector Erase high-voltage time	—	13	113	ms	1
$t_{hversall}$	Erase All high-voltage time	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

#### 6.4.1.2 Flash timing specifications — commands

**Table 23. Flash command timing specifications**

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{rd1sec1k}$	Read 1s Section execution time (flash sector)	—	—	60	$\mu$ s	1
$t_{pgmchk}$	Program Check execution time	—	—	45	$\mu$ s	1
$t_{rdsrc}$	Read Resource execution time	—	—	30	$\mu$ s	1
$t_{pgm4}$	Program Longword execution time	—	65	145	$\mu$ s	
$t_{ersscr}$	Erase Flash Sector execution time	—	14	114	ms	2
$t_{rd1all}$	Read 1s All Blocks execution time	—	—	1.8	ms	
$t_{rdonce}$	Read Once execution time	—	—	25	$\mu$ s	1
$t_{pgmonce}$	Program Once execution time	—	65	—	$\mu$ s	
$t_{ersall}$	Erase All Blocks execution time	—	88	650	ms	2
$t_{vfykey}$	Verify Backdoor Access Key execution time	—	—	30	$\mu$ s	1

1. Assumes 25 MHz flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

### 6.4.1.3 Flash high voltage current behaviors

Table 24. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I <sub>DD_PGM</sub>	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I <sub>DD_ERS</sub>	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

### 6.4.1.4 Reliability specifications

Table 25. NVM reliability specifications

Symbol	Description	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
Program Flash						
t <sub>nvmretp10k</sub>	Data retention after up to 10 K cycles	5	50	—	years	
t <sub>nvmretp1k</sub>	Data retention after up to 1 K cycles	20	100	—	years	
n <sub>nvmcycp</sub>	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40 °C ≤ T<sub>j</sub> ≤ 125 °C.

## 6.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

## 6.6 Analog

### 6.6.1 ADC electrical specifications

The 16-bit accuracy specifications listed in [Table 26](#) and [Table 27](#) are achievable on the differential pins ADCx\_DP0, ADCx\_DM0.

All other ADC channels meet the 13-bit differential/12-bit single-ended accuracy specifications.

## 6.6.1.1 16-bit ADC operating conditions

Table 26. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ. <sup>1</sup>	Max.	Unit	Notes
$V_{DDA}$	Supply voltage	Absolute	1.71	—	3.6	V	
$\Delta V_{DDA}$	Supply voltage	Delta to $V_{DD}$ ( $V_{DD} - V_{DDA}$ )	-100	0	+100	mV	2
$\Delta V_{SSA}$	Ground voltage	Delta to $V_{SS}$ ( $V_{SS} - V_{SSA}$ )	-100	0	+100	mV	2
$V_{REFH}$	ADC reference voltage high		1.13	$V_{DDA}$	$V_{DDA}$	V	3
$V_{REFL}$	ADC reference voltage low		$V_{SSA}$	$V_{SSA}$	$V_{SSA}$	V	3
$V_{ADIN}$	Input voltage	<ul style="list-style-type: none"> <li>16-bit differential mode</li> <li>All other modes</li> </ul>	VREFL	—	31/32 * VREFH	V	
$C_{ADIN}$	Input capacitance	<ul style="list-style-type: none"> <li>16-bit mode</li> <li>8-bit / 10-bit / 12-bit modes</li> </ul>	—	8	10	pF	
$R_{ADIN}$	Input resistance		—	2	5	k $\Omega$	
$R_{AS}$	Analog source resistance	13-bit / 12-bit modes $f_{ADCK} < 4$ MHz	—	—	5	k $\Omega$	4
$f_{ADCK}$	ADC conversion clock frequency	$\leq$ 13-bit mode	1.0	—	18.0	MHz	5
$f_{ADCK}$	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	5
$C_{rate}$	ADC conversion rate	$\leq$ 13-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	Ksps	6
$C_{rate}$	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	Ksps	6

1. Typical values assume  $V_{DDA} = 3.0$  V, Temp = 25 °C,  $f_{ADCK} = 1.0$  MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. For packages without dedicated VREFH and VREFL pins,  $V_{REFH}$  is internally tied to  $V_{DDA}$ , and  $V_{REFL}$  is internally tied to  $V_{SSA}$ .
4. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had  $< 8 \Omega$  analog source resistance. The  $R_{AS}/C_{AS}$  time constant should be kept to  $< 1$  ns.
5. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
6. For guidelines and examples of conversion rate calculation, download the [ADC calculator tool](#).

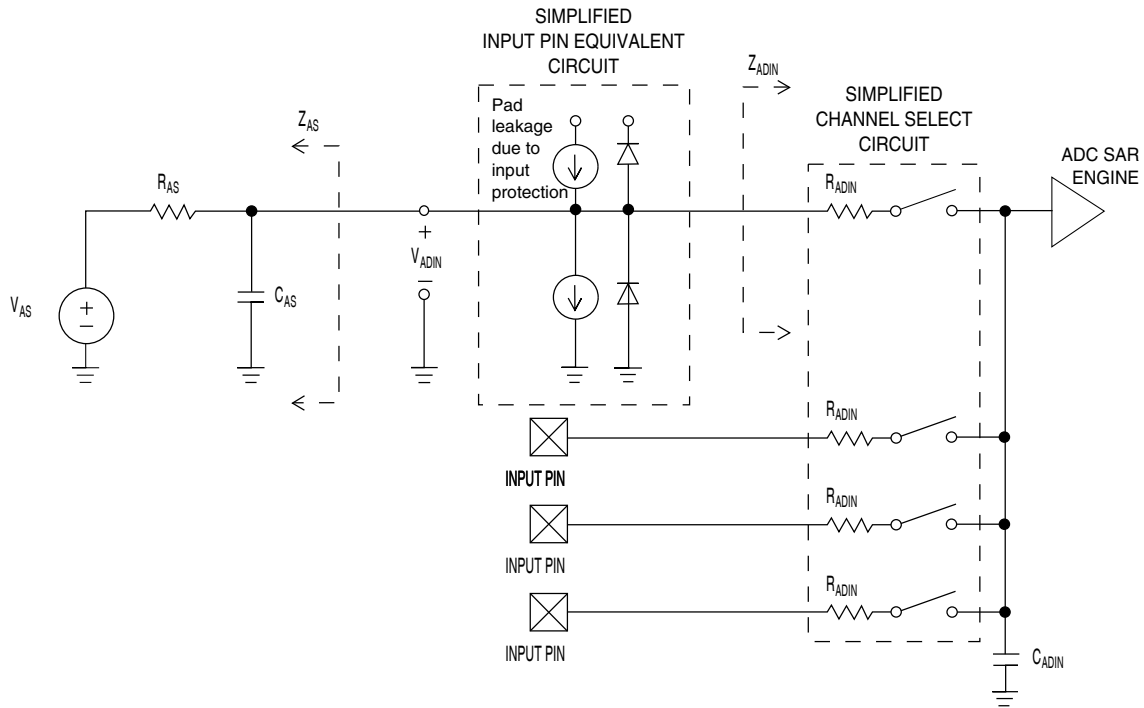


Figure 6. ADC input impedance equivalency diagram

### 6.6.1.2 16-bit ADC electrical characteristics

Table 27. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ )

Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
$I_{DDA\_ADC}$	Supply current		0.215	—	1.7	mA	3
$f_{ADACK}$	ADC asynchronous clock source	<ul style="list-style-type: none"> <li>ADLPC = 1, ADHSC = 0</li> <li>ADLPC = 1, ADHSC = 1</li> <li>ADLPC = 0, ADHSC = 0</li> <li>ADLPC = 0, ADHSC = 1</li> </ul>	1.2	2.4	3.9	MHz	$t_{ADACK} = 1/f_{ADACK}$
			2.4	4.0	6.1	MHz	
			3.0	5.2	7.3	MHz	
			4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	<ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>	—	±4	±6.8	LSB <sup>4</sup>	5
DNL	Differential non-linearity	12-bit modes	—	±0.7	-1.1 to +1.9	LSB <sup>4</sup>	5
		<12-bit modes	—	±0.2	-0.3 to 0.5		
INL	Integral non-linearity	12-bit modes	—	±1.0	-2.7 to +1.9	LSB <sup>4</sup>	5
		<12-bit modes	—	±0.5	-0.7 to +0.5		

Table continues on the next page...

**Table 27. 16-bit ADC characteristics ( $V_{REFH} = V_{DDA}$ ,  $V_{REFL} = V_{SSA}$ ) (continued)**

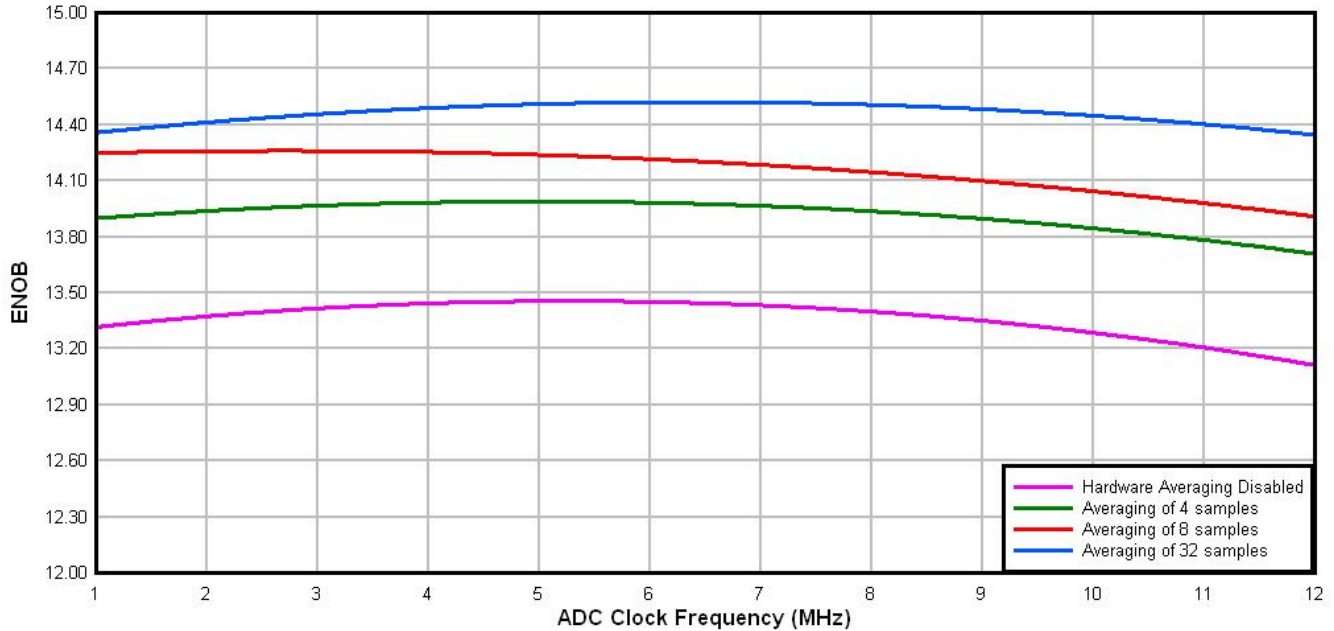
Symbol	Description	Conditions <sup>1</sup>	Min.	Typ. <sup>2</sup>	Max.	Unit	Notes
$E_{FS}$	Full-scale error	<ul style="list-style-type: none"> <li>12-bit modes</li> <li>&lt;12-bit modes</li> </ul>	—	-4	-5.4	LSB <sup>4</sup>	$V_{ADIN} = V_{DDA}$ <sup>5</sup>
$E_Q$	Quantization error	<ul style="list-style-type: none"> <li>16-bit modes</li> <li>≤13-bit modes</li> </ul>	—	-1 to 0	—	LSB <sup>4</sup>	
ENOB	Effective number of bits	16-bit differential mode					6
		<ul style="list-style-type: none"> <li>Avg = 32</li> </ul>	12.8	14.5	—	bits	
		<ul style="list-style-type: none"> <li>Avg = 4</li> </ul>	11.9	13.8	—	bits	
		16-bit single-ended mode					
<ul style="list-style-type: none"> <li>Avg = 32</li> </ul>	12.2	13.9	—	bits			
<ul style="list-style-type: none"> <li>Avg = 4</li> </ul>	11.4	13.1	—	bits			
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit differential mode					7
		<ul style="list-style-type: none"> <li>Avg = 32</li> </ul>	—	-94	—	dB	
		16-bit single-ended mode					
		<ul style="list-style-type: none"> <li>Avg = 32</li> </ul>	—	-85	—	dB	
SFDR	Spurious free dynamic range	16-bit differential mode					7
		<ul style="list-style-type: none"> <li>Avg = 32</li> </ul>	82	95	—	dB	
		16-bit single-ended mode					
		<ul style="list-style-type: none"> <li>Avg = 32</li> </ul>	78	90	—	dB	
$E_{IL}$	Input leakage error		$I_{in} \times R_{AS}$			mV	$I_{in}$ = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
$V_{TEMP25}$	Temp sensor voltage	25 °C	706	716	726	mV	8

- All accuracy numbers assume the ADC is calibrated with  $V_{REFH} = V_{DDA}$
- Typical values assume  $V_{DDA} = 3.0$  V, Temp = 25 °C,  $f_{ADCK} = 2.0$  MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC\_CFG1[ADLPC] (low power). For lowest power operation, ADC\_CFG1[ADLPC] must be set, the ADC\_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
- 1 LSB =  $(V_{REFH} - V_{REFL})/2^N$



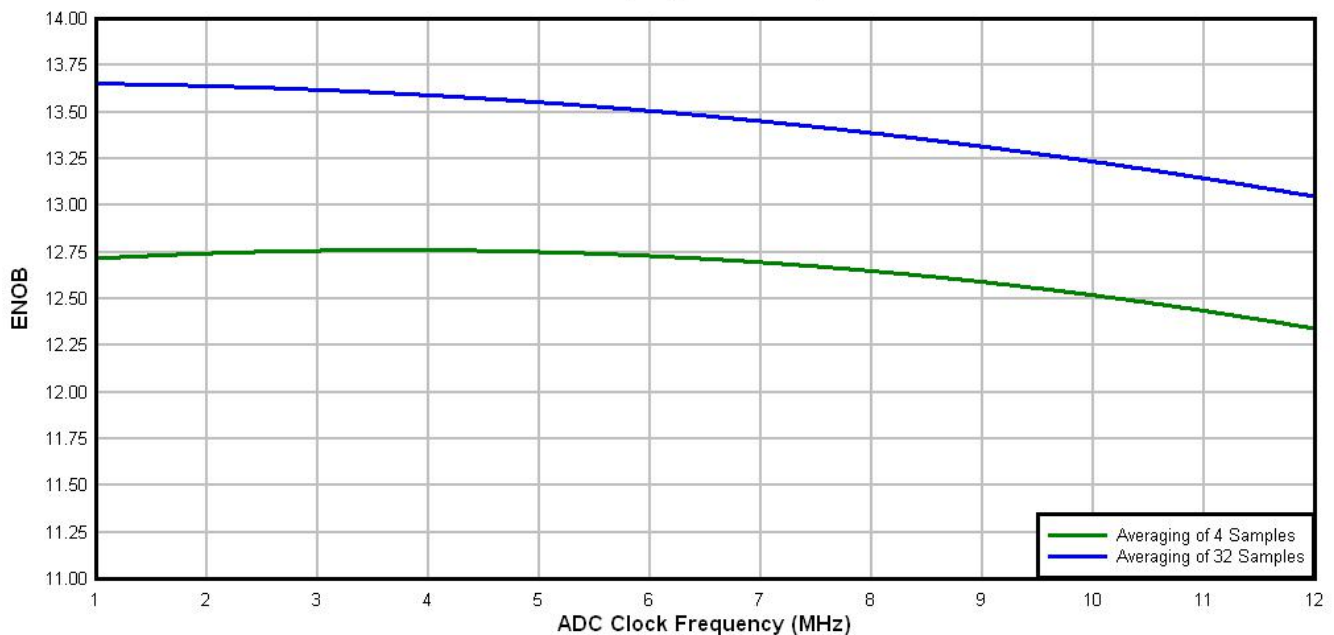
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

**Typical ADC 16-bit Differential ENOB vs ADC Clock**  
**100Hz, 90% FS Sine Input**



**Figure 7. Typical ENOB vs. ADC\_CLK for 16-bit differential mode**

**Typical ADC 16-bit Single-Ended ENOB vs ADC Clock**  
**100Hz, 90% FS Sine Input**



**Figure 8. Typical ENOB vs. ADC\_CLK for 16-bit single-ended mode**

## 6.6.2 CMP and 6-bit DAC electrical specifications

Table 28. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
$V_{DD}$	Supply voltage	1.71	—	3.6	V
$I_{DDHS}$	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	$\mu$ A
$I_{DDL S}$	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	$\mu$ A
$V_{AIN}$	Analog input voltage	$V_{SS} - 0.3$	—	$V_{DD}$	V
$V_{AIO}$	Analog input offset voltage	—	—	20	mV
$V_H$	Analog comparator hysteresis <sup>1</sup> <ul style="list-style-type: none"> <li>• CR0[HYSTCTR] = 00</li> <li>• CR0[HYSTCTR] = 01</li> <li>• CR0[HYSTCTR] = 10</li> <li>• CR0[HYSTCTR] = 11</li> </ul>	—	5 10 20 30	—	mV mV mV mV
$V_{CMPOH}$	Output high	$V_{DD} - 0.5$	—	—	V
$V_{CMPOI}$	Output low	—	—	0.5	V
$t_{DHS}$	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
$t_{DLS}$	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay <sup>2</sup>	—	—	40	$\mu$ s
$I_{DAC6b}$	6-bit DAC current adder (enabled)	—	7	—	$\mu$ A
INL	6-bit DAC integral non-linearity	-0.5	—	0.5	LSB <sup>3</sup>
DNL	6-bit DAC differential non-linearity	-0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to  $V_{DD}-0.6$  V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP\_DACCR[DACEN], CMP\_DACCR[VRSEL], CMP\_DACCR[VOSEL], CMP\_MUXCR[PSEL], and CMP\_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB =  $V_{reference}/64$

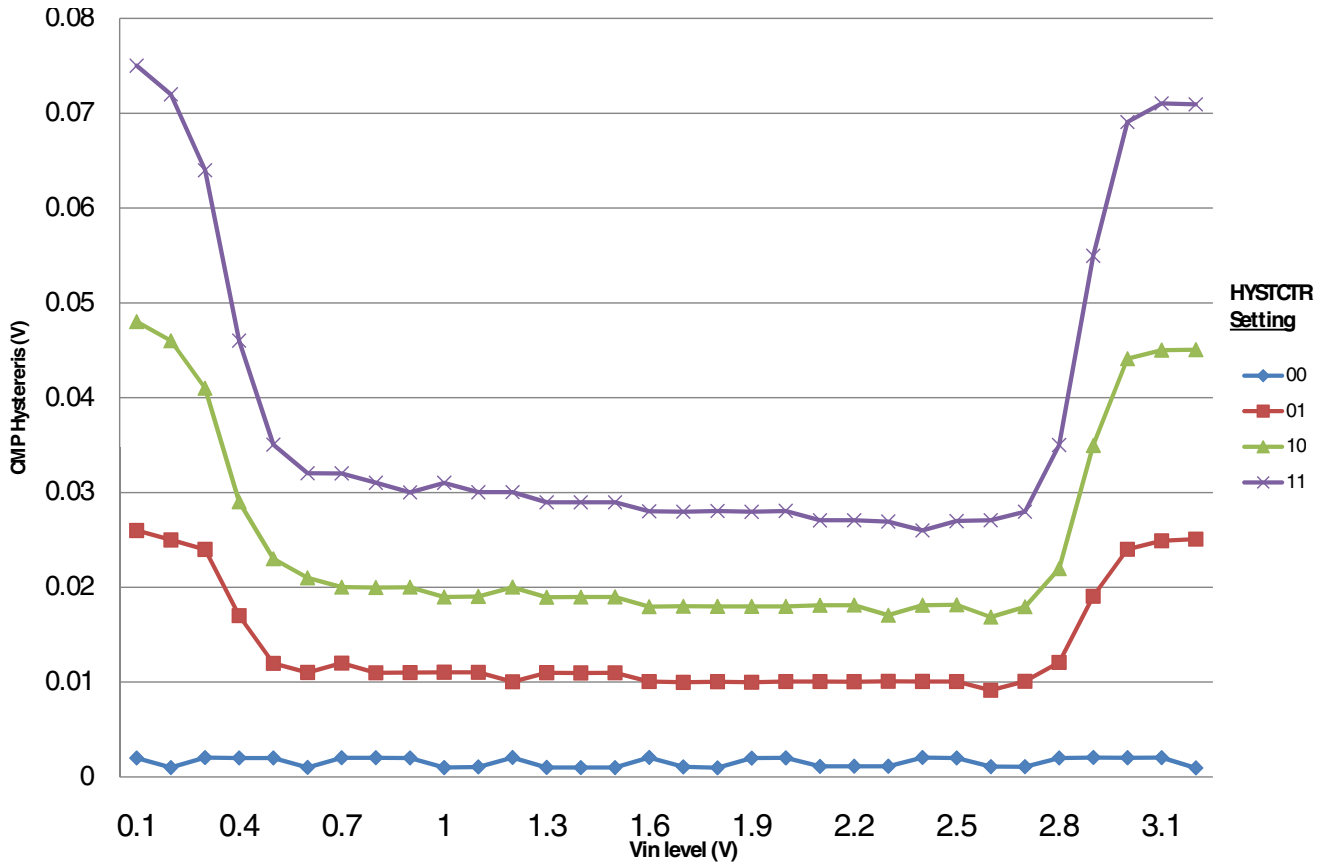


Figure 9. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

## Peripheral operating requirements and behaviors

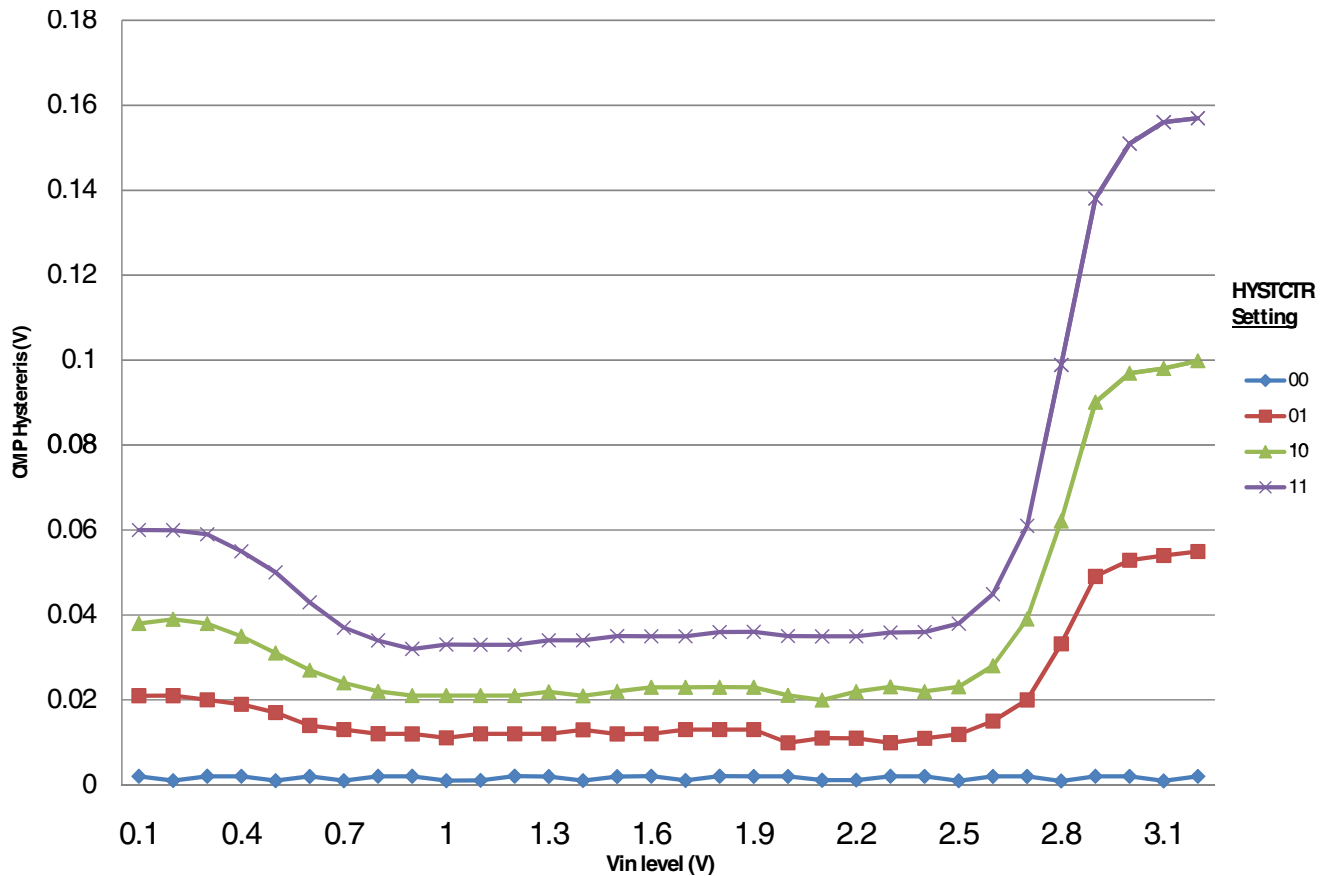


Figure 10. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

## 6.6.3 12-bit DAC electrical characteristics

### 6.6.3.1 12-bit DAC operating requirements

Table 29. 12-bit DAC operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
$V_{DDA}$	Supply voltage	1.71	3.6	V	
$V_{DACR}$	Reference voltage	1.13	3.6	V	1
$C_L$	Output load capacitance	—	100	pF	2
$I_L$	Output load current	—	1	mA	

1. The DAC reference can be selected to be  $V_{DDA}$  or  $V_{REFH}$ .
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC

### 6.6.3.2 12-bit DAC operating behaviors

Table 30. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$I_{DDA\_DACLP}$	Supply current — low-power mode	—	—	250	$\mu\text{A}$	
$I_{DDA\_DACHP}$	Supply current — high-speed mode	—	—	900	$\mu\text{A}$	
$t_{DACLP}$	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	$\mu\text{s}$	1
$t_{DACHP}$	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	$\mu\text{s}$	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	$\mu\text{s}$	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	$V_{DACR} - 100$	—	$V_{DACR}$	mV	
INL	Integral non-linearity error — high speed mode	—	—	$\pm 8$	LSB	2
DNL	Differential non-linearity error — $V_{DACR} > 2\text{ V}$	—	—	$\pm 1$	LSB	3
DNL	Differential non-linearity error — $V_{DACR} = V_{REF\_OUT}$	—	—	$\pm 1$	LSB	4
$V_{OFFSET}$	Offset error	—	$\pm 0.4$		%FSR	5
$E_G$	Gain error	—	$\pm 0.1$		%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \geq 2.4\text{ V}$	60	—	90	dB	
$T_{CO}$	Temperature coefficient offset voltage	—	3.7	—	$\mu\text{V}/\text{C}$	6
$T_{GE}$	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
$R_{op}$	Output resistance (load = 3 k $\Omega$ )	—	—	250	$\Omega$	
SR	Slew rate -80h → F7Fh → 80h <ul style="list-style-type: none"> <li>High power (<math>SP_{HP}</math>)</li> <li>Low power (<math>SP_{LP}</math>)</li> </ul>	1.2 0.05	1.7 0.12	— —	V/ $\mu\text{s}$	
BW	3dB bandwidth <ul style="list-style-type: none"> <li>High power (<math>SP_{HP}</math>)</li> <li>Low power (<math>SP_{LP}</math>)</li> </ul>	550 40	— —	— —	kHz	

- Settling within  $\pm 1$  LSB
- The INL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV
- The DNL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV
- The DNL is measured for 0 + 100 mV to  $V_{DACR} - 100$  mV with  $V_{DDA} > 2.4\text{ V}$
- Calculated by a best fit curve from  $V_{SS} + 100$  mV to  $V_{DACR} - 100$  mV
- $V_{DDA} = 3.0\text{ V}$ , reference select set for  $V_{DDA}$  ( $DACx\_CO:DACRFS = 1$ ), high power mode ( $DACx\_CO:LPEN = 0$ ), DAC set to 0x800, temperature range is across the full range of the device

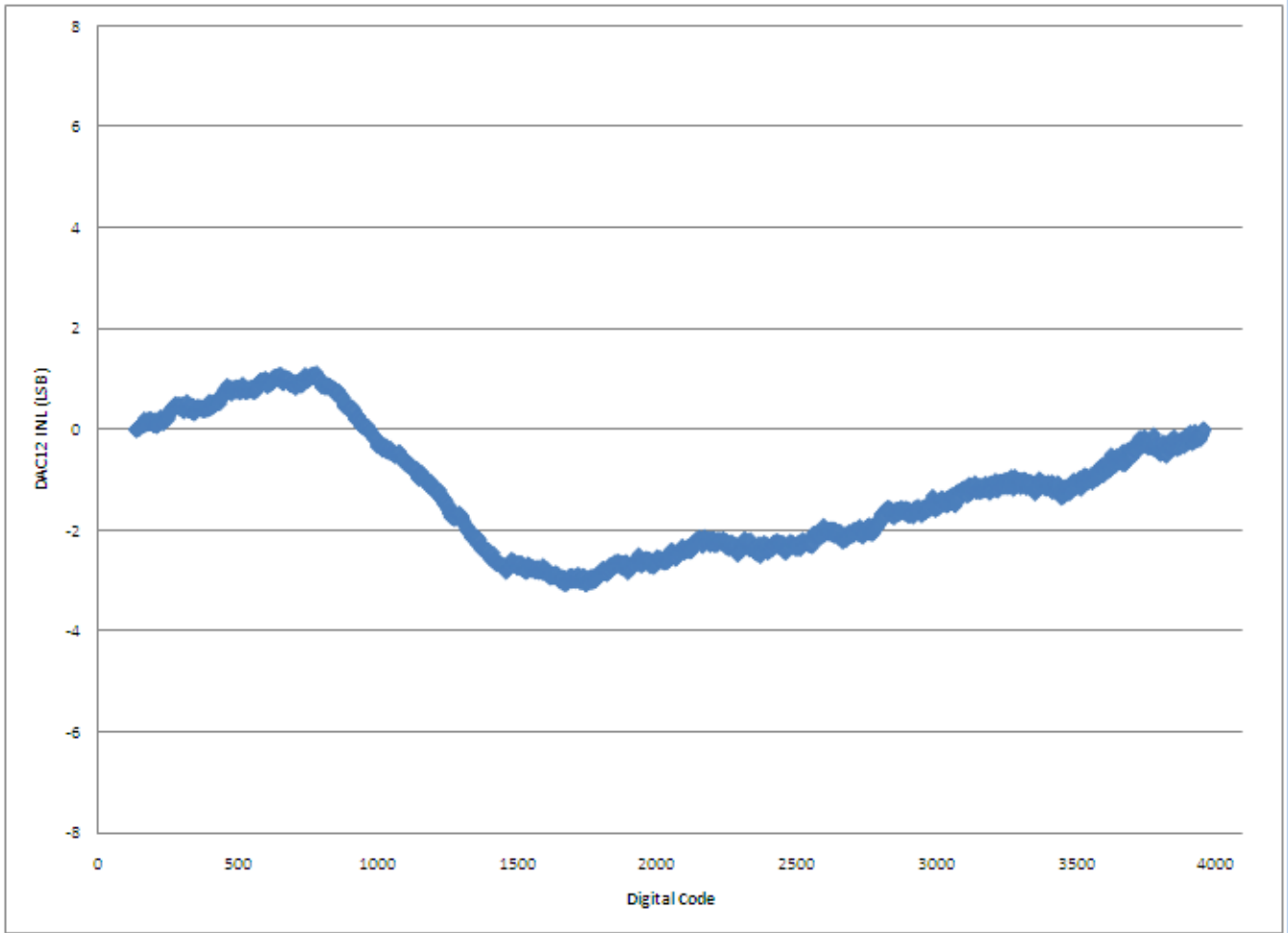


Figure 11. Typical INL error vs. digital code

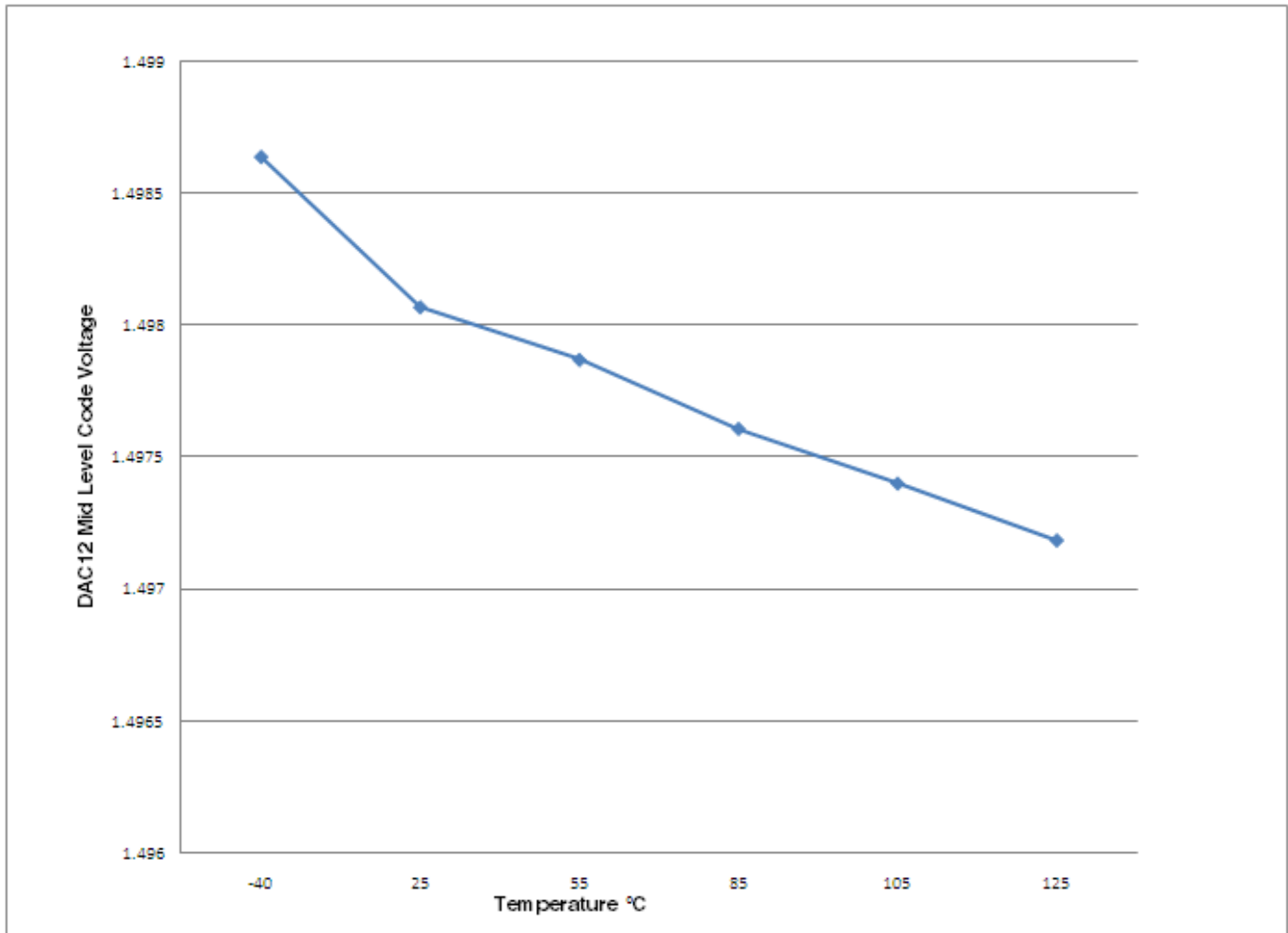


Figure 12. Offset at half scale vs. temperature

## 6.7 Timers

See [General switching specifications](#).

## 6.8 Communication interfaces

### 6.8.1 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

## Peripheral operating requirements and behaviors

All timing is shown with respect to 20%  $V_{DD}$  and 80%  $V_{DD}$  thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

**Table 31. SPI master mode timing on slew rate disabled pads**

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	$f_{op}$	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	$t_{SPSCK}$	SPSCK period	$2 \times t_{periph}$	$2048 \times t_{periph}$	ns	2
3	$t_{Lead}$	Enable lead time	1/2	—	$t_{SPSCK}$	—
4	$t_{Lag}$	Enable lag time	1/2	—	$t_{SPSCK}$	—
5	$t_{WSPSCK}$	Clock (SPSCK) high or low time	$t_{periph} - 30$	$1024 \times t_{periph}$	ns	—
6	$t_{SU}$	Data setup time (inputs)	18	—	ns	—
7	$t_{HI}$	Data hold time (inputs)	0	—	ns	—
8	$t_v$	Data valid (after SPSCK edge)	—	15	ns	—
9	$t_{HO}$	Data hold time (outputs)	0	—	ns	—
10	$t_{RI}$	Rise time input	—	$t_{periph} - 25$	ns	—
	$t_{FI}$	Fall time input				
11	$t_{RO}$	Rise time output	—	25	ns	—
	$t_{FO}$	Fall time output				

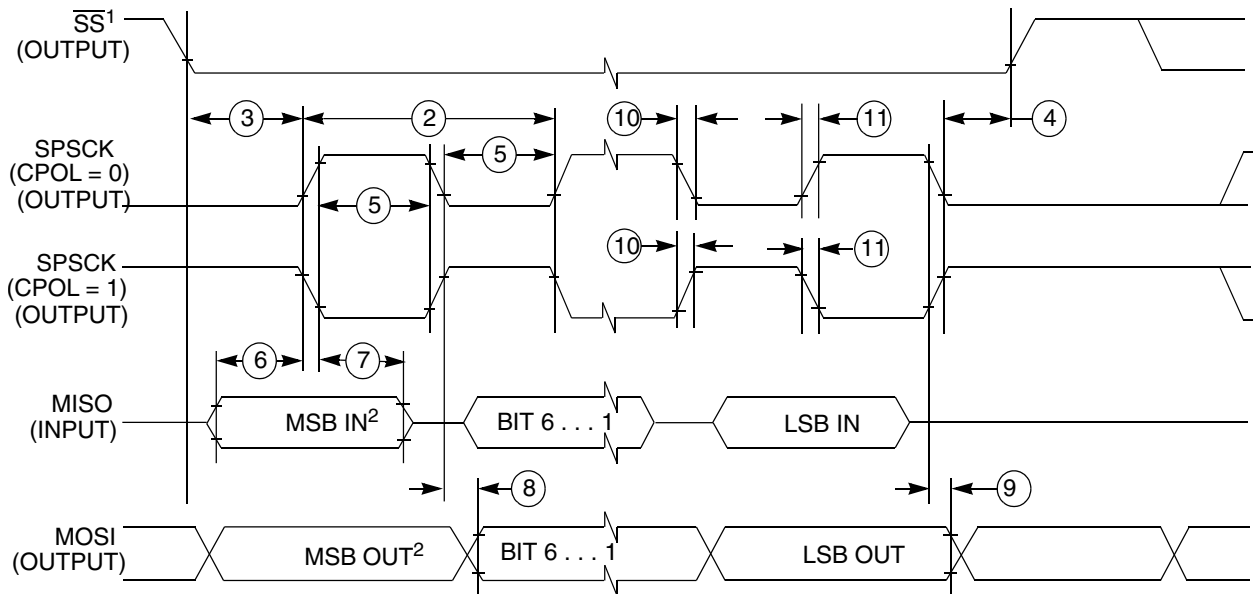
1. For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ). For SPI1  $f_{periph}$  is the system clock ( $f_{SYS}$ ).
2.  $t_{periph} = 1/f_{periph}$

**Table 32. SPI master mode timing on slew rate enabled pads**

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	$f_{op}$	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	$t_{SPSCK}$	SPSCK period	$2 \times t_{periph}$	$2048 \times t_{periph}$	ns	2
3	$t_{Lead}$	Enable lead time	1/2	—	$t_{SPSCK}$	—
4	$t_{Lag}$	Enable lag time	1/2	—	$t_{SPSCK}$	—
5	$t_{WSPSCK}$	Clock (SPSCK) high or low time	$t_{periph} - 30$	$1024 \times t_{periph}$	ns	—
6	$t_{SU}$	Data setup time (inputs)	96	—	ns	—
7	$t_{HI}$	Data hold time (inputs)	0	—	ns	—
8	$t_v$	Data valid (after SPSCK edge)	—	52	ns	—
9	$t_{HO}$	Data hold time (outputs)	0	—	ns	—
10	$t_{RI}$	Rise time input	—	$t_{periph} - 25$	ns	—
	$t_{FI}$	Fall time input				
11	$t_{RO}$	Rise time output	—	36	ns	—
	$t_{FO}$	Fall time output				

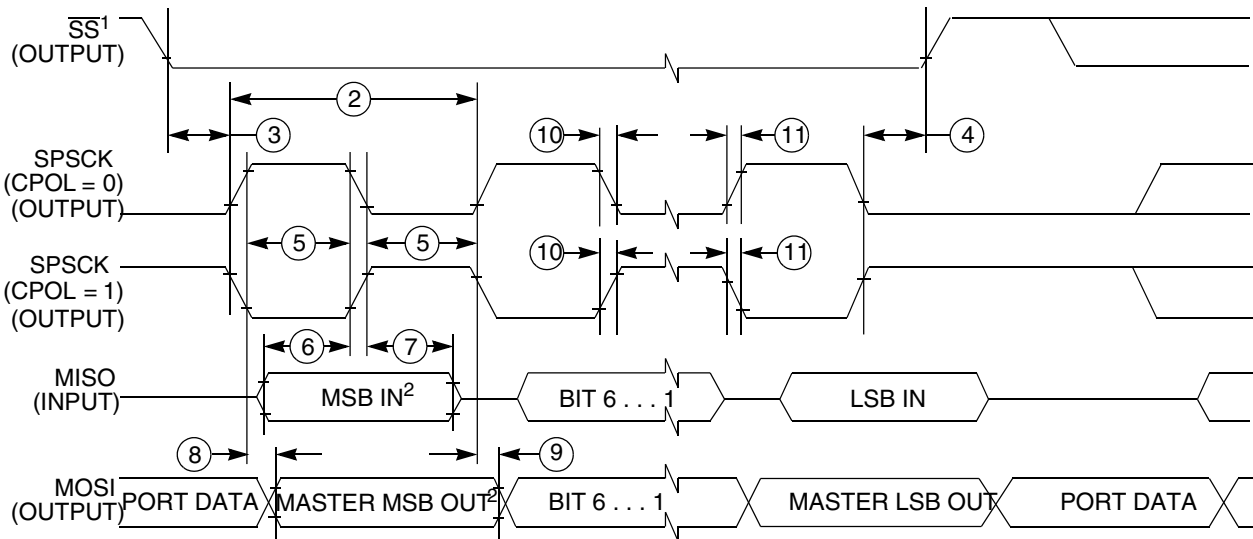
1. For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ). For SPI1  $f_{periph}$  is the system clock ( $f_{SYS}$ ).
2.  $t_{periph} = 1/f_{periph}$





1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 13. SPI master mode timing (CPHA = 0)**



1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure 14. SPI master mode timing (CPHA = 1)**

**Table 33. SPI slave mode timing on slew rate disabled pads**

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	$f_{op}$	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	$t_{SPSCK}$	SPSCK period	$4 \times t_{periph}$	—	ns	2
3	$t_{Lead}$	Enable lead time	1	—	$t_{periph}$	—
4	$t_{Lag}$	Enable lag time	1	—	$t_{periph}$	—
5	$t_{WSPSCK}$	Clock (SPSCK) high or low time	$t_{periph} - 30$	—	ns	—

Table continues on the next page...

**Table 33. SPI slave mode timing on slew rate disabled pads (continued)**

Num.	Symbol	Description	Min.	Max.	Unit	Note
6	$t_{SU}$	Data setup time (inputs)	2.5	—	ns	—
7	$t_{HI}$	Data hold time (inputs)	3.5	—	ns	—
8	$t_a$	Slave access time	—	$t_{periph}$	ns	3
9	$t_{dis}$	Slave MISO disable time	—	$t_{periph}$	ns	4
10	$t_v$	Data valid (after SPSC edge)	—	31	ns	—
11	$t_{HO}$	Data hold time (outputs)	0	—	ns	—
12	$t_{RI}$	Rise time input	—	$t_{periph} - 25$	ns	—
	$t_{FI}$	Fall time input				
13	$t_{RO}$	Rise time output	—	25	ns	—
	$t_{FO}$	Fall time output				

1. For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ). For SPI1  $f_{periph}$  is the system clock ( $f_{SYS}$ ).
2.  $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

**Table 34. SPI slave mode timing on slew rate enabled pads**

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	$f_{op}$	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	$t_{SPSC}$	SPSC period	$4 \times t_{periph}$	—	ns	2
3	$t_{Lead}$	Enable lead time	1	—	$t_{periph}$	—
4	$t_{Lag}$	Enable lag time	1	—	$t_{periph}$	—
5	$t_{WSPSC}$	Clock (SPSC) high or low time	$t_{periph} - 30$	—	ns	—
6	$t_{SU}$	Data setup time (inputs)	2	—	ns	—
7	$t_{HI}$	Data hold time (inputs)	7	—	ns	—
8	$t_a$	Slave access time	—	$t_{periph}$	ns	3
9	$t_{dis}$	Slave MISO disable time	—	$t_{periph}$	ns	4
10	$t_v$	Data valid (after SPSC edge)	—	122	ns	—
11	$t_{HO}$	Data hold time (outputs)	0	—	ns	—
12	$t_{RI}$	Rise time input	—	$t_{periph} - 25$	ns	—
	$t_{FI}$	Fall time input				
13	$t_{RO}$	Rise time output	—	36	ns	—
	$t_{FO}$	Fall time output				

1. For SPI0  $f_{periph}$  is the bus clock ( $f_{BUS}$ ). For SPI1  $f_{periph}$  is the system clock ( $f_{SYS}$ ).
2.  $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

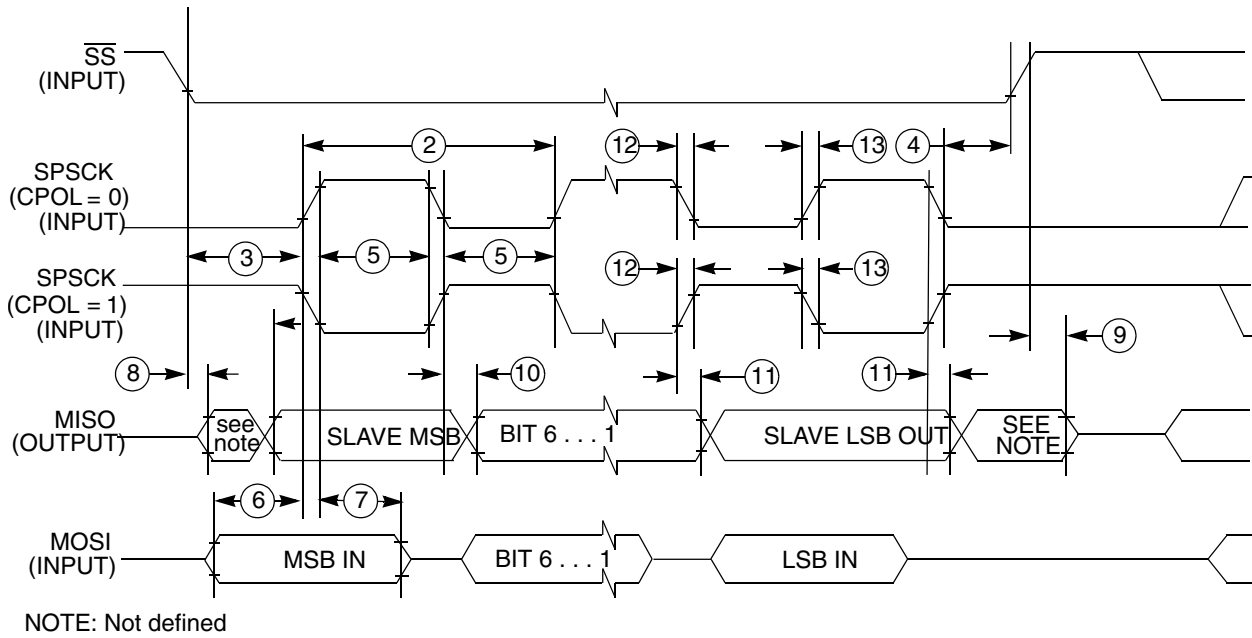


Figure 15. SPI slave mode timing (CPHA = 0)

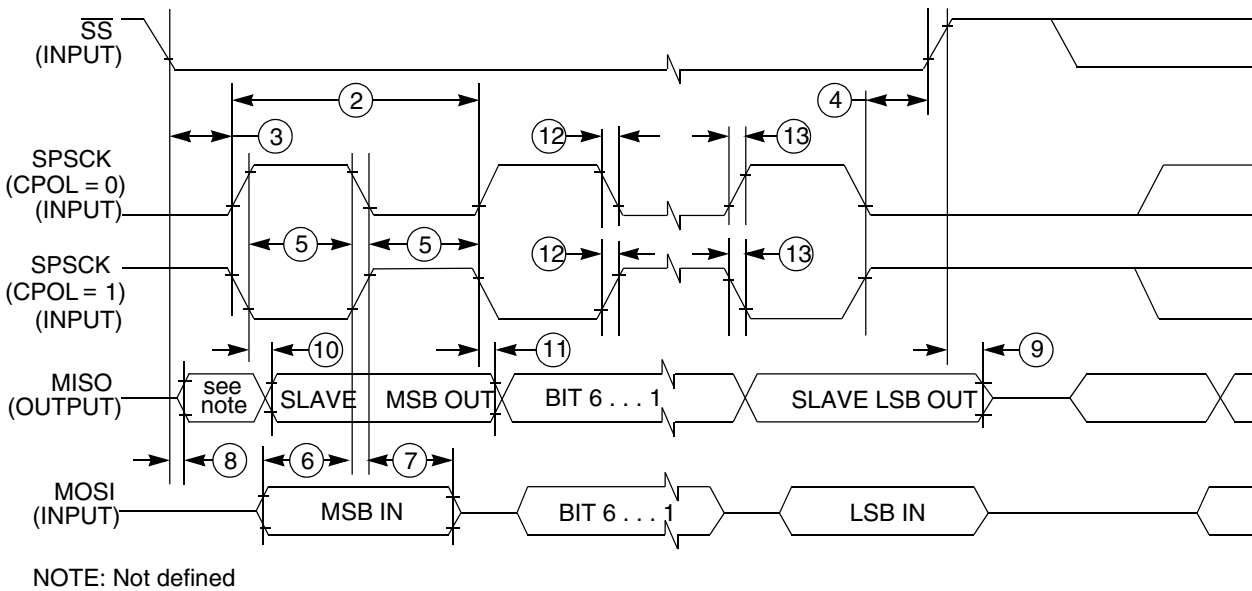


Figure 16. SPI slave mode timing (CPHA = 1)

### 6.8.2 Inter-Integrated Circuit Interface (I<sup>2</sup>C) timing

Table 35. I<sup>2</sup>C timing

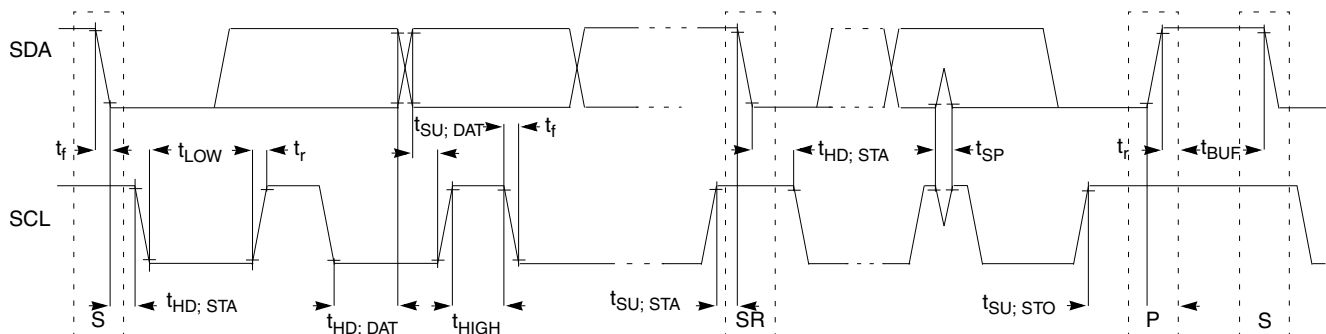
Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
SCL Clock Frequency	f <sub>SCL</sub>	0	100	0	400	kHz

Table continues on the next page...

**Table 35. I<sup>2</sup>C timing (continued)**

Characteristic	Symbol	Standard Mode		Fast Mode		Unit
		Minimum	Maximum	Minimum	Maximum	
Hold time (repeated) START condition. After this period, the first clock pulse is generated.	$t_{HD; STA}$	4	—	0.6	—	$\mu s$
LOW period of the SCL clock	$t_{LOW}$	4.7	—	1.3	—	$\mu s$
HIGH period of the SCL clock	$t_{HIGH}$	4	—	0.6	—	$\mu s$
Set-up time for a repeated START condition	$t_{SU; STA}$	4.7	—	0.6	—	$\mu s$
Data hold time for I <sup>2</sup> C bus devices	$t_{HD; DAT}$	0 <sup>1</sup>	3.45 <sup>2</sup>	0 <sup>3</sup>	0.9 <sup>1</sup>	$\mu s$
Data set-up time	$t_{SU; DAT}$	250 <sup>4</sup>	—	100 <sup>2, 5</sup>	—	ns
Rise time of SDA and SCL signals	$t_r$	—	1000	20 + 0.1C <sub>b</sub> <sup>6</sup>	300	ns
Fall time of SDA and SCL signals	$t_f$	—	300	20 + 0.1C <sub>b</sub> <sup>5</sup>	300	ns
Set-up time for STOP condition	$t_{SU; STO}$	4	—	0.6	—	$\mu s$
Bus free time between STOP and START condition	$t_{BUF}$	4.7	—	1.3	—	$\mu s$
Pulse width of spikes that must be suppressed by the input filter	$t_{SP}$	N/A	N/A	0	50	ns

1. The master mode I<sup>2</sup>C deasserts ACK of an address byte simultaneously with the falling edge of SCL. If no slaves acknowledge this address byte, then a negative hold time can result, depending on the edge rates of the SDA and SCL lines.
2. The maximum  $t_{HD; DAT}$  must be met only if the device does not stretch the LOW period ( $t_{LOW}$ ) of the SCL signal.
3. Input signal Slew = 10 ns and Output Load = 50 pF
4. Set-up time in slave-transmitter mode is 1 IPBus clock period, if the TX FIFO is empty.
5. A Fast mode I<sup>2</sup>C bus device can be used in a Standard mode I<sup>2</sup>C bus system, but the requirement  $t_{SU; DAT} \geq 250$  ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, then it must output the next data bit to the SDA line  $t_{rmax} + t_{SU; DAT} = 1000 + 250 = 1250$  ns (according to the Standard mode I<sup>2</sup>C bus specification) before the SCL line is released.
6. C<sub>b</sub> = total capacitance of the one bus line in pF.

**Figure 17. Timing definition for fast and standard mode devices on the I<sup>2</sup>C bus**

### 6.8.3 UART

See [General switching specifications](#).

## 6.8.4 I2S/SAI switching specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

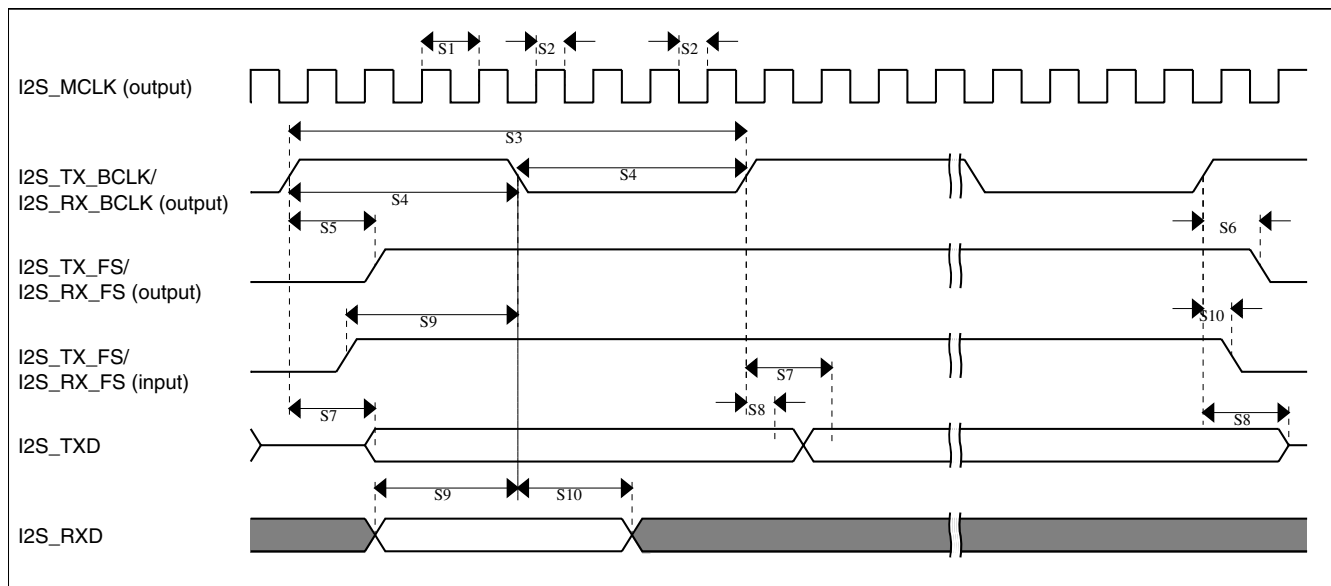
### 6.8.4.1 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

**Table 36. I2S/SAI master mode timing**

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK (as an input) pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15.5	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	19	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	26	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

## Peripheral operating requirements and behaviors



**Figure 18. I2S/SAI timing — master modes**

**Table 37. I2S/SAI slave mode timing**

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	33	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid <sup>1</sup>	—	28	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

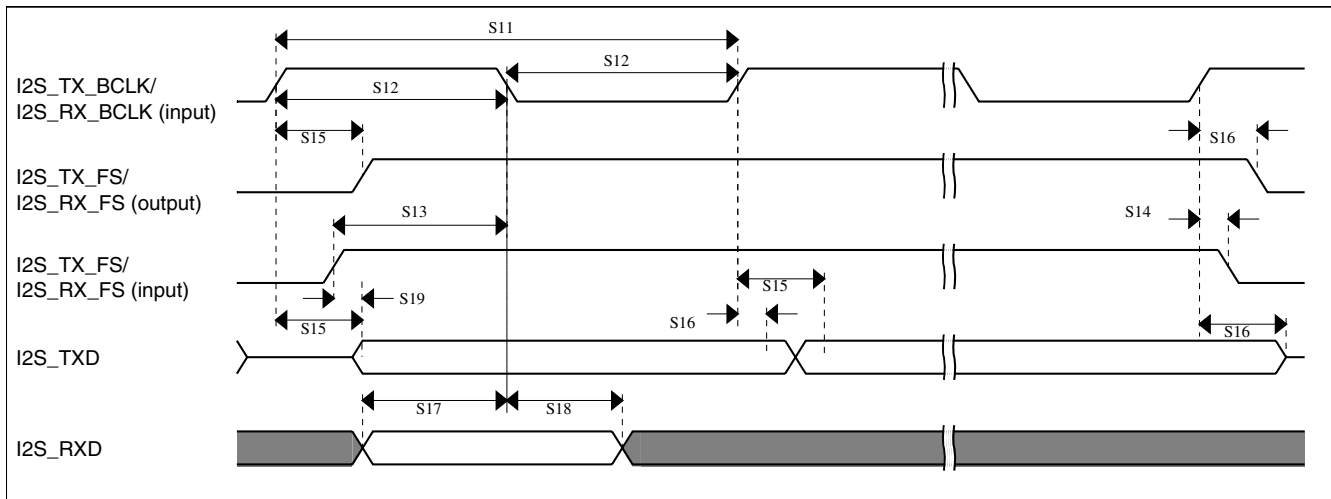


Figure 19. I2S/SAI timing — slave modes

#### 6.8.4.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 38. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid		—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK		—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

Peripheral operating requirements and behaviors

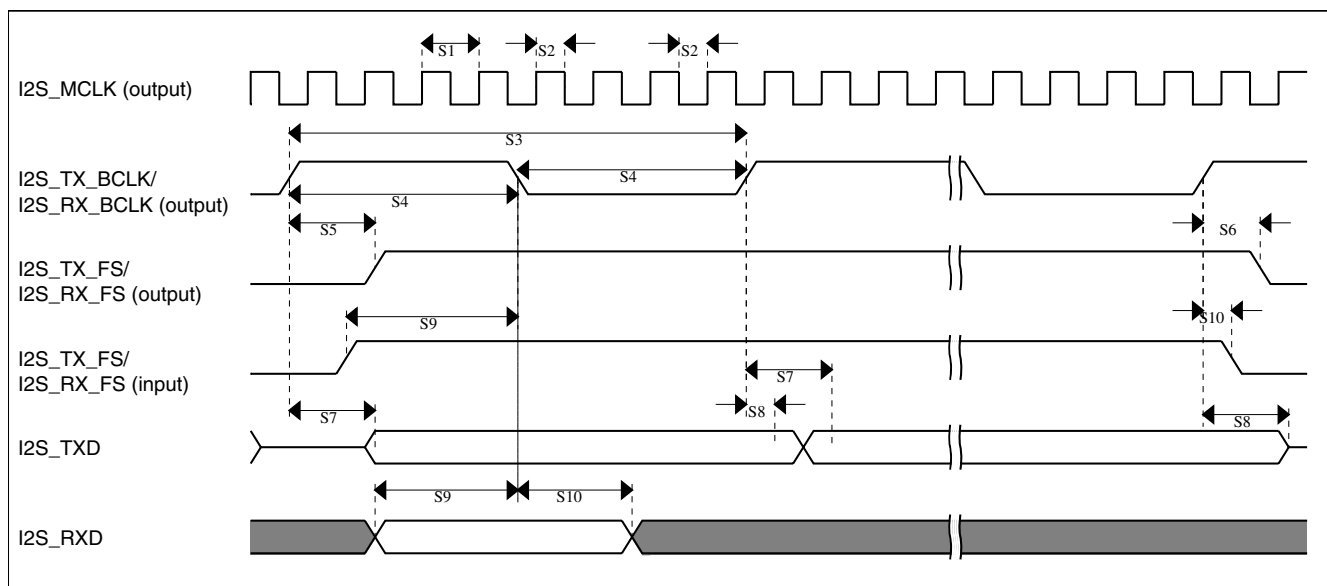


Figure 20. I2S/SAI timing — master modes

Table 39. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	—	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	—	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid <sup>1</sup>	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear



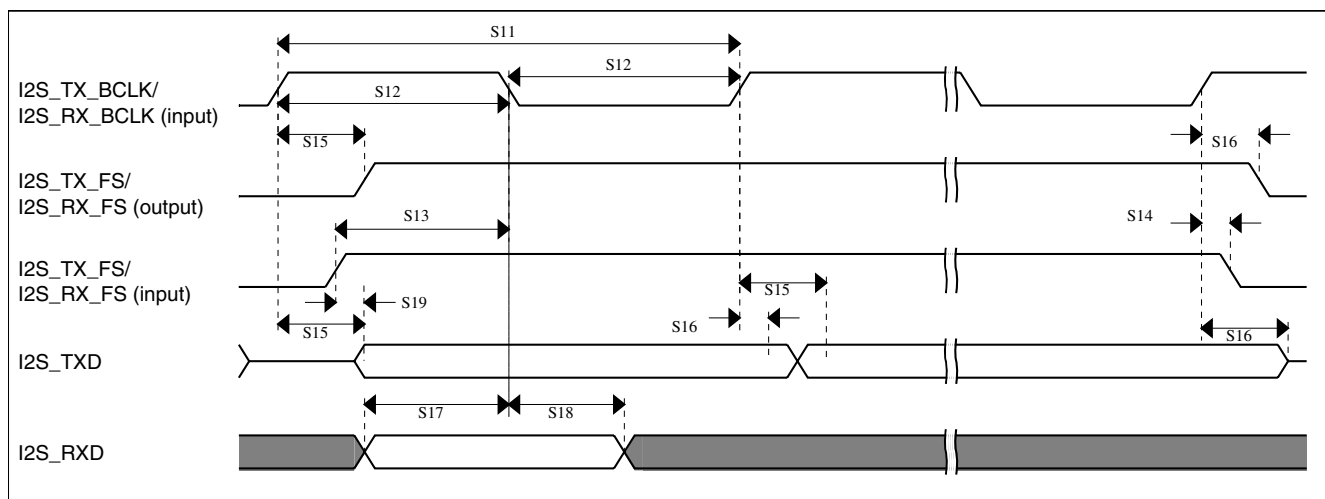


Figure 21. I2S/SAI timing — slave modes

## 6.9 Human-machine interfaces (HMI)

### 6.9.1 TSI electrical specifications

Table 40. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
TSI_RUNF	Fixed power consumption in run mode	—	100	—	μA
TSI_RUNV	Variable power consumption in run mode (depends on oscillator's current selection)	1.0	—	128	μA
TSI_EN	Power consumption in enable mode	—	100	—	μA
TSI_DIS	Power consumption in disable mode	—	1.2	—	μA
TSI_TEN	TSI analog enable time	—	66	—	μs
TSI_CREF	TSI reference capacitor	—	1.0	—	pF
TSI_DVOLT	Voltage variation of VP & VM around nominal values	0.19	—	1.03	V

## 7 Dimensions

### 7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

## Pinout

To find a package drawing, go to [freescale.com](http://freescale.com) and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
32-pin QFN	98ASA00473D
48-pin QFN	98ASA00466D
64-pin LQFP	98ASS23234W

## 8 Pinout

### 8.1 KL16 Signal Multiplexing and Pin Assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

64 LQFP	48 QFN	32 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	—	1	PTE0	DISABLED		PTE0	SPI1_MISO	UART1_TX	RTC_CLKOUT	CMP0_OUT	I2C1_SDA	
2	—	2	PTE1	DISABLED		PTE1	SPI1_MOSI	UART1_RX		SPI1_MISO	I2C1_SCL	
3	1	—	VDD	VDD	VDD							
4	2	—	VSS	VSS	VSS							
5	3	3	PTE16	ADC0_DP1/ ADC0_SE1	ADC0_DP1/ ADC0_SE1	PTE16	SPI0_PCS0	UART2_TX	TPM_CLKIN0			
6	4	4	PTE17	ADC0_DM1/ ADC0_SE5a	ADC0_DM1/ ADC0_SE5a	PTE17	SPI0_SCK	UART2_RX	TPM_CLKIN1		LPTMR0_ALT3	
7	5	5	PTE18	ADC0_DP2/ ADC0_SE2	ADC0_DP2/ ADC0_SE2	PTE18	SPI0_MOSI		I2C0_SDA	SPI0_MISO		
8	6	6	PTE19	ADC0_DM2/ ADC0_SE6a	ADC0_DM2/ ADC0_SE6a	PTE19	SPI0_MISO		I2C0_SCL	SPI0_MOSI		
9	7	—	PTE20	ADC0_DP0/ ADC0_SE0	ADC0_DP0/ ADC0_SE0	PTE20		TPM1_CH0	UART0_TX			
10	8	—	PTE21	ADC0_DM0/ ADC0_SE4a	ADC0_DM0/ ADC0_SE4a	PTE21		TPM1_CH1	UART0_RX			
11	—	—	PTE22	ADC0_DP3/ ADC0_SE3	ADC0_DP3/ ADC0_SE3	PTE22		TPM2_CH0	UART2_TX			
12	—	—	PTE23	ADC0_DM3/ ADC0_SE7a	ADC0_DM3/ ADC0_SE7a	PTE23		TPM2_CH1	UART2_RX			
13	9	7	VDDA	VDDA	VDDA							
14	10	—	VREFH	VREFH	VREFH							
15	11	—	VREFL	VREFL	VREFL							
16	12	8	VSSA	VSSA	VSSA							

64 LQFP	48 QFN	32 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
17	13	—	PTE29	CMPO_IN5/ ADC0_SE4b	CMPO_IN5/ ADC0_SE4b	PTE29		TPM0_CH2	TPM_CLKIN0			
18	14	9	PTE30	DAC0_OUT/ ADC0_SE23/ CMPO_IN4	DAC0_OUT/ ADC0_SE23/ CMPO_IN4	PTE30		TPM0_CH3	TPM_CLKIN1			
19	—	—	PTE31	DISABLED		PTE31		TPM0_CH4				
20	15	—	PTE24	DISABLED		PTE24		TPM0_CH0		I2C0_SCL		
21	16	—	PTE25	DISABLED		PTE25		TPM0_CH1		I2C0_SDA		
22	17	10	PTA0	SWD_CLK	TSIO_CH1	PTA0		TPM0_CH5				SWD_CLK
23	18	11	PTA1	DISABLED	TSIO_CH2	PTA1	UART0_RX	TPM2_CH0				
24	19	12	PTA2	DISABLED	TSIO_CH3	PTA2	UART0_TX	TPM2_CH1				
25	20	13	PTA3	SWD_DIO	TSIO_CH4	PTA3	I2C1_SCL	TPM0_CH0				SWD_DIO
26	21	14	PTA4	NMI_b	TSIO_CH5	PTA4	I2C1_SDA	TPM0_CH1				NMI_b
27	—	—	PTA5	DISABLED		PTA5		TPM0_CH2			I2S0_TX_BCLK	
28	—	—	PTA12	DISABLED		PTA12		TPM1_CH0			I2S0_TXD0	
29	—	—	PTA13	DISABLED		PTA13		TPM1_CH1			I2S0_TX_FS	
30	22	15	VDD	VDD	VDD							
31	23	16	VSS	VSS	VSS							
32	24	17	PTA18	EXTAL0	EXTAL0	PTA18		UART1_RX	TPM_CLKIN0			
33	25	18	PTA19	XTAL0	XTAL0	PTA19		UART1_TX	TPM_CLKIN1		LPTMR0_ALT1	
34	26	19	PTA20	RESET_b		PTA20						RESET_b
35	27	20	PTB0/ LLWU_P5	ADC0_SE8/ TSIO_CH0	ADC0_SE8/ TSIO_CH0	PTB0/ LLWU_P5	I2C0_SCL	TPM1_CH0				
36	28	21	PTB1	ADC0_SE9/ TSIO_CH6	ADC0_SE9/ TSIO_CH6	PTB1	I2C0_SDA	TPM1_CH1				
37	29	—	PTB2	ADC0_SE12/ TSIO_CH7	ADC0_SE12/ TSIO_CH7	PTB2	I2C0_SCL	TPM2_CH0				
38	30	—	PTB3	ADC0_SE13/ TSIO_CH8	ADC0_SE13/ TSIO_CH8	PTB3	I2C0_SDA	TPM2_CH1				
39	31	—	PTB16	TSIO_CH9	TSIO_CH9	PTB16	SPI1_MOSI	UART0_RX	TPM_CLKIN0	SPI1_MISO		
40	32	—	PTB17	TSIO_CH10	TSIO_CH10	PTB17	SPI1_MISO	UART0_TX	TPM_CLKIN1	SPI1_MOSI		
41	—	—	PTB18	TSIO_CH11	TSIO_CH11	PTB18		TPM2_CH0	I2S0_TX_BCLK			
42	—	—	PTB19	TSIO_CH12	TSIO_CH12	PTB19		TPM2_CH1	I2S0_TX_FS			
43	33	—	PTC0	ADC0_SE14/ TSIO_CH13	ADC0_SE14/ TSIO_CH13	PTC0		EXTRG_IN		CMPO_OUT	I2S0_TXD0	
44	34	22	PTC1/ LLWU_P6/ RTC_CLKIN	ADC0_SE15/ TSIO_CH14	ADC0_SE15/ TSIO_CH14	PTC1/ LLWU_P6/ RTC_CLKIN	I2C1_SCL		TPM0_CH0		I2S0_TXD0	
45	35	23	PTC2	ADC0_SE11/ TSIO_CH15	ADC0_SE11/ TSIO_CH15	PTC2	I2C1_SDA		TPM0_CH1		I2S0_TX_FS	
46	36	24	PTC3/ LLWU_P7	DISABLED		PTC3/ LLWU_P7		UART1_RX	TPM0_CH2	CLKOUT	I2S0_TX_BCLK	
47	—	—	VSS	VSS	VSS							
48	—	—	VDD	VDD	VDD							

## Pinout

64 LQFP	48 QFN	32 QFN	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
49	37	25	PTC4/ LLWU_P8	DISABLED		PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	TPM0_CH3	I2S0_MCLK		
50	38	26	PTC5/ LLWU_P9	DISABLED		PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ALT2	I2S0_RXD0		CMP0_OUT	
51	39	27	PTC6/ LLWU_P10	CMP0_IN0	CMP0_IN0	PTC6/ LLWU_P10	SPI0_MOSI	EXTRG_IN	I2S0_RX_BCLK	SPI0_MISO	I2S0_MCLK	
52	40	28	PTC7	CMP0_IN1	CMP0_IN1	PTC7	SPI0_MISO		I2S0_RX_FS	SPI0_MOSI		
53	—	—	PTC8	CMP0_IN2	CMP0_IN2	PTC8	I2C0_SCL	TPM0_CH4	I2S0_MCLK			
54	—	—	PTC9	CMP0_IN3	CMP0_IN3	PTC9	I2C0_SDA	TPM0_CH5	I2S0_RX_BCLK			
55	—	—	PTC10	DISABLED		PTC10	I2C1_SCL		I2S0_RX_FS			
56	—	—	PTC11	DISABLED		PTC11	I2C1_SDA		I2S0_RXD0			
57	41	—	PTD0	DISABLED		PTD0	SPI0_PCS0		TPM0_CH0			
58	42	—	PTD1	ADC0_SE5b	ADC0_SE5b	PTD1	SPI0_SCK		TPM0_CH1			
59	43	—	PTD2	DISABLED		PTD2	SPI0_MOSI	UART2_RX	TPM0_CH2	SPI0_MISO		
60	44	—	PTD3	DISABLED		PTD3	SPI0_MISO	UART2_TX	TPM0_CH3	SPI0_MOSI		
61	45	29	PTD4/ LLWU_P14	DISABLED		PTD4/ LLWU_P14	SPI1_PCS0	UART2_RX	TPM0_CH4			
62	46	30	PTD5	ADC0_SE6b	ADC0_SE6b	PTD5	SPI1_SCK	UART2_TX	TPM0_CH5			
63	47	31	PTD6/ LLWU_P15	ADC0_SE7b	ADC0_SE7b	PTD6/ LLWU_P15	SPI1_MOSI	UART0_RX		SPI1_MISO		
64	48	32	PTD7	DISABLED		PTD7	SPI1_MISO	UART0_TX		SPI1_MOSI		

## 8.2 KL16 pinouts

The following figures show the pinout diagrams for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see [KL16 Signal Multiplexing and Pin Assignments](#).

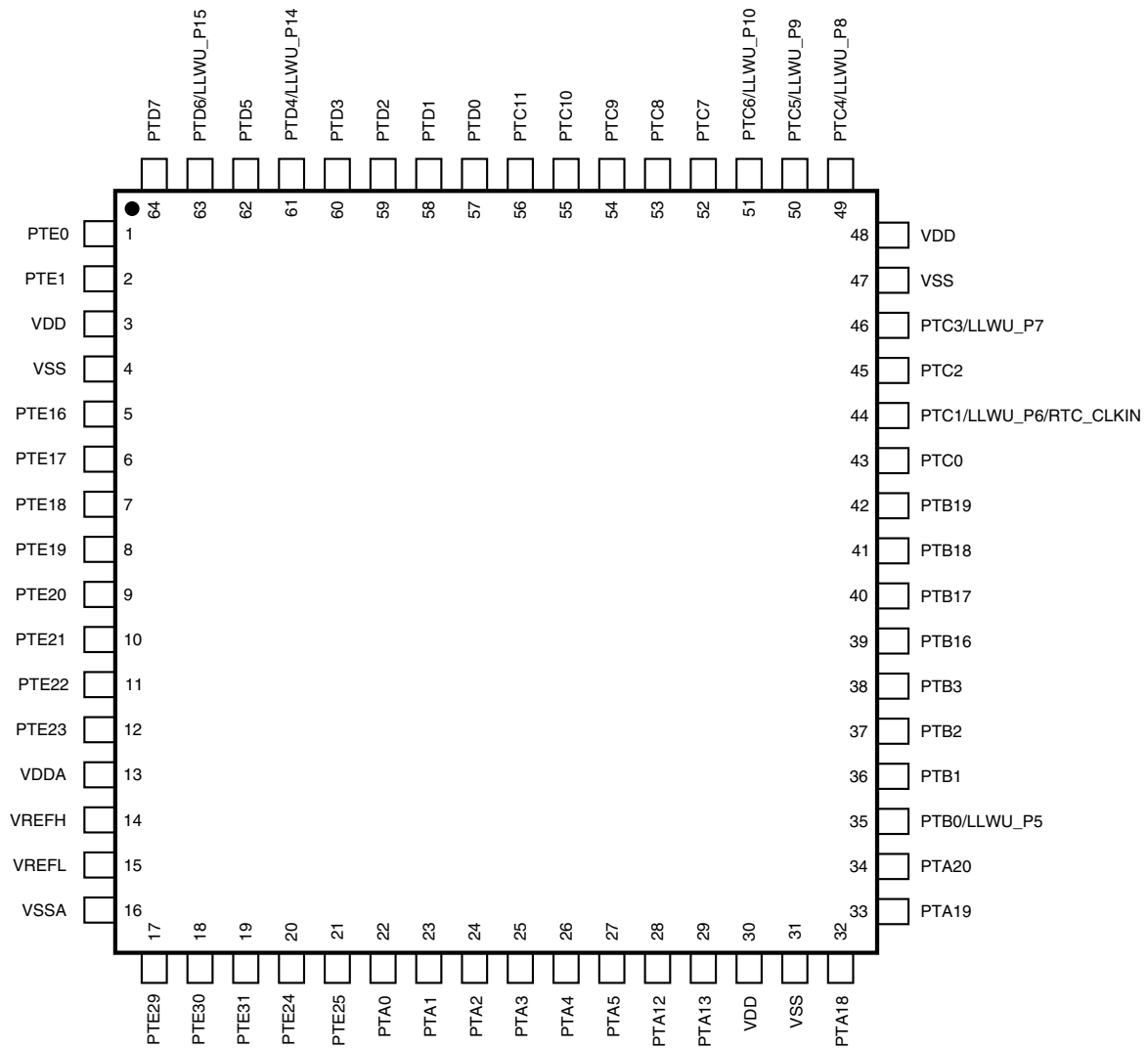


Figure 22. KL16 64-pin LQFP pinout diagram

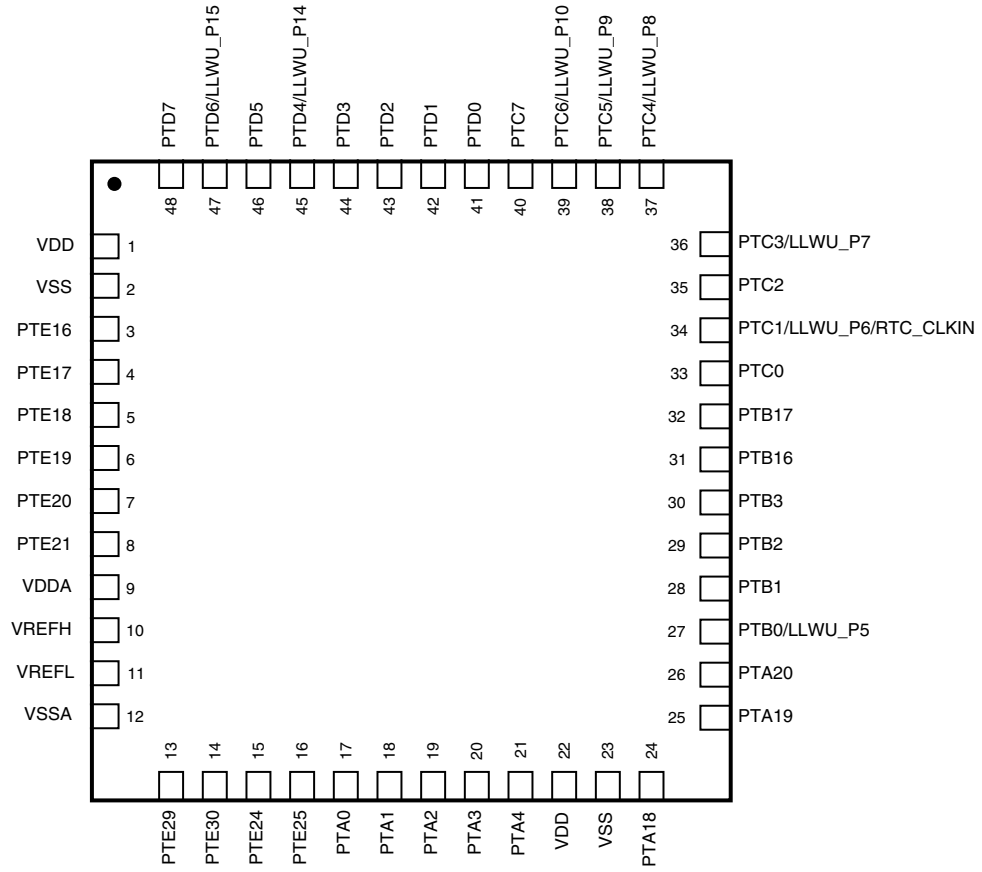


Figure 23. KL16 48-pin QFN pinout diagram

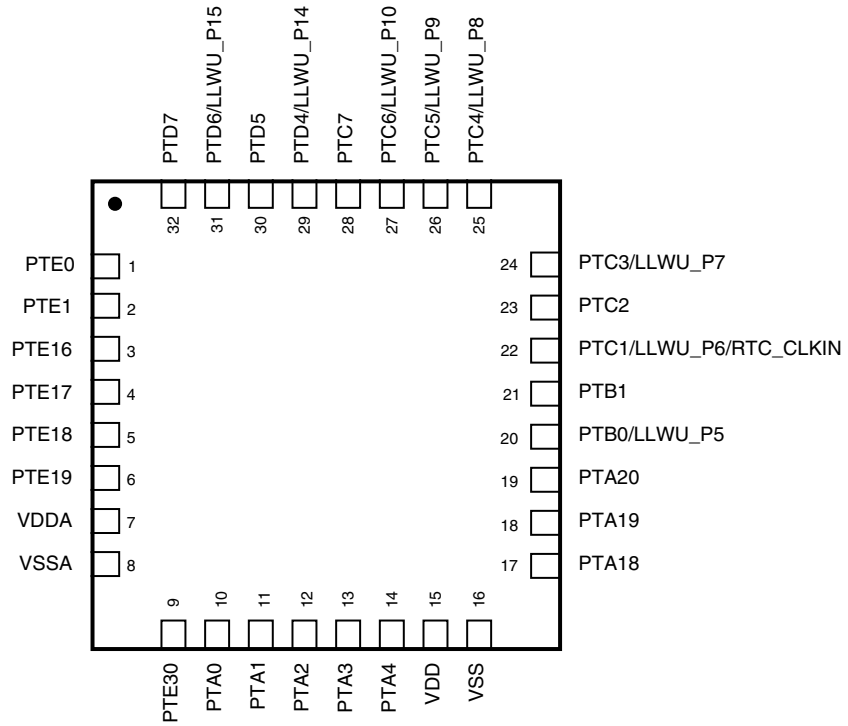


Figure 24. KL16 32-pin QFN pinout diagram



**How to Reach Us:**

**Home Page:**

[freescale.com](http://freescale.com)

**Web Support:**

[freescale.com/support](http://freescale.com/support)

Information in this document is provided solely to enable system and software implementers to use Freescale products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document.

Freescale reserves the right to make changes without further notice to any products herein. Freescale makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. Freescale does not convey any license under its patent rights nor the rights of others. Freescale sells products pursuant to standard terms and conditions of sale, which can be found at the following address: [freescale.com/SalesTermsandConditions](http://freescale.com/SalesTermsandConditions).

Freescale, the Freescale logo, Energy Efficient Solutions logo, and Kinetis are trademarks of Freescale Semiconductor, Inc., Reg. U.S. Pat. & Tm. Off. All other product or service names are the property of their respective owners. ARM and Cortex are the registered trademarks of ARM Limited.

© 2013 Freescale Semiconductor, Inc.

Document Number: KL16P64M48SF5

Rev. 2

10/2013

