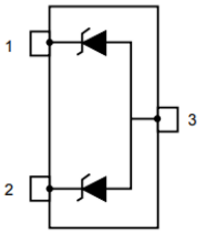
ESDAxxWY

Datasheet

Automotive dual-line unidirectional ESD protection in SOT323

SOT 323-3L (Jedec SC-70)



Pin layout

Product status link
ESDA14WY, ESDA18WY

Features

- AEC-Q101 qualified and PPAP capable
- Dual-line unidirectional ESD and EOS protection
- Very low leakage current at V_{RM} (I_R < 50 nA)
- Up to 290 W peak pulse power (8/20 µs)
- High ESD protection level: up to 30 kV
- Fast turn-on and low clamping voltage
- Operating T_j max: 175 °C
- SOT 323-3L package
- ECOPACK2 RoHS compliant component
- Complies with the following standards:
  - J-STD-020 MSL level 1 and UL94, V0
  - IPC7531 footprint and JEDEC registered package
  - ISO 10605 - C = 150 pF, R = 330 Ω:
    - ±30 kV (air and contact discharge)
  - ISO 10605 - C = 330 pF, R = 330 Ω:
    - ±30 kV (air and contact discharge)
  - ISO 7637-3:
    - Pulse 3a : -150 V; pulse 3b : +150 V
    - Pulse 2a: +/- 85 V

Application

Low speed and DC automotive applications where electrostatic discharges and other transients must be suppressed such as:

- MCUs and integrated circuits (SBC, DSP) low speed data lines and power lines
- MOSFET gate protection
- Switches and buttons
- Audio lines
- I2C, SPI communication bus

Description

ESDAxxWY series, automotive unidirectional transient voltage suppressor (TVS), has been designed for use in harsh environments to protect sensitive electronics from damage or latch-up due to electrical overstress (EOS), lightning surge and ESD without ageing effect and performance drifts.

It can therefore advantageously replace MOV (metal oxide varistor) or MLV (multi-layer varistor) as well as zener diodes, which are optimized for voltage regulation. It is the right choice for high reliability and quality systems.

In addition, this product is available in a small popular SOT323-3L (Jedec SC-70) with 2.1 mm x 2.0 mm package, ideal for space constrained applications.

1 Characteristics

1.1 Pin configuration and function

Table 1. ESDAxxWY series pin description

Pin #	Type	Description
1	I/O1	ESD protection cathode 1
2	I/O2	ESD protection cathode 2
3	GND	Common anode

Figure 1. ESDAxxWY series pinout (top view)

1.2 Absolute maximum ratings

Table 2. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter			Value	Unit
V_{ESD}	Electrostatic discharge	ISO 10605 - C = 150 pF, R = 330 Ω: Contact discharge Air discharge		 ±30 ±30	kV
		ISO 10605 - C = 330 pF, R = 330 Ω: Contact discharge Air discharge		 ±30 ±30	
P_{PP}	Peak pulse power	IEC 61000-4-5 (2 Ω) – t_p = 8/20 µs	ESDA14WY	250	W
			ESDA18WY	290	
I_{PP}	Peak pulse current	IEC 61000-4-5 (2 Ω) – t_p = 8/20 µs	ESDA14WY	13	A
			ESDA18WY	11	
T_j	Operating junction temperature range			-55 to +175	°C
T_{stg}	Storage temperature range			-65 to +175	
T_L	Maximum lead temperature for soldering during 10 s			260	

1.3 Electrical characteristics

Figure 2. **Electrical characteristics - parameter definitions**

V_{RM}	Maximum stand-off voltage
I_{RM}	Maximum leakage current at V_{RM}
V_{BR}	Breakdown voltage at I_{BR}
I_{BR}	Breakdown current
V_{CL}	Clamping voltage at I_{PP}
I_{PP}	Peak pulse current
V_F	Forward voltage drop at I_F
I_F	Forward current
R_D	Dynamic resistance
αT	Voltage temperature coefficient

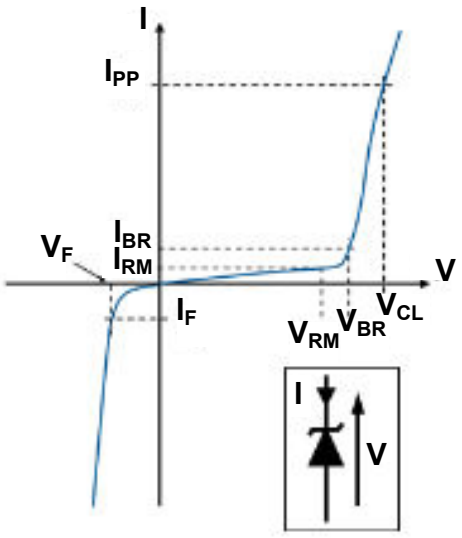


Table 3. **Electrical characteristics - parameter values (T_{amb} = 25 °C, unless otherwise specified)**

Type	I_{RM} at V_{RM}		V_{BR} at I_{BR}				8 / 20 µs(1)(2)			TLP 100 ns	C_L		αT(1)(3)	V_F at I_F	
							V_{CL}(4)	I_{PP}	R_D	V_{CL} at 16 A					
	Max.		Min.	Typ.	Max.		Max.	Max.	Typ.	Typ.	Typ.	Max.	Max.	Max.	
	µA	V	V	V	V	mA	V	A	Ω	V	pF	pF	10^{-4}/ °C	V	mA
ESDA14WY	0.05	12	14.2	15.4	16.8	1	23	13	0.41	17.5	125	150	8.7	1.2	200
ESDA18WY	0.05	16	18	19.3	20.5	1	27.7	11	0.61	21.7	95	120	8.7	1.2	200

1. *Specified by design – not tested in production.*
2. *Measured from pin 1 to 3 or pin 2 to pin 3, in accordance with IEC 61000-4-5 (8/20 µs current waveform).*
3. *To calculate V_{BR} or V_{CL} versus junction temperature, use the following formulas:*
   - *V_{BR} at T_J = V_{BR} at 25 °C x (1 + αT x (T_J - 25))*
   - *V_{CL} at T_J = V_{CL} at 25 °C x (1 + αT x (T_J - 25)).*
4. *To calculate maximum clamping voltage at other surge level, use the following formula:*
   - *V_{CL} max = V_{BR} max + R_D x $I_{PPappli}$*

   Where $I_{PPappli}$ is the surge current in the application.

1.4 Characteristics (curves)

Figure 3. Peak pulse current versus clamping voltage (8/20 µs waveform)

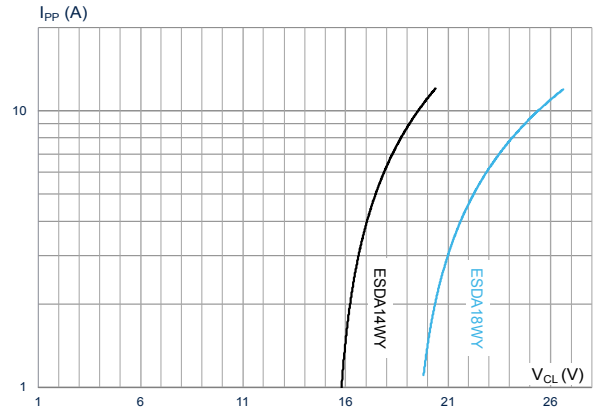


Figure 4. Peak forward current versus forward voltage drop (8/20 µs waveform)

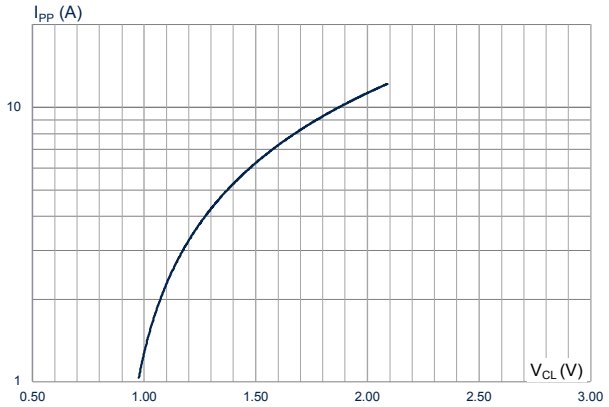


Figure 5. Junction capacitance versus reverse applied voltage

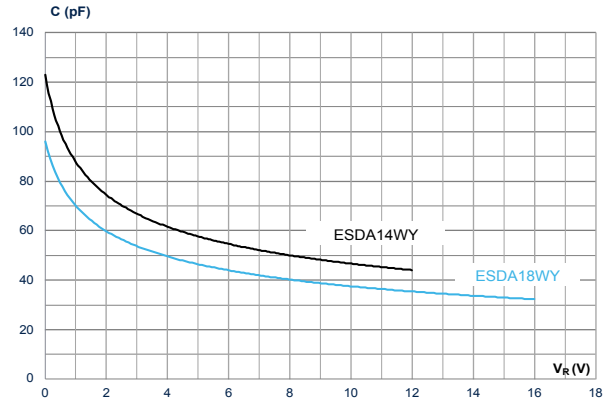


Figure 6. Leakage current versus junction temperature

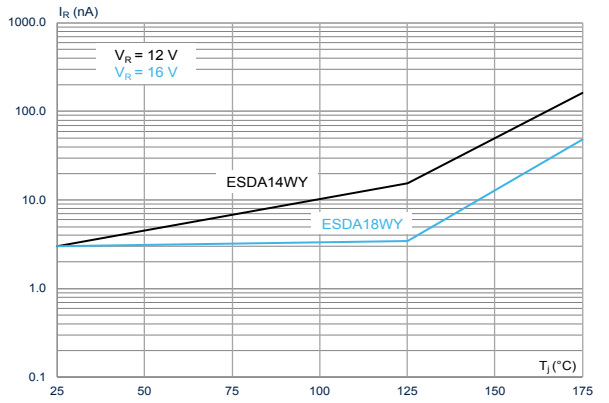


Figure 7. TLP characteristic

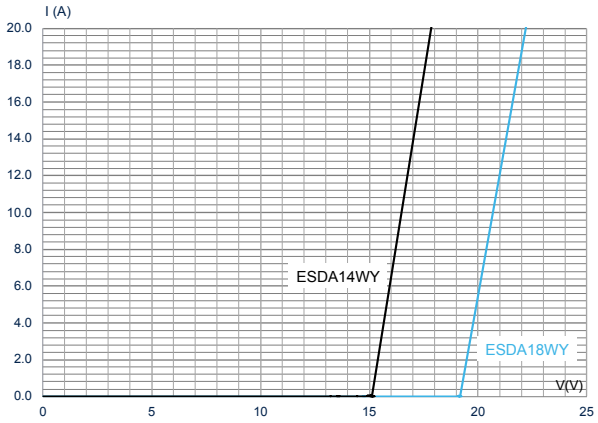


Figure 8. Reponse to ISO 10605 - C = 150 pF, R = 330 Ω (+8 kV contact)

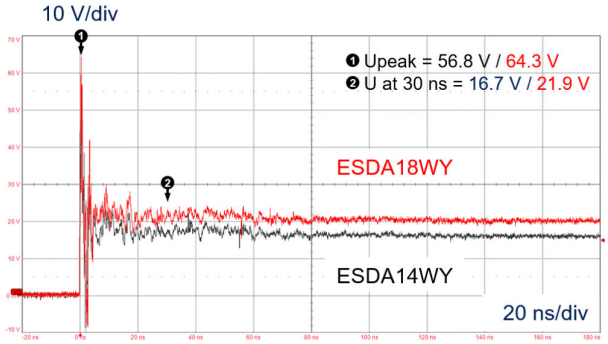


Figure 9. Reponse to ISO 10605 - C = 150 pF, R = 330 Ω (-8 kV contact)

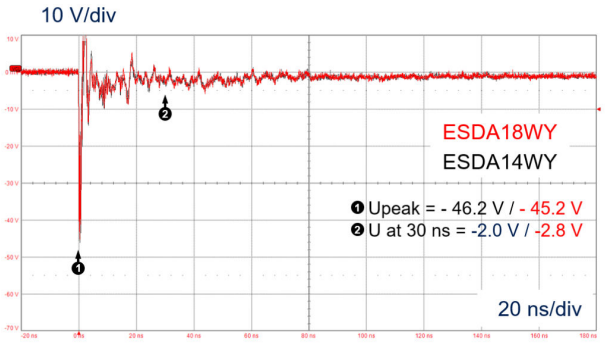


Figure 10. Response to ISO 7637-3 Pulse 3a: -150 V

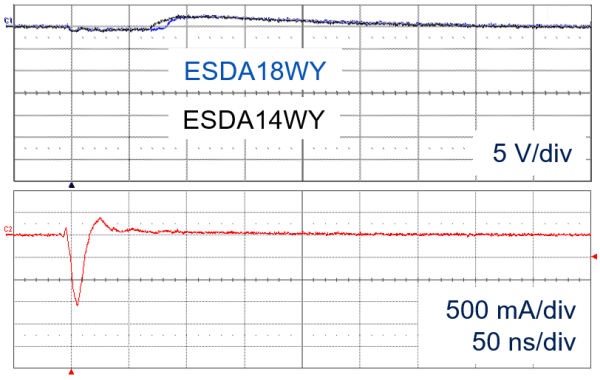


Figure 11. Response to ISO 7637-3 Pulse 3b: +150 V

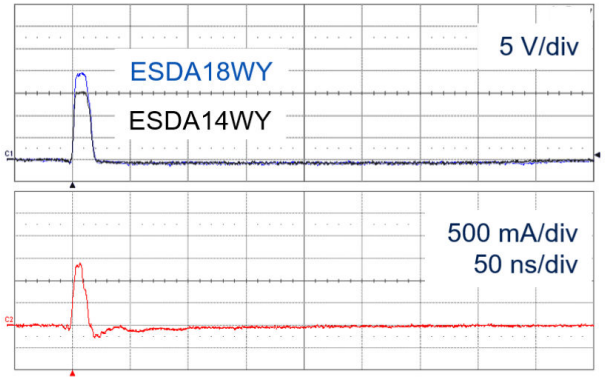


Figure 12. Response to ISO 7637-3 Pulse 2a: -85 V

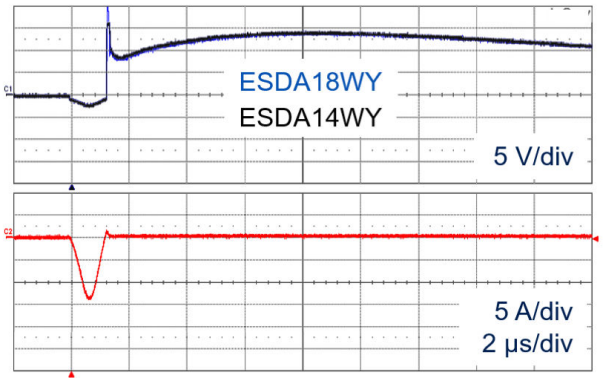
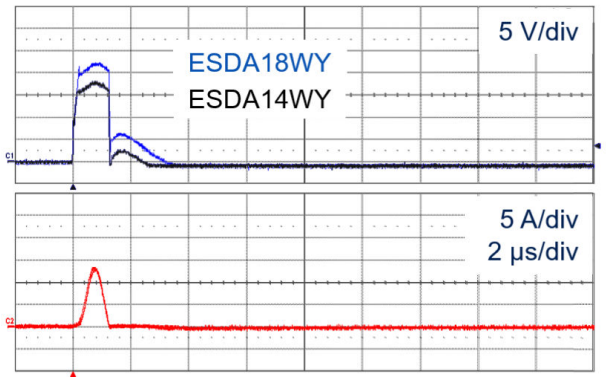


Figure 13. Response to ISO 7637-3 Pulse 2a: +85 V



2 Package information

To meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions, and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 SOT323-3L package information

- Epoxy meets UL 94,V0
- Lead-free package

Figure 14. SOT323-3L package outline

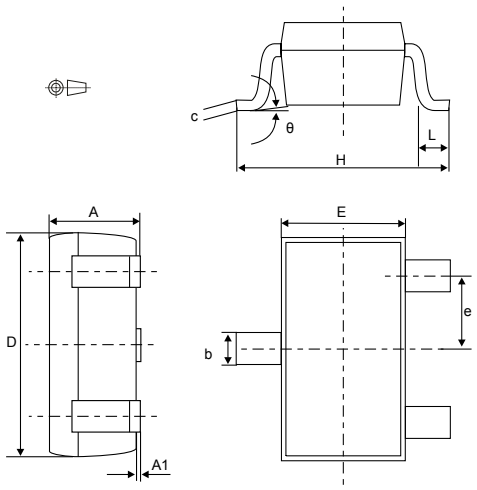


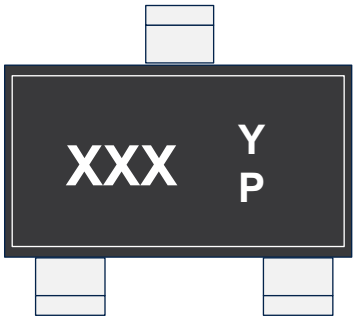
Table 4. SOT323-3L package mechanical data

Ref.	Dimensions					
	Millimeters			Inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.80		1.10	0.031		0.043
A1	0.00		0.10	0.000		0.003
b	0.25		0.40	0.0098		0.0157
c	0.10		0.26	0.003		0.0102
D	1.80	2.00	2.20	0.070	0.078	0.086
E	1.15	1.25	1.35	0.0452	0.0492	0.0531
e	0.60	0.65	0.70	0.024	0.026	0.028
H	1.80	2.10	2.40	0.070	0.082	0.094
L	0.10	0.20	0.30	0.004	0.008	0.012
Θ	0		30°	0		30°

1. *Values in inches are converted from mm and rounded to 3 or 4 decimal digits.*

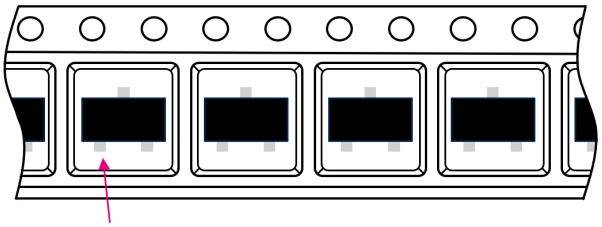
2.2 Packing and marking information

Figure 15. Marking layout



Y : Year
P : Assembly location
XXX: Marking value
Refer to Ordering information table

Figure 16. Package orientation in reel



Pin 1 located according to EIA-481

Note: Pocket dimensions are not on scale
Only pin 1 must be used to orient the component
for its placement on a PCB.

Figure 17. Reel dimensions (mm)

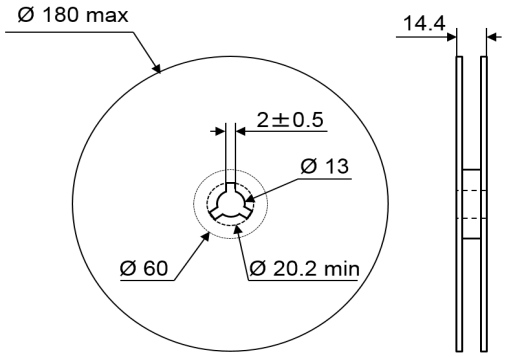


Figure 18. Tape and reel orientation

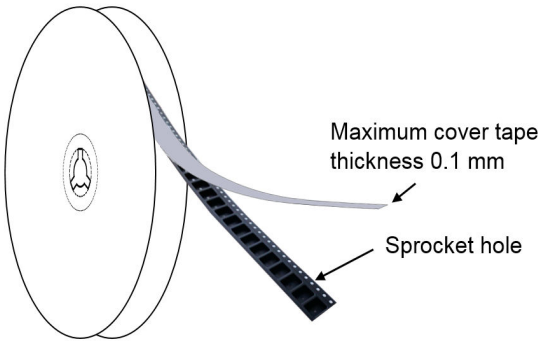


Figure 19. Inner box dimensions (mm)

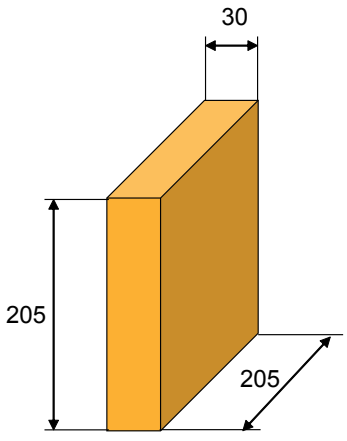
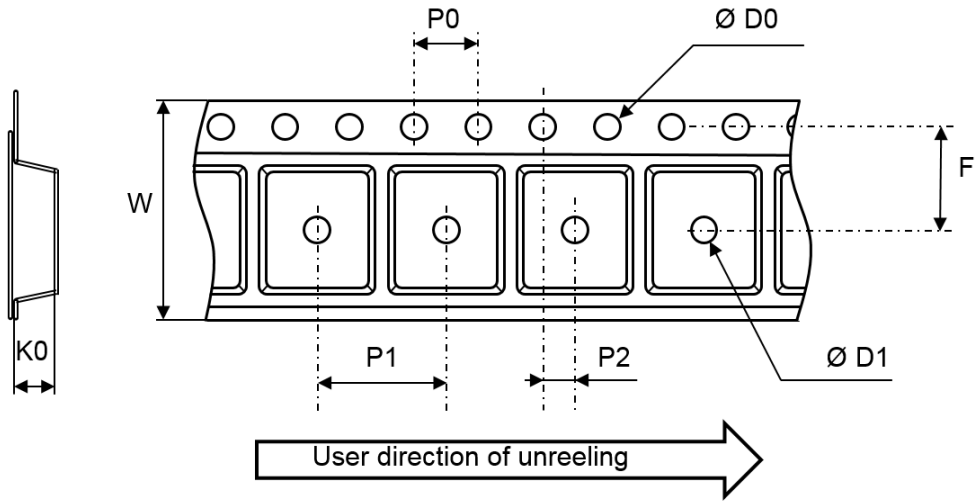


Figure 20. **Tape outline**

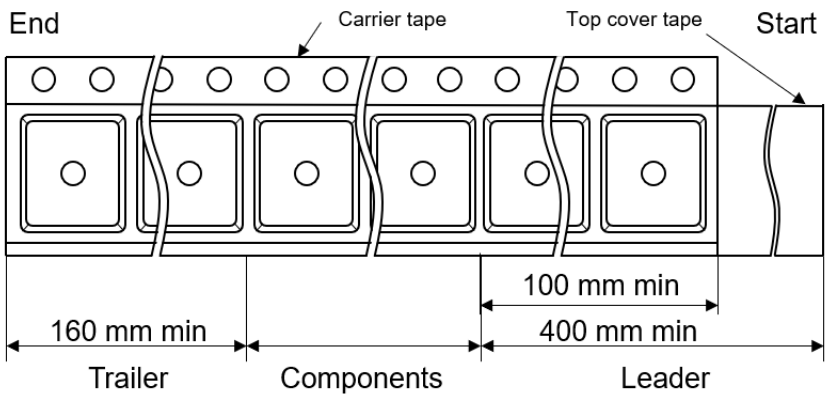


Note: Pocket dimensions are not on scale
Pocket shape may vary depending on package

Table 5. **Tape and reel mechanical data**

Ref.	Dimensions		
	Millimeters		
	Min.	Typ.	Max.
D0	1.50	1.55	1.60
D1	1.00		
F	3.45	3.50	3.55
K0	1.12	1.22	1.32
P0	3.90	4.00	4.10
P1	3.90	4.00	4.10
P2	1.95	2.00	2.05
W	7.90	8.00	8.30

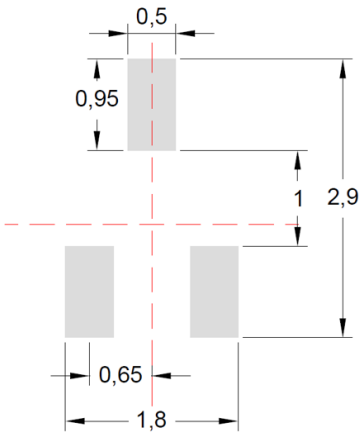
Figure 21. **Tape leader and trailer dimensions**



3 Recommendations on PCB assembly

3.1 Recommended footprint

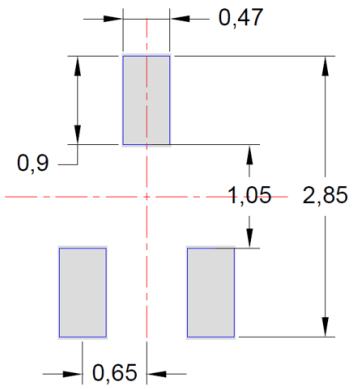
Figure 22. **Recommended footprint in mm**



3.2 Stencil opening design

- Stencil opening thickness: 75 µm to 125 µm / 3 mils to 5 mils
- Stencil opening ratio : 90%

Figure 23. **Stencil opening recommendations**



3.3 Solder paste

1. Halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste recommended.
3. Tack force high enough to resist component displacement during PCB movement.
4. Particles size 20-38 µm per IPCJ STD-005.

3.4 Placement

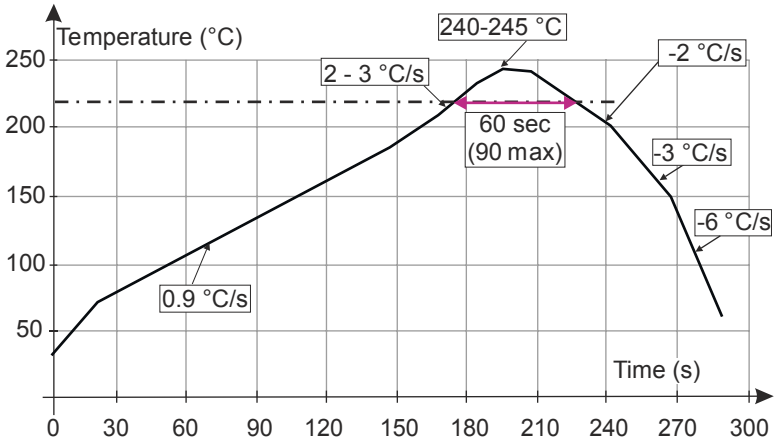
1. It is recommended to use leads recognition instead of package outline for accurate placement on footprint with adequate resolution tool.
2. Tolerance of ±50 µm is recommended.
3. 1.0 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
4. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.5 PCB design preference

1. Any via around or inside the footprint area must be closed to avoid solderpaste migration in the via.
2. Position and dimensions of the tracks should be well balanced. A symmetrical layout is recommended to prevent assembly troubles.

3.6 Reflow profile

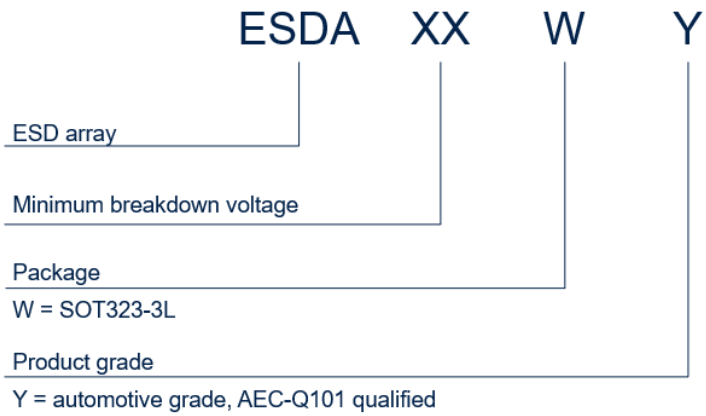
Figure 24. ST ECOPACK recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement. O_2 rate inside the oven must be below 500 ppm. Maximum soldering profile corresponds to the latest IPC/JEDEC J-STD-020.

4 Ordering information

Figure 25. **Ordering information scheme**



Order code	Marking	Package	Weight	Base qty.	Delivery mode
ESDA14WY	Y14(1)	SOT323-3L	6.6 mg	3000	Tape and reel
ESDA18WY	Y18(1)				

1. *The marking can be rotated by multiples of 90° to differentiate assembly locations.*

Revision history

Table 6. **Document revision history**

Date	Revision	Changes
16-Sep-2024	1	Initial release.

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