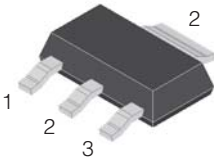
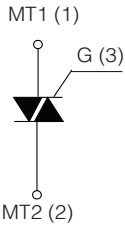




**LOGIC LEVEL TRIAC**

<p><b>SOT-223</b></p>  	<p><b>On-State Current</b> 1 Amp</p>	<p><b>Gate Trigger Current</b> &lt; 10 mA</p>	
	<p><b>Off-State Voltage</b> 400 V ÷ 800 V</p>		
	<p><b>FEATURES</b></p> <ul style="list-style-type: none"> <li>• Glass/passivated die junctions</li> <li>• Low current Triac</li> <li>• Ideal for automated placement</li> <li>• Low thermal resistance</li> <li>• High surge current capability</li> <li>• Low forward voltage drop</li> <li>• Solder dip 260°C, 10s</li> <li>• Component in accordance to RoHS 2011/65/EU and WEEE 2002/96/EC</li> <li>• Meets MSL level 3, per J-STD-020, LF maximum peak of 260° C</li> </ul>		  <b>RoHS COMPLIANT</b>
	<p><b>MECHANICAL DATA</b></p> <ul style="list-style-type: none"> <li>• <b>Case:</b> SOT-223. Epoxy meets UL 94V-0 flammability rating.</li> <li>• <b>Polarity:</b> As marked on the body.</li> <li>• <b>Terminals:</b> Matte tin plated leads, solderable per MIL-STD-750 Method 2026, J-STD-002 and JESD22-B102. Consumer grade, meets JESD 201 class 1A whisker test.</li> </ul>		
<p><b>TYPICAL APPLICATIONS</b></p> <p>Logic level versions are designed to interface directly with low power drivers such as microcontrollers.</p>			

**Maximun Ratings and Electrical Characteristics at 25°C**

SYMBOL	PARAMETER	CONDITIONS	Value	Unit
$I_{T(RMS)}$	RMS On-state Current (full sine wave)	All Conduction Angle, $T_c = 95^\circ C$	1	A
$I_{TSM}$	Non-repetitive On-State Current	Full Cycle, 60 Hz ( $t = 16.7$ ms)	8.5	A
$I_{TSM}$	Non-repetitive On-State Current	Full Cycle, 50 Hz ( $t = 20$ ms)	8	A
$I^2t$	Fusing Current	$t_p = 10$ ms, Half Cycle	0.32	A <sup>2</sup> s
$I_{GM}$	Peak Gate Current	20 $\mu$ s max. $T_j = 125^\circ C$	1	A
$P_{G(AV)}$	Average Gate Power Dissipation	$T_j = 125^\circ C$	0.1	W
$di/dt$	Critical rate of rise of on-state current	$I_G = 2x I_{GT}$ , $t_r \leq 100$ ns $f = 120$ Hz, $T_j = 125^\circ C$	20	A/ $\mu$ s
$T_j$	Operating Temperature		(-40 +125)	°C
$T_{stg}$	Storage Temperature		(-40 +150)	°C
$T_{sld}$	Soldering Temperature	10s max	260	°C

SYMBOL	PARAMETER	VOLTAGE			Unit
		D	M	N	
$V_{DRM}/V_{RRM}$	Repetitive Peak Off State Voltage	400	600	800	V

**LOGIC LEVEL TRIAC**

**Electrical Characteristics at Tamb = 25 °C**

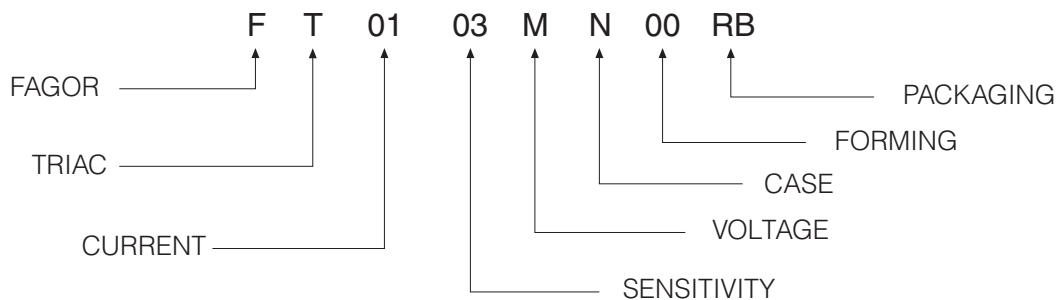
SYMBOL	PARAMETER	CONDITIONS	Quadrant		SENSITIVITY			Unit
					03	07	09	
I <sub>GT</sub> <sup>(1)</sup>	Gate Trigger Current	V <sub>D</sub> = 12 V <sub>DC</sub> , R <sub>L</sub> = 33Ω, T <sub>j</sub> = 25 °C	Q1÷Q3	MAX	3	5	10	mA
			Q4	MAX	5	7	10	mA
V <sub>GT</sub>	Gate Trigger Voltage	V <sub>D</sub> = 12 V <sub>DC</sub> , R <sub>L</sub> = 33Ω, T <sub>j</sub> = 25 °C	Q1÷Q4	MAX	1.3			V
V <sub>GD</sub>	Gate Non Trigger Voltage	V <sub>D</sub> = V <sub>DRM</sub> , R <sub>L</sub> = 3.3kΩ, T <sub>j</sub> = 125 °C	Q1÷Q4	MIN	0.2			V
I <sub>H</sub> <sup>(2)</sup>	Holding Current	I <sub>T</sub> = 50 mA, Gate open, T <sub>j</sub> = 25 °C		MAX	7	10	10	mA
I <sub>L</sub>	Latching Current	I <sub>G</sub> = 1.2 I <sub>GT</sub> , T <sub>j</sub> = 25 °C	Q1,Q3,Q4	MAX	7	10	15	mA
			Q2	MAX	15	20	25	mA
dV/dt <sup>(2)</sup>	Critical Rate of Voltage Rise	V <sub>D</sub> = 0.67 x V <sub>DRM</sub> , Gate open T <sub>j</sub> = 125 °C		MIN	10	20	50	V/μs
(di/dt) <sub>c</sub> <sup>(2)</sup>	Critical Rate of Current Rise	(dv/dt) <sub>c</sub> = 0.1 V/μs T <sub>j</sub> = 125 °C		MIN	1.2	1.8	2.5	A/ms
		(dv/dt) <sub>c</sub> = 10 V/μs T <sub>j</sub> = 125 °C		MIN	0.6	0.9	1.5	A/ms
		without snubber T <sub>j</sub> = 125 °C		MIN				
V <sub>TM</sub> <sup>(2)</sup>	On-state Voltage	I <sub>T</sub> = 1.1 Amp, t <sub>p</sub> = 380 μs, T <sub>j</sub> = 25 °C		MAX	1.5			V
V <sub>to</sub> <sup>(2)</sup>	Threshold Voltage	T <sub>j</sub> = 125 °C		MAX	0.95			V
r <sub>d</sub> <sup>(2)</sup>	Dynamic resistance	T <sub>j</sub> = 125 °C		MAX	1000			mΩ
I <sub>DRM</sub> /I <sub>RRM</sub>	Off-State Leakage Current	V <sub>D</sub> = V <sub>DRM</sub> , V <sub>R</sub> = V <sub>RRM</sub> , T <sub>j</sub> = 125 °C T <sub>j</sub> = 25 °C		MAX	0.5			mA
				MAX	5			μA
R <sub>th(j-c)</sub>	Thermal Resistance Junction-Case	for AC 360° conduction angle			80			°C/W
R <sub>th(j-a)</sub>	Thermal Resistance Junction-Ambient	S <sup>(3)</sup> = 5cm <sup>2</sup>			60			°C/W

(1) Minimum I<sub>GT</sub> is guaranteed at 5% of I<sub>GT</sub> max.

(2) For either polarity of electrode MT2 voltage with reference to electrode MT1.

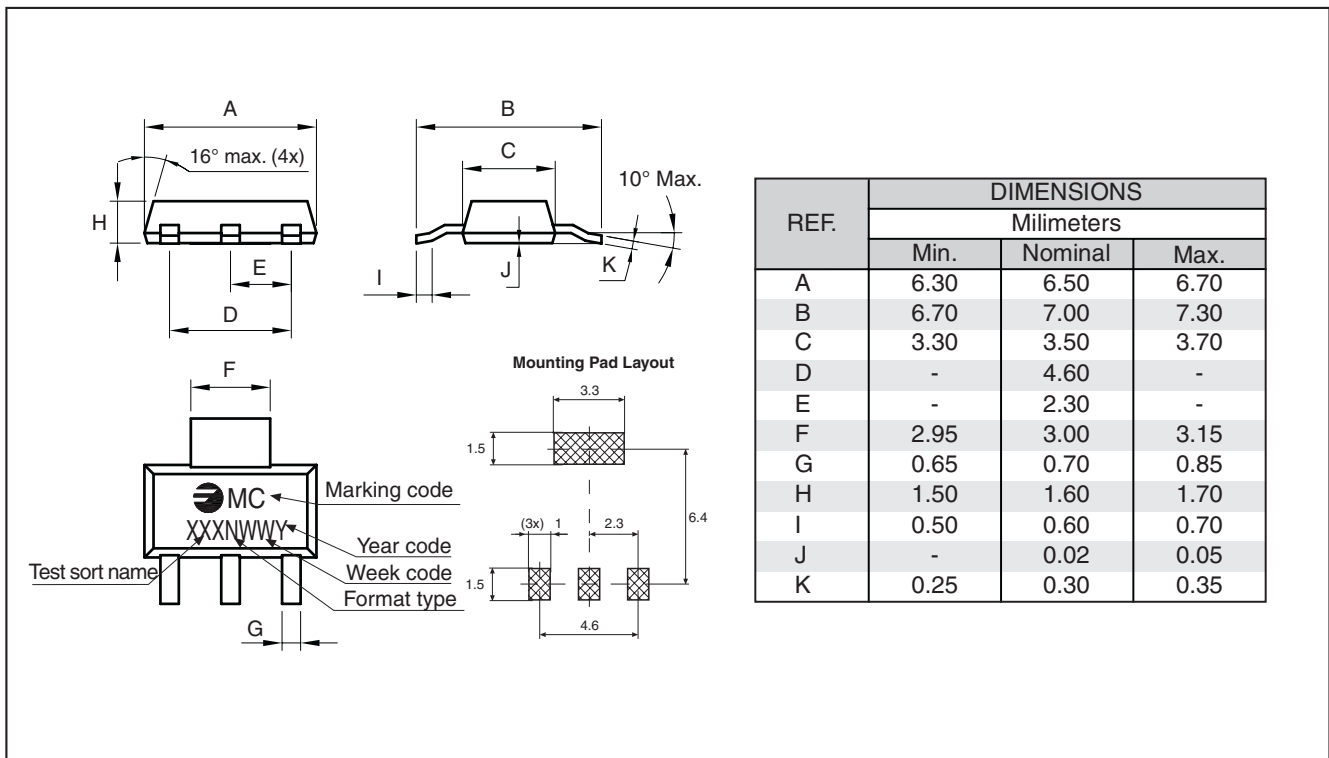
(3) S: Cooper surface under tab.

**Part Number Information**



**LOGIC LEVEL TRIAC**
**Ordering information**

PREFERRED P/N	PACKAGE CODE	DELIVERY MODE	BASE QUANTITY	UNIT WEIGHT (g)
FT0103DN 00RS	RS	REEL	1,000	0.116
FT0103DN 00RB	RB	REEL	2,500	0.116

**Package Outline Dimensions: (mm) (SOT-223)**


**LOGIC LEVEL TRIAC**

**Ratings and Characteristics (Ta 25 °C unless otherwise noted)**

Fig. 1: Maximum power dissipation versus RMS on-state current (full cycle)

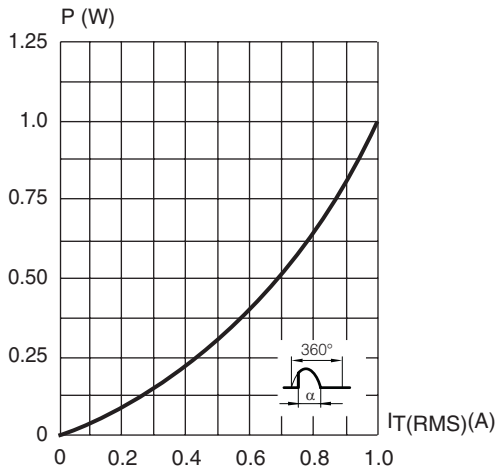


Fig. 2: RMS on-state current versus case temperature (full cycle).

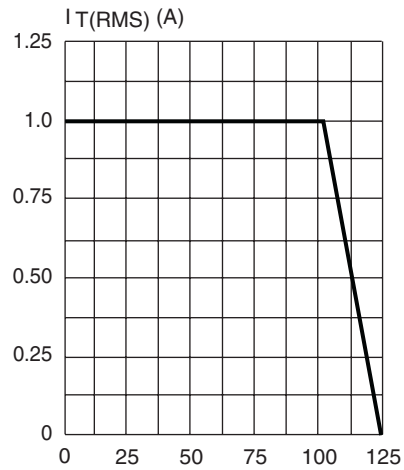


Fig. 3: Relative variation of thermal impedance versus pulse duration.

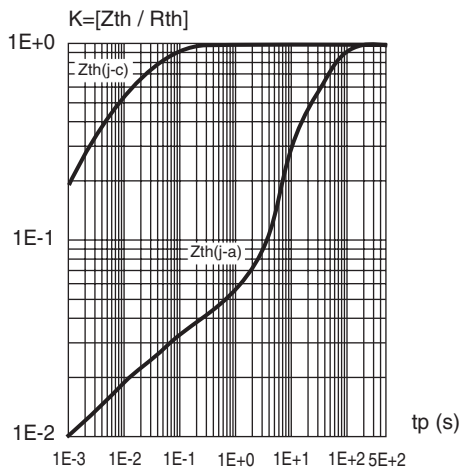


Fig. 4: On-state characteristics (maximum values)

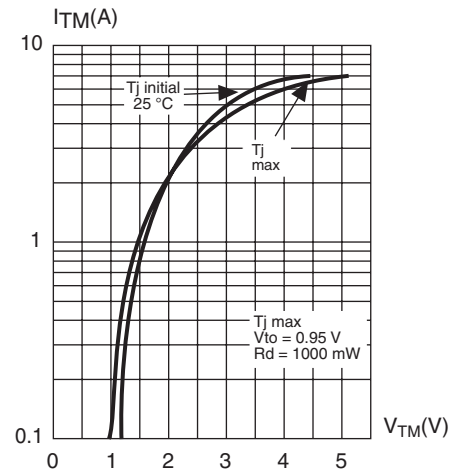


Fig. 5: Surge peak on-state current versus number of cycles

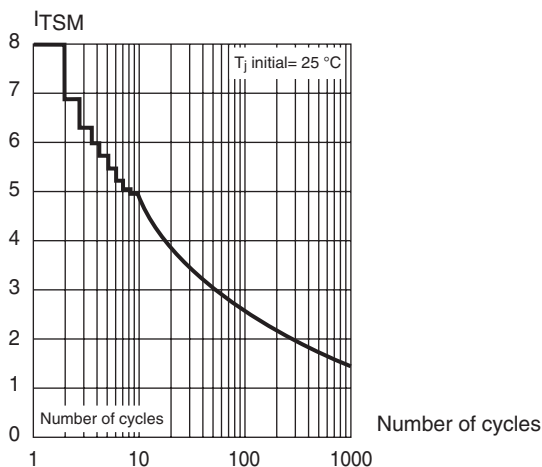
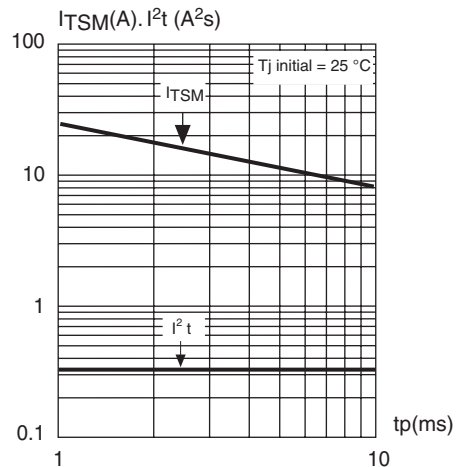


Fig. 6: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp<10ms, and corresponding value of I²t.



**LOGIC LEVEL TRIAC**

**Ratings and Characteristics (Ta 25 °C unless otherwise noted)**

Fig. 7: Relative variation of gate trigger current, holding current and latching versus junction temperature (typical values)

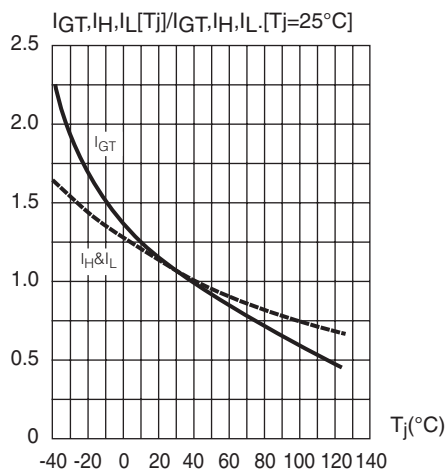


Fig. 8: Relative variation of critical rate of decrease of main current versus junction temperature

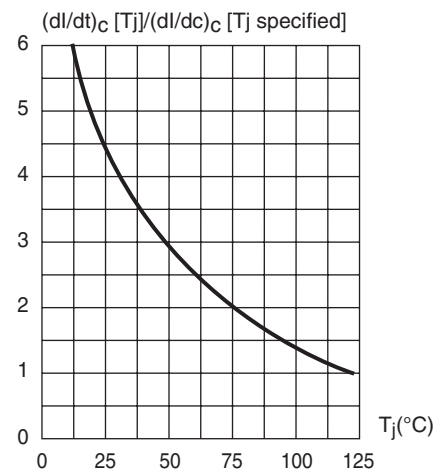
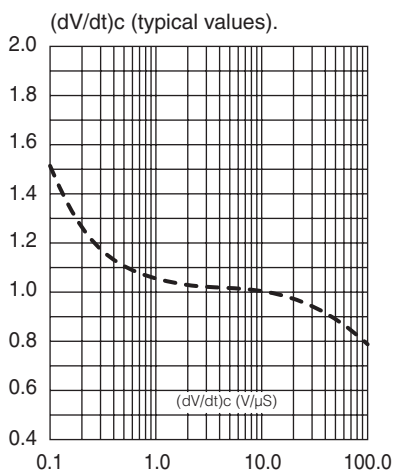


Fig. 9: Relative variation of critical rate of decrease of main current versus



**LOGIC LEVEL TRIAC****Revision History**

Date	Revision	Description of Changes
Oct-2014	0	Original Data Sheet
May-2016	1	Sensitivity 05 eliminated

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