

FEATURES

- Fully integrated boost converter with inductor
- 0.5 V – 1.6 V input range^a
- 1.4 V – 1.8 V output range
- 100 mA load continuous operation
- Up to 92% efficiency
- 5 MHz switching frequency (PWM)
- PFM light load mode
- 2 mm x 2 mm 6-pin LGA package
- 0.75 mm maximum profile
- Internal loop compensation
- Cycle-by-cycle current limit
- Soft-Start, OTP, SCP
- RoHS compliant

APPLICATIONS

- Hearing aids and wearables
- IoT sensors
- Single- and double-cell PV applications

^aDerating below 0.8 V

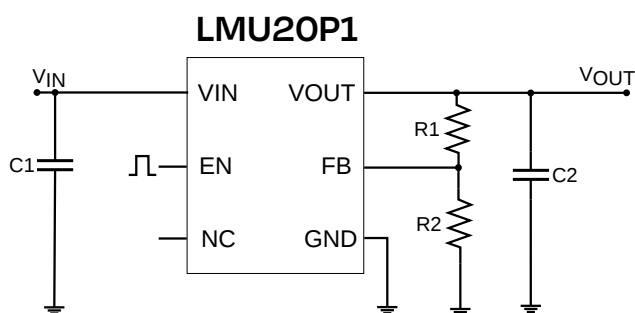
DESCRIPTION

The LMU20P1 is a miniaturized step-up Power Supply in Package (PSiP) offering small size and high efficiency. The PSiP includes an integrated switching controller, FETs, and an inductor in a compact 6-pin LGA package (2 mm x 2 mm x 0.75 mm), optimized for automated assembly by standard surface-mount pick-and-place equipment.

The LMU20P1 has a light-load efficiency enhancement function to achieve high efficiency across a wide load range and features a range of protection circuits that include soft start, over-temperature protection, short-circuit protection, and cycle-by-cycle current limit. The LMU20P1 has up to 92% efficiency and up to 80% efficiency at 100 μ A load.

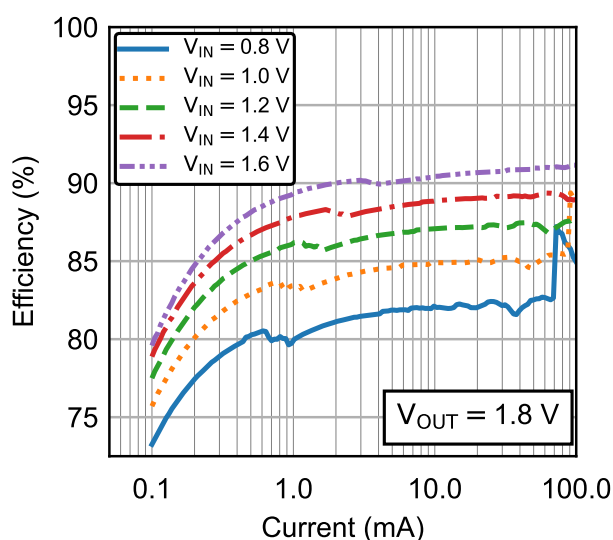
The LMU20P1 offers exceptionally low near-field radiation levels and a proprietary start-up circuit to minimize input inrush current.

TYPICAL APPLICATION



- $C1$ is the input capacitor
- $C2$ is the output capacitor
- $R1$ and $R2$ are the feedback resistors

EFFICIENCY



ABSOLUTE MAXIMUM RATINGS¹

All pins to GND	-0.2 V to +1.98 V
Operating Temperature Range	-40 °C to +85 °C
Junction Temperature Range	-40 °C to +150 °C
Maximum Reflow Temperature	+260 °C

ELECTRICAL CHARACTERISTICS

All values are measured or simulated at $T_A = +25\text{ °C}$, $C_{IN} = C_{OUT} = 10\text{ }\mu\text{F}$, $V_{IN} = V_{EN} = 1.5\text{ V}$, $V_{OUT} = 1.6\text{ V}$, Load = $18\text{ }\Omega$ unless otherwise specified.

Parameter	Symbol	Conditions & Notes	Min	Typ	Max	Unit
Input Quiescent Current	$I_{Q_IN_SD}$	EN=LOW		0.18		μA
	$I_{Q_IN_NSW}$	EN=HIGH, non-switching		0.7		μA
Input Voltage Range	V_{IN}	Derating at high load below 0.8 V	0.5		1.6	V
Min. Input Start-up Voltage	V_{IN_STRT}			0.8		V
Enable Voltage Threshold	V_{EN_HTL}	HIGH to LOW	0.3	0.5		V
	V_{EN_LTH}	LOW to HIGH		0.6	0.8	V
Enable Pin Leakage	I_{EN_LK}	$V_{EN} = 1.6\text{ V}$		0.5		nA
Feedback Pin Leakage	I_{FB_LK}	$V_{EN} = 1.6\text{ V}$		0.5		nA
Switching Frequency	f_{SW}			5.0		MHz
Feedback Voltage Reference	V_{REF}		394.0	400.0	407	mV
Output Quiescent Current	$I_{Q_OUT_NSW}$	EN=HIGH, non-switching		15		μA
Output Voltage Range	V_{OUT}		1.4		1.8	V
Output Current Limit	I_{OUT_LIM}		100.0			mA
Output Voltage Accuracy	$V_{OUT_ACC_PWM}$	PWM (Does not include feedback resistors tolerance)			± 2	%
	$V_{OUT_ACC_PFM}$	PFM (Does not include feedback resistors tolerance)			± 3	%

Table 1: Electrical Characteristics

¹Exposing the device to conditions beyond what is listed under "Absolute maximum ratings" may affect the reliability of the device or cause permanent damage.

PIN CONFIGURATION AND FUNCTION

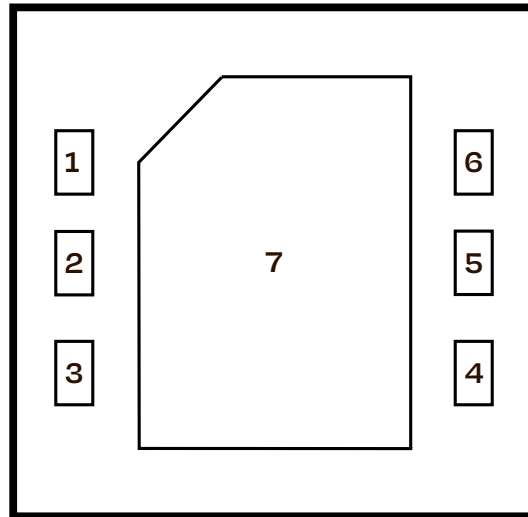


Figure 1: LMU20P1 (Top View)

Pin	Name	Description
1	NC	Do not connect.
2	GND	Power and signal ground.
3	VIN	Input voltage pin. Connect to the input capacitor.
4	EN	Enable pin. Connect to logic HIGH for normal operation.
5	FB	Feedback pin. Connect to VOUT through a resistor divider.
6	VOUT	Output voltage pin. Connect to the output capacitor.
7	GND	Thermal pad. Internally connected to ground.

Table 2: Pin Function

FUNCTIONAL BLOCK DIAGRAM

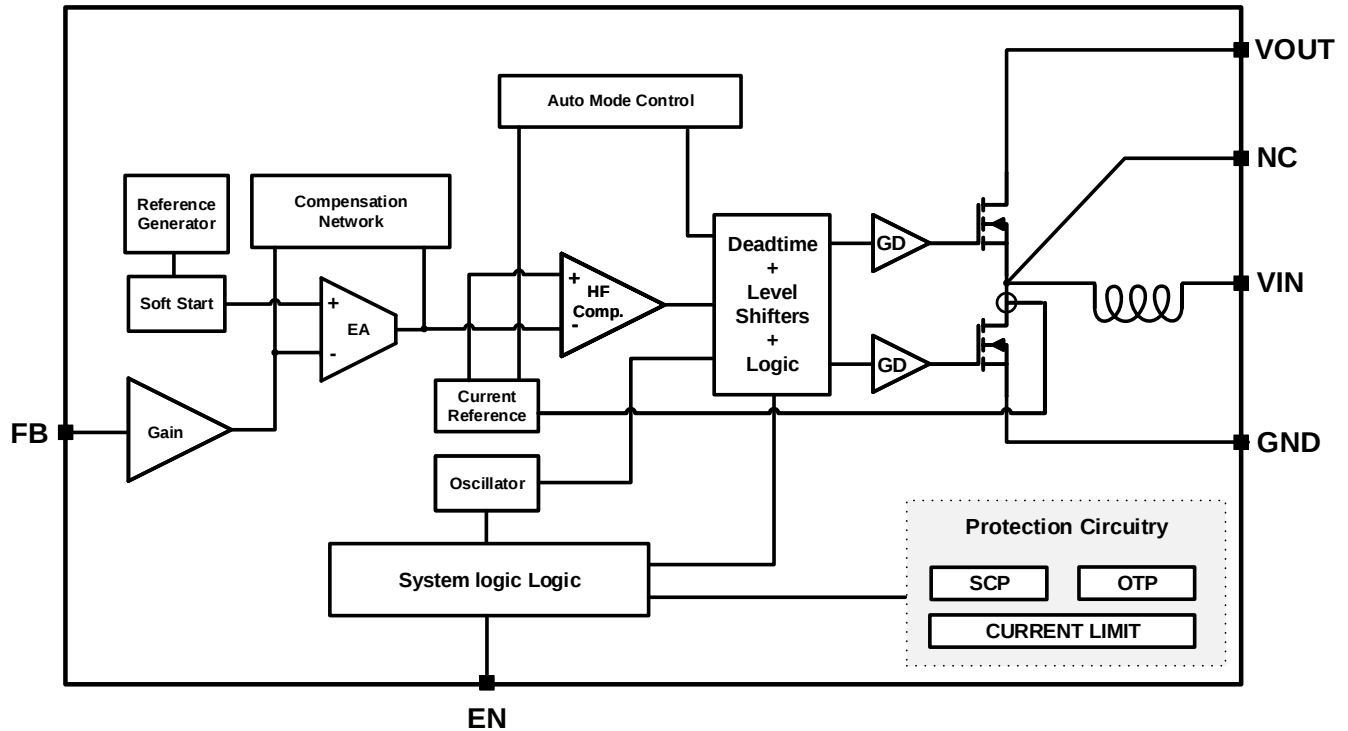
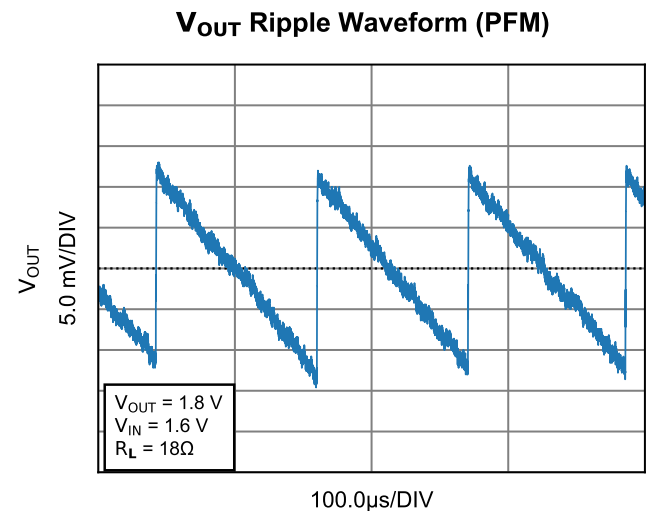
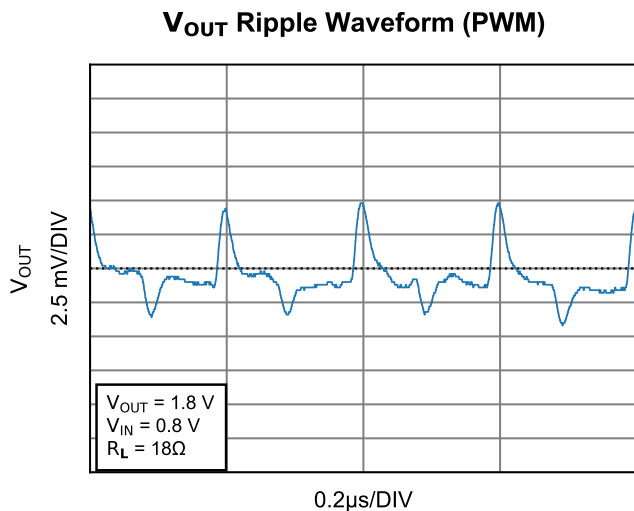
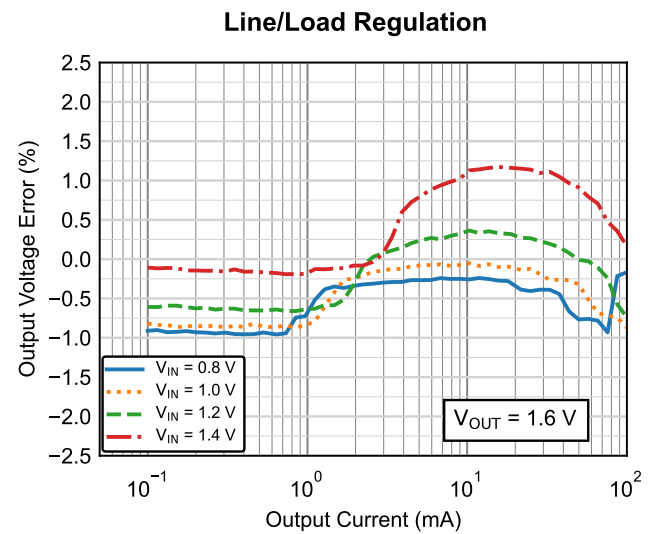
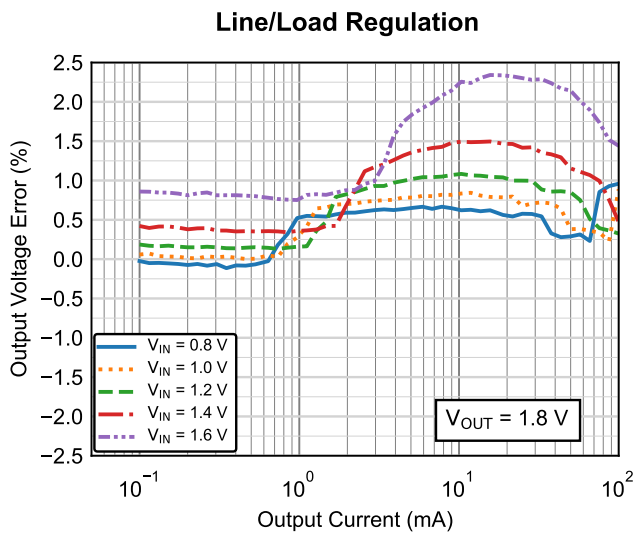
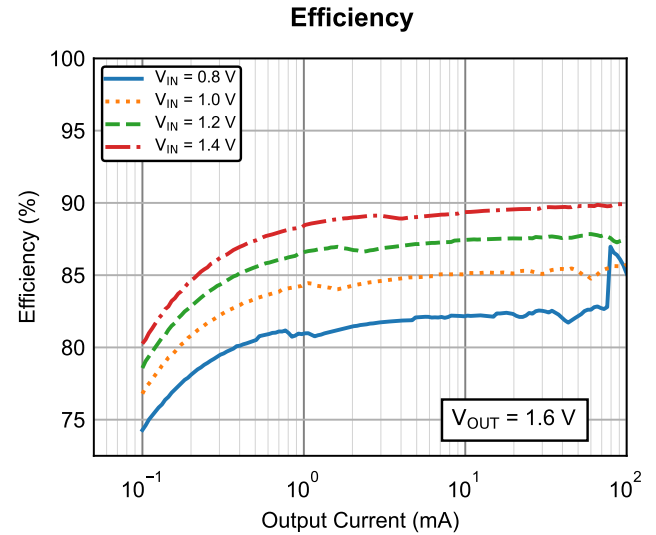
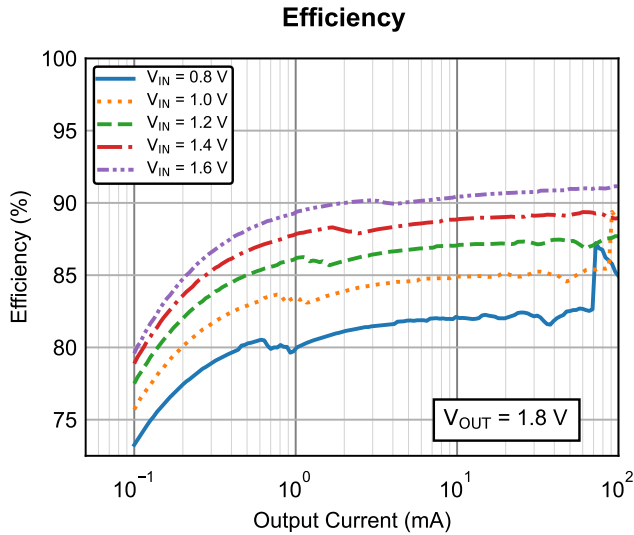
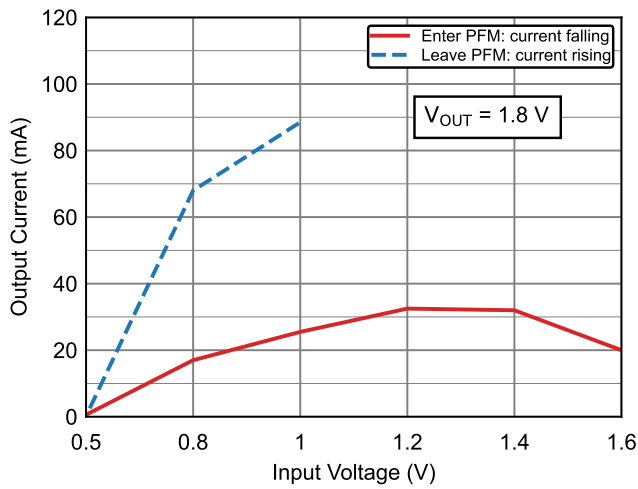
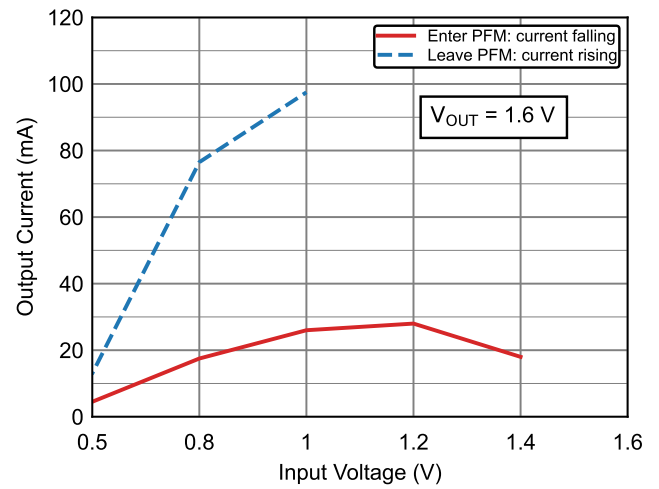
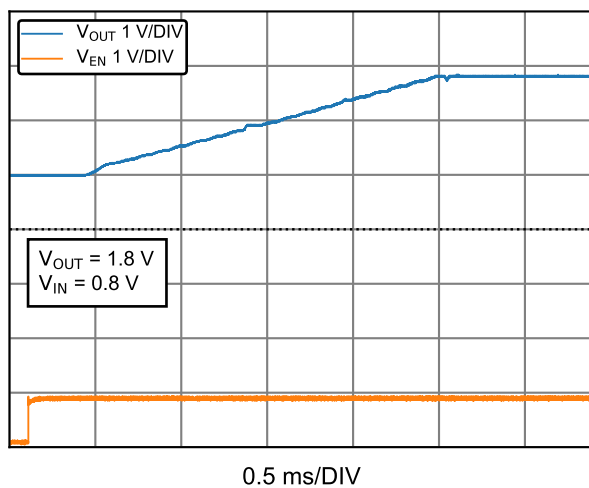
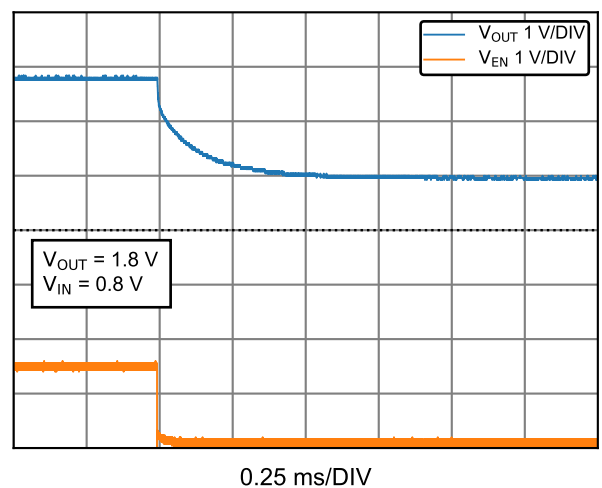
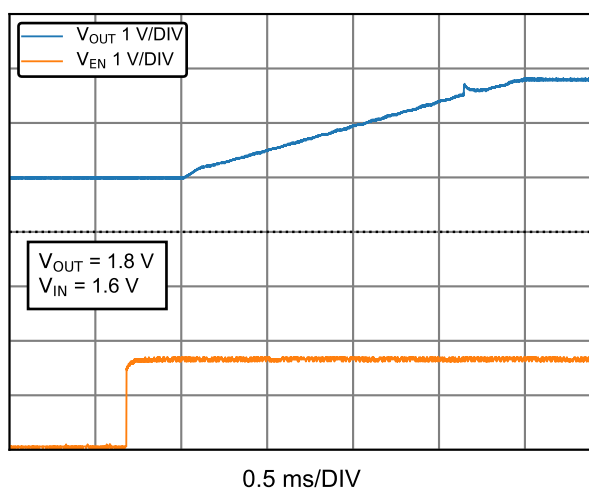
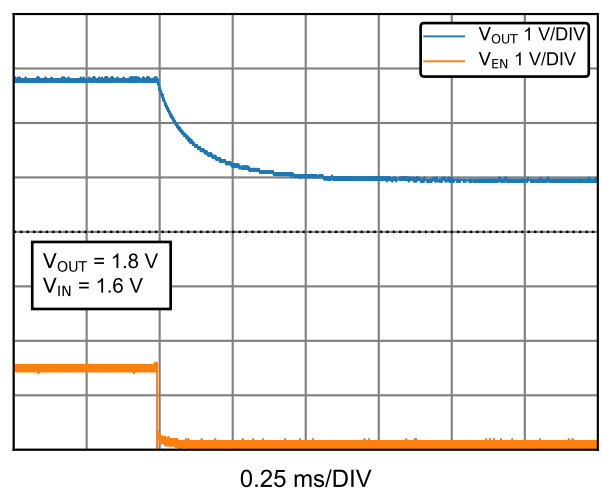


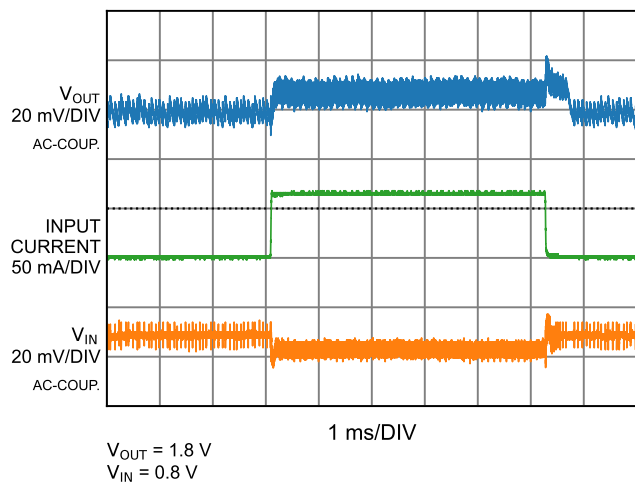
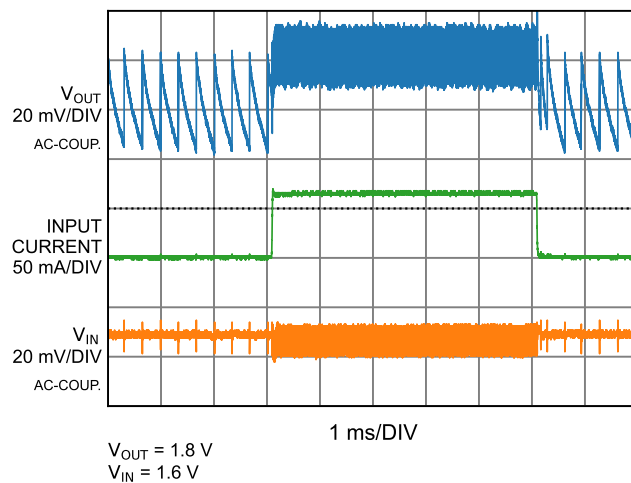
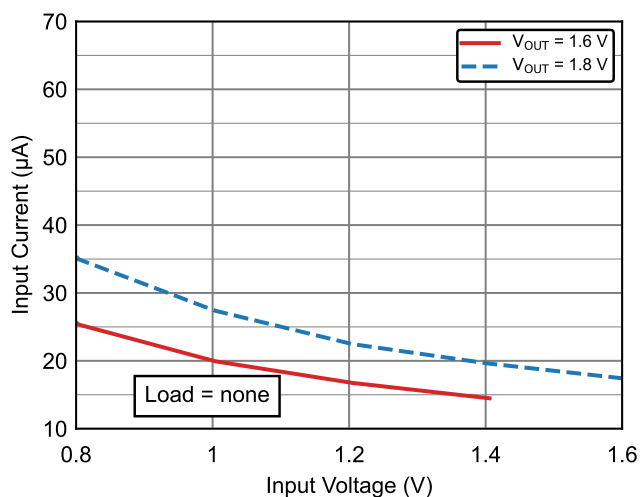
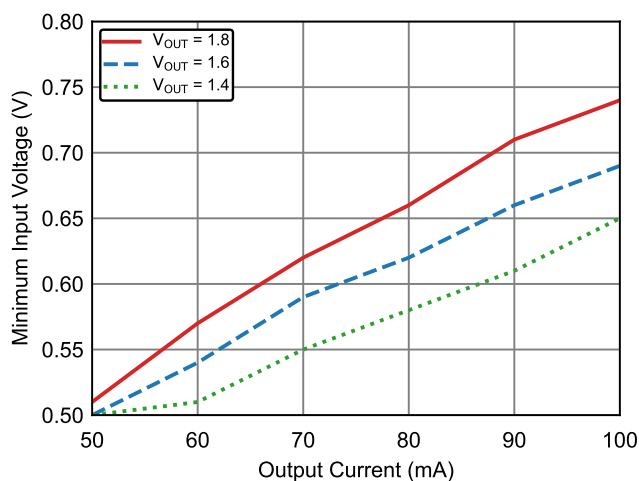
Figure 2: LMU20P1 Functional block diagram

TYPICAL PERFORMANCE CHARACTERISTICS

All values are measured or simulated at $T_A = +25\text{ }^{\circ}\text{C}$, $C_{IN} = C_{OUT} = 10\text{ }\mu\text{F}$ unless otherwise specified.



PFM/PWM Current Threshold

PFM/PWM Current Threshold

 V_{OUT} and Start-Up Waveform

 V_{OUT} and Shutdown Waveform

 V_{OUT} and Start-Up Waveform

 V_{OUT} and Shutdown Waveform


Load Transient Waveform

Load Transient Waveform

No load I_{IN} vs V_{IN}

Minimum V_{IN} at high load


APPLICATION INFORMATION

Typical Application Circuit

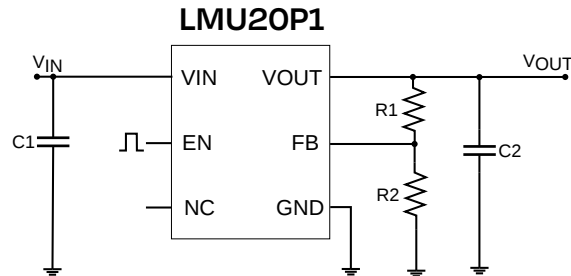


Figure 3: Typical circuit implementation of the LMU20P1

Input Capacitor Selection (C1)

A low ESL/ESR capacitor must be placed as close as possible to the package between the VIN pin and the GND pin. A 1- μ F 6.3-V X5R/X7R ceramic capacitor is required as a minimum input capacitor, though a 10- μ F capacitor is recommended due to capacitance derating. If there is a long connection between the DC source and the part, an additional bulk capacitor should be inserted between the DC source and input capacitor to provide a stable DC voltage.

Output Capacitor Selection (C2)

A low ESL/ESR capacitor must be placed as close as possible to the package between the VOUT pin and the GND pin. A 4.7- μ F 6.3-V X5R/X7R ceramic capacitor is required as a minimum output capacitor, though a 10- μ F capacitor is recommended due to capacitance derating. The output ripple is a function of the output capacitance and the parasitic ESL and ESR. Lower ESR and ESL (e.g. high-quality capacitors) and higher capacitance will reduce the ripple and improve the transient response. The loop compensation has no minimum requirement for ESR or ESL.

Feedback Resistor Selection

The output voltage of LMU20P1 is configured through resistors R1 and R2. The relationship between the resistor divider and the output voltage is given by:

$$\frac{R_1}{R_2} = \frac{V_{OUT}}{V_{REF}} + 1 \quad (1)$$

Rearranging for V_{OUT} yields:

$$V_{OUT} = \left(1 + \frac{R_1}{R_2}\right) \cdot V_{REF} \quad (2)$$

Careful consideration of the sizing of the resistor divider is necessary. Large resistor values contribute to a better light-load efficiency; however, they will impact the robustness and stability of the converter. It is recommended to select a value of 2.7 M Ω for R1 and select R2 according to equation 2. It is also recommended to keep the feedback trace as short and close to the module as possible.

Recommended Parts

Capacitors		Resistors	
Manufacturer	Family	Manufacturer	Family
Samsung	CL	Yageo	RC_L
Würth Elektronik	WCAP-CSGP	Panasonic	ERJ-2RK
Murata	GRM	Vishay	CRCW-C
TDK	C	Stackpole	RMCF

Table 3: Recommended component manufacturers and series.

DETAILED OPERATION DESCRIPTION

Modes of Operation

The LMU20P1 can operate in several different modes depending on load conditions to optimize efficiency and performance at all times. These modes are described below.

Normal Operation

The LMU20P1 is designed to operate in continuous-conduction mode (CCM) using pulse-width modulation (PWM) with a constant switching frequency of 5 MHz. A current-mode controller regulates the configured output voltage based on the measured low-side FET current.

Light Load Operation

For loads below a specified threshold, the LMU20P1 enters light-load operation mode. The device operates using pulse-frequency modulation (PFM), delivering a pulse of energy to the output capacitor upon detecting an error in the feedback voltage. As long as no error is detected, the switching node maintains a high-impedance state. In PFM, the device operates with a lower switching frequency depending on the input and output voltages, output capacitor size, and load. This mode offers excellent light-load efficiency, due to a substantial reduction in switching losses and quiescent current.

The table below provides an example of how the switching frequency changes under different load conditions.

V_{OUT}	V_{IN}	Load = 0 mA	Load = 15 mA	Load = 100 mA
1.8 V	0.8 V	740 Hz	400 KHz	5 MHz
1.8 V	1.6 V	145 Hz	100 KHz	5 MHz

Table 4: Switching frequency at different load conditions for $C_{in} = C_{out} = 10\mu F$.

Shutdown

The LMU20P1 enters shutdown mode by pulling the enable pin low or by triggering one of the protection circuits. In shutdown, the quiescent current is reduced and a minimum number of internal circuits are active. The device will return to normal operation after soft start.

Soft-Start Circuit

The LMU20P1 includes an internal soft-start circuit that slowly ramps the output voltage from 0 V to its set point. The soft-start lasts approximately 2 ms and ramps the output voltage in steps of 20 mV in a stair-case pattern with a step-period of approximately 100 μs in a staircase pattern. During soft-start the converter operates in asynchronous PWM mode with a temporary higher peak-current limit of 600 mA. This enables the converter to start during max load conditions, given a purely resistive load, and eliminates negative inductor currents. The soft-start circuit resets with each shutdown and protection event.

Over-Temperature Protection

The LMU20P1 enters thermal protection mode if the temperature of the internal die in the integrated circuit exceeds 150°C. During thermal protection mode the power-stage is off, and the output is high-impedance. The device will resume operation and initialize soft-start, once the temperature of the integrated circuit die falls below 135°C.

Short-Circuit Protection

To reduce the chances of permanent damage to the module, the LMU20P1 incorporates a short-circuit protection function. The short-circuit protection works by monitoring the feedback voltage, during both soft-start and normal operation, and triggers when the feedback voltage drops below 50% of V_{REF} . In case of a short-circuit event, the on-chip peak-current limiter will limit the peak current to approximately 500 mA. Once the short-circuit protection circuit triggers, the LMU20P1 will enter protection mode, keeping the module off for 10 ms before attempting a restart. If the short-circuit event persists, the module will continuously attempt to restart until it can recover.

Output current limit

During PWM mode, the LMU20P1 has a cycle-by-cycle inductor current limit of approximately 500 mA. This limits the total amount of power delivered to the output. If the operating conditions causes the converter to reach the cycle-by-cycle current limit, the converter will be unable to maintain the given output voltage and the output voltage will decrease until the short-circuit protection is triggered.

Low Voltage Startup

The LMU20P1 features a dedicated start-up circuit that enables start-up from an input voltage as low as 0.8 V. The feature is supported with soft-start and inrush-current limit operation. Once the output voltage reaches 95% of the target value, the internal circuitry is powered from the output and becomes independent of the input voltage source.

LAYOUT GUIDELINES

To achieve optimal performance with the LMU20P1, the board layout requires careful attention. Figure 4 shows the recommended printed circuit board (PCB) layout for the LMU20P1.

The input and output capacitors should be placed close to VIN and VOUT, respectively, to minimize the length of the traces. The ground should be unbroken and connected to the LMU20P1 exposed pad and GND pin. The unbroken ground connection yields short inductive loops and reduces EMI and ripple. To further reduce ESL, high-quality 0402 capacitors should be used. The feedback resistor divider should be placed close to the sensing output node, connecting the middle reference point to the FB pin. Thin traces should be used to reduce the capacitive coupling to other layers.

For a multilayer PCB, a large ground plane can be added to reduce the operational temperature of the LMU20P1.

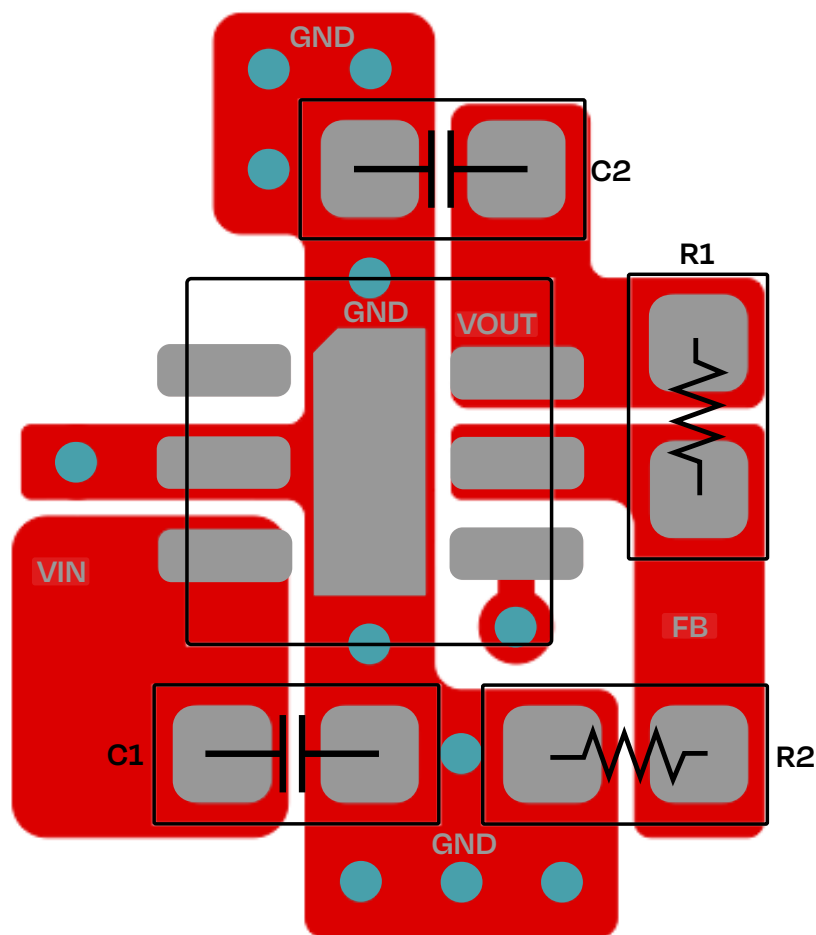


Figure 4: Recommended layout for optimal performance (top).

PACKAGE INFORMATION

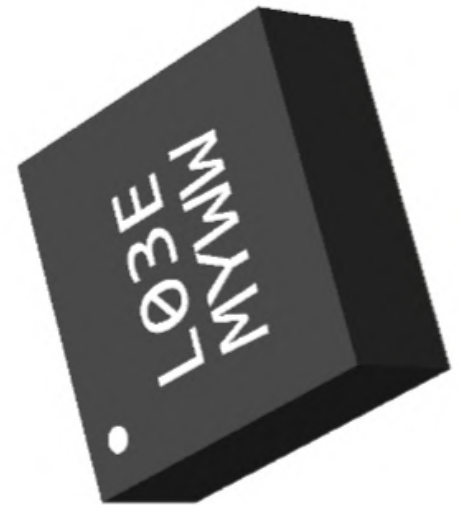
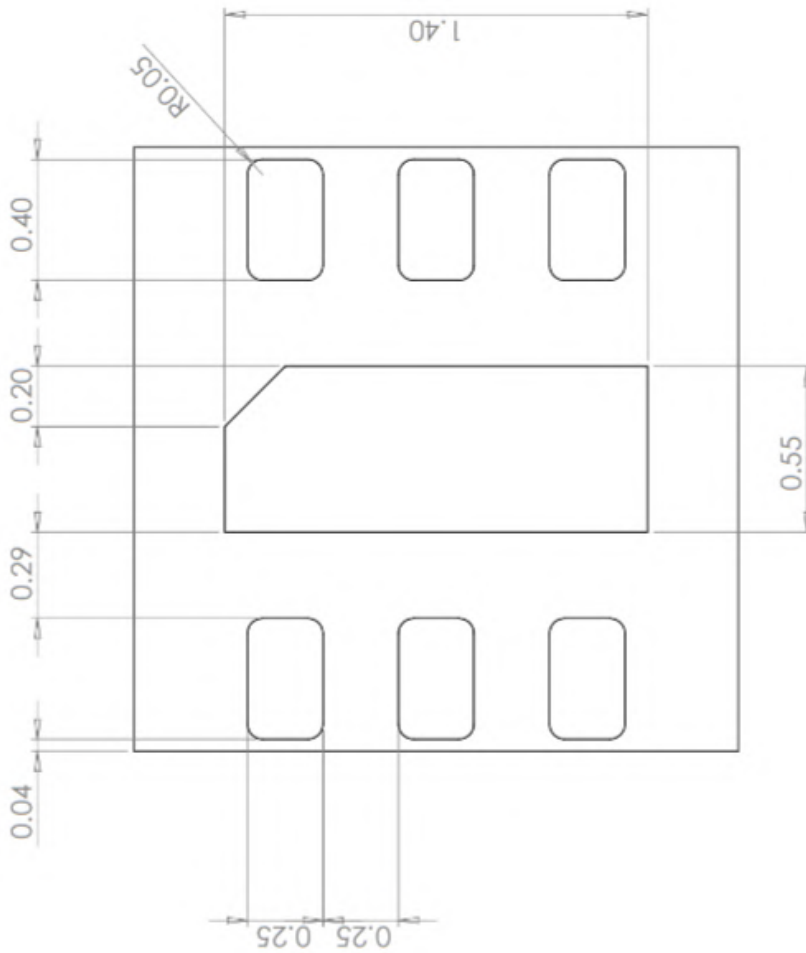
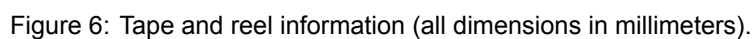


Diagram illustrating a reel with a label area. The reel is shown with a central hub and four spokes. A label area is indicated on the outer edge of the reel. A carrier tape is shown partially unspooled from the reel, and a cover tape is shown covering the label area.



Tape Width	Component Pitch	Hole Pitch	Reel Diameter	Units per Reel
8 mm	4 mm	4 mm	180 mm (7")	2500

REVISION HISTORY

Revision Number	Revision Date	Description	Pages Changed
1.0	23/05/2024	Public release	-
1.1	28/05/2025	Added information about de-rating for $V_{in} < 0.8V$	Page 1, 7

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